HV256

32-Channel High-Voltage Amplifier Array

Features

- Thirty-two Independent High-voltage Amplifiers
- 300V Operating Voltage
- 295V Output Voltage
- 2.2V/µs Typical Output Slew Rate
- Adjustable Output Current Source Limit
- Adjustable Output Current Sink Limit
- Internal Closed-loop Gain of 72V/V
- 12 MΩ Feedback Impedance
- Layout Ideal for Die Applications

Applications

- Microelectromechanical Systems (MEMS) Driver
- Piezoelectric Transducer Driver
- Optical Crosspoint Switches (Using MEMS Technology)

General Description

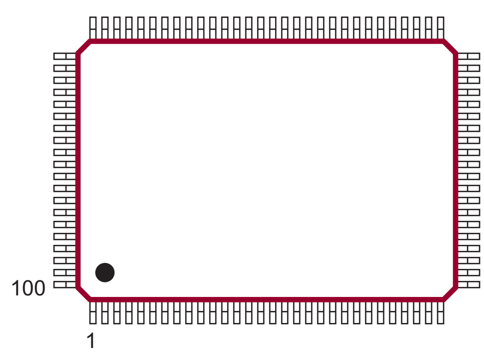
The HV256 is a 32-channel, high-voltage amplifier array integrated circuit. It operates on a single high-voltage supply, up to 300V, and two low-voltage supplies, V_{DD} and V_{NN}.

The input voltage range is from 0V to 4.096V. The internal closed-loop gain is 72V/V, giving an output voltage of 295V when 4.096V is applied. Input voltages of up to 5V can be applied but will cause the output to saturate. The maximum output voltage swing is 5V below the V_{PP} high-voltage supply. The outputs can drive capacitive loads of up to 3000 pF.

The maximum output source and sink currents can be adjusted by using two external resistors. An external R_{SOURCE} resistor controls the maximum sourcing current, and an external R_{SINK} resistor controls the maximum sinking current. The current limit is approximately 12.5V divided by the external resistor value. The setting is common for all 32 outputs. A low-voltage silicon junction diode is made available to help monitor the die temperature.

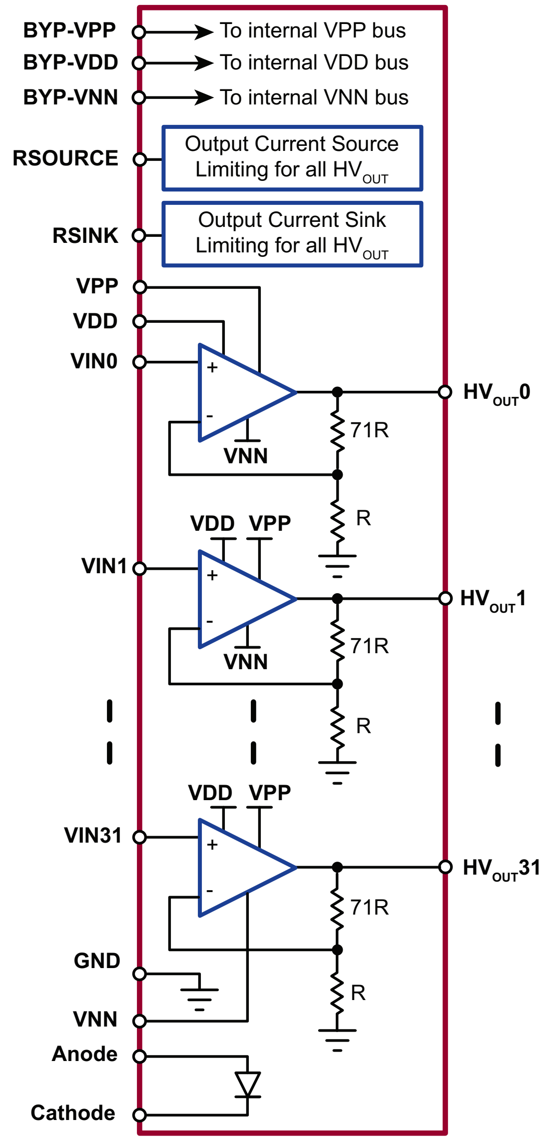
Package Type

100-lead MQFP
(Top view)

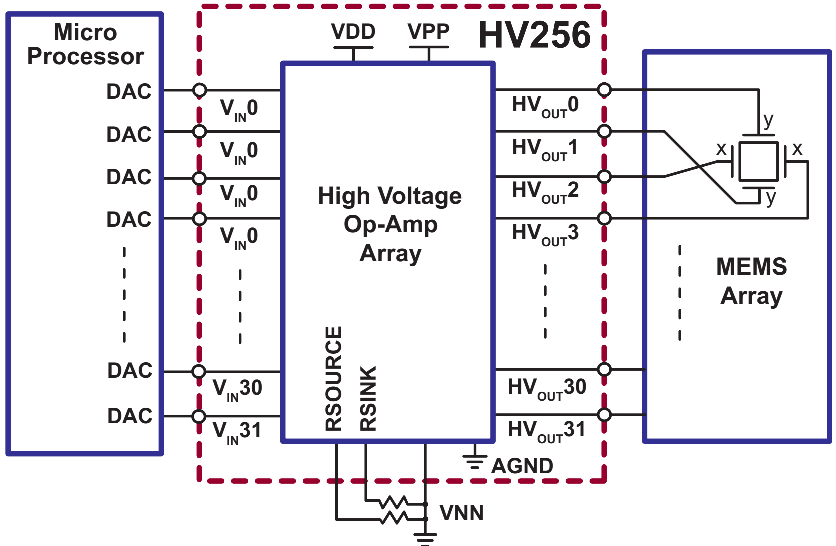


See Table 3-1 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

High-voltage Supply, V_{PP} 310V
Analog Low-voltage Positive Supply, AV_{DD} 8V
Digital Low-voltage Positive Supply, DV_{DD} 8V
Analog Low-voltage Negative Supply, AV_{NN} .... –7V
Digital Low-voltage Negative Supply, DV_{NN} .... –7V
Logic Input Voltage .... –0.5V to DV_{DD}
Analog Input Signal, V_{IN} .... 0V to 6V
Maximum Junction Temperature, T_J .... 150°C
Storage Temperature, T_S .... –65°C to +150°C

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
High-voltage Positive Supply	V_{PP}	125	—	300	V	
Low-voltage Positive Supply	V_{DD}	6	—	7.5	V	
Low-voltage Negative Supply	V_{NN}	–4.5	—	–6.5	V	
V_{PP} Supply Current	I_{PP}	—	—	0.8	mA	V_{PP} = 300V, All HV_{OUT} = 0V, No load
V_{DD} Supply Current	I_{DD}	—	—	5	mA	V_{DD} = 6V to 7.5V
V_{NN} Supply Current	I_{NN}	–6	—	—	mA	V_{NN} = –4.5V to –6.5V
Operating Temperature Range	T_J	–10	—	85	°C	

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over operating conditions unless otherwise noted.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
HV_{OUT} Voltage Swing	HV_{OUT}	0	—	V_{PP}–5	V	
Input Voltage Range	V_{IN}	0	—	5	V	
Input Voltage Offset	V_{INOS}	—	—	±50	mV	Input referred
Feedback Resistance from HV_{OUT} to Ground	R_{FB}	9.6	12	—	MΩ	
HV_{OUT} Capacitive Load	C_{LOAD}	0	—	3000	pF	
HV_{OUT} Sourcing Current Limiting Range	I_{SOURCE}	385	550	715	µA	R_{SOURCE} = 25 kΩ
HV_{OUT} Sinking Current Limiting Range	I_{SINK}	385	550	715	µA	R_{SINK} = 25 kΩ
External Resistance Range for Setting Maximum Current Source	R_{SOURCE}	25	—	250	kΩ	
External Resistance Range for Setting Maximum Current Sink	R_{SINK}	25	—	250	kΩ	

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over operating conditions unless otherwise noted						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Unit**	**Conditions**
HV_{OUT} Slew Rate Rise	SR	—	2.2	—	V/µs	No load
HV_{OUT} Slew Rate Fall		—	2	—	V/µs	No load
HV_{OUT} –3 dB Channel Bandwidth	BW	—	4	—	kHz	V_{PP} = 300V
Open-loop Gain	A_O	70	100	—	dB	
Closed-loop Gain	A_V	68.4	72	75.6	V/V	
DC Channel-to-channel Crosstalk	CT_{DC}	–80	—	—	dB	
Power Supply Rejection Ratio for V_{PP}, V_{DD} and V_{NN}	PSRR	–40	—	—	dB	
TEMPERATURE DIODE						
Peak Inverse Voltage	PIV	—	—	5	V	Cathode to anode
Forward Diode Drop	V_F	—	0.6	—	V	I_F = 100 µA, anode to cathode at T_A = 25°C
Forward Diode Current	I_F	—	—	100	µA	Anode to cathode
V_F Temperature Coefficient	T_C	—	–2.2	—	mV/°C	Anode to cathode

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Maximum Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
100-lead MQFP	θ_{JA}	—	39	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

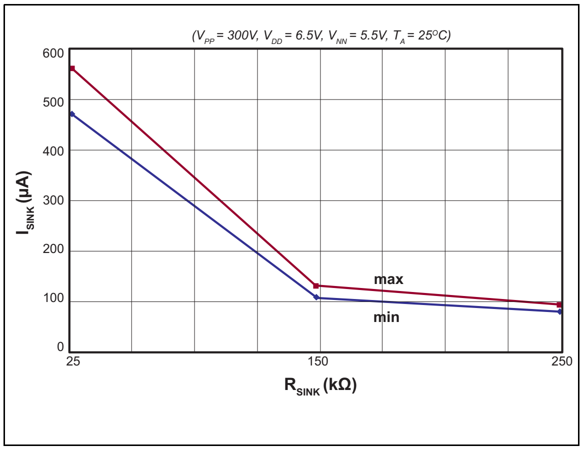


FIGURE 2-1: I_{SINK} vs. R_{SINK}.

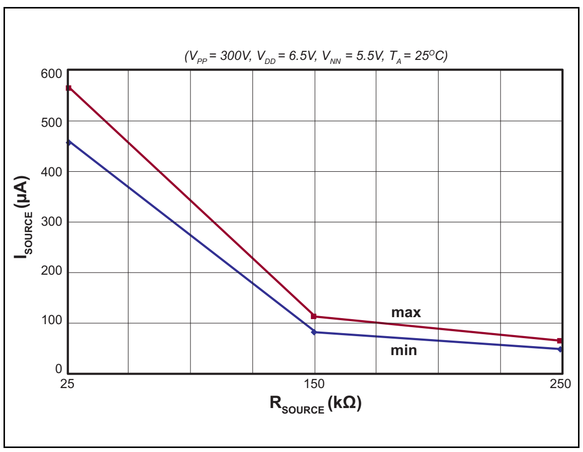


FIGURE 2-2: I_{SOURCE} vs. R_{SOURCE}.

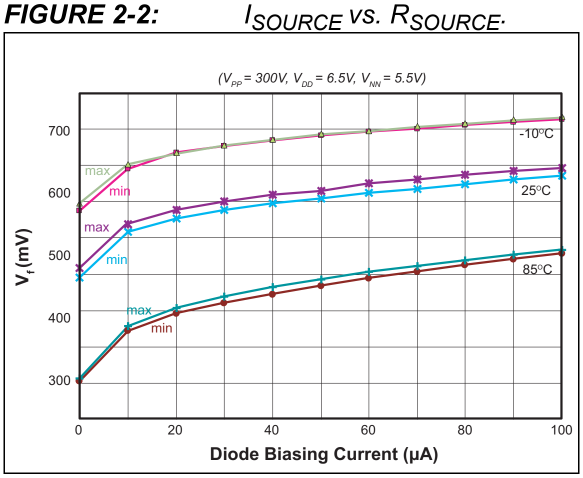


FIGURE 2-3: Temperature Diode vs. Temperature.

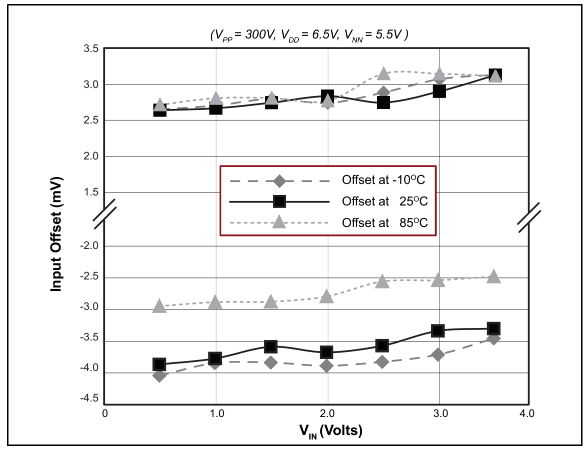


FIGURE 2-4: Input Offset vs. V_{IN} and Temperature.

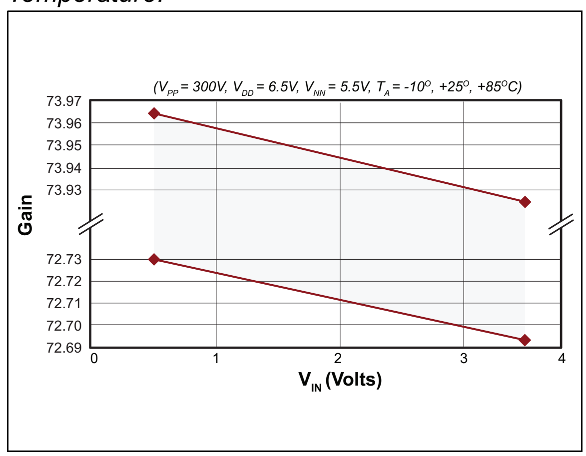


FIGURE 2-5: Gain vs. V_{IN}.

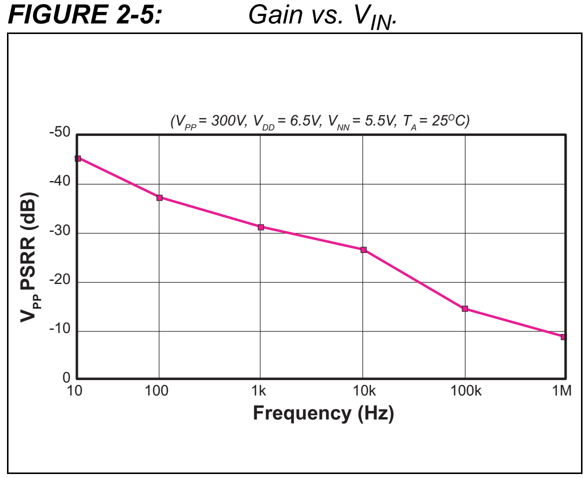


FIGURE 2-6: V_{PP} PSRR vs. Frequency.

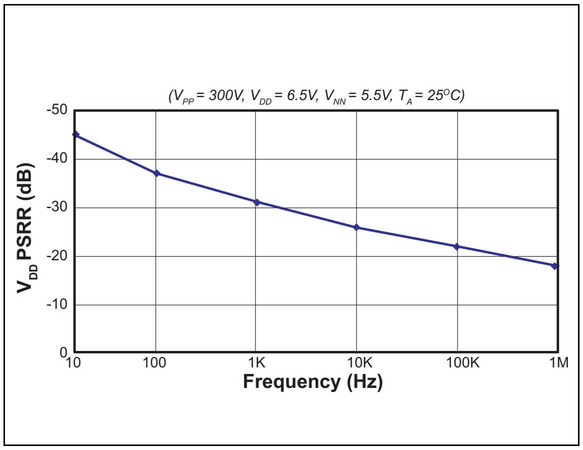


FIGURE 2-7: *V_{DD} PSRR vs. Frequency.*

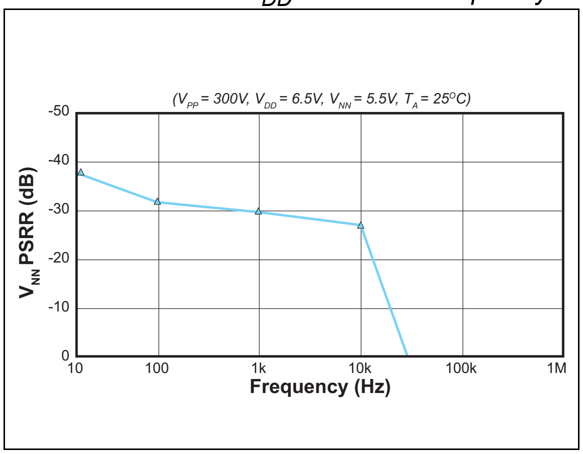


FIGURE 2-8: *V_{NN} PSRR vs. Frequency.*

3.0 PIN DESCRIPTION

The details on the pins of HV256 are listed on Table 3-1. Refer to **Package Type** for the location of pins.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	HVOUT31	Amplifier output
2	HVOUT30	Amplifier output
3	HVOUT29	Amplifier output
4	HVOUT28	Amplifier output
5	HVOUT27	Amplifier output
6	HVOUT26	Amplifier output
7	HVOUT25	Amplifier output
8	HVOUT24	Amplifier output
9	HVOUT23	Amplifier output
10	HVOUT22	Amplifier output
11	HVOUT21	Amplifier output
12	HVOUT20	Amplifier output
13	HVOUT19	Amplifier output
14	HVOUT18	Amplifier output
15	HVOUT17	Amplifier output
16	HVOUT16	Amplifier output
17	HVOUT15	Amplifier output
18	HVOUT14	Amplifier output
19	HVOUT13	Amplifier output
20	HVOUT12	Amplifier output
21	HVOUT11	Amplifier output
22	HVOUT10	Amplifier output
23	HVOUT9	Amplifier output
24	HVOUT8	Amplifier output
25	HVOUT7	Amplifier output
26	HVOUT6	Amplifier output
27	HVOUT5	Amplifier output
28	HVOUT4	Amplifier output
29	HVOUT3	Amplifier output
30	HVOUT2	Amplifier output
31	HVOUT1	Amplifier output
32	HVOUT0	Amplifier output
33	VPP	High-voltage positive supply. There are two pads in the die pad diagram.
34	NC	No connect
35	NC	No connect

TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
36	NC	No connect
37	NC	No connect
38	NC	No connect
39	GND	Digital ground. There are four pads in the die pad diagram.
40	VNN	Analog low-voltage negative supply. There are four pads in the die pad diagram.
41	NC	No connect
42	VDD	Analog low-voltage positive supply. There are four pads in the die pad diagram.
43	GND	Digital ground. There are four pads in the die pad diagram.
44	VNN	Analog low-voltage negative supply. There are four pads in the die pad diagram.
45	VDD	Analog low-voltage positive supply. There are four pads in the die pad diagram.
46	NC	No connect
47	NC	No connect
48	VIN0	Amplifier input
49	VIN1	Amplifier input
50	VIN2	Amplifier input
51	VIN3	Amplifier input
52	VIN4	Amplifier input
53	VIN5	Amplifier input
54	VIN6	Amplifier input
55	VIN7	Amplifier input
56	VIN8	Amplifier input
57	VIN9	Amplifier input
58	VIN10	Amplifier input
59	VIN11	Amplifier input
60	VIN12	Amplifier input
61	VIN13	Amplifier input
62	VIN14	Amplifier input
63	VIN15	Amplifier input
64	VIN16	Amplifier input
65	VIN17	Amplifier input
66	VIN18	Amplifier input
67	VIN19	Amplifier input
68	VIN20	Amplifier input
69	VIN21	Amplifier input
70	VIN22	Amplifier input
71	VIN23	Amplifier input
72	VIN24	Amplifier input
73	VIN25	Amplifier input
74	VIN26	Amplifier input

TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
75	VIN27	Amplifier input
76	VIN28	Amplifier input
77	VIN29	Amplifier input
78	VIN30	Amplifier input
79	VIN31	Amplifier input
80	NC	No connect
81	NC	No connect
82	NC	No connect
83	NC	No connect
84	NC	No connect
85	NC	No connect
86	GND	Digital ground. There are four pads in the die pad diagram.
87	VDD	Analog low-voltage positive supply. There are four pads in the die pad diagram.
88	VNN	Analog low-voltage negative supply. There are four pads in the die pad diagram.
89	GND	Digital ground. There are four pads in the die pad diagram.
90	NC	No connect
91	VDD	Analog low-voltage positive supply. There are four pads in the die pad diagram.
92	BYP-VNN	A low-voltage 1 nF to 10 nF decoupling capacitor across VNN and BYP-VNN is required.
93	BYP-VDD	A low voltage 1 nF to 10 nF decoupling capacitor across VDD and BYP-VDD is required.
94	VNN	Analog low-voltage negative supply. There are four pads in the die pad diagram.
95	ANODE	The anode side of a low-voltage silicon diode that can be used to monitor die temperature
96	CATHODE	The cathode side of a low-voltage silicon diode that can be used to monitor die temperature
97	RSINK	The external resistor from RSINK to VNN that sets the output current sinking limit. The current limit is approximately 12.5V divided by the RSINK resistor value.
98	RSOURCE	The external resistor from RSOURCE to VNN that sets the output current sourcing limit. The current limit is approximately 12.5V divided by the RSOURCE resistor value.
99	BYP-VPP	A low-voltage 1 nF to 10 nF decoupling capacitor across VPP and BYP-VPP is required.
100	VPP	High-voltage positive supply. There are four pads in the die pad diagram.

3.1 Pad Configuration

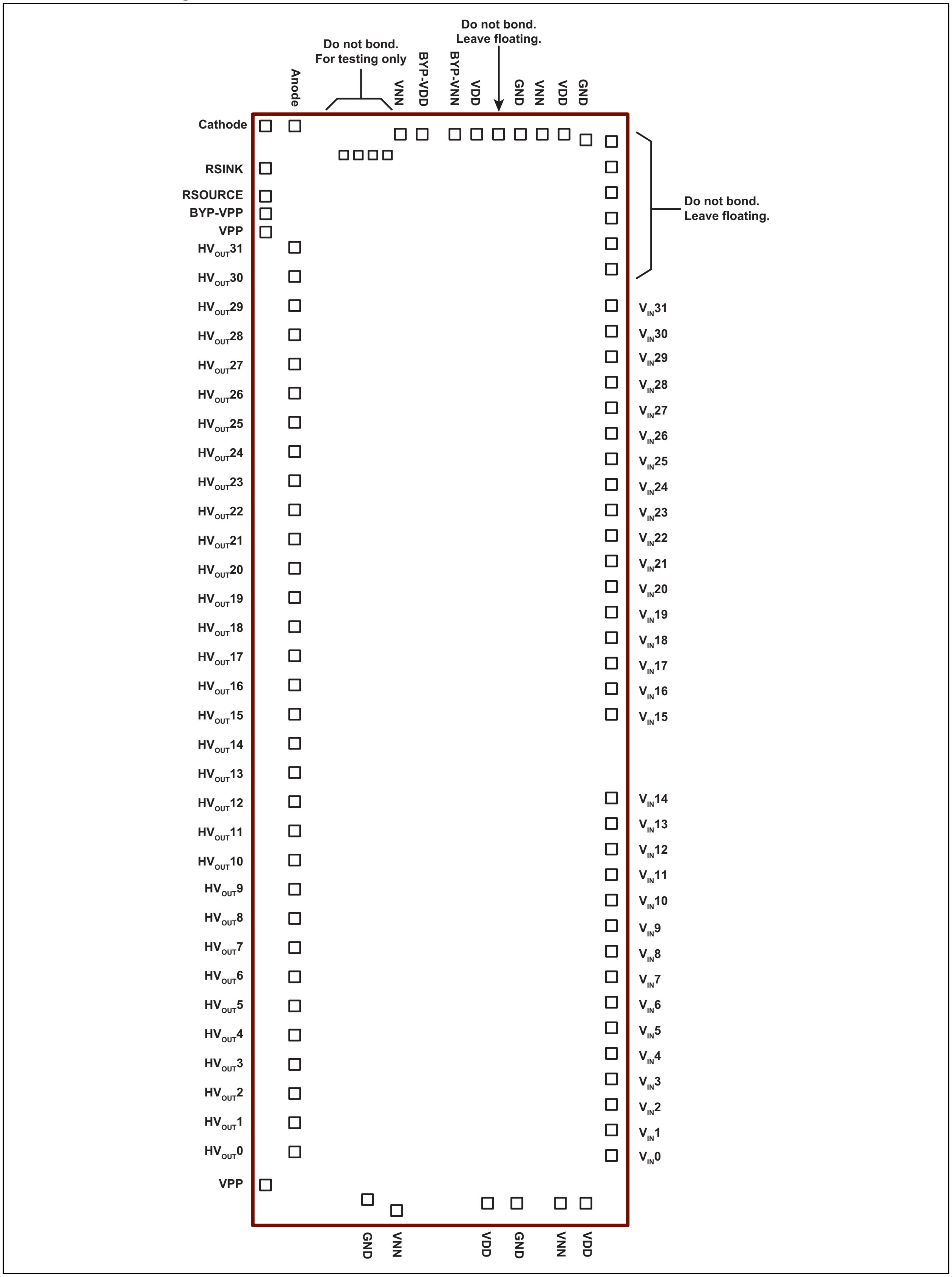


FIGURE 3-1: *Pad Configuration Drawing.*

TABLE 3-2: PAD COORDINATES

Chip Size: 17160 µm X 5830 µm
Center of Die: 0,0

Pad Name	X (µm)	Y (µm)
VPP	–8338.5	2708.5
HVOUT0	–7895	2305.5
HVOUT1	–7448.5	2305.5
HVOUT2	–7001.5	2305.5
HVOUT3	–6554.5	2305.5
HVOUT4	–6107.5	2305.5
HVOUT5	–5660.5	2305.5
HVOUT6	–5213.5	2305.5
HVOUT7	–4776.5	2305.5
HVOUT8	–4319.5	2305.5
HVOUT9	–3872.5	2305.5
HVOUT10	–3425.5	2305.5
HVOUT11	–2978.5	2305.5
HVOUT12	–2513.5	2305.5
HVOUT13	–2084.5	2305.5
HVOUT14	–1637.5	2305.5
HVOUT15	–1190.5	2305.5
HVOUT16	–743.5	2305.5
HVOUT17	–296.5	2305.5
HVOUT18	150	2305.5
HVOUT19	597.5	2305.5
HVOUT20	1044.5	2305.5
HVOUT21	1491.5	2305.5
HVOUT22	1938.5	2305.5
HVOUT23	2385.5	2305.5
HVOUT24	2832.5	2305.5
HVOUT25	3279.5	2305.5
HVOUT26	3726.5	2305.5
HVOUT27	4173.5	2305.5
HVOUT28	4620.5	2305.5
HVOUT29	5067.5	2305.5
HVOUT30	5514.5	2305.5
HVOUT31	5961.5	2305.5
VPP	6659	2709
BYP-VPP	7045	2709
RSOURCE	7489	2709
RSINK	7969	2709
CATHODE	8366	2709
ANODE	8366	2709
VNN	8047	425
BYP-VDD	8047	125.5
BYP-VNN	8047	–135.5
VDD	8047	–704.5

TABLE 3-2: PAD COORDINATES (CONTINUED)

Chip Size: 17160 µm X 5830 µm
Center of Die: 0,0

Pad Name	X (µm)	Y (µm)
GND	8047	–1424
VNN	8066.5	–1590
VDD	8066.5	–1958.5
GND	7867	–2192
VIN31	5043.5	–2686
VIN30	4638.5	–2686
VIN29	4233.5	–2686
VIN28	3828.5	–2686
VIN27	3423.5	–2686
VIN26	3018.5	–2686
VIN25	2613.5	–2686
VIN24	2208.5	–2686
VIN23	1803.5	–2686
VIN22	1398.5	–2686
VIN21	993.5	–2686
VIN20	588.5	–2686
VIN19	183.5	–2686
VIN18	–221.5	–2686
VIN17	–626.5	–2686
VIN16	–1031.5	–2686
VIN15	–1436.5	–2686
VIN14	–2412.5	–2686
VIN13	–2817	–2686
VIN12	–3222	–2686
VIN11	–3627	–2686
VIN10	–4032	–2686
VIN9	–4437	–2686
VIN8	–4842	–2686
VIN7	–5247	–2686
VIN6	–5652	–2686
VIN5	–6052	–2686
VIN4	–6462	–2686
VIN3	–6867	–2686
VIN2	–7272	–2686
VIN1	–7677	–2686
VIN0	–8082	–2686
VDD	–8373	–2250.5
VNN	–8373	–1949
GND	–8367	–1561
VDD	–8387	–1143
VNN	–8338.5	577.5
GND	–8341	916.5

4.0 FUNCTIONAL DESCRIPTION

4.1 Power-up/Power-down Sequence

4.1.1 EXTERNAL DIODE PROTECTION

The device can be damaged due to improper power-up/power-down sequence. To avoid this, please follow the acceptable power-up and power-down sequences in Table 4-1 and Table 4-2 and add two external diodes as shown in Figure 4-1. The first diode is a high-voltage diode across V_{PP} and V_{DD} where the anode of the diode is connected to V_{DD} and the cathode of the diode is connected to V_{PP}. Any low-current high-voltage diode such as a 1N4004 will be adequate. The second diode is a Schottky diode across V_{NN} and D_{GND} where the anode of the Schottky diode is connected to V_{NN} and the cathode is connected to D_{GND}. Any low-current Schottky diode such as a 1N5817 will be sufficient.

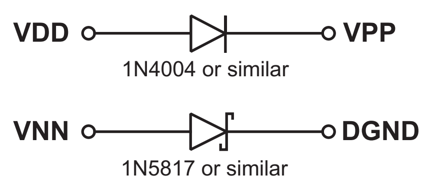


FIGURE 4-1: *Diode Configuration.*

4.1.2 RECOMMENDED POWER-UP/POWER-DOWN SEQUENCE

The HV256 needs all power supplies to be fully up and all channels refreshed with V_{SIG} = 0V to force all high-voltage outputs to 0V. Before that time, the high-voltage outputs may have temporary voltage excursions above or below GND level, depending on selected power-up sequence. To minimize the excursions, the V_{DD} and V_{NN} power supplies should be applied at the same time (or within a few nanoseconds). In addition, the suggested V_{PP} ramp-up speed should be 10 milliseconds or longer and the ramp-down should be 1 millisecond or longer.

TABLE 4-1: ACCEPTABLE POWER-UP SEQUENCES

Option 1		Option 2		Option 3	
Step	**Description**	**Step**	**Description**	**Step**	**Description**
1	V_{PP}	1	V_{NN}	1	V_{DD} and V_{NN}
2	V_{NN}	2	V_{DD}	2	Inputs
3	V_{DD}	3	V_{PP}	3	V_{PP}
4	Inputs and Anode	4	Inputs and Anode	4	Anode

TABLE 4-2: ACCEPTABLE POWER-DOWN SEQUENCES

Option 1		Option 2		Option 3	
Step	**Description**	**Step**	**Description**	**Step**	**Description**
1	Inputs and Anode	1	Inputs and Anode	1	Anode
2	V_{DD}	2	V_{PP}	2	V_{PP}
3	V_{NN}	3	V_{DD}	3	Inputs
4	V_{PP}	4	V_{NN}	4	V_{NN} and V_{DD}

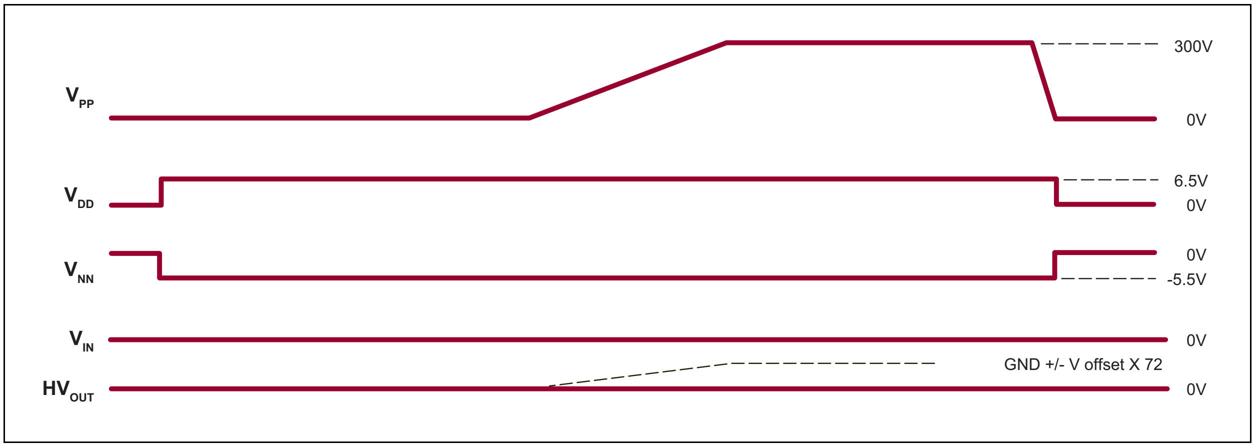


FIGURE 4-2: *Recommended Power-up/Power-down Timing.*

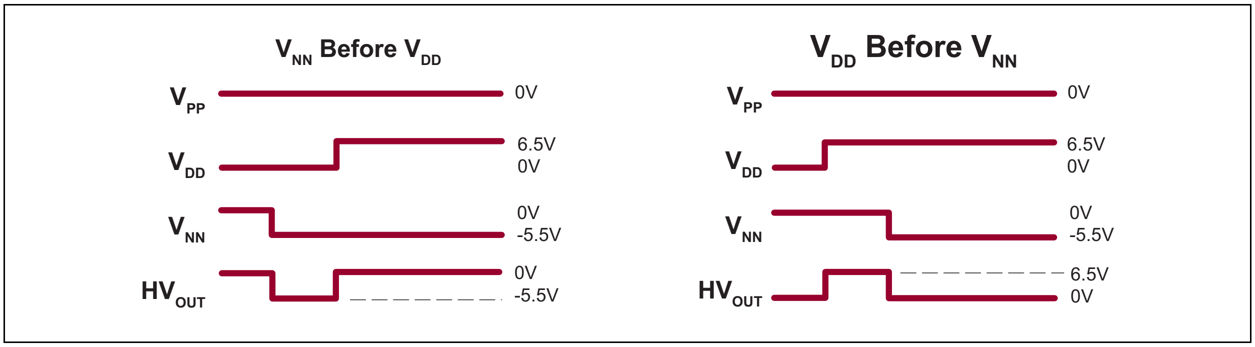


FIGURE 4-3: *HV_{OUT} Level at Power-up.*

4.2 R_{SINK}/R_{SOURCE}

The V_{DD}_BYP, V_{DD}_BYP and V_{NN}_BYP pins are internal high-impedance-current mirror gate nodes, brought out to maintain stable opamp biasing currents in noisy power supply environments. When 0.1 µF/25V bypass capacitors are added from between V_{PP}_BYP and V_{PP}, between V_{DD}_BYP and V_{DD}, and between V_{NN}_BYP and V_{NN}, they will force the high-impedance gate nodes to follow the fluctuation of power lines. The expected voltages at the V_{DD}_BYP and V_{NN}_BYP pins are typically 1.5V from their respectful power supply. The expected voltage at V_{PP}_BYP is typically 3V below V_{PP}.

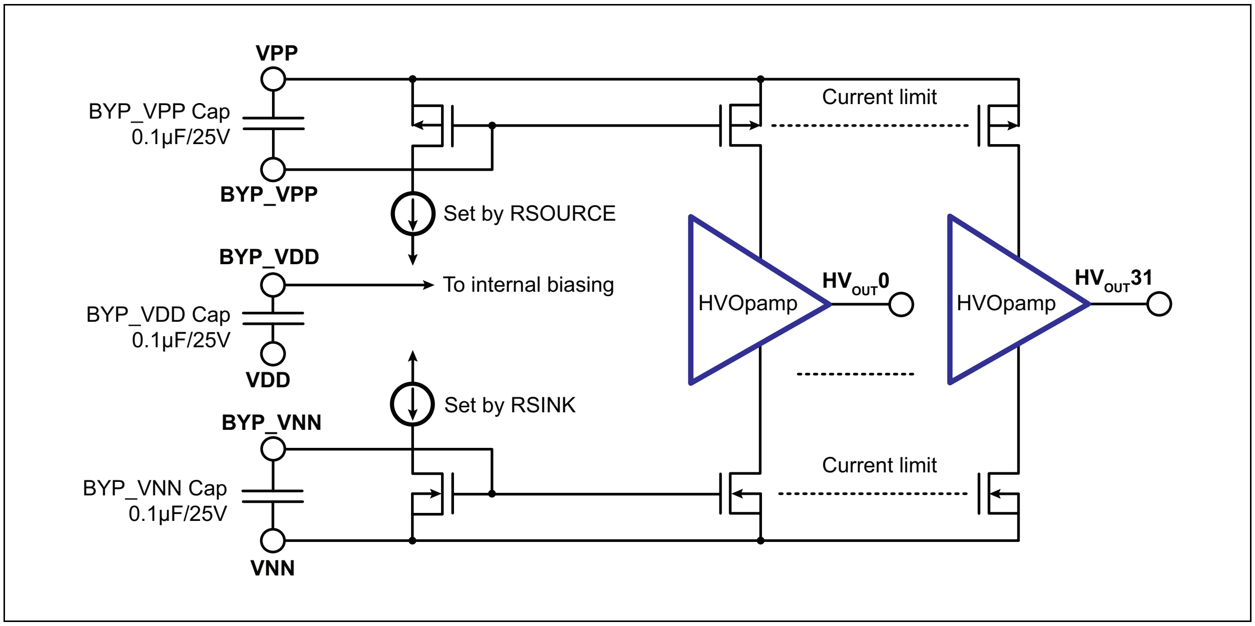
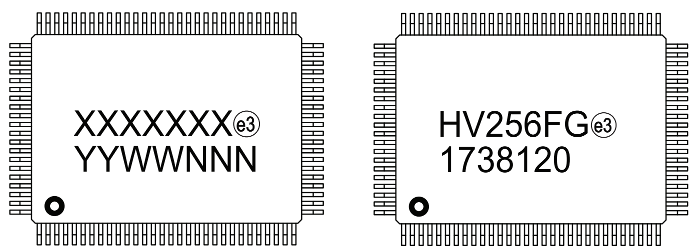


FIGURE 4-4: *Internal Reference Current Diagram.*

5.0 PACKAGE MARKING INFORMATION

5.1 Packaging Information

100-lead MQFP Example

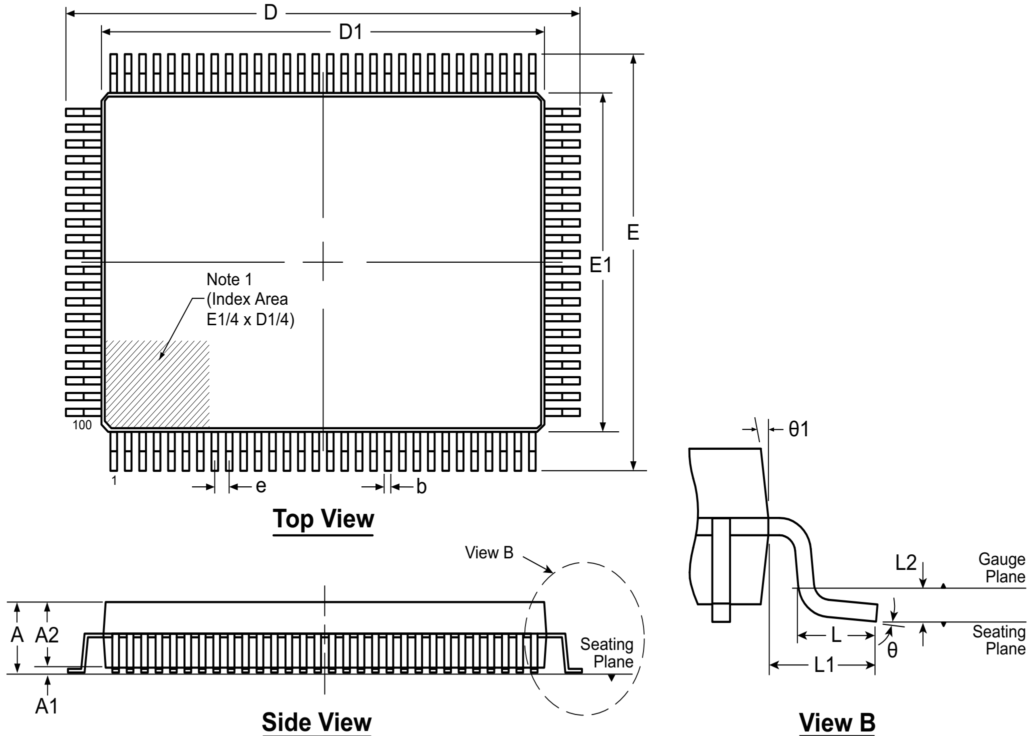


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

100-Lead MQFP Package Outline (FG)

20.00x14.00mm body, 3.15mm height (max), 0.65mm pitch, 3.20mm footprint



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.50*	0.00	2.50	0.22	22.95*	19.80*	16.95*	13.80*	0.65 BSC	0.73	1.60 REF	0.25 BSC	0°	5°
	NOM	-	-	2.70	-	23.20	20.00	17.20	14.00		0.88			-	-
	MAX	3.15	0.25	2.90	0.40	23.45*	20.20*	17.45*	14.20*		1.03			7°	16°

JEDEC Registration MS-022, Variation GC-2, Issue B, Dec. 1996.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (August 2017)

- Converted Supertex Doc# DSFP-HV256 to Microchip DS20005826A
- Changed the part marking format
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV256	=	32-Channel High-Voltage Amplifier Array
Package:	FG	=	100-lead MQFP
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	66/Tray for an FG Package

Example:

a) HV256FG-G: 32-Channel High-Voltage Amplifier Array, 100-lead MQFP, 66/Tray

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