

# Product Change Notification / SYST-22XRSR883

# Date:

25-Oct-2021

## **Product Category:**

Memory

# **PCN Type:**

**Document Change** 

## **Notification Subject:**

Data Sheet - 24AA256/24LC256/24FC256 256 Kbit I2C Serial EEPROM Data Sheet Document Revision

## **Affected CPNs:**

SYST-22XRSR883\_Affected\_CPN\_10252021.pdf SYST-22XRSR883\_Affected\_CPN\_10252021.csv

# **Notification Text:**

SYST-22XRSR883

Microchip has released a new Product Documents for the 24AA256/24LC256/24FC256 256 Kbit I2C Serial EEPROM Data Sheet of devices. If you are using one of these devices please read the document located at 24AA256/24LC256/24FC256 256 Kbit I2C Serial EEPROM Data Sheet.

#### Notification Status: Final

#### Description of Change:

1) Replaced terminology "Master" and "Slave" with "Host" and "Client" respectively;

- 2) Added Automotive Product Identification System;
- 3) Updated DFN, PDIP, SOIC, TDFN and TSSOP package drawings.

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 25 Oct 2021

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

# Attachments:

24AA256/24LC256/24FC256 256 Kbit I2C Serial EEPROM Data Sheet

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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If you wish to <u>change your PCN profile</u>, <u>including opt out</u>, please go to the <u>PCN home page</u> select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections. Affected Catalog Part Numbers (CPN)

24AA256-E/MF 24AA256-E/MS 24AA256-E/P 24AA256-E/SM 24AA256-E/SN 24AA256-E/ST 24AA256-I/MF 24AA256-I/MS 24AA256-I/MSRVE 24AA256-I/P 24AA256-I/S16K 24AA256-I/SM 24AA256-I/SN 24AA256-I/SN104 24AA256-I/SNRVE 24AA256-I/ST 24AA256-I/STRVE 24AA256-I/W16K 24AA256-I/WF16K 24AA256/SM 24AA256SC-I/S16K 24AA256SC-I/W16K 24AA256SC-I/WF16K 24AA256SC/WF0815K 24AA256T-E/MF 24AA256T-E/MNY 24AA256T-E/MS 24AA256T-E/SM 24AA256T-E/SN 24AA256T-E/ST 24AA256T-I/CS16K 24AA256T-I/MF 24AA256T-I/MNY 24AA256T-I/MS 24AA256T-I/MSRVE 24AA256T-I/SM 24AA256T-I/SN 24AA256T-I/SN104 24AA256T-I/SN105 24AA256T-I/SN15KV04 24AA256T-I/SNRVE 24AA256T-I/ST 24AA256T-I/STRVE 24AA256T/SM 24AA256UID-I/P 24AA256UID-I/SN

24AA256UID-I/ST 24AA256UIDT-I/SN 24AA256UIDT-I/ST 24FC256-E/SN 24FC256-E/ST 24FC256-E/ST16KVAO 24FC256-I/MF 24FC256-I/MS 24FC256-I/P 24FC256-I/SM 24FC256-I/SN 24FC256-I/ST 24FC256T-E/SN 24FC256T-E/ST 24FC256T-E/ST16KVAO 24FC256T-I/MF 24FC256T-I/MNY 24FC256T-I/MS 24FC256T-I/SM 24FC256T-I/SN 24FC256T-I/ST 24LC256-E/MF 24LC256-E/MS 24LC256-E/P 24LC256-E/SM 24LC256-E/SN 24LC256-E/SN15KVAO 24LC256-E/SN16KV03 24LC256-E/ST 24LC256-E/ST16KVAO 24LC256-E/ST22K 24LC256-E/STRVE 24LC256-I/MF 24LC256-I/MS 24LC256-I/MSRVF 24LC256-I/P 24LC256-I/PG 24LC256-I/PREL15K 24LC256-I/PRELRVA 24LC256-I/PRVE 24LC256-I/S15K 24LC256-I/SM 24LC256-I/SM15KVAO 24LC256-I/SM22K 24LC256-I/SMG 24LC256-I/SMRVE 24LC256-I/SMRVF 24LC256-I/SN 24LC256-I/SN15KVAO

24LC256-I/SN22K 24LC256-I/SNG 24LC256-I/SNREL 24LC256-I/SNRVE 24LC256-I/ST 24LC256-I/STA31 24LC256-I/STG 24LC256-I/WF0815K 24LC256-I/WNB16K 24LC256SC-I/S16K 24LC256SC-I/W0815K 24LC256SC-I/W0816K 24LC256SC-I/W16K 24LC256SC-I/WF0516K 24LC256SC-I/WF0715K 24LC256SC-I/WF0716K 24LC256SC-I/WF0815K 24LC256SC-I/WF0816K 24LC256SC-I/WF16K 24LC256SC/WF0815K 24LC256SC/WF0816K 24LC256T-E/MF 24LC256T-E/MNY 24LC256T-E/MS 24LC256T-E/SM 24LC256T-E/SMRVF 24LC256T-E/SN 24LC256T-E/SN15KV02 24LC256T-E/SN15KV03 24LC256T-E/SN15KV05 24LC256T-E/SN15KVAO 24LC256T-E/SN16KV02 24LC256T-E/SN16KV03 24LC256T-E/SN16KV04 24LC256T-E/SN16KVAO 24LC256T-E/SNRVE 24LC256T-E/ST 24LC256T-E/ST16KVAO 24LC256T-E/ST22K 24LC256T-E/STRVE 24LC256T-I/MF 24LC256T-I/MNY 24LC256T-I/MS 24LC256T-I/MSRVF 24LC256T-I/SM 24LC256T-I/SM15KVAO 24LC256T-I/SM16KVAO 24LC256T-I/SM22K 24LC256T-I/SMG

24LC256T-I/SMRVE 24LC256T-I/SMRVF 24LC256T-I/SN15KV01 24LC256T-I/SN15KVA0 24LC256T-I/SN16KVA0 24LC256T-I/SN16KVA0 24LC256T-I/SNRVE 24LC256T-I/SNRVF 24LC256T-I/SNRVF 24LC256T-I/ST 24LC256T-I/ST15KVA0 24LC256T-I/ST16KVA0 24LC256T-I/STA31 24LC256T-I/STA79



# 24AA256/24LC256/24FC256

# 256-Kbit I<sup>2</sup>C Serial EEPROM

#### **Device Selection Table**

Part Number	Vcc Range	Maximum Clock Frequency	Temperature Ranges	Available Packages
24AA256	1.7V-5.5V	400 kHz <sup>(1)</sup>	I, E	CS, MF, MS, P, SN, SM, MNY, ST
24LC256	2.5V-5.5V	400 kHz	I, E	MF, MS, P, SN, SM, MNY, ST
24FC256	1.7V-5.5V	1 MHz <sup>(2)</sup>	I	MF, MS, P, SN, SM, MNY, ST

**Note 1:** 100 kHz for Vcc < 2.5V.

2: 400 kHz for Vcc < 2.5V.

#### **Features**

- Single Supply with Operation Down to 1.7V for 24AA256 and 24FC256 Devices, 2.5V for 24LC256 Devices
- Low-Power CMOS Technology:
  - Write current: 3 mA, maximum
  - Standby current: 1 µA maximum (I-temp.)
- Two-Wire Serial Interface, I<sup>2</sup>C Compatible
- · Cascadable up to Eight Devices
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kHz, 400 kHz and 1 MHz Compatibility
- · Page Write Time: 5 ms, maximum
- Self-Timed Erase/Write Cycle
- 64-Byte Page Write Buffer
- Hardware Write-Protect
- ESD Protection >4000V
- More than One Million Erase/Write Cycles
- Data Retention >200 years
- Factory Programming Available
- · RoHS Compliant
- Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Extended (E): -40°C to +125°C
- Automotive AEC-Q100 Qualified

## Package Types

#### Packages

• 8-Ball CSP, 8-Lead DFN, 8-Lead MSOP, 8-Lead PDIP, 8-Lead SOIC, 8-Lead SOIJ, 8-Lead TDFN and 8-Lead TSSOP

### Description

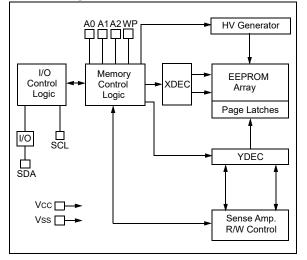
The Microchip Technology Inc. 24XX256<sup>(1)</sup> is a 32K x 8 (256-Kbit) Serial Electrically Erasable PROM (EEPROM), capable of operation across a broad voltage range (1.7V to 5.5V). It has been developed for advanced, low-power applications such as personal communications or data acquisition. This device also has a page write capability of up to 64 bytes of data. This device is capable of both random and sequential reads up to the 256K boundary. Functional address lines allow up to eight devices on the same bus, for up to 2 Mbit address space.

Note 1: 24XX256 is used in this document as a generic part number for the 24AA256/24LC256/24FC256 devices.

DFN/TDFN	DFN/TDFN MSOP/PDIP <sup>(1)</sup>		SOIC/SOIJ/TSSOP	CSP		
A2 3 🏹 6	Vcc WP SCL SDA	A0 1 A1 2 A2 3 Vss 4 X <b>7</b>	8 Vcc 7 WP 6 SCL 5 SDA	A0 亡 1 8 5 Vcc A1 亡 2 99 7 5 WP A2 亡 3 次 6 5 SCL Vss 亡 4 7 5 5 SDA	$WP \begin{array}{ c c c c c } \hline Vcc & A1 & A0 \\ \hline \bullet 1 & 2 & 3 \\ \hline \bullet 4 & 5 \\ \hline \bullet 6 & 7 & 8 \\ \hline SDA SCL VSS \end{array} A2$	

# 24AA256/24LC256/24FC256

## **Block Diagram**



## 1.0 ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings<sup>(†)</sup>

Vcc	6.5V
All inputs and outputs w.r.t. Vss	-0.6V to Vcc +1.0V
Storage temperature	-65°C to +150°C
Ambient temperature with power applied	-40°C to +125°C
ESD protection on all pins	≥4 kV

**† NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC CHA		STICS	Industrial ( Extended (	/	+1.7V to +1.7V to	
Param. No.	Symbol	Characteristic	Minimum	Maximum	Units	Conditions
D1	Vih	High-Level Input Voltage	0.7 Vcc	_	V	
D2	VIL	Low-Level Input Voltage	—	0.3 Vcc	V	$Vcc \ge 2.5V$
02	VIL	Low-Level input voltage	—	0.2 Vcc	V	Vcc < 2.5V
D3	VHYS	Hysteresis of Schmitt Trigger Inputs (SDA, SCL pins)	0.05 Vcc	_	V	Vcc ≥ 2.5V ( <b>Note 1</b> )
D4	Vol	Low-Level Output Voltage	—	0.40	V	IOL = 3.0 mA @ VCC = 4.5V IOL = 2.1 mA @ VCC = 2.5V
D5	ILI	Input Leakage Current	—	±1	μA	VIN = Vss or Vcc, WP = Vss VIN = Vss or Vcc, WP = Vcc
D6	ILO	Output Leakage Current	—	±1	μA	VOUT = Vss or Vcc
D7	Cin, Cout	Pin Capacitance (all inputs/outputs)	—	10	pF	Vcc = 5.0V ( <b>Note 1</b> ) Ta = +25°C, Fclk = 1 MHz
D8	ICC Read	Operating Current	—	400	μA	Vcc = 5.5V, SCL = 400 kHz
D9	ICC Write		—	3	mA	Vcc = 5.5V
			—	1	μA	SDA = SCL = Vcc = 3.6V A0, A1, A2, WP = Vss, I-Temp.
D10	Iccs	Standby Current	_	1.5	μA	SDA = SCL = Vcc = 5.5V A0, A1, A2, WP = Vss, I-Temp.
			_	5	μA	SDA = SCL = Vcc = 5.5V A0, A1, A2, WP = Vss, E-Temp.

#### TABLE 1-1: DC CHARACTERISTICS

**Note 1:** This parameter is periodically sampled and not 100% tested.

AC CHA	ARACTER	ISTICS	Industrial (I): Vcc = +1.7V to 5 Extended (E): Vcc = +1.7V to 5			
Param. No.	Symbol	Characteristic	Minimum	Maximum	Units	Conditions
			—	100	kHz	$1.7V \leq VCC < 2.5V$
1	FCLK	Clock Frequency	—	400	kHz	$2.5V \leq VCC \leq 5.5V$
1	FULK	Clock Frequency	—	400	kHz	$1.7V \le VCC < 2.5V$ (24FC256)
			—	1000	kHz	$2.5V \le VCC \le 5.5V$ (24FC256)
			4000	—	ns	$1.7V \leq VCC < 2.5V$
2	Тнідн	Clock High Time	600	—	ns	$2.5V \leq VCC \leq 5.5V$
Z	THIGH	Clock High Time	600	—	ns	$1.7V \le VCC < 2.5V$ (24FC256)
			500	—	ns	$2.5V \le VCC \le 5.5V$ (24FC256)
			4700	—	ns	$1.7V \leq VCC < 2.5V$
n	TLOW	Clock Low Time	1300	—	ns	$2.5V \le VCC \le 5.5V$
3	TLOW		1300		ns	1.7V ≤ VCC < 2.5V ( <b>24FC256</b> )
			500	—	ns	$2.5V \le VCC \le 5.5V$ (24FC256)
			—	1000	ns	1.7V ≤ VCC < 2.5V (Note 1)
4	TR	SDA and SCL Rise Time	_	300	ns	2.5V ≤ VCC ≤ 5.5V (Note 1)
+			_	300	ns	1.7V ≤ Vcc ≤ 5.5V ( <b>24FC256</b> ) (Note 1)
			—	300	ns	All except 24FC256 (Note 1)
5	T⊧	SDA and SCL Fall Time	_	100	ns	1.7V ≤ Vcc ≤ 5.5V ( <b>24FC256</b> ) (Note 1)
			4000	_	ns	$1.7V \leq VCC < 2.5V$
<b>^</b>	TURIOTA	Chart Canditian Hold Time	600	_	ns	$2.5V \le Vcc \le 5.5V$
6	THD:STA	Start Condition Hold Time	600	—	ns	$1.7V \le VCC < 2.5V$ (24FC256)
			250	—	ns	$2.5V \le VCC \le 5.5V$ (24FC256)
			4700	_	ns	$1.7V \leq VCC < 2.5V$
7	TSU:STA	Start Condition Satur Time	600	—	ns	$2.5V \leq VCC \leq 5.5V$
7	150.51A	Start Condition Setup Time	600	—	ns	$1.7V \le VCC < 2.5V$ (24FC256)
			250	_	ns	$2.5V \le VCC \le 5.5V$ (24FC256)
8	THD:DAT	Data Input Hold Time	0	_	ns	Note 2
			250	_	ns	$1.7V \leq VCC < 2.5V$
9	TSU:DAT	Data Input Setup Time	100		ns	$2.5V \leq Vcc \leq 5.5V$
			100	_	ns	$1.7V \le VCC \le 5.5V$ (24FC256)
			4000	_	ns	$1.7V \leq VCC < 2.5V$
10	Touvoto	Ston Condition Sofur Time	600		ns	$2.5V \le VCC \le 5.5V$
10	TSU:STO	Stop Condition Setup Time	600		ns	$1.7V \le VCC < 2.5V$ (24FC256)
			250	_	ns	2.5V ≤ Vcc ≤ 5.5V ( <b>24FC256</b> )

## TABLE 1-2: AC CHARACTERISTICS

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

**2:** As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

**3:** The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs, which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but ensured by characterization.

AC CHA	ARACTER	ISTICS (Continued)	Industrial (I Extended (B		+1.7V to +1.7V to	
Param. No.	Symbol	Characteristic	Minimum	Maximum	Units	Conditions
			4000		ns	$1.7V \leq VCC < 2.5V$
11	TSU:WP	WP Setup Time	600	_	ns	$2.5V \le VCC \le 5.5V$
			600	—	ns	1.7V ≤ VCC ≤ 5.5V ( <b>24FC256</b> )
			4700	—	ns	$1.7V \leq VCC < 2.5V$
12	THD:WP	WP Hold Time	1300	—	ns	$2.5V \le VCC \le 5.5V$
			1300	—	ns	1.7V ≤ Vcc ≤ 5.5V ( <b>24FC256</b> )
			—	3500	ns	1.7 V ≤ Vcc < 2.5V (Note 2)
		Output Valid from Clock	—	900	ns	2.5 V ≤ Vcc ≤ 5.5V (Note 2)
13 TAA	ΤΑΑ		—	900	ns	1.7V ≤ VCC < 2.5V ( <b>24FC256</b> ) (Note 2)
			_	400	ns	2.5 V ≤ Vcc ≤ 5.5V ( <b>24FC256</b> ) (Note 2)
		Bus Free Time: The time	4700		ns	$1.7V \leq VCC < 2.5V$
14	TBUF	the bus must be free before	1300	_	ns	$2.5V \le VCC \le 5.5V$
14	TBOF		1300		ns	1.7V ≤ VCC < 2.5V ( <b>24FC256</b> )
			500	—	ns	2.5V ≤ VCC ≤ 5.5V ( <b>24FC256</b> )
		Output fall time from VIH		250	ns	All except 24FC256 (Note 1)
15	TOF	minimum to Vı∟ maximum Cв ≤ 100 pF	10 + 0.1Св	250	ns	All except 24FC256 (Note 1)
16	TSP	Input Filter Spike Suppression (SDA and SCL pins)	_	50	ns	All except 24FC256 (Notes 1 and 3)
17	Twc	Write Cycle Time (byte or page)	—	5	ms	
18		Endurance	1,000,000	_	cycles	+25°C, 5.5V, Page mode (Note

## TABLE 1-2: AC CHARACTERISTICS

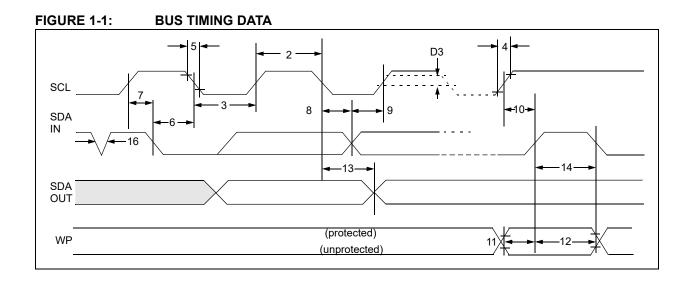
Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

**2:** As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

**3:** The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs, which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but ensured by characterization.

# 24AA256/24LC256/24FC256



## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

Name	DFN <sup>(1)</sup>	MSOP	PDIP	SOIC	SOIJ	TDFN <sup>(1)</sup>	TSSOP	CSP	Function
A0	1		1	1	1	1	1	3	User Configurable Chip Select
A1	2	_	2	2	2	2	2	2	User Configurable Chip Select
A2	3	3	3	3	3	3	3	5	User Configurable Chip Select
Vss	4	4	4	4	4	4	4	8	Ground
SDA	5	5	5	5	5	5	5	6	Serial Address/Data I/O
SCL	6	6	6	6	6	6	6	7	Serial Clock
WP	7	7	7	7	7	7	7	4	Write-Protect Input
Vcc	8	8	8	8	8	8	8	1	Power Supply

#### TABLE 2-1: PIN FUNCTION TABLE

**Note 1:** Exposed pad on DFN/TDFN can be connected to Vss or left floating.

## 2.1 A0, A1, A2 Chip Address Inputs

The A0, A1 and A2 inputs are used by the 24XX256 for multiple device operations. The levels on these inputs are compared with the corresponding bits in the client address. The chip is selected if the compare is true.

Note:	For the MSOP package only, pins A0 and
	A1 are not connected.

Up to eight devices (two for the MSOP package) may be connected to the same bus by using different Chip Select bit combinations. These inputs must be connected to either Vcc or Vss.

In most applications, the chip address inputs A0, A1 and A2 are hard-wired to logic '0' or logic '1'. For applications in which these pins are controlled by a microcontroller or other programmable device, the chip address pins must be driven to logic '0' or logic '1' before normal device operation can proceed.

## 2.2 Serial Data (SDA)

This is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open-drain terminal. Therefore, the SDA bus requires a pull-up resistor to Vcc (typical 10 k $\Omega$  for 100 kHz, 2 k $\Omega$  for 400 kHz and 1 MHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

## 2.3 Serial Clock (SCL)

This input is used to synchronize the data transfer to and from the device.

## 2.4 Write-Protect (WP)

This pin must be connected to either Vss or Vcc. If tied to Vss, write operations are enabled. If tied to Vcc, write operations are inhibited but read operations are not affected.

## 3.0 FUNCTIONAL DESCRIPTION

The 24XX256 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The bus must be controlled by a host device which generates the Serial Clock (SCL), controls the bus access, and generates the Start and Stop conditions while the 24XX256 works as a client. Both host and client can operate as a transmitter or receiver, but the host device determines which mode is activated.

## 4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line, while the clock line is high, will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

## 4.1 Bus Not Busy (A)

Both data and clock lines remain high.

## 4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high, determines a Start condition. All commands must be preceded by a Start condition.

## 4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line, while the clock (SCL) is high, determines a Stop condition. All operations must end with a Stop condition.

## 4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the host device and is, theoretically, unlimited (although only the last 64 will be stored when doing a write operation). When an overwrite does occur it will replace data in a First-In First-Out (FIFO) principle.

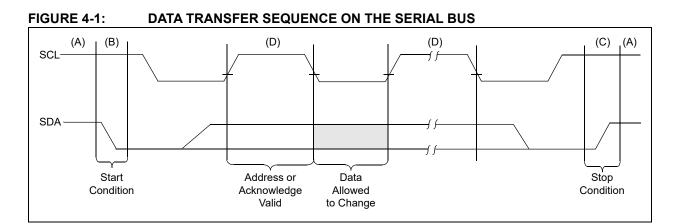
## 4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge signal after the reception of each byte. The host device must generate an extra clock pulse which is associated with this Acknowledge bit.

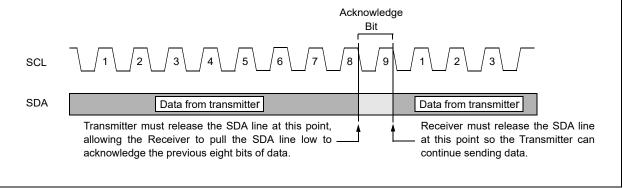
Note:	The 24XX256			•	-		
	Acknowledge	bits	if	an	internal		
	programming cycle is in progress.						

A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable-low during the high period of the Acknowledge-related clock pulse. Moreover, setup and hold times must be taken into account. During reads, a host must signal an end of data to the client by NOT generating an Acknowledge bit on the last byte that has been clocked out of the client. In this case, the client (24XX256) will leave the data line high to enable the host to generate the Stop condition.

# 24AA256/24LC256/24FC256







# 24AA256/24LC256/24FC256

## 5.0 DEVICE ADDRESSING

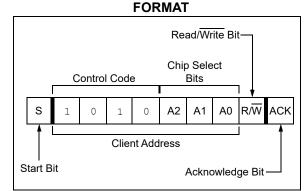
A control byte is the first byte received following the Start condition from the host device. The control byte consists of a 4-bit control code. For the 24XX256, this is set as '1010' binary for read and write operations. The next three bits of the control byte are the Chip Select bits (A2, A1, A0). The Chip Select bits allow the use of up to eight 24XX256 devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. These bits, in effect, are the three Most Significant bits of the word address. The combination of the 4-bit control code and the next three bits are called the client address.

For the MSOP package, the A0 and A1 pins are not connected. During device addressing, the A0 and A1 Chip Select bits (Figures 5-1 and 5-2) should be set to '0'. Only two 24XX256 MSOP packages can be connected to the same bus.

The last bit of the control byte is the Read/Write (R/W) bit and it defines the operation to be performed. When set to '1', a read operation is selected. When set to '0', a write operation is selected. The next two bytes received define the address of the first data byte (Figure 5-2). Because only A14...A0 are used, the upper address bits are a "don't care." The upper address bits are transferred first, followed by the Least Significant bits.

Following the Start condition, the 24XX256 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a '1010' code and appropriate device select bits, the client device outputs an Acknowledge signal on the SDA line. Depending on the state of the  $R/\overline{W}$  bit, the 24XX256 will select a read or write operation.

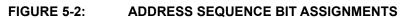
# FIGURE 5-1: CONTROL BYTE

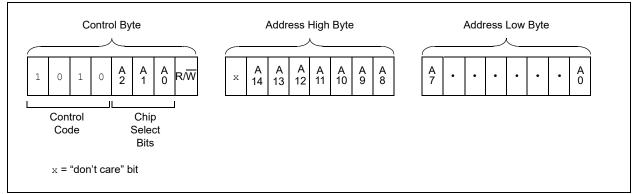


## 5.1 Contiguous Addressing Across Multiple Devices

The Chip Select bits A2, A1 and A0 can be used to expand the contiguous address space for up to 2-Mbit by adding up to eight 24XX256 devices on the same bus. In this case, software can use A0 of the control byte as address bit A15; A1 as address bit A16; and A2 as address bit A17. It is not possible to sequentially read across device boundaries.

For the MSOP package, up to two 24XX256 devices can be added for up to 512-Kbit of address space. In this case, software can use A2 of the control byte as address bit A17. Bits A0 (A15) and A1 (A16) of the control byte must always be set to a logic '0' for the MSOP.





## 6.0 WRITE OPERATIONS

## 6.1 Byte Write

Following the Start condition from the host, the control code (four bits), the Chip Select (three bits) and the R/W bit (which is a logic low) are clocked onto the bus by the host transmitter. This indicates to the addressed client receiver that the address high byte will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the host is the high-order byte of the word address and will be written into the Address Pointer of the 24XX256. The next byte is the Least Significant Address Byte. After receiving another Acknowledge signal from the 24XX256, the host device will transmit the data word to be written into the addressed memory location. The 24XX256 acknowledges again and the host generates a Stop condition. This initiates the internal write cycle and during this time, the 24XX256 will not generate Acknowledge signals (Figure 6-1). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command but no write cycle will occur, no data will be written, and the device will immediately accept a new command. After a byte write command, the internal address counter will point to the address location following the one that was just written.

**Note:** When doing a write of less than 64 bytes, the data in the rest of the page are refreshed along with the data bytes being written. This will force the entire page to endure a write cycle, for this reason endurance is specified per page.

## 6.2 Page Write

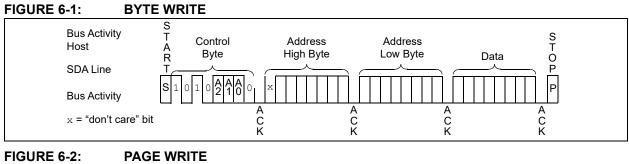
The write control byte, word address and the first data byte are transmitted to the 24XX256 in much the same way as in a byte write. The exception is that instead of generating a Stop condition, the host transmits up to 63 additional bytes, which are temporarily stored in the on-chip page buffer, and will be written into memory once the host has transmitted a Stop condition. Upon receipt of each word, the six lower Address Pointer bits, which form the byte counter, are internally incremented by one. If the host should transmit more than 64-bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command, but no write cycle will occur, no data will be written and the device will immediately accept a new command.

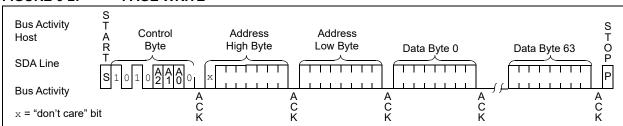
Note: Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of page size - 1. If a page write command attempts to write across a physical page boundary, the result is that the data wrap around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is, therefore, necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

## 6.3 Write Protection

The WP pin allows the user to write-protect the entire array (0000-7FFF) when the pin is tied to Vcc. If tied to Vss the write protection is disabled. The WP pin is sampled at the Stop bit for every write command (Figure 1-1). Toggling the WP pin after the Stop bit will have no effect on the execution of the write cycle.

# 24AA256/24LC256/24FC256



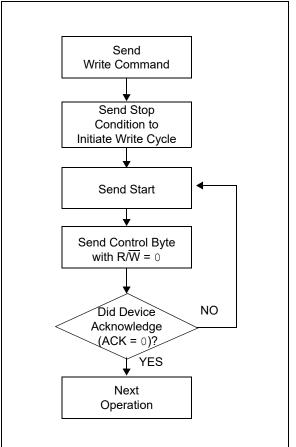


## 7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (This feature can be used to maximize bus throughput). Once the Stop condition for a write command has been issued from the host, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the host sending a Start condition, followed by the control byte for a write command (R/W = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, the Start bit and control byte must be resent. If the cycle is complete, then the device will return the ACK and the host can then proceed with the next read or write command. See Figure 7-1 for flow diagram.



#### ACKNOWLEDGE POLLING FLOW



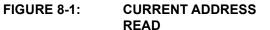
## 8.0 READ OPERATION

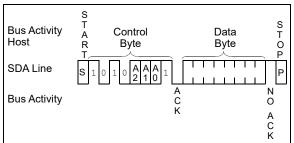
Read operations are initiated in much the same way as write operations, with the exception that the R/W bit of the control byte is set to '1'. There are three basic types of read operations: current address read, random read and sequential read.

### 8.1 Current Address Read

The 24XX256 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n (n is any legal address), the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with  $R/\overline{W}$  bit set to '1', the 24XX256 issues an Acknowledge and transmits the 8-bit data word. The host will not acknowledge the transfer, but does generate a Stop condition and the 24XX256 discontinues transmission (Figure 8-1).





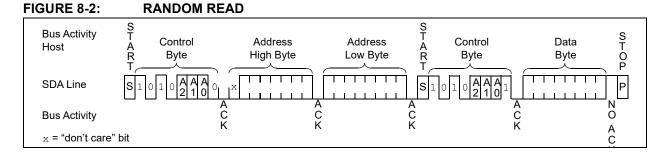
### 8.2 Random Read

Random read operations allow the host to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is done by sending the word address to the 24XX256 as part of a write operation (R/W bit set to '0'). Once the word address is sent, the host generates a Start condition following the Acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. The host then issues the control byte again, but with the R/W bit set to a one. The 24XX256 will then issue an Acknowledge and transmit the 8-bit data word. The host will not acknowledge the transfer, though it does generate a Stop condition, which causes the 24XX256 to discontinue transmission (Figure 8-2). After a random read command, the internal address counter will point to the address location following the one that was just read.

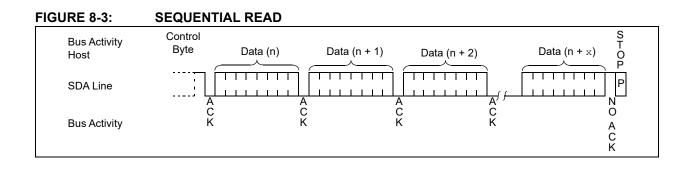
## 8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24XX256 transmits the first data byte, the host issues an Acknowledge (as opposed to the Stop condition used in a random read). This Acknowledge directs the 24XX256 to transmit the next sequentially addressed 8-bit word (Figure 8-3). Following the final byte transmitted to the host, the host will NOT generate an Acknowledge, but will generate a Stop condition.

To provide sequential reads, the 24XX256 contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation. The internal Address Pointer will automatically roll over from address 7FFF to address 0000 if the host acknowledges the byte received from the array address 7FFF.



# 24AA256/24LC256/24FC256



## 9.0 PACKAGING INFORMATION

## 9.1 Package Marking Information

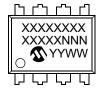


8-Lead DFN-S

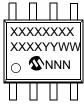




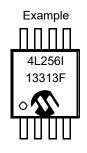
8-Lead PDIP (300 mil)

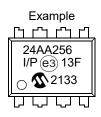


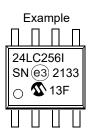
8-Lead SOIC (3.90 mm)











## Package Marking Information (Continued)

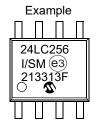






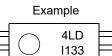








EF4
133
13
<u>_</u>



13F

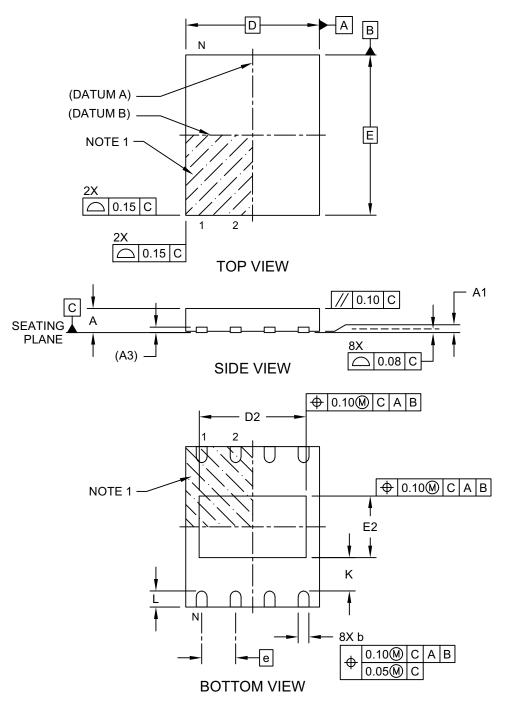
D. (	1 <sup>st</sup> Line Marking Codes								
Part No.	DFN	MSOP	PDIP	SOIC SOIJ		TDFN		TSSOP	CSP
	DFN	IVISOP	PDIP	3010	50IJ	I-Temp.	E-Temp.	1330P C	COP
24AA256	24AA256	4A256T <sup>(1)</sup>	24AA256	24AA256T <sup>(1)</sup>	24AA256	EF6	EF5	4AD	249
24LC256	24LC256	4L256T <sup>(1)</sup>	24LC256	24LC256T <sup>(1)</sup>	24LC256	EF4	EF3	4LD	—
24FC256	24FC256	4F256T <sup>(1)</sup>	24FC256	24FC256T <sup>(1)</sup>	24FC256	EF8	—	4FD	_

**Note 1:** T = Temperature grade (I, E)

r		
Legend	l: XXX	Part number or part number code
	Т	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	JEDEC <sup>®</sup> designator for Matte Tin (Sn)
	9	
Note:	Standard	OTP marking consists of Microchip part number, year code, week
	code and t	traceability code.
Nata		well realize a with respect to the UEDEO $^{\mathbb{R}}$ designator
Note:		nall packages with no room for the JEDEC <sup>®</sup> designator
	(e3), the m	arking will only appear on the outer carton or reel label.
Nata		
Note:		It the full Microchip part number cannot be marked on one line, it will
		l over to the next line, thus limiting the number of available
	characters	for customer-specific information.

## 8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S] Saw Singulated

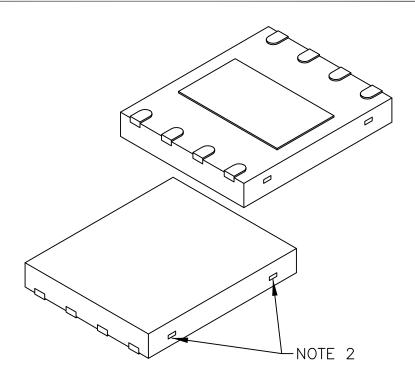
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-122 Rev C Sheet 1 of 2

## 8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S] Saw Singulated

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	
Number of Terminals	Ν		8		
Pitch	е				
Overall Height	А	0.80	0.85	1.00	
Standoff	A1	0.00	0.02	0.05	
Terminal Thickness	A3		0.20 REF		
Overall Length	D		5.00 BSC		
Exposed Pad Length	D2	3.90	4.00	4.10	
Overall Width	E		6.00 BSC		
Exposed Pad Width	E2	2.20	2.30	2.40	
Terminal Width	b	0.30	0.40	0.50	
Terminal Length	L	0.50	0.60	0.75	
Terminal-to-Exposed-Pad	К	0.20	-	-	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

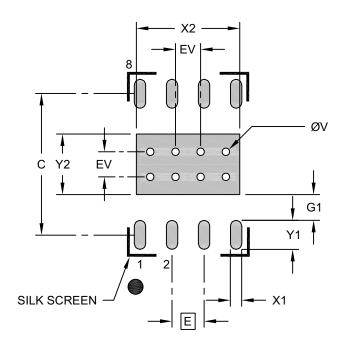
- 2. Package may have one ore more exposed tie bars at ends.
- 3. Package is saw singulated
- 4. Dimensioning and tolerancing per ASME Y14.5M
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-122 Rev C Sheet 2 of 2

## 8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S] Saw Singulated

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



## **RECOMMENDED LAND PATTERN**

Units		Ν	/ILLIMETER:	S
Dimensior	Limits	MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Optional Center Pad Width	X2			2.40
Optional Center Pad Length	Y2			4.10
Contact Pad Spacing	С		5.60	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.15
Contact Pad to Center Pad (X20)	G1	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

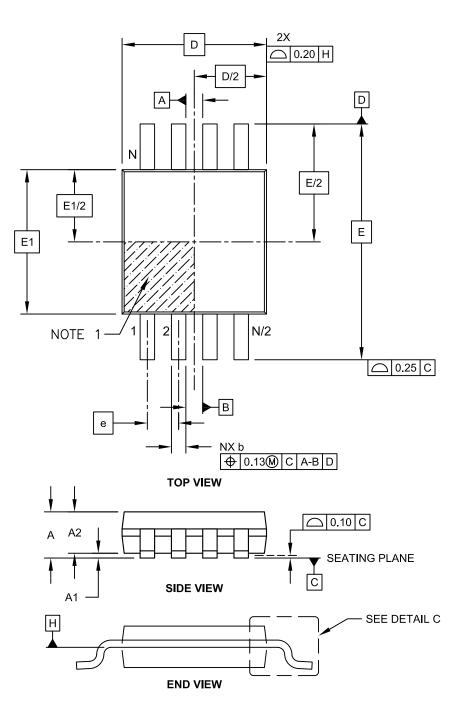
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2122 Rev C

## 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

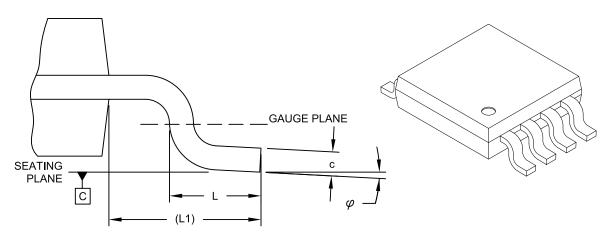
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-111C Sheet 1 of 2

#### 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C

	MILLIMETERS			
Dimensior	n Limits	MIN	NOM	MAX
Number of Pins	N		8	
Pitch	е		0.65 BSC	
Overall Height	Α	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E	4.90 BSC		
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1			
Foot Angle	φ	0°	-	8°
Lead Thickness	С	0.08	-	0.23
Lead Width	b	0.22	-	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or

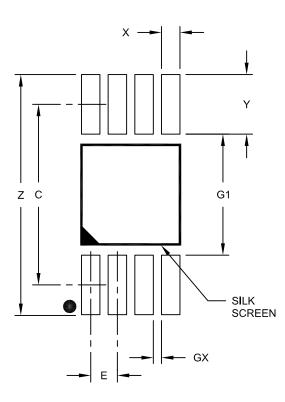
protrusions shall not exceed 0.15mm per side.

Dimensioning and tolerancing per ASME Y14.5M.
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

### 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



## RECOMMENDED LAND PATTERN

	Units		MILLIMETERS		
Dimensio	Dimension Limits		NOM	MAX	
Contact Pitch	E		0.65 BSC		
Contact Pad Spacing	С		4.40		
Overall Width	Z			5.85	
Contact Pad Width (X8)	X1			0.45	
Contact Pad Length (X8)	Y1			1.45	
Distance Between Pads	G1	2.95			
Distance Between Pads	GX	0.20			

#### Notes:

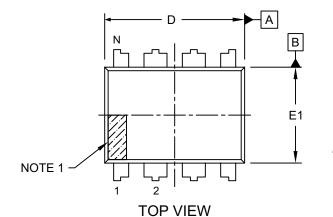
1. Dimensioning and tolerancing per ASME Y14.5M

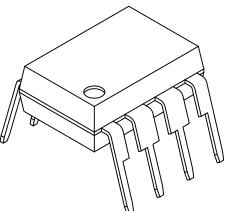
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

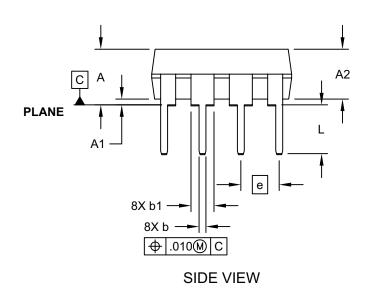
Microchip Technology Drawing No. C04-2111A

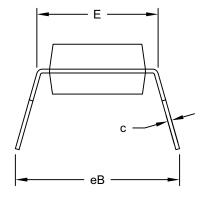
## 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging







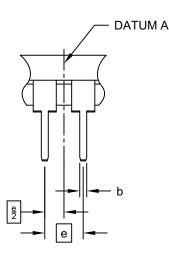


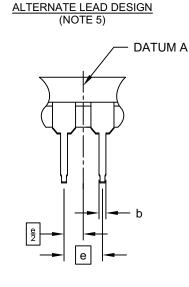
END VIEW

Microchip Technology Drawing No. C04-018-P Rev E Sheet 1 of 2

## 8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





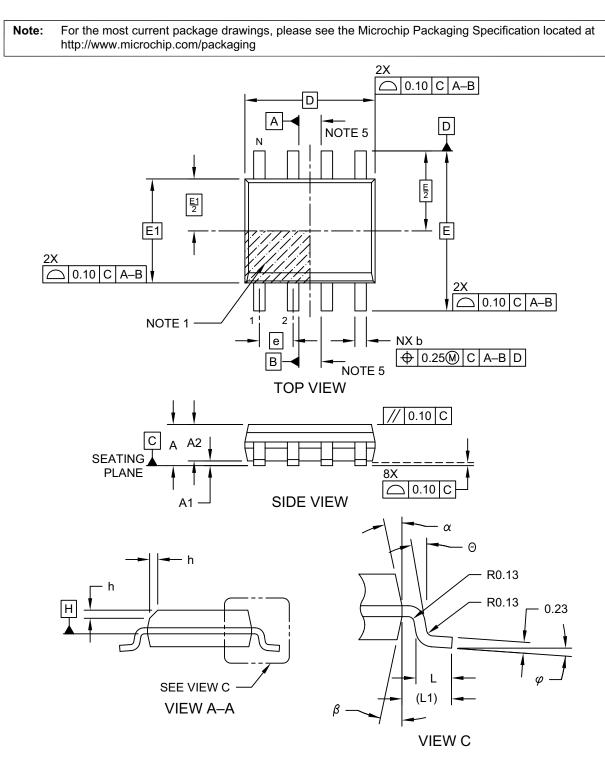
Units		INCHES			
Dimension	Limits	MIN	NOM	MAX	
Number of Pins	Ν	8			
Pitch	е		.100 BSC		
Top to Seating Plane	Α	-	-	.210	
Molded Package Thickness	A2	.115	.130	.195	
Base to Seating Plane	A1	.015	-	-	
Shoulder to Shoulder Width	E	.290	.310	.325	
Molded Package Width	E1	.240	.250	.280	
Overall Length	D	.348	.365	.400	
Tip to Seating Plane	L	.115	.130	.150	
Lead Thickness	С	.008	.010	.015	
Upper Lead Width	b1	.040	.060	.070	
Lower Lead Width	b	.014	.018	.022	
Overall Row Spacing §	eВ	-	-	.430	

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- 5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-P Rev E Sheet 2 of 2

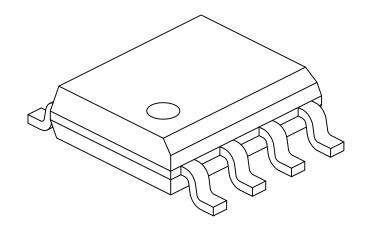
## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]



Microchip Technology Drawing No. C04-057-SN Rev F Sheet 1 of 2

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	Ν	<b>IILLIMETER</b>	S
Dimension	Limits	MIN	NOM	MAX
Number of Pins	Ν		8	
Pitch	е		1.27 BSC	
Overall Height	Α	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	С	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.

4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

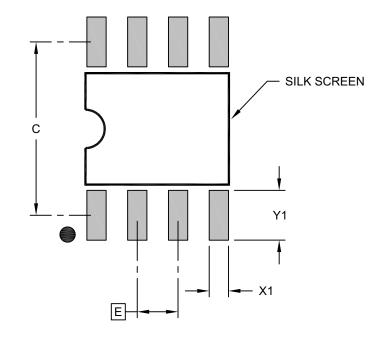
REF: Reference Dimension, usually without tolerance, for information purposes only.

5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev F Sheet 2 of 2

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



## RECOMMENDED LAND PATTERN

	Units		MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	
Contact Pitch	E		1.27 BSC		
Contact Pad Spacing	С		5.40		
Contact Pad Width (X8)	X1			0.60	
Contact Pad Length (X8)	Y1			1.55	

Notes:

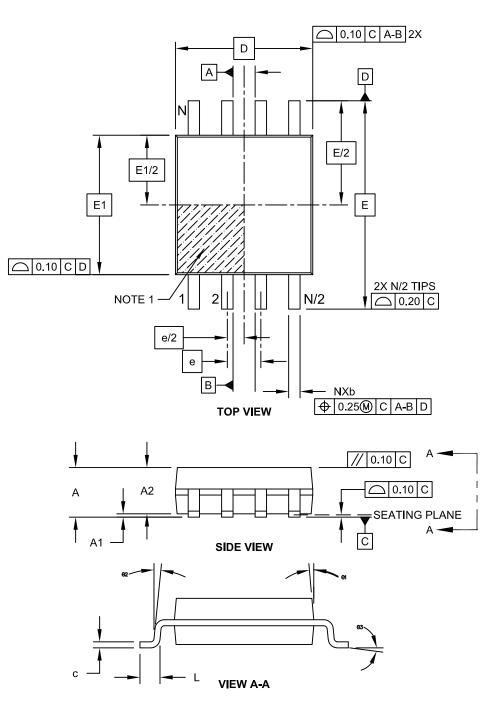
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev F

## 8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

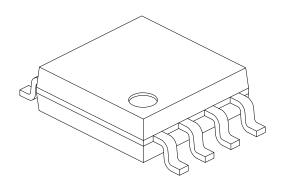
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-056C Sheet 1 of 2

## 8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	Units MILLIMETERS		
Dimensio	on Limits	MIN	NOM	MAX
Number of Pins	N		8	
Pitch	е		1.27 BSC	
Overall Height	Α	1.77	-	2.03
Standoff §	A1	0.05		0.25
Molded Package Thickness	A2	1.75	-	1.98
Overall Width	E		7.94 BSC	
Molded Package Width	E1		5.25 BSC	
Overall Length	D		5.26 BSC	
Foot Length	L	0.51	-	0.76
Lead Thickness	С	0.15	-	0.25
Lead Width	b	0.36	-	0.51
Mold Draft Angle	Θ1	-	-	15°
Lead Angle	Θ2	0°	-	8°
Foot Angle	Θ3	0°	-	8°

Notes:

1. SOIJ, JEITA/EIAJ Standard, Formerly called SOIC

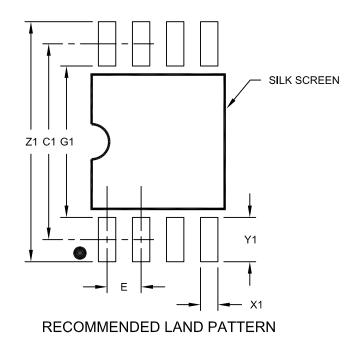
2. § Significant Characteristic

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.

Microchip Technology Drawing No. C04-056C Sheet 2 of 2

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS		
Dimensi	Dimension Limits		NOM	MAX	
Contact Pitch	E	1.27 BSC			
Overall Width	Z1			9.00	
Contact Pad Spacing	C1		7.30		
Contact Pad Width (X8)	X1			0.65	
Contact Pad Length (X8)	Y1			1.70	
Distance Between Pads	G1	5.60			
Distance Between Pads	G	0.62			

Notes:

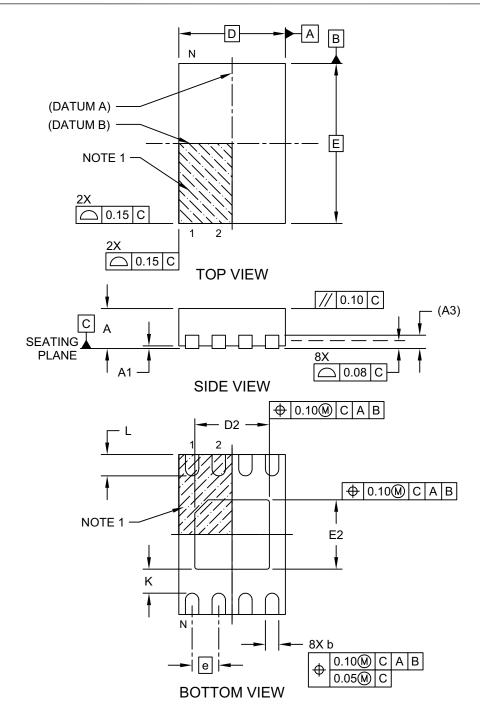
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2056C

### 8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

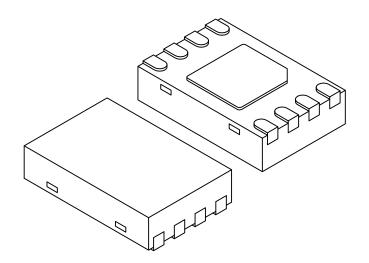
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-129-MN Rev E Sheet 1 of 2

### 8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units			MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX			
Number of Pins	Ν		8				
Pitch	е		0.50 BSC				
Overall Height	Α	0.70	0.75	0.80			
Standoff	A1	0.00	0.02	0.05			
Contact Thickness A3		0.20 REF					
Overall Length	D	2.00 BSC					
Overall Width	E	3.00 BSC					
Exposed Pad Length	D2	1.35	1.40	1.45			
Exposed Pad Width	E2	1.25	1.30	1.35			
Contact Width	b	0.20	0.25	0.30			
Contact Length	L	0.25	0.30	0.45			
Contact-to-Exposed Pad	K	0.20	-	-			

#### Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

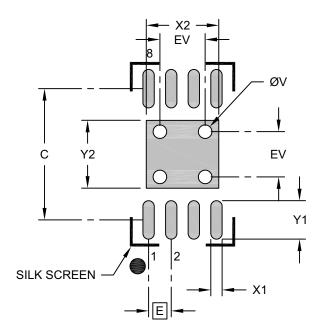
- 2. Package may have one or more exposed tie bars at ends.
- 3. Package is saw singulated
- 4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129-MN Rev E Sheet 2 of 2

#### 8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



#### RECOMMENDED LAND PATTERN

	Units			MILLIMETERS			
Dimensior	Dimension Limits			MAX			
Contact Pitch	Contact Pitch E		0.50 BSC				
Optional Center Pad Width	X2			1.60			
Optional Center Pad Length	Y2			1.50			
Contact Pad Spacing	С		2.90				
Contact Pad Width (X8)	X1			0.25			
Contact Pad Length (X8)	Y1			0.85			
Thermal Via Diameter	V		0.30				
Thermal Via Pitch	EV		1.00				

Notes:

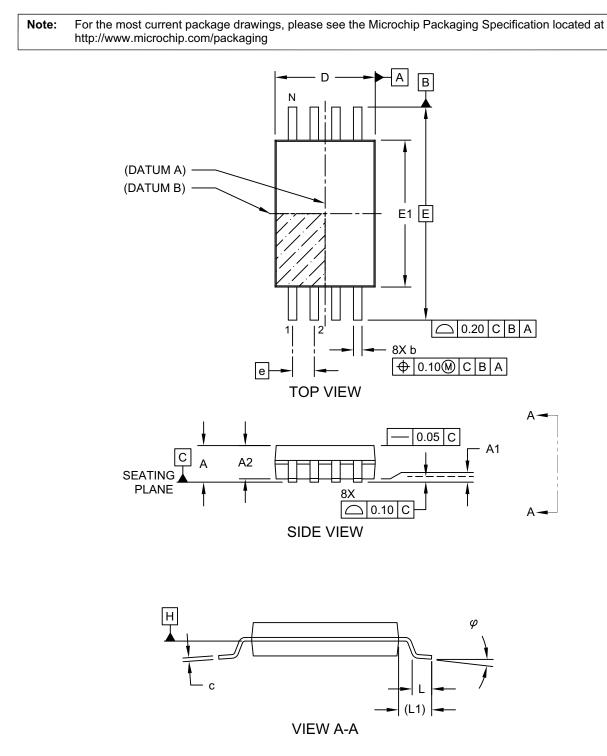
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-129-MN Rev. B

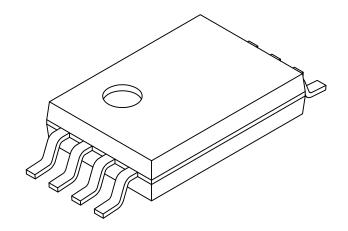
# 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]



Microchip Technology Drawing C04-086 Rev C Sheet 1 of 2

## 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units			MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX			
Number of Pins	N		8				
Pitch	е	0.65 BSC					
Overall Height	Α	-	-	1.20			
Molded Package Thickness	A2	0.80	1.00	1.05			
Standoff	A1	0.05	-	-			
Overall Width	E		6.40 BSC				
Molded Package Width	E1	4.30	4.40	4.50			
Overall Length	D	2.90	3.00	3.10			
Foot Length	L	0.45	0.60	0.75			
Footprint	Footprint L1		1.00 REF				
Lead Thickness	С	0.09	-	0.25			
Foot Angle	φ	0°	4°	8°			
Lead Width	b	0.19	-	0.30			

Notes:

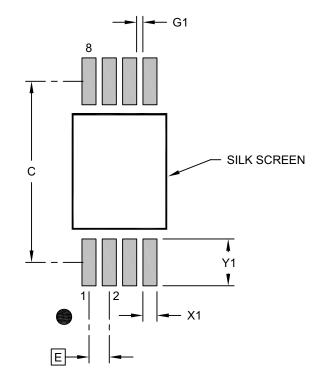
- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
- 3. Dimensioning and tolerancing per ASME Y14.5M
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086 Rev C Sheet 2 of 2

## 8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



## RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimension	Dimension Limits		NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	С		5.80	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.50
Contact Pad to Center Pad (X6)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

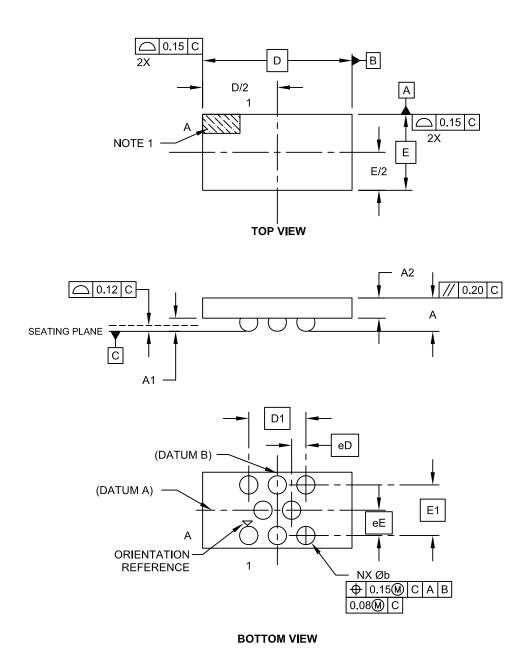
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2086 Rev B

#### 8-Lead Chip Scale Package (CS) - [CSP]

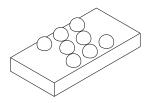
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-6001C Sheet 1 of 2

#### 8-Lead Chip Scale Package (CS) - [CSP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units			MILLIMETERS			
Dimensio	on Limits	MIN	NOM	MAX			
Number of Contacts	N		8				
Overall Grid X-Pitch	Overall Grid X-Pitch E1		0.886 BSC				
Overall Grid Y-Pitch	D1	1.00 BSC					
Adjacent Column X-Pitch	еE	0.443 BSC					
Adjacent Row Y-Pitch	eD		0.25 BSC				
Overall Height	Α	0.53 0.59 0		0.64			
Die Height	A2	0.33	0.36	0.38			
Bump Height	A1	0.20	0.23	0.26			
Overall Width	Е	NOTE 4					
Overall Length	D	NOTE 4					
Ball Diameter		0.30	0.32	0.34			

Notes:

1. Orientation reference feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

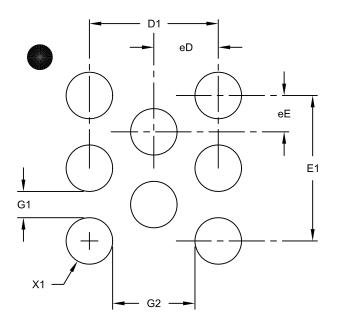
REF: Reference Dimension, usually without tolerance, for information purposes only.

4. Package size varies with specific devices. Please contact your local Microchip representative for specific details

Microchip Technology Drawing C04-6001C Sheet 2 of 2

8-Lead Chip Scale Package (CS) - [CSP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



## RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimensi	Dimension Limits			MAX
Number of Contacts	N	8		
Contact Pitch Y	eE		0.25	
Contact Pitch X	eD		0.443	
Contact Pad Spacing	E1		1.00	
Contact Pad Spacing	D1		0.886	
Contact Pad Diameter (X8)	X1			0.32
Distance Between Pads		0.18		
Distance Between Pads	G2	0.56		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-8001A

# APPENDIX A: REVISION HISTORY

### **Revision X (10/2021)**

Replaced terminology "Master" and "Slave" with "Host" and "Client" respectively; Added Automotive Product Identification System; Updated DFN, PDIP, SOIC, TDFN and TSSOP package drawings.

#### **Revision W (08/2019)**

Updated content throughout for clarification.

#### **Revision V (08/2018)**

Updated First Line Marking Codes table.

#### Revision U (11/2013)

Updated Iccs.

#### Revision T (04/2013)

Added TDFN Package.

#### Revision S (12/2012)

Revise Automotive E-temp.

### Revision R (07/2011)

Added Chip Scale package.

#### Revision Q (05/10)

Revised Table 1-1, Table 1-2, Section 6.1; Updated Package Drawings.

#### **Revision P**

Revised Features; Changed 1.8V voltage to 1.7V; Replaced Package Drawings; Revised markings (8-lead SOIC); Revised Product ID System.

#### **Revision N**

Revised Sections 2.1 and 2.4. Removed 14-Lead TSSOP Package.

#### **Revision M**

Added 1.8V 400 kHz option for 24FC256.

#### **Revision L**

Corrections to Section 1.0, Electrical Characteristics.

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# **PRODUCT IDENTIFICATION SYSTEM (NON-AUTOMOTIVE)**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	<u>[X]</u> <sup>(1)</sup>	<u>-</u> ¥	/XX	Examples: a) 24AA256-I/P: Industrial Temperature,
Device	Tape and Reel Option	Temperature Range	Package	1.7V, PDIP package. b) 24AA256T-I/SN: Tape and Reel, Industrial
Device: Tape and Reel		256-Kbit I <sup>2</sup> C Ser	ial EEPROM S-Kbit I <sup>2</sup> C Serial	Temperature, 1.7V, SOIC package. c) 24AA256-I/ST: Industrial Temperature, 1.7V, TSSOP package. d) 24AA256-I/MS: Industrial Temperature, 1.7V, MSOP package. e) 24LC256-E/P: Extended Temperature, 2.5V, PDIP package.
Option:		nd Reel <sup>(1)</sup>		<ul> <li>f) 24LC256-I/SN: Industrial Temperature, 2.5V, SOIC package.</li> <li>g) 24LC256T-I/SN: Tape and Reel, Industrial</li> </ul>
Temperature Range:		to +85°C (Industri to +125°C (Extend	/	Temperature, 2.5V, SOIC package. h) 24LC256-I/MS: Industrial Temperature, 2.5V, MSOP package.
Package:	6x5x0.6 MS = Plastic I (MSOP P = Plastic (PDIP) SN = Plastic Body, 8 SM = Plastic Body, 8 MNY = Plastic 2x3x0.7 ST = Plastic	) Dual In-Line – 30 Small Outline - N -Lead (SOIC) Small Outline - N -Lead (SOIJ) Dual Flat, No Lea '5 mm Body, 8-Le Thin Shrink Smal (TSSOP)	ead (DFN-S) ne Package, 8-Lead 0 mil Body, 8-Lead larrow, 3.90 mm fedium, 5.28 mm ad Package - ead (TDFN) Il Outline – 4.4 mm,	<ul> <li>i) 24FC256-I/P: Industrial Temperature, 1.7V, High-Speed, PDIP package.</li> <li>j) 24FC256-I/SN: Industrial Temperature, 1.7V, High-Speed, SOIC package.</li> <li>k) 24FC256T-I/SN: Tape and Reel, Industrial Temperature, 1.7V, High-Speed, SOIC package.</li> <li>l) 24AA256T-CS16K: Tape and Reel, Industrial Temperature, 1.7V, Chip Scale package.</li> <li>m) 24AA256T-E/SN: Tape and Reel, Extended Temperature, 1.7V, SOIC package.</li> <li>Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.</li> <li>2: 16K indicates 160K technology.</li> </ul>

# **PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	<u>[X]<sup>(1)</sup></u>	¥	<u>/xx</u>	<u>xxx<sup>(2, 3)</sup></u>	Examples:
Device	Tape and Reel Option	Temperature Range	Package	Variant	<ul> <li>a) 24LC256T-I/SN16KVAO: Tape and Reel, Automotive Grade 3, 2.5V, SOIC Package.</li> <li>b) 24LC256T-I/ST16KVAO: Tape and Reel,</li> </ul>
Device: Tape and Reel	24FC256 =	2.5V, 256-Kbit I <sup>2,</sup> 1.7V, High-Spee EEPROM Standard packag	d, 256-Kbit l <sup>2</sup>	<sup>2</sup> C Serial	<ul> <li>Automotive Grade 3, 2.5V, TSSOP Package.</li> <li>c) 24LC256T-I/SM16KVAO: Tape and Reel, Automotive Grade 3, 2.5V, SOIJ Package.</li> <li>d) 24FC256T-E/ST16KVAO: Tape and Reel, Automotive Grade 1, High-Speed, 1.7V.</li> </ul>
Option:		Tape and Reel <sup>(1)</sup>		57	TSSOP Package.
Temperature Range: Package:	E = MS = SN = SM = ST =	-40°C to +85°C -40°C to +125°C Plastic Micro Sma 8-Lead (MSOP) Plastic Small Outl Body, 8-Lead (SC Plastic Small Outl Body, 8-Lead (SC Plastic Thin Shrin 4.4 mm, 8-Lead (	C (AEC-Q100 all Outline Pa line – Narrow DIC) ine – Medium DIJ) ak Small Outl TSSOP)	) Grade 1) ckage, r, 3.90 mm h, 5.28 mm ine,	<ul> <li>Note 1: Tape and Reel identifier of appears in the catalog part num description. This identifier is used ordering purposes and is not prin on the device package. Check v your Microchip Sales Office package availability with the Ta and Reel option.</li> <li>2: The VAO/VXX automotive varia have been designed, manufactur tested and qualified in accordar with AEC-Q100 requirements automotive applications.</li> </ul>
Variant <sup>(2,3)</sup> :	15KVXX = 16KVAO =	Standard Automo Customer-Specifi Process <sup>(4)</sup> Standard Automo Customer-Specifi Process	c Automotive tive, 16K Pro	, 15K ocess	<ol> <li>For customers requesting a PPAI customer-specific part number be generated and provided. A PP is not provided for VAO part nu bers.</li> </ol>
					4: Not recommended for new desig

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