Product Change Notification / RMES-16MJGC219

Date:

17-Sep-2021

Product Category:

8-bit Microcontrollers, Memory

PCN Type:

Manufacturing Change

Notification Subject:

CCB 4098 Final Notice: Qualification of 36.5K process technology for selected products of the 25AA640A and 25LC640A device families.

Affected CPNs:

RMES-16MJGC219_Affected_CPN_09172021.pdf
RMES-16MJGC219_Affected_CPN_09172021.csv

Notification Text:

PCN Status: Final notification

PCN Type: Manufacturing Change

Microchip Parts Affected: Please open one of the files found in the Affected CPNs section

NOTE: For your convenience Microchip includes identical files in two formats (.pdf and .xls).

Description of Change: Qualification of 36.5K process technology for selected products of the 25AA640A and 25LC640A device families.

Pre and Post Change Summary:

	Pre Change	Post Change	
Wafer Technology	160K wafer technology	160K wafer technology	36.5K wafer technology

Fabrication Location	Microchip Fabrication Sites FAB 2 and FAB4 (Tempe, AZ and Gresham, OR, USA)	Microchip Fabrication Sites FAB 2 and FAB4 (Tempe, AZ and Gresham, OR, USA)	Microchip Technology Colorado – Fab 5 (MCSO)
Wafer Diameter	8 inches (200 mm)	8 inches (200 mm)	6 inches (150mm)
Quality certification	ISO/TS16949	ISO/TS16949	ISO/TS16949

Impacts to Data Sheet: None

Change Impact: None

Reason for Change: To improve manufacturability by qualifying an additional fabrication site.

Change Implementation Status: In Progress

Estimated First Ship Date:
December 01, 2021 (date code: 2149)

NOTE: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

Time Table Summary:

	September 2021					**>**	**December 2021**			
Workweek	36	37	38	39	40		49	50	51	52
Final PCN Issue Date			X							
Qual Report Availability			X							
Estimated Implementation Date							X			

Method to Identify Change: Traceability code

Qualification Report: Please open the attachments included with this PCN labeled as PCN_#_Qual_Report

Revision History: September 17, 2021: Issued final notification.

The change described in this PCN does not alter Microchip's current regulatory compliance regarding the material content of the applicable products.

Attachments:

PCN_RMES-16MJGC219_Qual_Report.pdf

Please contact your local Microchip sales office with questions or concerns regarding this notification.

Terms and Conditions:

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If you wish to change your PCN profile, including opt out, please go to the PCN home page select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

25AA640A-E/MF
25AA640A-E/MS
25AA640A-E/P
25AA640A-E/SN
25AA640A-E/ST
25AA640A-I/MF
25AA640A-I/MS
25AA640A-I/P
25AA640A-I/SN
25AA640A-I/ST
25AA640AT-E/MF
25AA640AT-E/MNY
25AA640AT-E/MS
25AA640AT-E/SN
25AA640AT-E/ST
25AA640AT-I/MNY
25AA640AT-I/MS
25AA640AT-I/SN
25AA640AT-I/ST
25AA640AX-I/ST
25AA640AXT-I/ST
25LC640A-E/MF
25LC640A-E/MS
25LC640A-E/P
25LC640A-E/SN
25LC640A-E/ST
25LC640A-H/SN
25LC640A-I/MF
25LC640A-I/MS
25LC640A-I/P
25LC640A-I/SN
25LC640A-I/ST
25LC640AT-E/MNY
25LC640AT-E/MS
25LC640AT-E/SN
25LC640AT-E/ST
25LC640AT-H/SN
25LC640AT-I/MNY
25LC640AT-I/MS
25LC640AT-I/SN
25LC640AT-I/ST
25LC640AX-E/ST
25LC640AX-I/ST
25LC640AXT-E/ST
25LC640AXT-I/ST

QUALIFICATION REPORT SUMMARY

RELIABILITY LABORATORY

PCN #: RMES-16MJGC219

Date:
March 12, 2021

Qualification of 36.5K process technology for selected products of the 25AA640A and 25LC640A device families.

Purpose: Qualification of 36.5K process technology for selected products of the 25AA640A and 25LC640A device families.

I. Summary:

In keeping with guidelines established in Microchip specification QCI-39000, three lots of 365S6 product were stressed to meet JEDEC JESD47 guidelines. Stress tests were designed to be compatible with eventual AEC Grade 0 Qualification, and those results are included as a 'work in progress'.

Conclusion:

Based on the results, 365S6 product built at FAB5 meets the guidelines specified in the qualification plan. Therefore, the C2 mask revision of the device can be released to production as an Industrial Grade product for standard temperature (I grade; -40C to +85C), extended temperature (E grade -40C and +125C), and high temperature (H grade -40C to +150C) applications.

II. Device Description:

Device	25LC640A,25AA640A, AT25640B, 25CS640
Released Mask	365S6 C2
MSL	3305
CCB#	4098
Product	64kBit SPI SEEPROM Memory
Qual Report /Memo log No.	ML032021003A
Document Revision	A

III. Qualification Material:

Test Lot	Lot 1	Lot 2	Lot 3
CPN	25CS640	25CS640	25CS640
MASK	365S6 C1	365S6 C2	365S6 C2
WAFER LOT	C0U0480B	B0U0481	0X1410B
WAFER FAB	FAB5	FAB5	FAB5
ASSEMBLY LOT	MTAI210701652.000	MTAI211802312.000	MTAI213702225.300
PACKAGE	8L SOIC	8L SOIC	8L SOIC
ASSEMBLY SITE	MTAI	MTAI	MTAI
FINAL TEST	MTAI	MTAI	MTAI
QUAL TESTS –SJ	ELFR, DLT, END/DLT, END/DR, ESD/LU, END (25C, 85C, 125C, 150C))	ELFR, DLT, END/DLT, END/DR, ESD/LU, END (25C, 85C, 125C, 150C)	ELFR, DLT, END/DLT, END/DR, END (25C, 85C, 125C, 150C)

IV. Qualification Data:

Endurance / Dynamic Life Test (Stress conducted at MCHP San Jose)

Stress Method	MIL-STD 883 Method 1033		
Stress Condition	T_a = 85ºC / V_{cc} = 5.5V / 400,000 cycles (Write 0x00h)		
Min Sample Size	77 pieces/lot		
Test Temperatures	25C, -40C, 85C, 125C, 150C		
Lot #; Fail / Pass	Lot 1; 0 Fails / 92	Lot 2; 0 Fails / 92	Lot 3; 0 Fails / 92
Stress Method	MIL-STD 883 Method 1005		
Stress Condition	T_a = 150ºC / V_{CC}= 5.5V / 408 hours		
Min Sample Size	77 pieces/lot		
Test Temperatures	25C, -40C, 85C, 125C, 150C		
Readpoint 1	96 hours		
Lot #; Fail / Pass	Lot 1; 0 Fails / 92	Lot 2; 0 Fails / 92	Lot 3; 0 Fails / 92
Readpoint 2	+312 hours (Minimum 408 hours Total)		
Lot # Fail / Pass	Lot 1; 0 Fails / 92	Lot 2; 0 Fails / 92	Lot 3; 0 Fails / 92

Endurance / Data Retention (Stress conducted at MCHP San Jose)

Stress Method	MIL-STD 883 Method 1033		
Stress Condition	T_a = 85ºC / V_{cc} = 5.5V / 400,000 cycles (Write 0x00h)		
Min Sample Size	236 pieces/lot		
Test Temperatures	25C, -40C, 85C, 125C, 150C		
Lot #; Fail / Pass	Lot 1 0 Fails / 236	Lot 2; 0 Fails / 236	Lot 3; 0 Fails / 236
Stress Method	JESD22A-103		
Stress Condition	T_a = 175ºC 504 hours		
Min Sample Size	231 pieces/lot		
Test Temperatures	25C, -40C, 85C, 125C, 150C		
Readpoint 1	96 hours		
Lot # Fail / Pass	Lot 1; 0 Fails / 236	Lot 2; 0 Fails / 246	Lot 3; 0 Fails / 246
Readpoint 2	+408 hours (504 hours Total)		
Lot # Fail / Pass	Lot 1; 0 Fails / 236	Lot 2; 0 Fails / 246	Lot 3; 0 Fails / 246

Endurance Testing (Stress conducted at MCHP San Jose)

Test Method	MIL-STD 883 Method 1033
Test Condition	Ta = +25°C / V_{CC}= 5V / 4,000,000 cycles Write 0x00h
Min Sample Size	Not Required
Readpoint 1 – 9	Every 400,000 Cycles
Lot #; Fail / Pass, Test Criteria	Lot 1; 0 / 92, QC Test 25C, -40C, 85C, 125C, 150C 0 / 10. Margin Test at +25C
Readpoint 10	4,000,000 Cycles
Lot #; Fail / Pass, Test Criteria	Lot 1; 0 / 92, QC Test 25C, -40C, 85C, 125C, 150C 0 / 10. Margin Test at +25C

Early Life Reliability (ELFR) + Dynamic Life Test (Stress conducted at MCHP San Jose)

Stress Method	MIL-STD 883 Method 1005		
Stress Condition	T_a = 150ºC / V_{CC}= 5.5V / 408 hours		
Min Sample Size	ELFR 800 Pieces/Lot, 0 Fails		
Readpoint 1 Test Temperatures	24 hours 25C, -40C, 85C, 125C, 150C		
Lot# Fail / Pass	Lot 1 0 Fails / 810	Lot 3 0 Fails / 815	Lot 4 0 Fails / 814
Min Sample Size	DLT 600 Pieces/Lot, 0 Fails		
Readpoint 2 Test Temperatures	+408 hours (504 Total) 25C, -40C, 85C, 125C, 150C		
Lot# Fail / Pass	Lot 1 0 Fails / 610	Lot 3 0 Fails / 615	Lot 4 0 Fails / 615

Electrical distributions of key parametric measurements were captured from all three lots.

ESD & Latchup Characterization (Stress conducted at MCHP San Jose)

Product Lot 1 Rev C1

Test	Sample Size	Reference Method	Highest passing Result
ESD – HBM	15	JEDEC JS-001-2017	Pass ±6000 V
CDM	18	JEDEC JS-002	Pass ±2000 V
Latch Up @ 25°C	6	JESD78	200mAmp Pass
Latch Up @ 85°C	6	JESD78	200mAmp Pass
Latch Up @ 125°C	6	JESD78	200mAmp Pass
Latch Up @ 150°C	6	JESD78	200mAmp Pass

Product Lot 2 Rev C2

Test	Sample Size	Reference Method	Highest passing Result
ESD – HBM	15	JEDEC JS-001-2017	Pass ±6000 V
CDM	18	JEDEC JS-002	Pass ±2000 V
Latch Up @ 25°C	6	JESD78	200mAmp Pass
Latch Up @ 85°C	6	JESD78	200mAmp Pass
Latch Up @ 125°C	6	JESD78	200mAmp Pass
Latch Up @ 150°C	6	JESD78	200mAmp Pass

All parts were tested at -40°C, 25°C, 85°C, 125°C, 150°C and passed all criteria of the tests.