



## Product Change Notification / SYST-04IAMU502

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**Date:**

06-Nov-2020

**Product Category:**

8-bit Microcontrollers

**PCN Type:**

Silicon Die Revision

**Notification Subject:**

ERRATA - ATtiny212/412 Silicon Errata and Data Sheet Clarification

**Affected CPNs:**

[SYST-04IAMU502\\_Affected\\_CPN\\_11062020.pdf](#)

[SYST-04IAMU502\\_Affected\\_CPN\\_11062020.csv](#)

**Notification Text:**

SYST-04IAMU502

Microchip has released a new Product Documents for the ATtiny212/412 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at [ATtiny212/412 Silicon Errata and Data Sheet Clarification](#).

**Notification Status:** Final**Description of Change:** 1) Added die revision C

## 2) Added new errata:

- Device: Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration

## Values

- ADC: ADC Interrupt Flags Cleared When Reading RESH
- CCL: The CCL Must be Disabled to Change the Configuration of a Single LUT
- TCA: Restart Will Reset Counter Direction in NORMAL and FRQ Mode
- TCB: CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode
- TCD: Asynchronous Input Events Not Working When TCD Counter Prescaler is Used
- USART:
  - Full Range Duty Cycle Not Supported When Validating LIN Sync Field
  - Open-Drain Mode Does Not Work When TXD is Configured as Output
  - Start-of-Frame Detection Can Unintentionally be Enabled in Active Mode when RXCIF is '0'

**Impacts to Data Sheet:** None

**Reason for Change:** To Improve Productivity

**Change Implementation Status:** Complete

**Estimated First Ship Date:** 06 Nov 2020

NOTE: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

**Markings to Distinguish Revised from Unrevised Devices:** Traceability Code

## **Attachments:**

[ATtiny212/412 Silicon Errata and Data Sheet Clarification](#)

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Affected Catalog Part Numbers (CPN)

ATTINY212-SSF

ATTINY212-SSFR

ATTINY212-SSN

ATTINY212-SSNR

ATTINY412-SSF

ATTINY412-SSFR

ATTINY412-SSN

ATTINY412-SSNR



# ATtiny212/412

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## ATtiny212/412 Silicon Errata and Data Sheet Clarification

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The ATtiny212/412 devices you have received conform functionally to the current device data sheet ([www.microchip.com/DS40001911](http://www.microchip.com/DS40001911)), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATtiny212/412 devices.

**Notes:**

- This document summarizes all the silicon errata issues from all revisions of silicon, previous as well as current
- Refer to the Device/Revision ID section in the current device data sheet ([www.microchip.com/DS40001911](http://www.microchip.com/DS40001911)) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

### 1. Silicon Issue Summary

#### Legend

- Erratum is not applicable.
- X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision		
		Rev. A	Rev. B	Rev. C
Device	2.2.1 The Temperature Sensor is Not Calibrated on Parts with Date Code 727, 728 and 1728 (Year 2017, Week 27/28)	-	X	-
	2.2.2 Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values	X	X	X
AC	2.3.1 AC Interrupt Flag Not Set Unless Interrupt is Enabled	X	-	-
	2.3.2 False Triggers May Occur Under Certain Conditions	X	-	-
ADC	2.4.1 One Extra Measurement Performed After Disabling ADC Free-Running Mode	X	X	X
	2.4.2 Changing ADC Control Bits During Free-Running Mode not Working	X	-	-
	2.4.3 ADC Wake-Up with WCMP	X	-	-
	2.4.4 SAMPDLY and ASDV Does Not Work Together With SAMPLEN	X	-	-
	2.4.5 ADC Functionality Cannot be Ensured with CLKADC Above 1.5 MHz and a Setting of 25% Duty Cycle	X	X	X
	2.4.6 ADC Performance Degrades with CLKADC Above 1.5 MHz and VDD < 2.7V	X	X	X
	2.4.7 ADC Interrupt Flags Cleared When Reading RESH	X	-	-
CCL	2.5.1 Connecting LUTs in Linked Mode Requires OUTEN Set to '1'	X	X	X
	2.5.2 D-latch is Not Functional	X	X	X
	2.5.3 The CCL Must be Disabled to Change the Configuration of a Single LUT	X	X	X
RTC	2.6.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler	X	X	X
	2.6.2 Disabling the RTC Stops the PIT	X	X	X
TCA	2.7.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X	X	X
TCB	2.8.1 Minimum Event Duration Must Exceed the Selected Clock Period	X	X	X
	2.8.2 The TCB Interrupt Flag is Cleared When Reading CCMPH	X	-	-
	2.8.3 TCB Input Capture Frequency and Pulse-Width Measurement Mode Not Working with Prescaled Clock	X	-	-
	2.8.4 The TCA Restart Command Does Not Force a Restart of TCB	X	X	X
	2.8.5 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode	X	X	X
TCD	2.9.1 Asynchronous Input Events Not Working When TCD Counter Prescaler is Used	X	X	X

.....continued				
Peripheral	Short Description	Valid for Silicon Revision		
		Rev. A	Rev. B	Rev. C
TWI	2.10.1 TIMEOUT Bits in the TWI.MCTRLB Register are Not Accessible	X	-	-
	2.10.2 TWI Smart Mode Gives Extra Clock Pulse	X	-	-
	2.10.3 TWI Master Mode Wrongly Detects the Start Bit as a Stop Bit	X	-	-
	2.10.4 The TWI Master Enable Quick Command is Not Accessible	X	-	-
USART	2.11.1 TXD Pin Override Not Released When Disabling the Transmitter	X	X	X
	2.11.2 Frame Error on a Previous Message May Cause False Start Bit Detection	X	X	X
	2.11.3 Full Range Duty Cycle Not Supported When Validating LIN Sync Field	X	X	X
	2.11.4 Open-Drain Mode Does Not Work When TXD is Configured as Output	X	X	X
	2.11.5 Start-of-Frame Detection Can Unintentionally be Enabled in Active Mode when RXCIF is '0'	X	X	X

## 2. Silicon Errata Issues

### 2.1 Errata Details

- Erratum is not applicable.
- X Erratum is applicable.

### 2.2 Device

#### 2.2.1 The Temperature Sensor is Not Calibrated on Parts with Date Code 727, 728 and 1728 (Year 2017, Week 27/28)

The temperature sensor is not calibrated on parts with date code 727/728 (used on QFN packages) and 1728 (used on SOIC packages).

##### Work Around

If temperature sensor calibration data is required, devices with the affected date code may be returned through the Microchip RMA service. Devices with this date code are no longer shipped by Microchip.

##### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
-	X	-

#### 2.2.2 Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values

Writing the OSCLOCK fuse in FUSE.OSCCFG to '1' prevents the automatic loading of calibration values from the signature row. The device will run with an uncalibrated OSC20M oscillator.

##### Work Around

Do not use OSCLOCK for locking the oscillator calibration value. The oscillator calibration value can be locked by writing LOCK in CLKCTRL.OSC20MCALIBB to '1'.

##### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

### 2.3 AC - Analog Comparator

#### 2.3.1 AC Interrupt Flag Not Set Unless Interrupt is Enabled

ACn.STATUS.CMP is not set if the ACn.INTCTRL.CMP is not set.

##### Work Around

Enable ACn.INTCTRL.CMP or use ACn.STATUS.STATE for polling.

### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

### 2.3.2 False Triggers May Occur Under Certain Conditions

False triggers may occur on falling input pin:

- For common-mode voltage below 0.5V
- For common-mode voltage above 0.5V if the slew rate is greater than 1 V/μs

#### Work Around

None.

### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

## 2.4 ADC - Analog-to-Digital Converter

### 2.4.1 One Extra Measurement Performed After Disabling ADC Free-Running Mode

The ADC may perform one additional measurement after clearing ADCn.CTRLA.FREERUN.

#### Work Around

Write ADCn.CTRLA.ENABLE to '0' to stop the Free-Running mode immediately.

### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

### 2.4.2 Changing ADC Control Bits During Free-Running Mode not Working

If control signals are changed during Free-Running mode, the new configuration is not properly taken into account in the next measurement. This is valid for the ADC.CTRLB, ADC.CTRLC, ADC.SAMPCTRL registers and the ADC.MUXPOS, ADC.WINLT and ADC.WINHT registers.

#### Work Around

Disable ADC Free-Running mode before updating the ADC.CTRLB, ADC.CTRLC, ADC.SAMPCTRL, ADC.MUXPOS, ADC.WINLT or ADC.WINHT registers.

### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

### 2.4.3 ADC Wake-Up with WCMP

When waking up from Standby sleep mode with ADC WCMP interrupt, the ADC is disabled for a few cycles before the device enters Active mode. A new INITDLY is required before the next conversion.

#### Work Around

Use INITDLY before the next conversion.



### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

#### 2.4.4 SAMPDLY and ASDV Does Not Work Together With SAMPLEN

Using SAMPCTRL.SAMPLEN at the same time as CTRLD.SAMPDLY or CTRLD.ASDV will cause an unpredictable sampling length.

#### Work Around

When setting SAMPCTRL.SAMPLEN greater than 0x0, the CTRLD.SAMPDLY and CTRLD.ASDV must be cleared.

### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

#### 2.4.5 ADC Functionality Cannot be Ensured with CLK<sub>ADC</sub> Above 1.5 MHz and a Setting of 25% Duty Cycle

The ADC functionality cannot be ensured if CLK<sub>ADC</sub> > 1.5 MHz with ADCn.CALIB.DUTYCYC set to '1'.

#### Work Around

If ADC is operated with CLK<sub>ADC</sub> > 1.5 MHz, ADCn.CALIB.DUTYCYC must be set to '0' (50% duty cycle).

### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

#### 2.4.6 ADC Performance Degrades with CLK<sub>ADC</sub> Above 1.5 MHz and VDD < 2.7V

The ADC INL performance degrades if CLK<sub>ADC</sub> > 1.5 MHz and ADCn.CALIB.DUTYCYC set to '0' for VDD < 2.7V.

#### Work Around

None.

### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

#### 2.4.7 ADC Interrupt Flags Cleared When Reading RESH

ADCn.INTFLAGS.RESRDY and ADCn.INTFLAGS.WCOMP are cleared when reading ADCn.RESH.

#### Work Around

In 8-bit mode, read ADCn.RESH to clear the flag or clear the flag directly.

### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

## 2.5 CCL - Configurable Custom Logic

### 2.5.1 Connecting LUTs in Linked Mode Requires OUTEN Set to '1'

Connecting the LUTs in linked mode requires LUTnCTRLA.OUTEN set to '1' for the LUT providing the input source.

**Work Around**

Use an event channel to link the LUTs or do not use the corresponding I/O pin for other purposes.

**Affected Silicon Revisions**

Rev. A	Rev. B	Rev. C
X	X	X

### 2.5.2 D-latch is Not Functional

The CCL D-latch is not functional.

**Work Around**

None.

**Affected Silicon Revisions**

Rev. A	Rev. B	Rev. C
X	X	X

### 2.5.3 The CCL Must be Disabled to Change the Configuration of a Single LUT

To reconfigure a LUT, the CCL peripheral must be disabled (write ENABLE in CCL.CTRLA to '0'). Writing ENABLE to '0' will disable all the LUTs, and affects the LUTs not under reconfiguration.

**Work Around**

None

**Affected Silicon Revisions**

Rev. A	Rev. B	Rev. C
X	X	X

## 2.6 RTC - Real-Time Counter

### 2.6.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler

Any write to the RTC.CTRLA register resets the 15-bit prescaler resulting in a longer period on the current count or period.

**Work Around**

None.

**Affected Silicon Revisions**

Rev. A	Rev. B	Rev. C

X	X	X
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### 2.6.2 Disabling the RTC Stops the PIT

Writing RTC.CTRLA.RTCEN to '0' will stop the PIT.

Writing RTC.PITCTRLA.PITEN to '0' will stop the RTC.

#### Work Around

Do not disable the RTC or the PIT if any of the modules are used.

#### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

## 2.7 TCA - Timer/Counter A

### 2.7.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to the NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset direction to default. The default is counting upwards.

#### Work Around

None.

#### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

## 2.8 TCB - Timer/Counter B

### 2.8.1 Minimum Event Duration Must Exceed the Selected Clock Period

Event detection will fail if TCBn receives an input event with a high/low period shorter than the period of the selected clock source (CLKSEL in TCBn.CTRLA). This applies to the TCB modes (CNTMODE in TCBn.CTRLB) *Time-Out Check* and *Input Capture Frequency and Pulse-Width Measurement* mode.

#### Work Around

Ensure that the high/low period of input events is equal to or longer than the period of the selected clock source (CLKSEL in TCBn.CTRLA).

#### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

### 2.8.2 The TCB Interrupt Flag is Cleared When Reading CCMPH

TCBn.INTFLAGS.CAPT is cleared when reading TCBn.CCMPH instead of CCMPL.

#### Work Around

Read both TCBn.CCMPL and TCBn.CCMPH.

### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

### 2.8.3 TCB Input Capture Frequency and Pulse-Width Measurement Mode Not Working with Prescaled Clock

The TCB Input Capture Frequency and Pulse-Width Measurement mode may lock to Freeze state if CLKSEL in TCB.CTRLA is set to any other value than 0x0.

#### Work Around

Only use CLKSEL equal to 0x0 when using Input Capture Frequency and Pulse-Width Measurement mode.

### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

### 2.8.4 The TCA Restart Command Does Not Force a Restart of TCB

The TCA restart command does not force a restart of the TCB when TCB is running in SYNCUPD mode. TCB is restarted only after a TCA OVF.

#### Work Around

None.

### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

### 2.8.5 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode

When the TCB is operating in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CNT and CCMP registers operate as 16-bit registers for read and write. They cannot be read or written independently.

#### Work Around

Use 16-bit register access. Refer to the data sheet for further information.

### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

## 2.9 TCD - Timer/Counter D

### 2.9.1 Asynchronous Input Events Not Working When TCD Counter Prescaler is Used

When the TCD is configured to use asynchronous input events (CFG in TCDn.EVCTRLx is '0x2') and the TCD Counter Prescaler (CNTPRES in TCDn.CTRLA) is different from '0x0' events can be missed.

### Work Around

Use the TCD Synchronization Prescaler (SYNCPRES in TCDn.CTRLA) instead of the TCD Counter Prescaler. Alternatively, use synchronous input events (CFG in TCDn.EVCTRLx is not '0x2') if the input events are longer than one CLK\_TCD\_CNT cycle.

### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

## 2.10 TWI - Two-Wire Interface

### 2.10.1 TIMEOUT Bits in the TWI.MCTRLB Register are Not Accessible

The TIMEOUT bits in the TWI.MCTRLB register are not accessible from software.

### Work Around

When initializing TWI, BUSSTATE in TWI.MSTATUS must be brought into IDLE state by writing 0x1 to it.

### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

### 2.10.2 TWI Smart Mode Gives Extra Clock Pulse

TWI Master with Smart mode enabled gives an extra clock pulse on the SCL line after sending NACK.

### Work Around

None.

### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

### 2.10.3 TWI Master Mode Wrongly Detects the Start Bit as a Stop Bit

If TWI is enabled in Master mode followed by an immediate write to the MADDR register, the bus monitor recognizes the Start bit as a Stop bit.

### Work Around

Wait for a minimum of two clock cycles from TWI.MCTRLA.ENABLE until TWI.MADDR is written.

### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

### 2.10.4 The TWI Master Enable Quick Command is Not Accessible

TWI.MCTRLA.QCEN is not accessible from software.

### Work Around

None.

### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	-	-

## 2.11 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

### 2.11.1 TXD Pin Override Not Released When Disabling the Transmitter

The USART will not release the TXD pin override if:

- The USART transmitter is disabled by writing the TXEN bit in USART.CTRLB to '0' while the USART receiver is disabled (RXEN in USART.CTRLB is '0')
- Both the USART transmitter and receiver are disabled at the same time by writing the TXEN and RXEN bits in USART.CTRLB to '0'

#### Work Around

There are two possible work arounds:

- Make sure the receiver is enabled (RXEN in USART.CTRLB is '1') while disabling the transmitter (writing TXEN in USART.CTRLB to '0')
- Writing to any register in the USART after disabling the transmitter will start the USART for long enough to release the pin override of the TXD pin

### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

### 2.11.2 Frame Error on a Previous Message May Cause False Start Bit Detection

A false start bit detection will trigger if receiving a frame with RXDATAH.FERR set and reading the RXDATAL before the RxD line goes high.

#### Work Around

Wait for the RXD pin to go high before reading RXDATA, for instance, by polling the bit in PORTn.IN where the RXD pin is located.

### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

### 2.11.3 Full Range Duty Cycle Not Supported When Validating LIN Sync Field

For the LIN sync field, the USART is validating each bit to be within  $\pm 15\%$  instead of the time between falling edges as described in the LIN specification, which allows a minimum duty cycle of 43.5% and a maximum duty cycle of 57.5%.

#### Work Around

None.

### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C

X	X	X
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### 2.11.4 Open-Drain Mode Does Not Work When TXD is Configured as Output

When the USART TXD pin is configured as an output, it can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

#### Work Around

Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '0' when using Open-Drain mode.

#### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

### 2.11.5 Start-of-Frame Detection Can Unintentionally be Enabled in Active Mode when RXCIF is '0'

The Start-of-Frame Detector can unintentionally be enabled when the device is in Active mode and when the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is '0'. If the Receive Data (RXDATA) registers are read while receiving new data, RXCIF is cleared, and the Start-of-Frame Detector will be enabled and falsely detects the following falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data. Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode, so no interrupt will be triggered.

#### Work Around

Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in Active mode. Enable it again by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

#### Affected Silicon Revisions

Rev. A	Rev. B	Rev. C
X	X	X

### **3. Data Sheet Clarifications**

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet ([www.microchip.com/DS40001911](http://www.microchip.com/DS40001911)).

**Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

#### **3.1 None**

There are no known data sheet clarifications as of this publication date.



## 4. Document Revision History

**Note:** The data sheet clarification document revision is independent of the die revision and the device variant (last letter of the ordering number).

### 4.1 Revision History

Doc. Rev.	Date	Comments
C	11/2020	<ul style="list-style-type: none"> <li>• Added die revision C</li> <li>• Added new errata:               <ul style="list-style-type: none"> <li>– Device: <i>Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values</i></li> <li>– ADC: <i>ADC Interrupt Flags Cleared When Reading RESH</i></li> <li>– CCL: <i>The CCL Must be Disabled to Change the Configuration of a Single LUT</i></li> <li>– TCA: <i>Restart Will Reset Counter Direction in NORMAL and FRQ Mode</i></li> <li>– TCB: <i>CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode</i></li> <li>– TCD: <i>Asynchronous Input Events Not Working When TCD Counter Prescaler is Used</i></li> <li>– USART:                   <ul style="list-style-type: none"> <li>• <i>Full Range Duty Cycle Not Supported When Validating LIN Sync Field</i></li> <li>• <i>Open-Drain Mode Does Not Work When TXD is Configured as Output</i></li> <li>• <i>Start-of-Frame Detection Can Unintentionally be Enabled in Active Mode when RXCIF is '0'</i></li> </ul> </li> </ul> </li> </ul>
B	10/2019	<ul style="list-style-type: none"> <li>• Updated document template</li> <li>• The ADC errata, <b>ADC Functionality Cannot be Ensured with ADCCLK Above 1.5 MHz for All Conditions</b>, has been split into two separate erratas and rewritten</li> </ul>
A	06/2019	Initial document release

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