



Product Change Notification - KSRA-07HVQF409

Date:

22 Jan 2020

Product Category:

8-bit Microcontrollers; Capacitive Touch Sensors

Affected CPNs:**Notification subject:**

CCB 4031 Initial Notice: Qualification of Microchip Technology Tempe – Fab 2 (TMGR) as an additional fabrication site for selected Atmel products.

Notification text:**PCN Status:**

Initial notification.

PCN Type:

Manufacturing Change

Microchip Parts Affected:

Please open one of the icons found in the Affected CPNs section above.

NOTE: For your convenience Microchip includes identical files in two formats (.pdf and .xls).

Description of Change:

Qualification of Microchip Technology Tempe - Fab 2 (TMGR) as an additional fabrication site for selected Atmel products.

Pre Change:

Fabricated at Microchip Technology Colorado - Fab 5 (MCSO) using 6 inch wafer

Post Change:

Fabricated at Microchip Technology Colorado - Fab 5 (MCSO) using 6 inch wafer or Microchip Technology Tempe - Fab 2 (TMGR) using 8 inch wafer

Pre and Post Change Summary:

	Pre Change	Post Change	
Fabrication Supplier and Location	Microchip Technology Colorado - Fab 5 (MCSO)	Microchip Technology Colorado - Fab 5 (MCSO)	Microchip Technology Tempe - Fab 2 (TMGR)
Wafer Diameter	6 inches	6 inches	8 inches
Die size	No change	No change	No change
Quality Certification	ISO9001/TS16949 or IATF16949	ISO9001/TS16949 or IATF16949	ISO9001/TS16949 or IATF16949

Impacts to Data Sheet:

None

Change Impact:

None

Reason for Change:

To improve manufacturability and on-time delivery performance by qualifying a second fabrication source at Microchip Technology Tempe - Fab 2 (TMGR) fabrication site.

Change Implementation Status:

In Progress

Estimated Qualification Completion Date:

June 2020

Note: Please be advised the qualification completion times may be extended because of unforeseen business conditions however implementation will not occur until after qualification has completed and



a final PCN has been issued. The final PCN will include the qualification report and estimated first ship date. Also note that after the estimated first ship date guided in the final PCN customers may receive pre and post change parts.

Time Table Summary:

Workweek	December 2019				-->	June 2020				
	49	50	51	52		23	24	25	26	27
Initial PCN Issue Date		X								
Qual Report Availability										X
Final PCN Issue Date										X

Method to Identify Change:

Traceability code

Qualification Plan:

Please open the attachments included with this PCN labeled as PCN_#_Qual_Plan.

Revision History:

December 11, 2019: Issued initial notification.

January 08, 2020: Re-issued initial notification to update the Qualification Plan and Affected CPN list.

January 22, 2020: Re-issued initial notification to revise the Affected CPN list based on the updated scope.

The change described in this PCN does not alter Microchip's current regulatory compliance regarding the material content of the applicable products.

Attachment(s):

[PCN_KSRA-07HVQF409 Qual Plan.pdf](#)

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Affected Catalog Part Numbers (CPN)

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ATMEGA1284-PU
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QUALIFICATION PLAN SUMMARY

PCN #: KSRA-07HVQF409

**Date:
November 01, 2019**

**Qualification of Microchip Technology Tempe – Fab 2 (TMGR)
as an additional fabrication site for selected Atmel products.**

Purpose: Qualification of Microchip Technology Tempe – Fab 2 (TMGR) as an additional fabrication site for selected Atmel products.

CCB No: 4031

Die Qualification Plan: 3 lots per QCI-39000

Test / Evaluation	Test Conditions / Parameters
Operating (Dynamic) Life	<ul style="list-style-type: none"> • 150°C for 408 hrs at Vdd max
High Temp. Retention Bake (DLT) / High Temperature Operating Life (HTOL)	<ul style="list-style-type: none"> • 504 hrs @ 175°C.
Endurance Cycling	<ul style="list-style-type: none"> • 10,000 flash Erase/Write cycles at 85°C • 100,000 EEPROM Erase/Write cycles at 85°C
ESD HBM	<ul style="list-style-type: none"> • Tested at 500V, 1000V, and 2000V
Latch-up	<ul style="list-style-type: none"> • Should meet a minimum of +/- 105mA injection on I/O pins with a clamp of 1.5 x VMax on the positive injection and 0.5 x VMax on the negative injection. Power supply pin shall be stressed at 1.5 x VMax with a 200mA clamp.
Electrical Validation	<ul style="list-style-type: none"> • 30 units from one wafer lot. Datalog parameters at room, hot and cold at vcc min/max and frequency min/max. Collection of this data may be done as part of any qualification test's pre or post functional testing or from a separate group of parts"

Package Qualification Plan

Misc.	Assembly site	MMT
	BD Number	A-064764 / A
	MP Code (MPC)	35473YRXBC01
	Part Number (CPN)	ATMega328P-15MZ
	MSL information	MSL-1/260
	Assembly Shipping Media (T/R, Tube/Tray)	T/R
	Base Quantity Multiple (BQM)	5000
	Reliability Site	MPHIL
	CCB No.	4031
Lead-Frame	Paddle size	150x150 mils
	Material	C194
	DAP Surface Prep	Bare CU
	Treatment	None
	Process	Saw Singulated
	Part Number	10103202
	Lead Plating	Matte Tin
Bond Wire	Material	CuPdAu
Die Attach	Part Number	3280
	Conductive	Yes
MC	Part Number	G700LTD
PKG	PKG Type	VQFN
	Pin/Ball Count	32
	PKG width/size	5x5x0.9mm

Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly)	Qty of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Test Site	Special Instructions
Standard Pb-free Solderability	J-STD-002; Perform 8 hour steam aging for Matte tin finish and 1 hour steam aging for NiPdAu finish prior to testing. Standard Pb-free: Matte tin/ NiPdAu finish, SAC solder, wetting temp 245°C for both SMD & through hole packages.	22	5	1	27	> 95% lead coverage	5	MTAI	Standard Pb-free solderability is the requirement. SnPb solderability (backward solderability- SMD reflow soldering) is required for any plating related changes and highly recommended for other package BOM changes.
Backward Solderability	J-STD-002 ;Perform 8 hours steam aging for Matte tin finish and 1 hour steam aging for NiPdAu finish prior to testing. Backward: Matte tin/ NiPdAu finish, SnPb solder, wetting temp 215°C for SMD.	22	5	1	27	> 95% lead coverage	5	MTAI	
Wire Bond Pull - WBP	Mil. Std. 883-2011	5	0	3	15	0 fails after TC	5	MMT/MTAI	30 bonds from a minimum of 5 devices.
Wire Bond Shear - WBS	CDF-AEC-Q100-001	5	0	3	15	0	5	MMT/MTAI	30 bonds from a minimum of 5 devices.
Wire Sweep		5	0	3	15	0		MMT	Required for any reduction in wire bond thickness.
Die Shear	Mil. Std. 883-2011	5	0	3	15	0			
Physical Dimensions	Measure per JESD22 B100 and B108	10	0	3	30	0	5	MMT	
External Visual	Mil. Std. 883-2009/2010	All devices prior to submission for qualification testing	0	3	ALL	0	5	MMT/ MTAI	
Preconditioning - Required for surface mount devices	+150°C Bake for 24 hours, moisture loading requirements per MSL level + 3X reflow at peak reflow temperature per Jedec-STD-020E for package type; Electrical test pre and post stress at +25°C MSL1/MSL3 @ 260°C	231	15	3	738	0	15	MTAI Post test: ASEM	Spares should be properly identified. 77 parts from each lot to be used for HAST, Autoclave, Temp Cycle test.
Biased HAST	+130°C/85% RH for 96 hrs. Electrical test pre and post stress at +25°C.	77	5	3	246	0	10	MTAI Post test: ASEM	Spares should be properly identified. Use the parts which have gone through Pre-conditioning.
Unbiased HAST	+130°C/85% RH for 96 hrs. Electrical test pre and post stress at +25°C.	77	5	3	246	0	10	MTAI Post test: ASEM	Spares should be properly identified. Use the parts which have gone through Pre-conditioning.
Temp Cycle	-65°C to +150°C for 500 cycles. Electrical test pre and post stress at hot temp; 3 gram force WBP, on 5 devices from 1 lot, test following Temp Cycle stress.	77	5	3	246	0	15	MTAI Post test: ASEM	Spares should be properly identified. Use the parts which have gone through Pre-conditioning.