Product Change Notification - SYST-03FYTJ911

Date:

04 Jan 2019

Product Category:

Ethernet Switches

Affected CPNs:

Notification subject:

ERRATA - KSZ9563R Silicon Errata and Data Sheet Clarification Errata Document Revision

Notification text:

SYST-03FYTJ911

Microchip has released a new DeviceDoc for the KSZ9563R Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at KSZ9563R Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: - Removed module: "PTP messages get dropped in PTP 2-Step Mode" - Added new module 9

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 04 Jan 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed..

Markings to Distinguish Revised from Unrevised Devices:N/A

Attachment(s):

KSZ9563R Silicon Errata and Data Sheet Clarification

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Affected Catalog Part Numbers (CPN)

KSZ9563RNXC
KSZ9563RNXC-TR
KSZ9563RNXI
KSZ9563RNXI-TR

KSZ9563R

KSZ9563R Silicon Errata and Data Sheet Clarification

This document describes known silicon errata for the Microchip KSZ9563R. The silicon errata discussed in this document are for silicon revisions as listed in Table 1. The silicon revision can be determined by the device's top marking. A summary of KSZ9563R silicon errata is provided in Table 2.

TABLE 1: AFFECTED SILICON REVISIONS

Part Number	Silicon Revision
KSZ9563RNX	B2

TABLE 2: SILICON ISSUE SUMMARY

Item Number	Silicon Issue Summary	Affected Silicon Revisions
1.	When tail tag is enabled, frame length field check fails for 802.3 frames	B2
2.	Port based priority remapping is not supported	B2
3.	1000BASE-T PMA-EEE fails to meet the IEEE Refresh Time specification	B2
4.	1000BASE-T Master Mode may not link up successfully on the first attempt	B2
5.	1000BASE-T Transmit Output Voltage may fail to meet IEEE compliance specification	B2
6.	1000BASE-T Transmitter Distortion fails to meet IEEE compliance specification	B2
7.	Transmission halt with late collisions	B2
8.	LEDx_0 in Single-LED Mode does not indicate link activity	B2
9.	GPIO_2 does not function properly	B2

Silicon Errata Issues

Module 1: When tail tag is enabled, frame length field check fails for 802.3 frames

DESCRIPTION

The comparison of the length field of the Ethernet frame with the actual length of the data field portion of the frame fails for the ingress packets with tail tag. This issue is not applicable to packets with the type field in the frame.

END USER IMPLICATIONS

The packets will be dropped when length check fails for the packet.

Work Around

Disable the length check in bit 3 of the register 0x0330 (Global Switch MAC Control Register 0). The Microchip provided driver disables the length check.

PLAN

This erratum will not be corrected in a future revision.

Module 2: Port based priority remapping is not supported

DESCRIPTION

The 802.1Q-2014 Clause 6 (6.9.4 Regenerating priority) describes the Priority Regeneration Table for the reception port, which is required to support an AVB boundary port. The boundary port in the AVB domain needs to remap the priority field of the incoming traffic.

Since the device do not support port based priority remapping, the port cannot be used as a boundary port.

This erratum is not applicable if all the device ports are AVB domain ports.

END USER IMPLICATIONS

The device port cannot be used as an AVB domain boundary port to networks that utilize the scheduler.

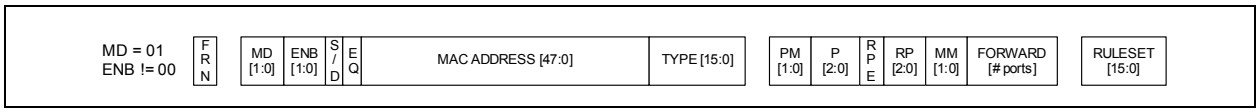
Work Around

A software workaround is available to remap the priority of all the incoming traffic to the port. The workaround uses an ACL (Access Control List) mechanism to remap the priority of the incoming traffic to 0. With the workaround, there is no impact on AVB traffic. If the incoming traffic uses QoS, priorities are also remapped to 0. This may have a minor impact on the QoS traffic (i.e., all the QoS traffic uses one egress queue instead of using the two queues available in the device).The workaround is available in Microchip provided driver software.

Software Workaround:

Program the ACL rule to remap all the incoming layer 2 packets to priority 0 (ACL rule format shown in Figure 1).

FIGURE 1: ACL RULE FORMAT



Rule Description:

MD = 01 : Layer 2
ENB = 10 : Comparison on EtherType value
EQ = 0 & TYPE = 0 : I.e., all packets (condition is when EtherType != 0)
PM = 11 : Always change priority to P[2:0]
P = 0 : Priority value to be changed

PLAN

This erratum will not be corrected in a future revision.

Module 3: 1000BASE-T PMA-EEE fails to meet the IEEE Refresh Time specification

DESCRIPTION

The device's 1000BASE-T Transmit Refresh Time for Waketx time (Full) is approximately 1.47-1.48µs, versus the <1.40µs indicated in the IEEE specification.

END USER IMPLICATIONS

With the default setting, the Refresh Time is slightly outside the specification, and the transmitter is not fully compliant with the IEEE standard. This may degrade performance with some 1000BASE-T EEE PHY link partners.

Work Around

Write to the following MMD register for each PHY port [1-2] to set the Refresh Time to 0.85µs:

[MMD]	[register]	[data]
0x3	0xE	0x0021

PLAN

This erratum will not be corrected in a future revision.

Module 4: 1000BASE-T Master Mode may not link up successfully on the first attempt

DESCRIPTION

The device's first 1000BASE-T link-up attempt when in Master Mode may drop link immediately before always linking successfully and maintaining link on the second attempt. This behavior occurs mainly at long cable lengths (~100 meters).

END USER IMPLICATIONS

When the device operates in 1000BASE-T Master Mode, the system application needs to account for a possible second link-up attempt, especially with long cable.

Work Around

None.

PLAN

This erratum will not be corrected in a future revision.

Module 5: 1000BASE-T Transmit Output Voltage may fail to meet IEEE compliance specification

DESCRIPTION

The device's 1000BASE-T Transmit Output Voltage Template may fail to meet the following IEEE specifications when operating at low voltage (-5% of nominal for AVDDH and core supply voltages) and high temperature (+85°C).

1. Percent difference between Points A, B may slightly exceed the <1.0% per the IEEE specification.
2. Peak Voltage for Points A, B, C, D, F, H may slightly touch the voltage template defined per the IEEE specification.

END USER IMPLICATIONS

It is unlikely the marginal specification failures will impact system performance. Extensive testing has been performed to ensure the device can inter-operate with different Gigabit PHY link partners.

Work Around

None.

PLAN

This erratum will not be corrected in a future revision.

Module 6: 1000BASE-T Transmitter Distortion fails to meet IEEE compliance specification

DESCRIPTION

The device's 1000BASE-T Transmitter Distortion is approximately 40mV, versus the <10mV indicated in the IEEE specification.

END USER IMPLICATIONS

It is unlikely this specification failure will impact system performance. The following link to the Gigabit Transmit Distortion Testing document on the IEEE802.org website also questions the validity of this measurement:

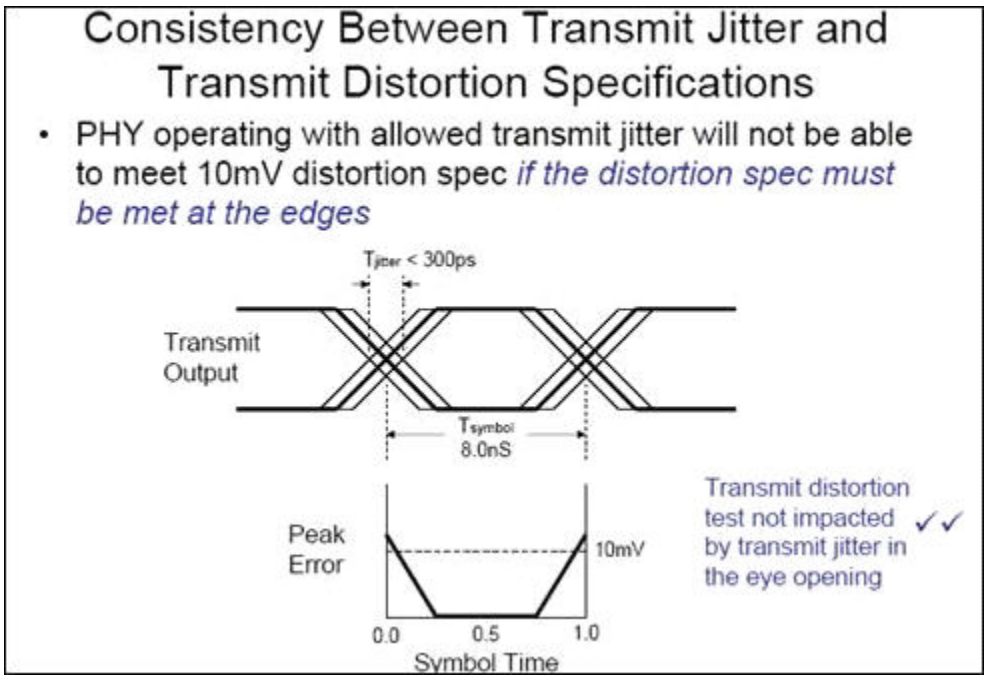
http://www.ieee802.org/3/axay/public/may_07/sefidvash_1_0507.pdf

IEEE testing calls for <10mV peak transmitter distortion for at least 60% of the UI within the eye opening. However, this measurement might not be valid, as the transmit distortion test is sensitive to transmit jitter. Refer to the explanation below, taken from the aforementioned IEEE document.

The Gigabit Transmit Distortion Testing document indicates:

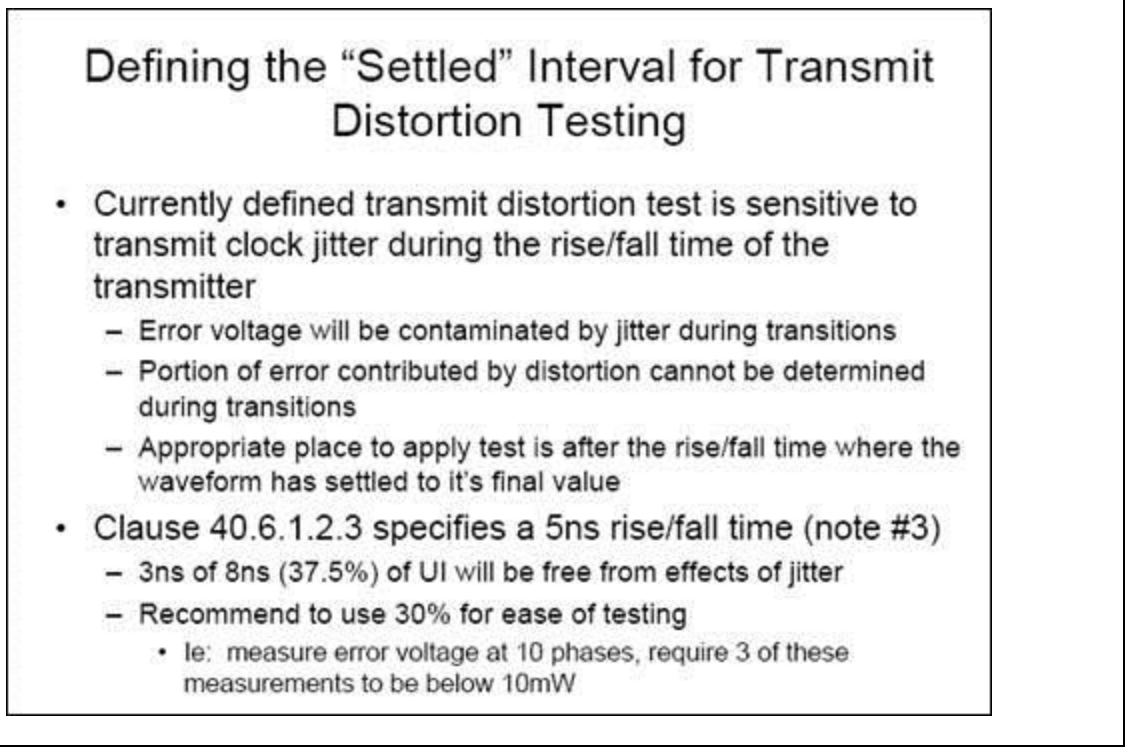
- On page 6, a contradiction between Transmit Jitter and Transmit Distortion requirements:

FIGURE 2: IEEE DOCUMENT PAGE 6



- On page 7:
  - The transmit distortion test is sensitive to transmit clock jitter during the rise/fall time.
  - It is recommended to change the requirement to use at least 30%, instead of at least 60%, of the UI within the eye opening for the <10mV peak transmitter distortion.

FIGURE 3: IEEE DOCUMENT PAGE 7



Extensive testing has been performed to ensure the device can inter-operate with different Gigabit PHY link partners.

Work Around

None.

PLAN

This erratum will not be corrected in a future revision.

Module 7: Transmission halt with late collisions

DESCRIPTION

Section 4 of the IEEE 802.3 Specification details Carrier Sense Multiple Access / Collision Detection (CSMA/CD) parameters when operating in half-duplex mode. The first 512 bit times are designated as the slotTime, which is the maximum amount of time allowed for a collision to occur. If a link partner is configured incorrectly, where the PHY is linking in half-duplex mode but the MAC is configured in full-duplex mode, there is a chance that the link partner will generate a collision after the first 512 bit times, violating the IEEE 802.3 specification. These late collisions, combined with other factors, can cause the switch port transmitter to lock up and stop sending packets. The receiver will still function.

END USER IMPLICATIONS

If this erratum occurs, the switch will stop transmitting data to the half-duplex port, making it seem the half-duplex link partner has stopped communicating to the network. The more traffic there is, the greater the risk of the violating link partner generating a late collision that will affect the port.

Work Around

Ideally, the link partner that is violating the specification would need to be updated so the MAC and PHY are correctly configured to the same duplex setting. If the link partner cannot be modified to conform to the IEEE 802.3 specification, the switch can be re-configured to full-duplex when late collisions are detected to avoid a lock up condition. Of note, each switch port functions independently. Therefore, any work around must be implemented separately for each port.

Method 1:

To avoid transmitter lock up, when a port is linked in half-duplex mode, the software should monitor the TxLateCollision MIB counter (MIB Index 0x16). If the number is ever non-zero, the software should force the link to function in full-duplex mode by disabling auto-negotiation and setting full-duplex and the appropriate speed in the PHY Basic Control Registers (addresses 0xN100 - 0xN101).

Method 2:

To detect transmitter lock up, the software should monitor the TxByteCnt (MIB Index 0x81) and the RxByteCnt (MIB Index 0x80). If the RxByteCnt is incrementing but the TxByteCnt remains the same, the software should perform a hard reset of the switch.

PLAN

This erratum will not be corrected in a future revision.

Module 8: LEDx_0 in Single-LED Mode does not indicate link activity

DESCRIPTION

The PHY Port (1-2) LEDx_0 does not go low in the presence of link activity when in Single-LED Mode.

END USER IMPLICATIONS

Link activity cannot be determined in Single-LED Mode. However, LEDx_1 will indicate if the link is up or down. The lack of status lends to uncertainty that traffic is passing through the port.

Work Around

No work around exists for Single-LED Mode. Both PHY port LEDs work properly in Tri-Color Dual-LED Mode, which is the default LED mode.

PLAN

This erratum will not be corrected in a future revision.

Module 9: GPIO_2 does not function properly

DESCRIPTION

Pins GPIO_1 and GPIO_2 are intended to output programmed signals that are timed to the internal clock. They may also be used for timestamping of input signals. GPIO_1 functions as intended, but GPIO_2 does not. GPIO_2 outputs a 25MHz clock when link is up on either of the two PHY ports, preventing it's use as a GPIO. If a second GPIO output pin is needed, the LED2_1 pin can be re-assigned for this purpose.

END USER IMPLICATIONS

GPIO_2 cannot be used for input timestamping or for outputting programmed signals. The 25MHz clock output on GPIO_2 cannot be disabled, so it is best to leave the pin unconnected on board designs. LED2_1 can be assigned to take the place of GPIO_2 for output functionality, but this displaces the LED functionality of LED2_1.

There is no alternative for input timestamping on GPIO_2. Input timestamping is available only on GPIO_1, not on any other pins.

Work Around

The output functionality of GPIO_2 can be routed to LED2_1 by setting bit 3 in the LED2_0/LED2_1 Source Register at address 0x0128 - 0x012B.

No other changes are required. When setting up the trigger output units, any output programmed to go to GPIO_2 will output on LED2_1 if the above bit is set. Any of the three trigger units can be used.

PLAN

This erratum will not be corrected in a future revision.

APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS80000786C (12-04-18)	Module 9.	Added new errata.
	Module: “PTP messages get dropped in PTP 2-Step Mode”	Removed errata from document.
DS80000786B (08-17-18)	Modules 7., 8.	Added new errata.
DS80000786A (04-05-18)	All	Initial release.

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