



## Product Change Notification - SYST-26RFRB563

**Date:**

27 Apr 2018

**Product Category:**

Ethernet Switches

**Affected CPNs:**



**Notification subject:**

ERRATA - KSZ9896C Silicon Errata & Data Sheet Clarification Errata Document Revision

**Notification text:**

SYST-26RFRB563

Microchip has released a new DeviceDoc for the KSZ9896C Silicon Errata & Data Sheet Clarification of devices. If you are using one of these devices please read the document located at [KSZ9896C Silicon Errata & Data Sheet Clarification](#).

**Notification Status:** Final

**Description of Change:** 1) Added new errata for “When tail tag is enabled, frame length field check fails for 802.3 frames”. 2) Removed “Frame Length Field Check mode is disabled” errata, which is superseded by the Module 12.

**Impacts to Data Sheet:** None

**Reason for Change:** To Improve Productivity

**Change Implementation Status:** Complete

**Date Document Changes Effective:** 27 Apr 2018

**NOTE:** Please be advised that this is a change to the document only the product has not been changed..

**Markings to Distinguish Revised from Unrevised Devices:** N/A

**Attachment(s):**

[KSZ9896C Silicon Errata & Data Sheet Clarification](#)

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Affected Catalog Part Numbers (CPN)

KSZ9896CLX-ENG

KSZ9896CTXC

KSZ9896CTXC-TR

KSZ9896CTXI

KSZ9896CTXI-TR

## KSZ9896C Silicon Errata and Data Sheet Clarification

This document describes known silicon errata for functional revisions A1 of the KSZ9896C. The silicon errata discussed in this document are for silicon revisions as listed in [Table 1](#). The silicon revision can be determined by the device's top marking. A summary of KSZ9896C silicon errata is provided in [Table 2](#).

Some errata work arounds may require modifying register values. If the system design does not include a processor to manage the switch, a small 8-bit PIC or AVR microcontroller can be used to configure the switch via the I<sup>2</sup>C or SPI interface. These low-cost microcontrollers are available in packages as small 8-pins, with integrated oscillator and non-volatile program memory. The microcontroller does not need a MII or RMII connection to the switch. Alternatively, the switch can be configured by a remote computer via the in-band management feature of the switch. The default port for in-band management is port .

**TABLE 1: AFFECTED SILICON REVISIONS**

Part Numbers	Silicon Revision	Package Top Mark
KSZ9896CTX	A1	B000

**TABLE 2: SILICON ISSUE SUMMARY**

Item Number	Silicon Issue Summary	Affected Silicon Revisions
1.	<a href="#">Register settings are needed to improve PHY receive performance</a>	A1
2.	<a href="#">Transmit waveform amplitude can be improved (1000BASE-T, 100BASE-TX, 10BASE-Te)</a>	A1
3.	<a href="#">Energy Efficient Ethernet (EEE) feature select must be manually disabled</a>	A1
4.	<a href="#">Toggling PHY Powerdown can cause errors or link failures in adjacent PHYs</a>	A1
5.	<a href="#">Certain PHY registers must be written as pairs instead of singly</a>	A1
6.	<a href="#">Register settings are required to meet data sheet supply current specifications</a>	A1
7.	<a href="#">Automatic SPI Data Out Edge Select may cause issues</a>	A1
8.	<a href="#">1000BASE-T Transmitter Distortion fails to meet IEEE compliance specification</a>	A1
9.	<a href="#">No Pause frames are generated for ingress rate limiting with an EEE link</a>	A1
10.	<a href="#">Link drop can occur when back pressure is enabled in 100BASE-TX half-duplex mode</a>	A1
11.	<a href="#">Port may hang in half-duplex mode when No Excessive Collision Drop feature is enabled</a>	A1
12.	<a href="#">When tail tag is enabled, frame length field check fails for 802.3 frames</a>	A1

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## Silicon Errata Issues

### Module 1: Register settings are needed to improve PHY receive performance

#### DESCRIPTION

The default receiver settings are not optimized. Receive errors may occur, especially at longer cable lengths.

#### END USER IMPLICATIONS

For best receiver performance, users should write the following PHY MMD registers. This is done individually for each port (1-5) using any of the management interfaces: MDC/MDIO, I<sup>2</sup>C, SPI, or in-band.

#### Work around

Write to the following MMD registers for each PHY port [1-5]:

[MMD]	[register]	[data]
0x01	0x6F	0xDD0B
0x01	0x8F	0x6032
0x01	0x9D	0x248C
0x01	0x75	0x0060
0x01	0xD3	0x7777
0x1C	0x06	0x3008
0x1C	0x08	0x2001

#### PLAN

This erratum will not be corrected in a future revision.

### Module 2: Transmit waveform amplitude can be improved (1000BASE-T, 100BASE-TX, 10BASE-Te)

#### DESCRIPTION

The transmit waveform amplitude can be improved for 10BASE-Te, 100BASE-TX and 1000BASE-T.

#### END USER IMPLICATIONS

With the default settings, the waveform amplitude may be outside the specifications in some corner case conditions, and the transmitter may not be fully compliant with the IEEE standard. This may degrade performance under some conditions.

#### Work around

Write to the following MMD registers for each PHY port [1-5]:

[MMD]	[register]	[data]
0x1C	0x4	0x00D0

#### PLAN

This erratum will not be corrected in a future revision.

## Module 3: Energy Efficient Ethernet (EEE) feature select must be manually disabled

### DESCRIPTION

The EEE feature is enabled by default, but it is not fully operational. It must be manually disabled through register controls. If not disabled, the PHY ports can auto-negotiate to enable EEE, and this feature can cause link drops when linked to another device supporting EEE.

### END USER IMPLICATIONS

If the link partner does not support EEE, then EEE will not be activated and there will be no problem with link drops. This is also true if auto-negotiation is disabled, since EEE is activated only if auto-negotiated between the two link partners.

If the link partner is not known, or if the link partner is EEE capable, then the EEE feature should be manually disabled to avoid link drop problems.

#### Work around

Disable EEE by writing to the following registers. This is done individually for each PHY port (1-5) using any of the management interfaces: MDC/MDIO, I<sup>2</sup>C, SPI, or in-band.

EEE is disabled by clearing bits [2:1] of the PHY indirect register: MMD 7, address 3Ch.

MMD register:

[MMD]	[register]	[data]
7	0x3C	0x0000

### PLAN

This erratum will not be corrected in a future revision.

## Module 4: Toggling PHY Powerdown can cause errors or link failures in adjacent PHYs

### DESCRIPTION

The PHY power down is controlled by bit 11 in registers 0xN100-0xN101. It provides separate power down control for each PHY. When a PHY is brought out of power down by clearing this bit, the resulting power surge can disrupt an adjacent PHY, causing data errors or temporary link down on that port.

### END USER IMPLICATIONS

Data errors or link down can occur in an active PHY when its neighbor is brought out of power down mode.

#### Work around

Avoid dynamically changing the power down state of any PHYs if other PHYs may be linked and active. Only change the power up or power down state of a PHY when no other PHYs on the chip are linked and possibly passing traffic.

### PLAN

This erratum will not be corrected in a future revision.

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## Module 5: Certain PHY registers must be written as pairs instead of singly

### DESCRIPTION

When using SPI, I<sup>2</sup>C, or in-band register access, writes to certain PHY registers are performed as 32-bit writes instead of 16-bit writes.

The PHY control and status registers are 16-bit registers. They occupy the byte address range 0xN100 to 0xN13F, where N is the port number. Registers from 0xN100 to 0xN11F function normally and can be written either 16- or 8-bits at a time.

An error in the register access logic causes all writes from 0xN120 to 0xN13F to be 32-bit writes. For example, a 16-bit write to register 0xN122-0xN123 also results in all zeros being written to register 0xN120-0x121. Also, a 16-bit write to register 0xN120-0xN121 causes all zeros to be written to 0xN122-0xN123.

### END USER IMPLICATIONS

This issue is relevant only to write operations, not to reads. When writing only 16-bits to a register in this address range, all zeros will be written to the adjacent register. This may change the PHY settings and cause the PHY to malfunction.

#### **Work around**

To avoid writing zero to an adjacent register, always write the registers in this address range in pairs as 32-bits:

0xN120 - 0xN123

0xN124 - 0xN127

0xN128 - 0xN12B

0xN12C - 0xN12F

Note that some of these registers are not defined in the data sheet. In order to avoid writing inappropriate data to any undefined register, the register should be read before writing (i.e. read-modify-write). Do not assume that undocumented registers should be all zeros.

### PLAN

This erratum will not be corrected in a future revision.

## Module 6: Register settings are required to meet data sheet supply current specifications

### DESCRIPTION

The power supply current specifications in the data sheet are based on the following register settings. Without these register changes, the AVDDH current is approximately 40% greater, the AVDDL current is approximately 56% greater, and total chip power is approximately 26% greater when all PHY ports are linked at 1000Mb/s.

### END USER IMPLICATIONS

If the following register settings are not made, the chip can dissipate more power than indicated in the data sheet for the AVDDH and AVDLL power rails. This means that under the worst case conditions (all PHY ports linked at 1000 Mb/s), the junction temperature may approach or exceed 125°C when operating at the maximum ambient temperature. Device and system thermal analysis should use the increased AVDDH and AVDLL current values if the following register settings are not made. The voltage regulators supplying AVDDH and AVDLL must also have adequate current capacity.

#### Work around

Write to the following MMD registers for each PHY port [1-5]:

[MMD]	[register]	[data]
0x1C	0x13	0x6EFF
0x1C	0x14	0xE6FF
0x1C	0x15	0x6EFF
0x1C	0x16	0xE6FF
0x1C	0x17	0x00FF
0x1C	0x18	0x43FF
0x1C	0x19	0xC3FF
0x1C	0x1A	0x6FFF
0x1C	0x1B	0x07FF
0x1C	0x1C	0x0FFF
0x1C	0x1D	0xE7FF
0x1C	0x1E	0xEFFF
0x1C	0x20	0xEEEE

### PLAN

This erratum will not be corrected in a future revision.

## Module 7: Automatic SPI Data Out Edge Select may cause issues

### DESCRIPTION

Automatic SPI Data Out Edge Select is a feature that is normally enabled in register 0x0100. It detects the SPI clock frequency and selects either the rising clock edge or falling clock edge to clock out the SPI data based on that frequency. The behavior is not fully predictable when the SPI clock frequency is near 25MHz, which may cause the SPI interface to stop functioning. Also, it does not adapt to changes in the SPI clock frequency.

### END USER IMPLICATIONS

The SPI interface may stop functioning if the inappropriate clock edge is selected, or if the clock rate changes. Generally there is no problem when operating at lower clock rates, such as below 15 MHz.

#### Work around

When operating the SPI above 15 MHz, it is suggested to disable the automatic feature by clearing register 0x0100 bit 1, and at the same time setting bit 0 to the desired value to manually select the mode of operation.

### PLAN

This erratum will not be corrected in a future revision.



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## Module 8: 1000BASE-T Transmitter Distortion fails to meet IEEE compliance specification

### DESCRIPTION

The device's 1000BASE-T Transmitter Distortion is approximately 40mV, versus the <10mV indicated in the IEEE specification.

### END USER IMPLICATIONS

It is unlikely this specification failure will impact system performance. The following link to the Gigabit Transmit Distortion Testing document on the IEEE802.org website also questions the validity of this measurement:

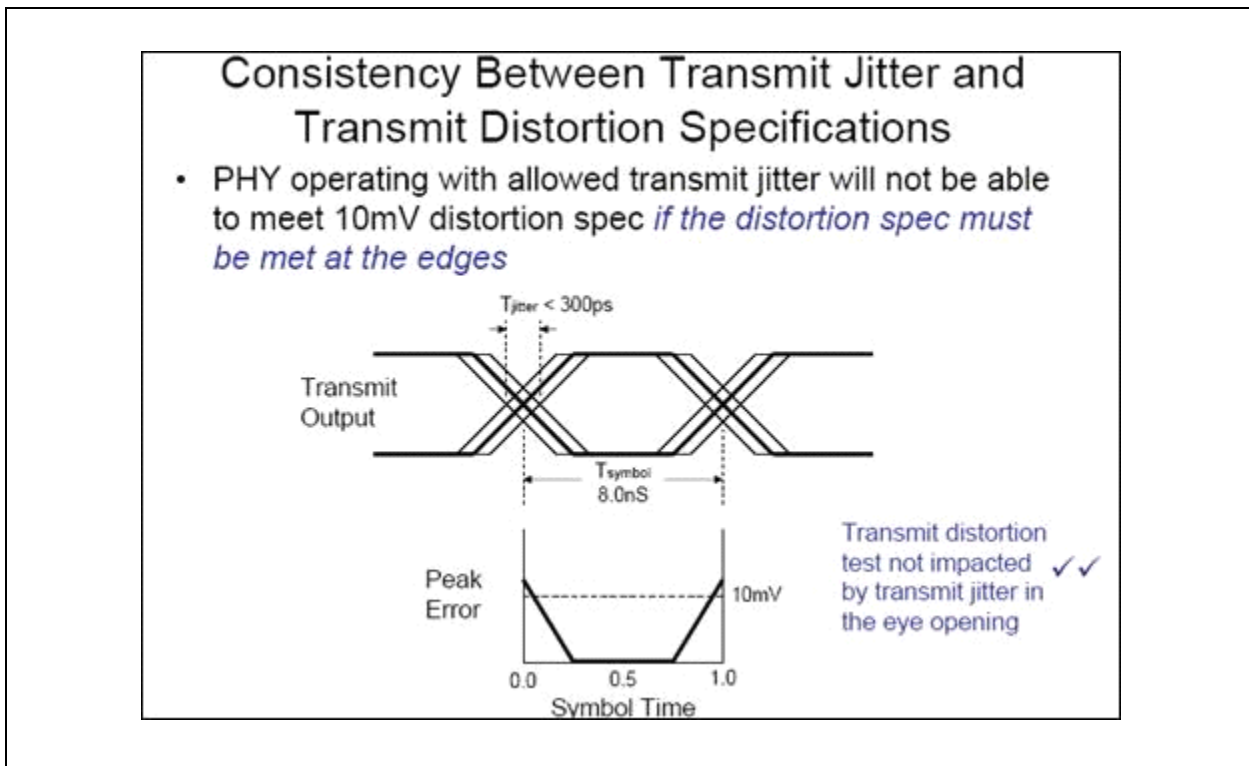
[http://www.ieee802.org/3/axay/public/may\\_07/sefidvash\\_1\\_0507.pdf](http://www.ieee802.org/3/axay/public/may_07/sefidvash_1_0507.pdf)

IEEE testing calls for <10mV peak transmitter distortion for at least 60% of the UI within the eye opening. However, this measurement might not be valid, as the transmit distortion test is sensitive to transmit jitter. Refer to the explanation below, taken from the aforementioned IEEE document.

The Gigabit Transmit Distortion Testing document indicates:

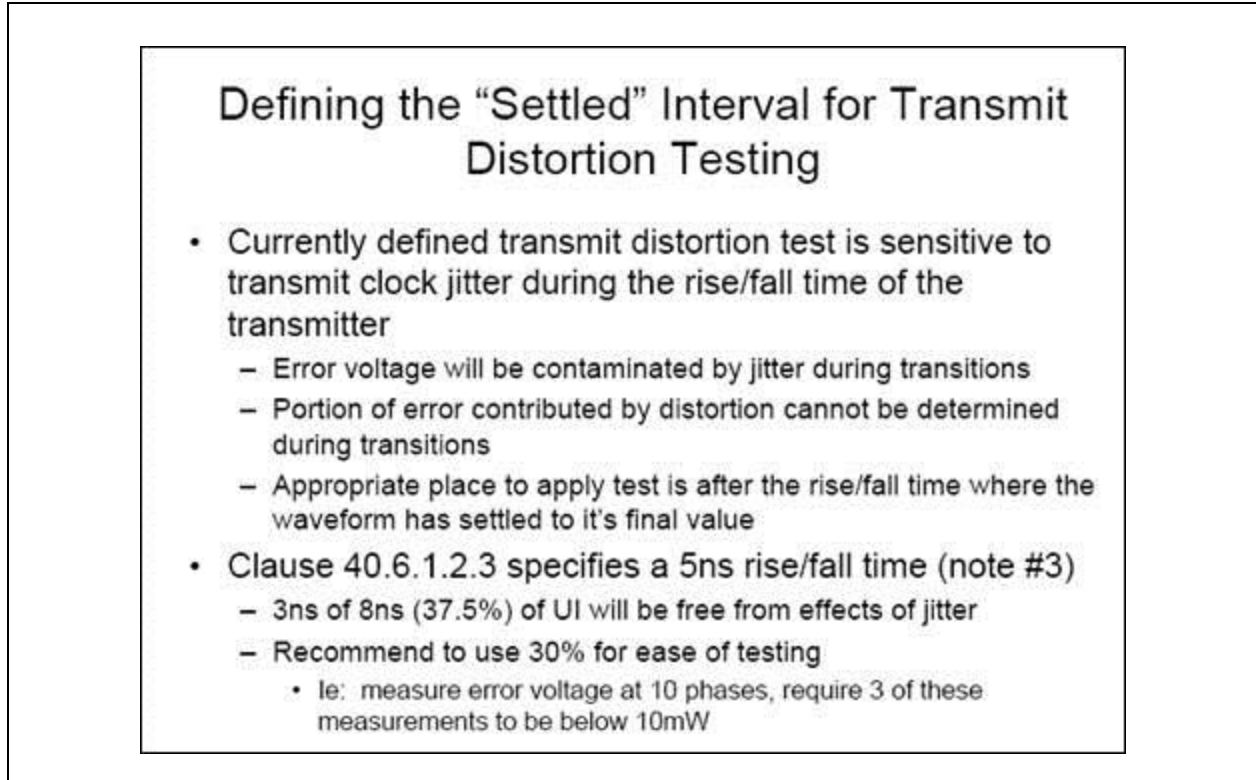
- On page 6, a contradiction between Transmit Jitter and Transmit Distortion requirements:

**FIGURE 1: IEEE DOCUMENT PAGE 6**



- On page 7:
  - The transmit distortion test is sensitive to transmit clock jitter during the rise/fall time.
  - It is recommended to change the requirement to use at least 30%, instead of at least 60%, of the UI within the eye opening for the <10mV peak transmitter distortion.

**FIGURE 2: IEEE DOCUMENT PAGE 7**



Extensive testing has been performed to ensure the device can inter-operate with different Gigabit PHY link partners.

**Work around**

None.

PLAN

This erratum will not be corrected in a future revision.

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## Module 9: No Pause frames are generated for ingress rate limiting with an EEE link

### DESCRIPTION

When an Energy Efficient Ethernet (EEE) link is established with another device, and ingress rate limiting is set up, the port may not generate Pause frames in response to ingress traffic exceeding the rate limit. It also assumes that the Ingress Rate Limit Flow Control Enable bit in register 0xN403 has been set.

### END USER IMPLICATIONS

If Pause frames are not generated by the switch, then the link partner will not be able to regulate the rate at which it sends traffic, making ingress rate limiting ineffective. Note that when the flow control function is enabled for ingress rate limiting, the ingress port will not drop packets when the rate limit is exceeded - it relies only on flow control for limiting the ingress rate.

#### Work around

The problem can be resolved by writing to the following three global registers. Note that these registers may not be documented in the data sheet.

Global registers:

[addr]	[data]
0x03C0	0x4090
0x03C2	0x0080
0x03C4	0x2000

### PLAN

This erratum will not be corrected in a future revision.

## Module 10: Link drop can occur when back pressure is enabled in 100BASE-TX half-duplex mode

### DESCRIPTION

When back pressure is enabled for 100BASE-TX half duplex mode, CRS-based back pressure is the default mode. In this mode, if the switch forwards long packets and the link partner is set up to detect and respond to jabber, then the link partner may drop link. The link down condition is temporary.

### END USER IMPLICATIONS

If all of the above conditions are met, then this problem is likely to occur, which will be disruptive, even though it is self-healing. If any of the above conditions are not present, then the problem will not occur. In general, half-duplex is not common. It is also very uncommon for NICs or switches to implement jabber-based link drop since they are normally full-duplex. This function is seen mostly in hubs, which are half duplex.

#### Work around

The workaround is to change the back pressure mode from CRS-based to collision-based by clearing bit 5 in register 0x0331. This completely eliminates the link drop problem. This register can be written using the SPI, I<sup>2</sup>C, or in-band management interface, but not via the MIIM interface.

Global register:

[addr]	[data]
0x0331	0xD0

### PLAN

This erratum will not be corrected in a future revision.

## **Module 11: Port may hang in half-duplex mode when No Excessive Collision Drop feature is enabled**

### DESCRIPTION

This issue is seen when two of these switch devices are connected together and are configured in the same way. The two devices use the same back-off algorithm and their back-off can become synchronized, causing lock-up.

### END USER IMPLICATIONS

“No excessive collision drop” is a feature that may be used for half duplex to potentially improve collision performance. It is controlled in register 0x0300, and is disabled by default. If it is enabled and the link partner is a similar device, then lock up can occur on the link. It will persist until the link is broken (either physically or by register) and re-established.

#### **Work around**

The problem is avoided by enabling the Alternate back-off algorithm when using the No excessive collision drop feature. This is done by setting bit 7 in register 0x0330. This register can be written using the SPI, I<sup>2</sup>C, or in-band management interface, but not via the MIIM interface.

### PLAN

This erratum will not be corrected in a future revision.

## **Module 12: When tail tag is enabled, frame length field check fails for 802.3 frames**

### DESCRIPTION

The comparison of the length field of the Ethernet frame with the actual length of the data field portion of the frame fails for the ingress packets with tail tag. This issue is not applicable to packets with the type field in the frame.

### END USER IMPLICATIONS

The packets will be dropped when length check fails for the packet.

#### **Work around**

Do not set the length check in bit 3 of the register 0x0330 (Global Switch MAC Control Register 0). The Microchip provided driver disables the length check.

### PLAN

This erratum will not be corrected in a future revision.

## APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS80000757B (04-15-18)	Module 12.	Added new errata for “When tail tag is enabled, frame length field check fails for 802.3 frames”. Removed “Frame Length Field Check mode is disabled” errata, which is superseded by the Module 12.
DS80000757A (08-10-17)	All	Initial release.

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