

Product Change Notification - SYST-15YLYB526

Date: 18 Jan 2016

Product Category: SMSC

Affected CPNs:  

Notification subject: ERRATA - LAN91C111/LAN91C111i Family Silicon Errata and Data Sheet Clarification Errata Document Revision

Notification text:

SYST-15YLYB526

Microchip has released a new DeviceDoc for the LAN91C111/LAN91C111i Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at [LAN91C111/LAN91C111i Family Silicon Errata and Data Sheet Clarification](#).

Notification Status: Final

Description of Change: Replaces SMSC version LAN91C111/LAN91C111i Anomaly Rev. 1.1 (03-22-13).

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 18 Jan 2016

NOTE: Please be advised that this is a change to the document only the

product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s): [LAN91C111/LAN91C111i Family Silicon Errata and Data Sheet Clarification](#)

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Affected Catalog Part Numbers (CPN)

LAN91C111-NU

LAN91C111-NS-A00

LAN91C111-NS

LAN91C111I-NU

LAN91C111I-NS

LAN91C111/LAN91C111i Family Silicon Errata and Data Sheet Clarification

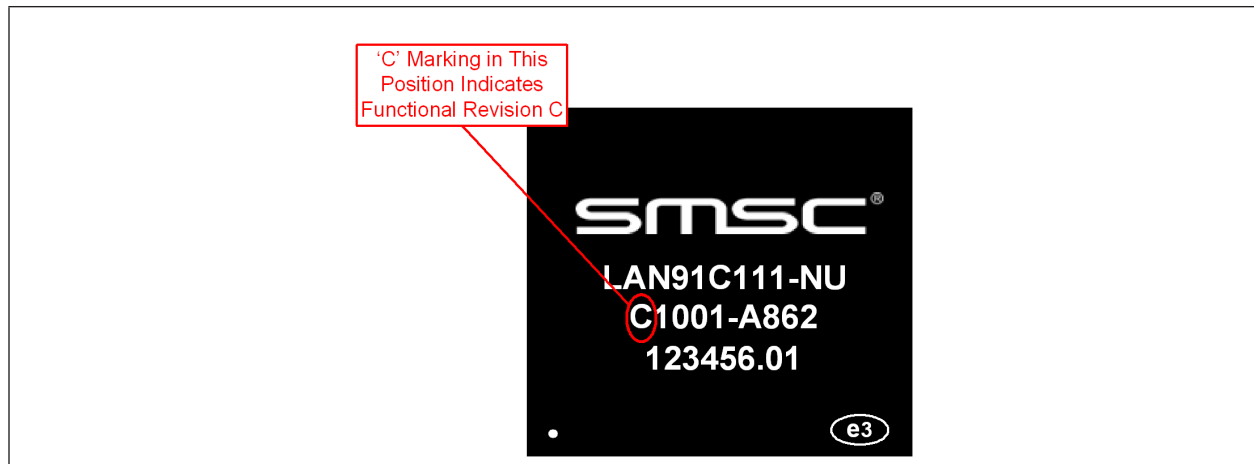
This document describes known anomalies for functional revision C of the LAN91C111/LAN91C111i device. The functional revision can be determined by its top marking as indicated in [Figure 1](#).

TABLE 1: SILICON ISSUE SUMMARY

Hardware Functional Rev C	Description
X	Module 1 : “The TX Interrupt is Erroneously Set”
X	Module 2 : “Packets with Improper Frame Lengths Not Discarded”
X	Module 3 : “PHY Management Interface Read Cycle Structure”
X	Module 4 : “TX Output Signal Amplitude Symmetry Over Limit”
X	Module 5 : “Internal PHY Power-Down”

Legend: X = Applicable to the Functional Rev.

FIGURE 1: TOP MARKING FOR FUNCTIONAL REVISION C DEVICE



Note: [Figure 1](#) details the top markings of an example part. Other than the highlighted functional revision marking, other top marking values may differ (manufacture date, lot codes, industrial temperature part, etc.).

LAN91C111/111i

Silicon Errata Issue

Module 1: The TX Interrupt is Erroneously Set

Description

This anomaly may occur when the host loads the transmit buffer with a packet that is 32 bytes or smaller and the PAD_EN bit is set in the Transmit Control Register, instructing the LAN91C111/LAN91C111i to pad packets smaller than 64 bytes with extra 0's (Ethernet packets must be at least 64 bytes long). Under certain conditions, such as heavy traffic with many collisions, the LAN91C111/LAN91C111i will erroneously set the transmit interrupt (TX INT) in the Interrupt Status Register despite the entire packet successfully loading into the transmit buffer.

End User Implications

Padding of frames that are 32 bytes or smaller must be performed by the driver instead of the LAN91C111/LAN91C111i. Compensating for this anomaly may produce a very slight increase in driver overhead.

Solution

For frames that are 32 bytes or smaller, the driver should disable the LAN91C111/LAN91C111i from inserting padding by clearing the PAD_EN bit in the Transmit Control Register. Padding of these frames must then be performed by the driver.

Plan

There are no plans to address this anomaly in hardware.

Module 2: Packets with Improper Frame Lengths Not Discarded

Description

Packets with a valid CRC and LLC checksum, but which have a length field that does not match the actual length of the packet, will be accepted by the LAN91C111/LAN91C111i instead of being filtered out as erroneous packets. Some examples of this include the following:

- A 64-byte packet with 46 bytes of data and 18 bytes of padding, with valid LLC checksum and CRC, but where the length field is set to 48 bytes.
- A 504-byte packet with 486 bytes of data, with valid LLC checksum and CRC, but with a length field set to 488 bytes.

In addition, the LAN91C111/LAN91C111i will accept frames with valid CRC that are longer than 1514 bytes (the longest legal Ethernet packet size).

End User Implications

Some erroneous packets will not be filtered by the LAN91C111/LAN91C111i.

Solution

The application must rely upon upper protocol layers to perform improper frame length filtering, resulting in a small amount of additional overhead.

Plan

There are no plans to address this anomaly in hardware.

Module 3: PHY Management Interface Read Cycle Structure

Description

For reading MII Registers, the IEEE recommends the insertion of 2 turn-around [Z] bits on the MDIO signal between the address portion and the data portion of the read cycle. The LAN91C111/LAN91C111i MII interface will only work properly if one turn-around bit is inserted.

End User Implications

This anomaly can be eliminated by implementing the software workaround described below. This workaround has no impact on performance or functionality.

Solution

In the software routine that implements the read cycle for accessing the PHY MII Registers, only one bit [Z] should be implemented for the turnaround bit instead of the suggested two bits [Z0].

For a more detailed description, please refer to “Example Routines to Read and Write the PHY Registers” in Application Note 9.6 “LAN91C111/LAN91C111i Technical Reference Manual”.

Plan

There are no plans to address this anomaly in hardware.

Module 4: TX Output Signal Amplitude Symmetry Over Limit

Description

The Transmit differential voltage output signal amplitude symmetry is over the IEEE limit of 102%. The range of the failure is from 102.0% to 102.3%.

End User Implications

There have been no reported real world network failures or inconsistencies attributed to this anomaly. The difference in the two amplitudes can be considered extremely minimal in the range of failures recorded.

Solution

None.

Plan

There are no plans to address this anomaly in hardware.

Module 5: Internal PHY Power-Down

Description

When the LAN91C111/LAN91C111i's internal PHY is powered-down via the PDN bit of the Control Register, X25OUT duty cycle distortion may cause Ethernet communication failures.

End User Implications

The internal PHY should not be powered-down using the PDN bit. PDN should always be cleared.

Solution

Do not set the PDN bit. If the internal PHY will not be used in the design, power savings can be achieved by disabling the PHY transmitter via the XMTPDN bit of the Configuration 1 Register.

Plan

There are no plans to address this anomaly in hardware.

LAN91C111/111I

APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS80000684A, 01/14/2016		Replaces SMSC version LAN91C111/LAN91C111i Anomaly Rev. 1.1 (03-22-13).
Rev. 1.0 (03-22-13)		Document co-branded: Microchip logo added; company disclaimer modified.
Rev. 1.0 (04-20-10)		Initial release.

NOTES:

LAN91C111/111I

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