

Product Change Notification - SYST-07CTIP051

Date: 11 Jan 2016

Product Category: SMSC

Affected CPNs:  

Notification subject: ERRATA - LAN951x FamilySilicon Errata and Data Sheet Clarification Errata Document Revision

Notification text: SYST-07CTIP051

Microchip has released a new DeviceDoc for the LAN951x FamilySilicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at [LAN951x FamilySilicon Errata and Data Sheet Clarification](#).

Notification Status: Final

Description of Change: Replaces SMSC version LAN951x Anomaly Rev. 1.1 (11-27-12).

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 11 Jan 2016

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s): [LAN951x FamilySilicon Errata and Data Sheet Clarification](#)

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Affected Catalog Part Numbers (CPN)

LAN9512-JZX-TR

LAN9512-JZX

LAN9512I-JZX

LAN9513-JZX-TR

LAN9513-JZX

LAN9513I-JZX-CAG

LAN9513I-JZX

LAN9514-JZX-TR

LAN9514-JZX

LAN9514I-JZX

LAN951x Family Silicon Errata and Data Sheet Clarification

This document describes known anomalies for functional revisions A and B of the LAN951x family of devices (LAN9512i/ LAN9512j, LAN9513/ LAN9513i, and LAN9514/ LAN9514i). The functional revision can be determined by its top marking as indicated in Figure 1 and Figure 2.

TABLE 1: SILICON ISSUE SUMMARY

Hardware Functional Rev A	Hardware Functional Rev B	Description
X	—	Module 1 : “Invalid USB Reset Prevents High-speed Operation”
X	X	Module 2 : “EEPROM Write or Erase Operation False Time-out”

Legend: X = Applicable to the Functional Rev.

FIGURE 1: TOP MARKING FOR FUNCTIONAL REVISION A DEVICE

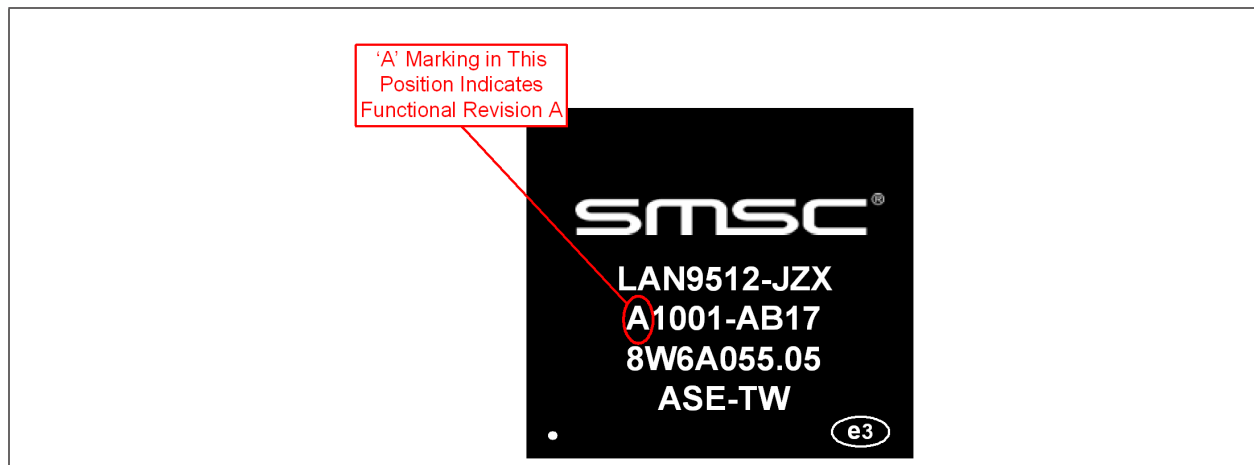
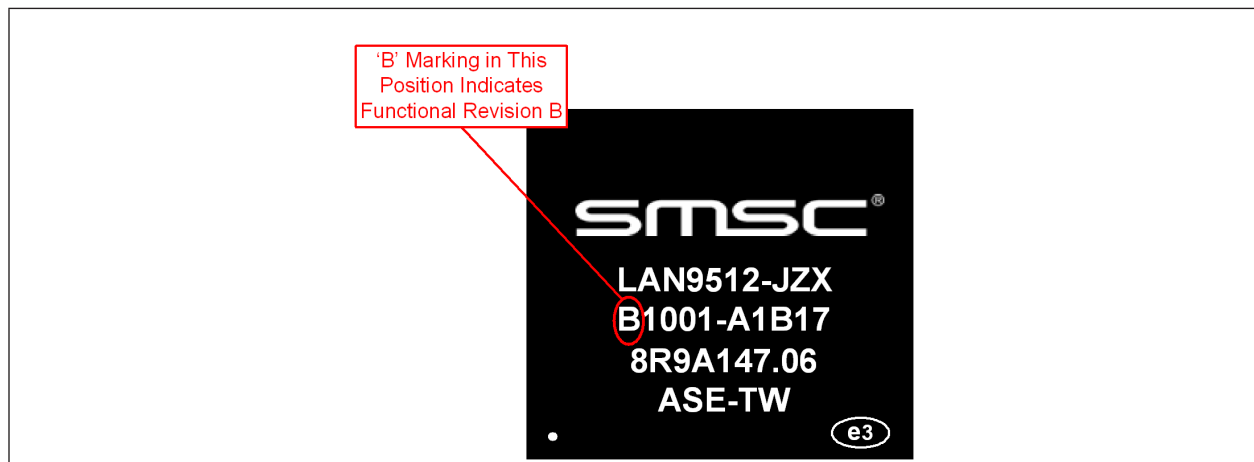


FIGURE 2: TOP MARKING FOR FUNCTIONAL REVISION B DEVICE



LAN951X

Note: These figures detail an example of the LAN9512 part. Other than the highlighted functional revision marking, other top marking values may differ (manufacture date, lot codes, etc.).

Silicon Errata Issue

Module 1: Invalid USB Reset Prevents High-speed Operation

Description

The USB 2.0 specification defines that a USB Reset (SE0 line state) must be at least 10 milliseconds long for a USB host and device to correctly negotiate the operating speed (for example, high- or full-speed). Microsoft® Windows® XP, Windows Vista and Windows 7 generates illegal USB Resets that are shorter than 10 ms. The short USB Resets have been observed when resuming from suspend (S3) and hibernate (S4) states on multiple platforms and southbridges. Microsoft has confirmed that the illegal short USB Reset violates the USB 2.0 specification and is a bug in the USB host driver.

As a result of the illegal reset, the LAN951x cannot enter high-speed operation and will remain in full-speed mode.

End User Implications

The user will notice that the LAN951x and devices connected to the LAN951x are running at full-speed instead of at high-speed. In Microsoft operating systems, a message notifies the user that high-speed capable devices have been plugged into full-speed ports.

Solution

Microsoft provides a hotfix on their support website. The link is <http://support.microsoft.com/kb/972485> for Windows Vista. Also note that this anomaly has been corrected in functional revision B of the LAN951x.

Plan

This anomaly has been corrected in functional revision B of the LAN951x.

Module 2: EEPROM Write or Erase Operation False Time-out

Description

The LAN951x may time-out during EEPROM write or erase operations. Affected EEPROM opcodes include WRITE, WRAL, ERASE and ERAL. Other EEPROM operations, including EEPROM reads as well as loading parameters on power-up or reset, are not affected.

During the affected cycle, the LAN951x will initiate the valid EEPROM write or erase operation. The operation will complete normally, but on completion, the LAN951x will initiate a second, anomalous EEPROM operation. In all cases, the second operation is ignored by the EEPROM and no data corruption occurs. Since the second operation is ignored by the EEPROM, the EPC Busy bit may not be cleared within 30 mS, thereby setting the EPC time-out bit.

End User Implications

There are no implications to the end user. In all cases the intended write or erase operation completes normally and the anomalous operation is ignored by the EEPROM. The false time-out should be ignored and the LAN951x can continue to use the EEPROM normally.

Solution

The user is advised to use the latest EEPROM programming tools provided by Microchip. The following versions detect the false time-out and take appropriate corrective actions:

- MS-DOS® utility version 2.0.4, or newer
- Windows® XP utility version 3.1.3.0, or newer

Please contact your Microchip Field Applications Engineer for the latest version of the programming tool.

Plan

There are no plans to address this anomaly in hardware.

APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS80000685A, 01/06/2016	Replaces SMSC version LAN951x Anomaly Rev. 1.1 (11-27-12).	
Rev. 1.1 (11-27-12)	Entire document.	Document co-branded: Microchip logo added, modification to legal disclaimer.
Rev. 1.1 (04-12-10)	Entire document.	Added top marking information.
	Section Module 2 : “EEPROM Write or Erase Operation False Time-out”	Added section.
Rev. 1.0 (08-26-09)	Initial release.	

LAN951X

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