

Product Change Notification - JAON-03JUWF661

Date: 04 Sep 2015

Product Category: Memory

Notification subject: CCB 940 Final Notice - Additional Fabrication Site: Qualification of 220K (0.18 micron) process technology for selected products of the 24AA256, 24FC256 and 24LC256 device families.

Notification text:

PCN Status:

Final notification

Microchip Parts Affected:

Please open the attachments found in the attachments field below labeled as PCN_#_Affected_CPN.

NOTE: For your convenience Microchip includes identical files in two formats (.pdf and .xls).

Description of Change:

Qualification of 220K (0.18 micron) process technology for selected products of the 24AA256, 24FC256 and 24LC256 device families.

Impacts to Data Sheet:

None

Reason for Change:

To improve manufacturability by qualifying an additional fabrication site.

Change Implementation Status:

In progress

Estimated First Ship Date:

October 15, 2015 (date code: 1542)

NOTE:

1. Please be advised that after the estimated first ship date customers may receive pre and post change parts.
2. In order to receive products only fabricated with the current 160K process please use the revised part number identified with RVF added to the end of the part number (see example below).

Standard Part Number: 24xx256x-x/xx

Revised Part Number (160K only): 24xx256x-x/xxRVF

Markings to Distinguish Revised from Unrevised Devices:

Traceability code

Revision History:

September 4, 2015: Issued final notification

The change described in this P_{CN} does not alter Microchip's current regulatory compliance regarding the material content of the applicable products.

Attachment(s):

[PCN_JAON-03JUWF661_Qual_Report.pdf](#) [PCN_JAON-03JUWF661_Affected_CPN.pdf](#) [PCN_JAON-03JUWF661_Affected_CPN.xls](#)

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| PCN_JAON-03JUWF661 |
|--------------------|
| CATALOG_PART_NBR |
| 24AA256-E/MF |
| 24AA256-E/MS |
| 24AA256-E/P |
| 24AA256-E/SM |
| 24AA256-E/SN |
| 24AA256-E/ST |
| 24AA256-I/MF |
| 24AA256-I/MS |
| 24AA256-I/P |
| 24AA256-I/SM |
| 24AA256-I/SN |
| 24AA256-I/ST |
| 24AA256T-E/MF |
| 24AA256T-E/MS |
| 24AA256T-E/SM |
| 24AA256T-E/SN |
| 24AA256T-E/ST |
| 24AA256T-I/MF |
| 24AA256T-I/MS |
| 24AA256T-I/SM |
| 24AA256T-I/SN |
| 24AA256T-I/ST |
| 24FC256-I/MF |
| 24FC256-I/MS |
| 24FC256-I/P |
| 24FC256-I/SM |
| 24FC256-I/SN |
| 24FC256-I/ST |
| 24FC256T-I/MF |
| 24FC256T-I/MS |
| 24FC256T-I/SM |
| 24FC256T-I/SN |
| 24FC256T-I/ST |
| 24LC256-E/MF |
| 24LC256-E/MS |
| 24LC256-E/P |
| 24LC256-E/SM |
| 24LC256-E/SN |
| 24LC256-E/ST |
| 24LC256T-E/MF |
| 24LC256T-E/MS |
| 24LC256T-E/SM |
| 24LC256T-E/SN |
| 24LC256T-E/ST |



PCN #: JAON-03JUWF661

**Date:
August 20, 2015**

**Qualification of an additional fabrication site for selected
products of the 24AA256, 24FC256 and 24LC256 device
families**

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QUALIFICATION DATA

Early Life Failure Rate Testing (ELFR):

| | |
|---------------------------|---|
| Test Method | AEC-Q100 |
| Test Condition | 150°C HTOL for 24 hours |
| Sample Size (800 ea. min) | 815, 824, 818 |
| Lot 1 | 0/815 (Fail/Pass) ^a |
| Lot 2 | 0/822 ^b (Fail/Pass) ^a |
| Lot 3 | 0/817 ^c (Fail/Pass) ^a |

^a Post Test was @ -40°C, ambient, 85°C & 125°C.

^b Two devices were discounted due to loss/handler damage.

^c One device was discounted due to V/M damage.

High Temperature Operating Life (HTOL)

| | |
|---------------------------|---|
| Test Method | MIL-STD 883 Method 1005 |
| Test Condition | 150°C HTOL for 408 hours |
| Sample Size (600 ea. min) | 615, 624, 620 |
| Lot 1 | 0/615 (Fail/Pass) ^a |
| Lot 2 | 0/623 ^d (Fail/Pass) ^a |
| Lot 3 | 0/620 (Fail/Pass) ^a |

^a Post Test was @ -40°C, ambient, 85°C & 125°C.

^d One device was discounted as Non-Fail after retest in Failure Analysis.

Endurance Cycling & Retention Bake (EDR / RET)

| | |
|---------------------------|---|
| Test Method | MIL-STD 883 Method 1033 |
| Test Condition | 10,000 Erase-Write cycles @ 85°C / Retention Bake @ 175°C for 504 hours |
| Sample Size (231 ea. min) | 241, 241, 241 |
| Lot 1 | 0/241 (Fail/Pass) ^a |
| Lot 2 | 0/241 (Fail/Pass) ^a |
| Lot 3 | 0/241 (Fail/Pass) ^a |

^a Post Test was @ -40°C, ambient, 85°C & 125°C.

Endurance Cycling / High Temperature Operating Life (EDR / HTOL-DLT)

| | |
|--------------------------|--|
| Test Method | MIL-STD 883 Method 1033 |
| Test Condition | 10,000 Erase-Write cycles @ 85°C / 150°C HTOL for 408 hours |
| Sample Size (77 ea. min) | 82, 82, 82 |
| Lot 1 | 0/82 (Fail/Pass) ^a |
| Lot 2 | 0/81e (Fail/Pass) ^a |
| Lot 3 | 0/81f (Fail/Pass) ^a |

^a Post Test was @ -40°C, ambient, 85°C & 125°C.

^e One device was discounted due to V/M damage.

^f One device was discounted after Failure Analysis, ESD FA# T151156

ESD

| Test | Reference Method | Sample Size | Result |
|-----------|------------------|-------------------|---|
| ESD – HBM | JEDEC JS-001 | 18ea ^h | +/- 6000V ^g |
| ESD – MM | ESD22-A115 | 18ea ^h | +/- 500V ^g |
| Latch-up | JESD78 | 12ea | 6 Pass @ 25°C ^g 6 Pass @ 125°C ^g |
| CDM | ANSI/ESD S5.3.1 | 18 | Pass up to +/- 2000V ^g |

^g Post Test was @ ambient & 125°C.

^h Three Pin Stress combinations were used, all pins with respect to Vss, all pins with respect to Vdd, all non-supply pins with respect to non-supply pins