

Product Change Notification - JAON-01QMAQ209

Date: 08 Apr 2015

Product Category: Memory; RF and Security; Supertex; Analog (Thermal, Power Management & Safety); Analog (Linear & Mixed Signal) AND Interface; Radio Frequency Devices; Touch Sensing Technologies; 8-bit Microcontrollers

Notification subject: CCB 1566 Initial Notice: Qualification of LPI assembly site as an additional site for selected products in 8L SOIC package.

Notification text:

PCN Status:

Initial notification

Microchip Parts Affected:

See attachments of affected catalog part numbers (CPN) labeled as...

P_{CN}_JAON-01QMAQ209_Affected_CPN.xls

P_{CN}_JAON-01QMAQ209_Affected_CPN.pdf

Description of Change:

Qualification of LPI assembly site as an additional site for selected products in 8L SOIC package.

NOTE: Selected products are non-automotive devices. Please

review the affected CPN lists (attached) to identify the actual parts affected.

Pre Change:

MTAI or MMT or ATES assembly site

Post Change:

MTAI or MMT or ATES or LPI assembly site

Impacts to Data Sheet:

None

Reason for Change:

To improve on-time delivery performance by qualifying LPI as an additional assembly site.

Change Implementation Status:

In Progress

Estimated First Ship Date:

May 15, 2015 (date code: 1520)

NOTE: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

Markings to Distinguish Revised from Unrevised Devices:

Traceability code

Revision History:

April 08, 2015: Issued initial notification.

The change described in this P_{CN} does not alter Microchip's current regulatory compliance regarding the material content of the applicable products.

Attachment(s):

[PCN_JAON-01QMAQ209_Qual_Plan.pdf](#) [PCN_JAON-01QMAQ209_Affected_CPN.pdf](#) [PCN_JAON-01QMAQ209_Affected_CPN.xls](#)

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MICROCHIP

QUALIFICATION PLAN

PCN #: JAON-01QMAQ209

**Date:
Mar 25, 2015**

**Qualification of LPI assembly site as an additional site for
selected products in 8L SOIC package.**

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Purpose: _____ Qualification of LPI assembly site as an additional site for selected products in 8L SOIC package.

MP code: _____ DEDX2

Part No.: _____ 24LC512

BD No.: _____ BDM-000731 rev.A

CCB No.: _____ 1566.01

Package:

Type _____ 8L SOIC

Width or Size _____ 150 mils

Die thickness: _____ 15 mils

Die size: _____ 78.7 x 111.0 mils

Lead frame:

Paddle size: _____ 95 x 130 mils

Material _____ CDA194

Surface _____ Ag spot

Process _____ Stamp

Lead Lock _____ No

Part Number _____ 09S000823

Treatment _____ None

Wire:

Material _____ Au

Die Attach Epoxy:

Part Number _____ 8340

Conductive _____ Yes

Mold Compound: _____ G600

Lead finish _____ Matte tin

Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Qty of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Special Instructions
Standard Pb-free Solderability	JESD22B-102E; Perform 8 hour steam aging for Matte tin finish and 1 hour steam aging for NiPdAu finish prior to testing. Standard Pb-free: Matte tin/ NiPdAu finish, SAC solder, wetting temp 245°C for both SMD & through hole packages.	22	5	1	27	> 95% lead coverage	5	Standard Pb-free solderability is the requirement. SnPb solderability (backward solderability—SMD reflow soldering) is required for any plating related changes and highly recommended for other package BOM changes.
Standard SnPb Solderability	JESD22B-102E; Perform 8 hour steam aging prior to testing. Standard SnPb: SnPb finish, SnPb solder, wetting temp 215°C for SMD & 245°C for through hole packages.	22	5	1	27	> 95% lead coverage	5	
Backward Solderability	JESD22B-102E; Perform 8 hours steam aging for Matte tin finish and 1 hour steam aging for NiPdAu finish prior to testing. Backward: Matte tin/ NiPdAu finish, SnPb solder, wetting temp 215°C for SMD.	22	5	1	27	> 95% lead coverage	5	
Wire Bond Pull - WBP	Mil. Std. 883-2011	5	0	1	5	0 fails after TC	5	30 bonds from a minimum of 5 devices.
Wire Bond Shear - WBS	CDF-AEC-Q100-001	5	0	1	5	0	5	30 bonds from a minimum of 5 devices.
Physical Dimensions	Measure per JESD22 B100 and B108	10	0	3	30	0	5	
External Visual	Mil. Std. 883-2009/2010	All devices prior to submission for qualification testing	0	3	ALL	0	5	
HTSL (High Temp Storage Life)	+175 C for 504 hours or 150°C for 1008 hrs. Electrical test pre and post stress at +25C and hot temp.	45	5	1	50	0	10	Must be in progress at time of package release to production, but completion is not required for release to production.

Test Name	Conditions	Sample Size	Min. Qty of Spares per Lot (should be properly marked)	Qty of Lots	Total Units	Fail Accept Qty	Est. Dur. Days	Special Instructions
Preconditioning - Required for surface mount devices	+150°C Bake for 24 hours, moisture loading requirements per MSL level + 3X reflow at peak reflow temperature per Jedec-STD-020D for package type; Electrical test pre and post stress at +25°C. MSL-1 @ 260°C	231	15	4	984	0	15	Spares should be properly identified. 77 parts from each lot to be used for HAST, Autoclave, Temp Cycle test.
HAST	+130°C/85% RH for 96 hours. Electrical test pre and post stress at +25°C and hot temp. 1 lot tested at 125C	77	5	4	328	0	10	Spares should be properly identified. Use the parts which have gone through Pre-conditioning.
Unbiased HAST	+130°C/85% RH for 96 hrs	77	5	4	328	0	10	Spares should be properly identified. Use the parts which have gone through Pre-conditioning.
Temp Cycle	-65°C to +150°C for 500 cycles. Electrical test pre and post stress at hot temp; 3 gram force WBP, on 5 devices from 1 lot, test following Temp Cycle stress. 1 lot tested at 125C	77	5	4	328	0	15	Spares should be properly identified. Use the parts which have gone through Pre-conditioning.

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