



**MxL86110**

Ethernet PHY

**Single Port Gigabit Ethernet PHY**

MxL86110C

MxL86110I

**Data Sheet**

Revision 1.2, 2025-07-02

Reference ID 620799

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## Revision History

**Current:** Revision 1.2, 2025-07-02

**Previous:** Revision 1.1, 2023-02-20

| Page | Major changes since Revision 1.1                                                                                                                                                                                                                                                                                                                                                      |
|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| All  | <ul style="list-style-type: none"> <li>Implemented language improvements and grammar corrections.</li> <li>Reformatted all &lt;REGISTER_NUMBER&gt;.&lt;FIELD_NUMBER&gt; (BB.CC) references to remove bold.</li> </ul>                                                                                                                                                                 |
| 13   | <b>Preface</b> <ul style="list-style-type: none"> <li>Added Document Conventions and Document Information.</li> </ul>                                                                                                                                                                                                                                                                 |
| 14   | <b>Chapter 1 Product Overview</b> <ul style="list-style-type: none"> <li>Corrected the text from 'CLKOUT' to 'GPC'.</li> </ul>                                                                                                                                                                                                                                                        |
| 15   | <b>Section 1.1 Features</b> <ul style="list-style-type: none"> <li>Corrected the 'CAT5' to 'CAT5e'.</li> </ul>                                                                                                                                                                                                                                                                        |
| 21   | <b>Table 3 Ethernet Media Interface Signals</b> <ul style="list-style-type: none"> <li>Moved pin 39 from 'Power Supply Pins' to 'Ethernet Media Interface'.</li> <li>Renamed the table's subheading to 'Ethernet Port Ethernet Media Interface'.</li> </ul>                                                                                                                           |
| 21   | <b>Table 4 RGMII Interface Signals</b> <ul style="list-style-type: none"> <li>Corrected 'soft pin-strapping' to 'pin strapping'.</li> </ul>                                                                                                                                                                                                                                           |
| 23   | <b>Table 5 LED Interface Signals</b> <ul style="list-style-type: none"> <li>Corrected 'soft pin-strapping' to 'pin strapping'.</li> </ul>                                                                                                                                                                                                                                             |
| 25   | <b>Table 7 Miscellaneous Signals</b> <ul style="list-style-type: none"> <li>Removed 'Crystal' from the function names.</li> <li>Arranged the pin numbers in ascending order.</li> </ul>                                                                                                                                                                                               |
| 26   | <b>Table 8 Power Supply Pins</b> <ul style="list-style-type: none"> <li>Pin 30 DCDC_REG0: Changed the function's long name from 'Internal DC/DC SVR Converter Output' to 'Switch Regulator 1.1 V Output' and updated the reference to the correct figure.</li> <li>Pin 39: Moved to the 'Ethernet Media Interface' table.</li> </ul>                                                  |
| 27   | <b>Section 2.2.3.6.1 Power Supply Using Integrated DC/DC SVR Converter</b> <ul style="list-style-type: none"> <li>Added this section to inform customers that this feature is available for use.</li> </ul>                                                                                                                                                                           |
| 32   | <b>Figure 10 Reset Timing Diagram</b> <ul style="list-style-type: none"> <li>Differentiated 'T<sub>reset</sub>' into two different periods: 'T<sub>reset_1</sub>' and 'T<sub>reset_2</sub>'.</li> </ul>                                                                                                                                                                               |
| 32   | <b>Table 11 Reset Timing Characteristics</b> <ul style="list-style-type: none"> <li>Differentiated 'T<sub>reset</sub>' into two different periods: 'T<sub>reset_1</sub>' and 'T<sub>reset_2</sub>'.</li> </ul>                                                                                                                                                                        |
| 32   | <b>Section 3.11 PHY Address</b> <ul style="list-style-type: none"> <li>Added 'PHYAD0' to correctly reflect the three pins required to set the PHY address.</li> </ul>                                                                                                                                                                                                                 |
| 33   | <b>Figure 11 RGMII Connection Diagram</b> <ul style="list-style-type: none"> <li>Corrected the position of the resistors in the figure.</li> <li>Simplified the figure title.</li> </ul>                                                                                                                                                                                              |
| 41   | <b>Table 16 Registers Overview - Standard Management</b> <ul style="list-style-type: none"> <li>STD_CTRL.SSM: Updated the description correcting the PHY mirror from '1.06' to '1.0.6'.</li> <li>STD_CTRL.SSL: Removed non-applicable information about 2500 Mbit/s operation.</li> <li>STD_PHYID2: Corrected the note to reference the 'Chip Ordering Information' table.</li> </ul> |

## Revision History (continued)

|     |                                                                                                                                                                                                                                                                                                                                                                                                                                     |
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| 63  | <p><b>Table 17 Registers Overview - PHY-specific Management Registers</b></p> <ul style="list-style-type: none"> <li>PHY_ADS_CTL: Corrected the reset value from '0082C<sub>H</sub>' to '082C<sub>H</sub>'.</li> <li>PHY_ADS_CTL: Redacted bits 11:5 by marking as Reserved. These bits are not for customer use.</li> </ul>                                                                                                        |
| 71  | <p><b>Section 5.2.5 Speed Auto Downgrade Control Register (Register 20)</b></p> <ul style="list-style-type: none"> <li>PHY_ADS_CTL: Corrected the reset value from '0082C<sub>H</sub>' to '082C<sub>H</sub>'.</li> <li>PHY_ADS_CTL: Redacted bits 11:5 by marking as Reserved. These bits are not for customer use.</li> <li>Renamed the RES fields.</li> </ul>                                                                     |
| 73  | <p><b>Section 5.2.7 Extended Register's Data Register (Register 31)</b></p> <ul style="list-style-type: none"> <li>PHY_EXT_DATA.EXTD: Updated the description to reference the &lt;REGISTER_NAME&gt;.&lt;FIELD_NAME&gt; (BB.CC), PHY_EXT_ADR.EXTA.</li> </ul>                                                                                                                                                                       |
| 81  | <p><b>Chapter 7 Extended Register Detailed Description</b></p> <ul style="list-style-type: none"> <li>Reformatted all trailing hexadecimal indicators in register summary tables to use subscript.</li> </ul>                                                                                                                                                                                                                       |
| 83  | <p><b>Section 7.1.1 Chip Configuration Register (Register A001<sub>H</sub>)</b></p> <ul style="list-style-type: none"> <li>COM_EXT_CHIP_CFG.GERXC: Improved and expanded the description.</li> <li>COM_EXT_CHIP_CFG.RXDLY: Corrected the description from 'Tx' to 'Rx'.</li> <li>COM_EXT_CHIP_CFG.ELDO: Corrected the description and correctly marked that the default value is '0<sub>B</sub> LDO Disabled (Default)'.</li> </ul> |
| 89  | <p><b>Section 7.1.4 RGMII In-Band Status and MDIO Configuration Register (Register A005<sub>H</sub>)</b></p> <ul style="list-style-type: none"> <li>COM_EXT_RGMII_MIDO_CFG.EBA: Changed the default to '0<sub>B</sub> Disabled'.</li> <li>Renamed the RES fields.</li> </ul>                                                                                                                                                        |
| 94  | <p><b>Section 7.1.9 Wake on LAN Control Register (Register A00A<sub>H</sub>)</b></p> <ul style="list-style-type: none"> <li>Corrected the register's subheading from 'Wake on LAN Address Byte 1 and 0'.</li> <li>COM_EXT_LED_BLINK_CFG.RES: Removed extra 'Reserved' text.</li> </ul>                                                                                                                                              |
| 95  | <p><b>Section 7.1.10 LED General Configuration Register (Register A00B<sub>H</sub>)</b></p> <ul style="list-style-type: none"> <li>Aligned the register reference to use the &lt;REGISTER_NAME&gt;.&lt;FIELD_NAME&gt; (BB.CC) naming format.</li> <li>COM_EXT_LED_GEN_CFG.COLBS: Corrected the text from 'value' to 'valid'.</li> <li>COM_EXT_LED_GEN_CFG.RES: Removed 'Reserved. The default is 0<sub>B</sub>'.</li> </ul>         |
| 97  | <p><b>Section 7.1.11 LED0 Configuration Register (Register A00C<sub>H</sub>)</b></p> <ul style="list-style-type: none"> <li>COM_EXT_LED0_CFG.LFDE0: Improved the description for 1<sub>B</sub>.</li> </ul>                                                                                                                                                                                                                          |
| 104 | <p><b>Section 7.1.14 LED Blinking Configuration Register (Register A00F<sub>H</sub>)</b></p> <ul style="list-style-type: none"> <li>COM_EXT_LED_BLINK_CFG: Changed a space to an underscore in the name from 'COM_EXT_LED BLINK_CFG'.</li> <li>COM_EXT_LED_BLINK_CFG.RES: Removed extra 'Reserved' text.</li> <li>COM_EXT_LED_BLINK_CFG.LFEQ1: Inserted a space in between the '1' and 'Frequency' in the description.</li> </ul>   |
| 105 | <p><b>Section 7.1.15 Pin Driving Strength Configuration Register (Register A010<sub>H</sub>)</b></p> <ul style="list-style-type: none"> <li>Corrected the register name from 'LED Blinking Configuration Register'.</li> <li>Expanded the information regarding drive strength values to align with other register descriptions for RSDR, RSD2, DSE, DM, RSD10, DII, and DL.</li> </ul>                                             |
| 107 | <p><b>Section 7.1.16 SyncE Configuration Register (Register A012<sub>H</sub>)</b></p> <ul style="list-style-type: none"> <li>Corrected the register name from 'Pin Driving Strength Configuration Register'.</li> </ul>                                                                                                                                                                                                             |

## Revision History (continued)

|     |                                                                                                                                                                                                                                                                                                                                                                                |
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| 109 | <b>Section 7.2.1 10 M Base-Tx Debug Mode Register (Register 000A<sub>H</sub>)</b> <ul style="list-style-type: none"> <li>Corrected 'BASE-T' to 'BASE-Tx' in the subheading's description.</li> <li>Renamed the RES fields.</li> <li>UTP_EXT_10BT_DBG.RES0: Removed extra 'Reserved' text.</li> </ul>                                                                           |
| 110 | <b>Section 7.2.2 Sleep Mode Control Register (Register 0027<sub>H</sub>)</b> <ul style="list-style-type: none"> <li>Renamed the RES fields.</li> </ul>                                                                                                                                                                                                                         |
| 111 | <b>Section 7.2.3 Packet Rx Valid High Register (Register 00A3<sub>H</sub>)</b> <ul style="list-style-type: none"> <li>UTP_EXT_PKG_RX_VALID_0.PIVH: Corrected the location of the lower 16-bits from 'UTP_EXT_PKG_RX_OS_1.PIVL' to 'UTP_EXT_PKG_RX_VALID_1.PIVL'.</li> </ul>                                                                                                    |
| 113 | <b>Section 7.2.5 Packet Rx Oversize High Register (Register 00A5<sub>H</sub>)</b> <ul style="list-style-type: none"> <li>Corrected the register's subheading from 'Packet Rx Oversize Low Register'.</li> </ul>                                                                                                                                                                |
| 114 | <b>Section 7.2.6 Packet Rx Oversize Low Register (Register 00A6<sub>H</sub>)</b> <ul style="list-style-type: none"> <li>Corrected the register's subheading from 'Packet Rx Valid Low Register'.</li> </ul>                                                                                                                                                                    |
| 115 | <b>Section 7.2.7 Packet Rx Undersize High Register (Register 00A7<sub>H</sub>)</b> <ul style="list-style-type: none"> <li>UTP_EXT_PKG_RX_US_0.PIUGH: Corrected the field's long name from 'Good Rx Packet Count High' to 'Rx Undersize Packet Count High'.</li> </ul>                                                                                                          |
| 116 | <b>Section 7.2.8 Packet Rx Undersize Low Register (Register 00A8<sub>H</sub>)</b> <ul style="list-style-type: none"> <li>UTP_EXT_PKG_RX_US_1.PIUGL: Corrected the field's long name from 'Good Rx Packet Count Low' to 'Rx Undersize Packet Count Low'.</li> </ul>                                                                                                             |
| 118 | <b>Section 7.2.10 Packet Rx CRC Oversize Register (Register 00AA<sub>H</sub>)</b> <ul style="list-style-type: none"> <li>UTP_EXT_PKG_RX_OS_BAD.PIOB: Corrected '&gt;=' to '&gt;'.</li> </ul>                                                                                                                                                                                   |
| 119 | <b>Section 7.2.11 Packet Rx Fragment Register (Register 00AB<sub>H</sub>)</b> <ul style="list-style-type: none"> <li>Corrected the register's subheading from 'Packet Rx CRC Oversize Register'.</li> <li>UTP_EXT_PKG_RX_FRAGMENT.PIF: Corrected '&lt;=' to '&lt;'.</li> </ul>                                                                                                 |
| 120 | <b>Section 7.2.12 Packet Rx No SFD Register (Register 00AC<sub>H</sub>)</b> <ul style="list-style-type: none"> <li>Corrected the register's subheading from 'Packet Rx CRC Oversize Register'.</li> </ul>                                                                                                                                                                      |
| 121 | <b>Section 7.2.13 Packet Tx High Register (Register 00AD<sub>H</sub>)</b> <ul style="list-style-type: none"> <li>Corrected the register's subheading from 'Packet Rx CRC Oversize Register'.</li> </ul>                                                                                                                                                                        |
| 125 | <b>Section 7.2.17 Packet Tx Undersize High Register (Register 00B1<sub>H</sub>)</b> <ul style="list-style-type: none"> <li>Corrected the register's subheading from 'Oversize Low'.</li> </ul>                                                                                                                                                                                 |
| 126 | <b>Section 7.2.18 Packet Tx Undersize Low Register (Register 00B2<sub>H</sub>)</b> <ul style="list-style-type: none"> <li>UTP_EXT_PKG_TX_US_1.POUGL: Corrected the field's long name from 'Good Tx Packet Count Low' to 'Tx Undersize Packet Count Low'.</li> <li>UTP_EXT_PKG_TX_US_1.POUGL: Corrected the packet length from '&gt; 1518 bytes' to '&lt; 64 bytes'.</li> </ul> |
| 127 | <b>Section 7.2.19 Packet Tx CRC Register (Register 00B3<sub>H</sub>)</b> <ul style="list-style-type: none"> <li>Corrected the register's subheading from 'Packet Tx Undersize Low Register'.</li> </ul>                                                                                                                                                                        |
| 131 | <b>Table 24 Absolute Maximum Ratings</b> <ul style="list-style-type: none"> <li>Removed the typical values column.</li> </ul>                                                                                                                                                                                                                                                  |
| 132 | <b>Table 25 Supply Voltage and Temperature</b> <ul style="list-style-type: none"> <li>Corrected the VDD3V3/VDDDAV3 minimum value from '2.97' to '3.14'.</li> </ul>                                                                                                                                                                                                             |
| 134 | <b>Table 27 Device Power Consumption</b> <ul style="list-style-type: none"> <li>Corrected the 'VDDP' table header cell to 'VDDP3V3'.</li> </ul>                                                                                                                                                                                                                                |
| 134 | <b>Table 28 Maximum Device Power Consumption</b> <ul style="list-style-type: none"> <li>Corrected the 'VDDP' table header cell to 'VDDP3V3'.</li> </ul>                                                                                                                                                                                                                        |

## Revision History (continued)

|             |                                                                                                                                                                          |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 142         | <b>Figure 17 PG-QFN-40 Mechanical Drawing</b> <ul style="list-style-type: none"><li>Increased figure resolution.</li></ul>                                               |
| 144         | <b>Section 9.2 Chip Identification and Ordering Information</b> <ul style="list-style-type: none"><li>Added a note about where to find the latest information.</li></ul> |
| 147         | <b>Terminology</b> <ul style="list-style-type: none"><li>Added the terms I<sup>2</sup>C, LQFP, MBIST, RGMII, RMII, XO, and XTC.</li><li>Removed SGMII.</li></ul>         |
| <b>Page</b> | <b>Major changes since Revision 1.0</b>                                                                                                                                  |
| All         | Added a Third-Party Trademark Declarations section.                                                                                                                      |
| 14          | <b>Chapter 1 Product Overview</b> <ul style="list-style-type: none"><li>Updated chapter.</li></ul>                                                                       |
| 15          | <b>Section 1.1 Features</b> <ul style="list-style-type: none"><li>Updated chapter.</li></ul>                                                                             |
| 18          | <b>Chapter 2 External Signals</b> <ul style="list-style-type: none"><li>Updated chapter.</li></ul>                                                                       |
| 28          | <b>Chapter 3 Functional Description</b> <ul style="list-style-type: none"><li>Updated chapter.</li></ul>                                                                 |
| 37          | <b>Chapter 4 MDIO and MMD Register Interface Description</b> <ul style="list-style-type: none"><li>Updated chapter.</li></ul>                                            |
| 41          | <b>Section 5.1 Standard Management Registers</b> <ul style="list-style-type: none"><li>Updated chapter.</li></ul>                                                        |
| 63          | <b>Section 5.2 PHY-specific Management Registers</b> <ul style="list-style-type: none"><li>Updated chapter.</li></ul>                                                    |
| 75          | <b>Section 6.1 Standard PCS Registers for MMD=0003<sub>H</sub></b> <ul style="list-style-type: none"><li>Updated chapter.</li></ul>                                      |
| 78          | <b>Section 6.2 Standard Auto-Negotiation Registers for MMD=0007<sub>H</sub></b> <ul style="list-style-type: none"><li>Updated chapter.</li></ul>                         |
| 82          | <b>Section 7.1 Common Extended Register</b> <ul style="list-style-type: none"><li>Updated chapter.</li></ul>                                                             |
| 108         | <b>Section 7.2 UTP Extended Register</b> <ul style="list-style-type: none"><li>Updated chapter.</li></ul>                                                                |
| 131         | <b>Chapter 8 Electrical Characteristics</b> <ul style="list-style-type: none"><li>Updated chapter.</li></ul>                                                             |
| 141         | <b>Chapter 9 Package Outline</b> <ul style="list-style-type: none"><li>Updated chapter.</li></ul>                                                                        |
| 147         | <b>Terminology</b> <ul style="list-style-type: none"><li>Updated chapter.</li></ul>                                                                                      |
|             |                                                                                                                                                                          |

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## Preface

This Data Sheet describes the features and system architecture of the single port Gigabit Ethernet PHYs MxL86110C and MxL86110I.

*Note: The device address map is considered as a flat address map implementation. There is no mailbox functionality behind the MDIO interface.*

## Document Conventions

In the interest of brevity, this document uses short names to represent full MaxLinear product names.

|                  |                                                        |
|------------------|--------------------------------------------------------|
| <b>MxL86110</b>  | Synonym used for the Single Port Ethernet PHY MxL86110 |
| <b>MxL86110C</b> | Ethernet PHY MxL86110C                                 |
| <b>MxL86110I</b> | Ethernet PHY MxL86110I                                 |

## Document Information

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### Organization of this Document

- [Chapter 1, Product Overview](#)  
This chapter provides an overview.
- [Chapter 2, External Signals](#)  
This chapter provides the external signals.
- [Chapter 3, Functional Description](#)  
This chapter provides the function description.
- [Chapter 4, MDIO and MMD Register Interface Description](#)  
This chapter describes the MDIO and MMD register format.
- [Chapter 5, MDIO Registers Detailed Description](#)  
This chapter details the MDIO registers.
- [Chapter 6, MMD Registers Detailed Description](#)  
This chapter details the MDD registers.
- [Chapter 7, Extended Register Detailed Description](#)  
This chapter details the extended register.
- [Chapter 8, Electrical Characteristics](#)  
This chapter provides the electrical specifications.
- [Chapter 9, Package Outline](#)  
This chapter provides information about the package.
- [Standards References](#)
- [Terminology](#)

**Attention:** *MaxLinear only guarantees the behavior of the device based on documented registers.*

*The device does not offer any protection against access to other non-documented addresses over the MDIO interface.*

## 1 Product Overview

The MxL86110 is a low power Ethernet PHY transceiver integrated circuit following the IEEE 802.3 [1] standard. It offers a cost-optimized solution that is well-suited for routers, switches, and home gateways. It performs data transmission on an Ethernet twisted pair copper cable of category CAT5e or higher. The MxL86110 supports 1000, 100, and 10 Mbit/s data rates.

On the Ethernet twisted pair interface, the MxL86110 is compliant with the 1000BASE-T (IEEE802.3 Clause 40), 100BASE-TX (IEEE 802.3 Clause 25), and 10BASE-T<sub>e</sub> (IEEE 802.3 Clause 14) standards defined by the IEEE 802.3 [1]. This interface supports the Energy-Efficient Ethernet (EEE) feature in accordance with IEEE802.3 [1] to reduce idle mode power consumption. Power saving at the system level is also possible with the Wake-on-LAN feature. A low-EMI line driver with integrated termination facilitates PCB design.

The MxL86110 supports a standard MDIO management interface as defined in IEEE 802.3 Clause 22 and Clause 45 [1]. The MDIO serial interface operates with a clock running up to 12.5 MHz. This allows a management entity (the external chip implementing the MAC) to access standard MDIO / MMD registers to control the MxL86110 behavior, or to read the link status. In addition, vendor specific register banks allow MxL86110-specific configuration of LED and Wake-on-LAN features. The MDIO and MMD registers are documented in [Chapter 5](#) and [Chapter 6](#), respectively. The MxL86110 is also configurable via pin strapping.

The MxL86110 is able to drive up to three LEDs. Each LED is independently programmable to indicate the link speed, and traffic activity. Several indication schemes are selectable.

A DC/DC converter is integrated within the MxL86110. A single external power supply of 3.3 V is sufficient to power the chip, with the internal DC/DC converter generating 1.1 V to supply the low voltage domains. External supply of both 3.3 V and 1.1 V is also an option.

The MxL86110 is available in a Quad Flat Non-leaded package (PG-QFN-40). It therefore provides an ideal solution for footprint-sensitive applications such as SFP copper modules or Ethernet Controllers. Furthermore, the MxL86110 design supports a reduced external bill of materials, for example through the integration of termination resistors at both the MDI and MII. The GPC pin is able to be optionally used to provide a 25 MHz reference clock, allowing for multiple PHY devices to be cascaded while using only one crystal.

The MxL86110 uses a PG-QFN-40 package which is 5 x 5 mm in size.

The MxL86110 has a built-in switching regulator for 1.1 V core power.

The MxL86110 has a built-in LDO providing 2.5/1.8 V power for the RGMII I/O interface.

## 1.1 Features

This section provides an overview of the features supported by the MxL86110.

### Communication Interfaces

- The multiple speed, single-port Ethernet PHY interface to the twisted pair cable supports:
  - Ethernet modes and standards: 1000BASE-T (IEEE 802.3), 100BASE-TX (IEEE 802.3) and 10BASE-T (IEEE 802.3)
  - Ethernet twisted pair copper cable of category CAT5e or higher
  - Low EMI voltage mode line driver with integrated termination resistors
  - Transformerless Ethernet for backplane applications
  - Auto-Negotiation (ANEG) with extended next page support
  - Auto-MDIX and polarity correction
  - Auto-Downspeed (ADS)
  - Energy-Efficient Ethernet (EEE) and power down mode
  - Wake-on-LAN (WoL)
  - 10k byte jumbo frame support.
- RGMII Interface
- The management interface supports the communication between the Station Management Entity (STA) and the MxL86110 using:
  - An MDIO slave interface that provides access to the standard registers in the MMD as described in IEEE 802.3 Clause 22 and Clause 45 [\[1\]](#) and listed in [Chapter 5](#) and [Chapter 6](#).
  - An MDIO interface clock of up to 12.5 MHz
  - Three MDIO message frame types as described in IEEE 802.3: Clause 22, Clause 22 Extended, and Clause 45 [\[1\]](#)

LED Interface, which supports:

- Up to three LEDs
- Single color LEDs
- Connection of LED to ground or 3.3 V
- Several LED indication schemes (link/activity, link speed)
- Configuration of LED indication via Extended Registers

Supports one interrupt output to external controller.

## Clocking and Timing Features

- 25 MHz crystal operation

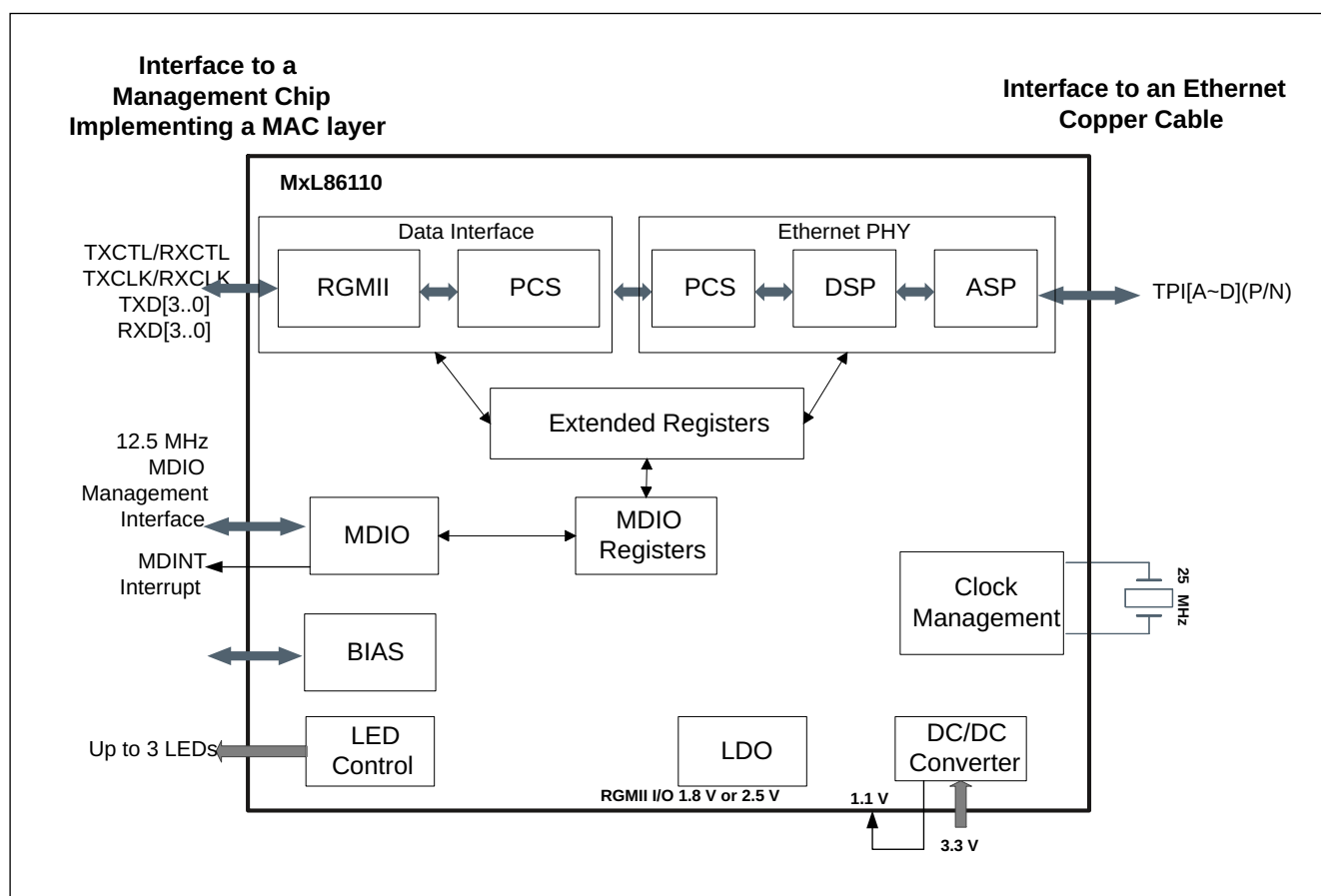
## Power Supply

- Single 3.3 V power supply, when using the integrated switching regulator to DC/DC converter to generate the 1.1 V power supply rail
- If the internal integrated DC/DC converter is not used, an additional 1.1 V supply must be provided externally
- Built-in LDO for RGMII IO power 2.5/1.8 V

## 1.2 Block Diagram

**Figure 1** shows the block diagram for the MxL86110. The main interfaces are:

- Data interface to a MAC processor, using RGMII
- Slave control interface driven by a MAC processor, using MDIO slave
- Interrupt signal MDINT allowing the MxL86110 to notify the MAC processor about a change of status
- LED control
- Twisted Pair Interface (TPI)



**Figure 1 MxL86110 Block Diagram**

## 1.3 Target Applications

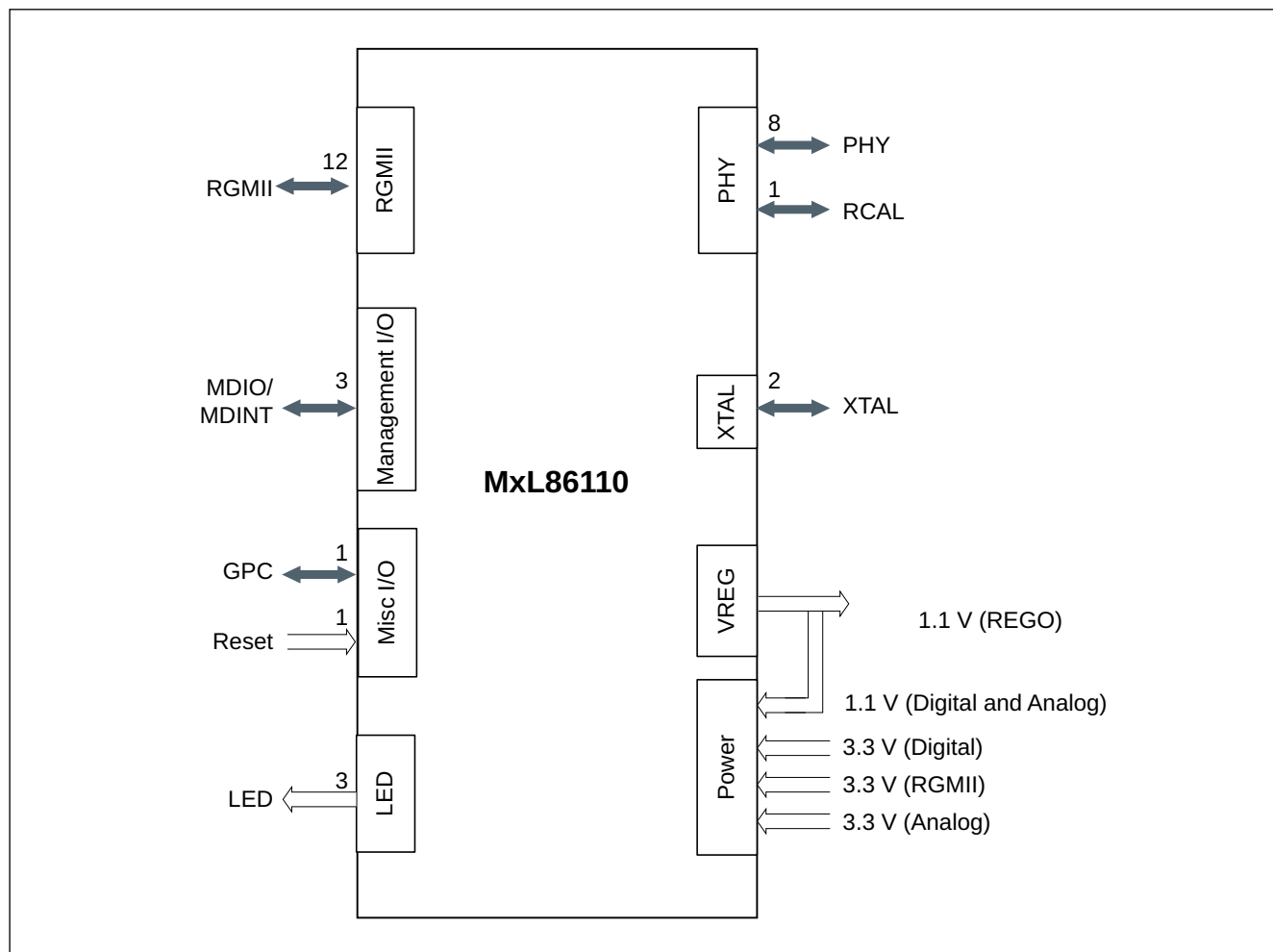
- Gateways
- Routers
- Wi-Fi access points
- Set-top-boxes
- IP-phones
- Digital TVs
- Ethernet switches
- NAS
- DVD Players
- Game consoles
- Printers
- Office machines
- Industrial PCs
- IoT devices
- PoE applications

## 2 External Signals

This chapter describes the signal mapping to the package.

### 2.1 Overview

**Figure 2** provides an overview of the external interfaces of the MxL86110.



**Figure 2** MxL86110 External Signals Overview

## 2.2 External Signal Description

This section provides the pin diagram, abbreviations for pin types and buffer types, as well as tables describing the input and output signals.

### 2.2.1 Pin Diagram

Figure 3 shows the pin layout for the MxL86110 package.

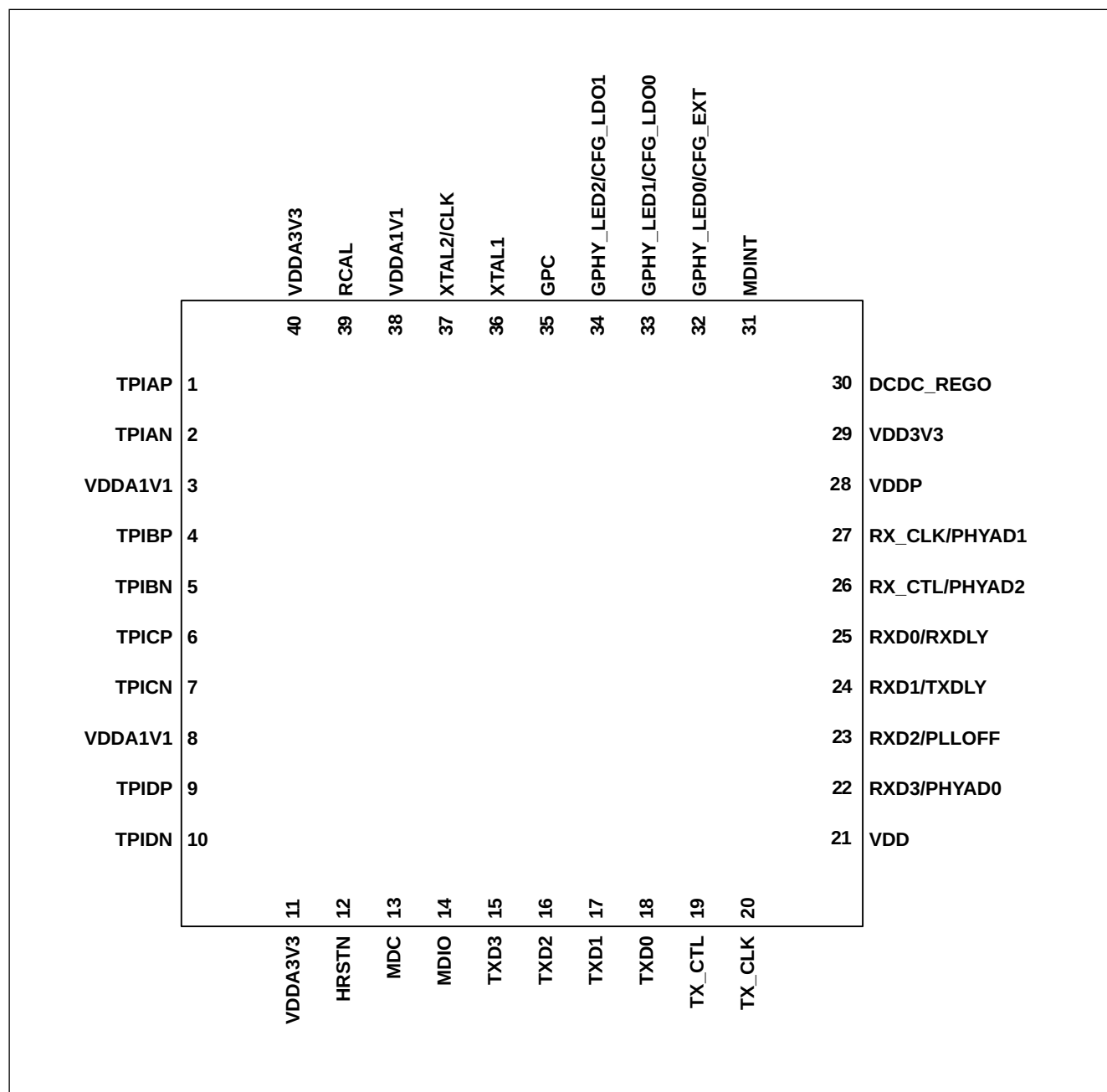


Figure 3 Pin Diagram for MxL86110

## 2.2.2 Abbreviations

Abbreviations that are used in the signal tables are summarized in [Table 1](#) and [Table 2](#).

**Table 1 Abbreviations for Pin Type**

| Abbreviations | Description                                       |
|---------------|---------------------------------------------------|
| I             | Input only, digital levels                        |
| O             | Output only, digital levels                       |
| I/O           | Bidirectional input/output signal, digital levels |
| AI            | Input only, analog levels                         |
| AO            | Output only, analog levels                        |
| AI/O          | Bidirectional, analog levels                      |
| PWR           | Power                                             |
| GND           | Ground                                            |

**Table 2 Abbreviations for Buffer Type**

| Abbreviations | Description                                                                                    |
|---------------|------------------------------------------------------------------------------------------------|
| A             | Analog characteristics<br>See <a href="#">Electrical Characteristics</a> for more information. |
| GND           | Ground                                                                                         |
| OD            | Open Drain                                                                                     |
| PU            | Internal pull-up resistor                                                                      |
| PD            | Internal pull-down resistor                                                                    |

## 2.2.3 Input/Output Signals

A detailed description of all the pins is given in [Table 3](#) to [Table 7](#).

In [Table 3](#) to [Table 7](#), the signal names highlighted in bold are the same as the pin name.

The primary function is listed first and then alternate functions.

### 2.2.3.1 Ethernet Media Interface

[Table 3](#) describes the Ethernet Media Interface's TPI pins which uses pins 1-10.

**Table 3 Ethernet Media Interface Signals**

| Pin No.                                | Name  | Pin Type | Buffer Type | Function                                                                                     |
|----------------------------------------|-------|----------|-------------|----------------------------------------------------------------------------------------------|
| Ethernet Port Ethernet Media Interface |       |          |             |                                                                                              |
| 1                                      | TPIAP | AI/AO    | A           | Twisted Pair Transmit/Receive Positive/Negative                                              |
| 2                                      | TPIAN | AI/AO    | A           |                                                                                              |
| 4                                      | TPIBP | AI/AO    | A           |                                                                                              |
| 5                                      | TPIBN | AI/AO    | A           |                                                                                              |
| 6                                      | TPICP | AI/AO    | A           |                                                                                              |
| 7                                      | TPICN | AI/AO    | A           |                                                                                              |
| 9                                      | TPIDP | AI/AO    | A           |                                                                                              |
| 10                                     | TPIDN | AI/AO    | A           |                                                                                              |
| Ethernet Port Ethernet Media Interface |       |          |             |                                                                                              |
| 39                                     | RCAL  | AO       | A           | Calibration of GPHY Ethernet Port<br>Connect a high precision resistor of 2.49 kΩ ±1% to GND |

### 2.2.3.2 RGMII

[Table 4](#) describes the RGMII interface-related pins which uses pins 15-20 and 22-27.

**Table 4 RGMII Interface Signals**

| Pin No.                        | Name        | Pin Type | Buffer Type | Function                                                                                                                            |
|--------------------------------|-------------|----------|-------------|-------------------------------------------------------------------------------------------------------------------------------------|
| <b>RGMII Interface Signals</b> |             |          |             |                                                                                                                                     |
| 15                             | <b>TXD3</b> | I        | PD          | <b>RGMII: Transmit Data Bit 3</b><br>This pin carries bit 3 of the TXD[3:0] RGMII transmit data vector. It is synchronous with TXC. |
| 16                             | <b>TXD2</b> | I        | PD          | <b>RGMII: Transmit Data Bit 2</b><br>This pin carries bit 2 of the TXD[3:0] RGMII transmit data vector. It is synchronous with TXC. |
| 17                             | <b>TXD1</b> | I        | PD          | <b>RGMII: Transmit Data Bit 1</b><br>This pin carries bit 1 of the TXD[3:0] RGMII transmit data vector. It is synchronous with TXC. |
| 18                             | <b>TXD0</b> | I        | PD          | <b>RGMII: Transmit Data Bit 0</b><br>This pin carries bit 0 of the TXD[3:0] RGMII transmit data vector. It is synchronous with TXC. |

External Signals

Table 4 RGMII Interface Signals (continued)

| Pin No. | Name              | Pin Type | Buffer Type | Function                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|---------|-------------------|----------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19      | TX_CTL            | I        | PD          | <b>RGMII: Transmit Control</b><br>This pin is the transmit control signal for the TXD[3:0] RGMII transmit data vector. It is synchronous with TXC.                                                                                                                                                                                                                                                                                        |
| 20      | TX_CLK            | I        | PD          | <b>RGMII: Transmit Clock</b><br>The TXC signal is a continuous clock signal and provides the timing reference for the transfer of TX_EN_CTL and TXD[3:0]. The nominal frequency of this clock is 125 MHz for 1000 Mbit/s, 25 MHz for 100 Mbit/s, and 2.5 MHz for 10 Mbit/s. Depending on the speed selection, this clock is assumed to be properly adjusted by the MAC. The frequency deviation is assumed to be smaller than +/- 50 ppm. |
| 22      | RXD3<br>/PHYAD0   | I/O      | PD          | <b>RGMII: Receive Data Bit 3</b><br>This pin carries bit 3 of the RXD[3:0] RGMII receive data vector. It is synchronous with RXC.<br><b>PHYAD0:</b> This pin reads in pin-strapping information during reset.                                                                                                                                                                                                                             |
| 23      | RXD2<br>/PLLOFF   | I/O      | PD          | <b>RGMII: Receive Data Bit 2</b><br>This pin carries bit 2 of the RXD[3:0] RGMII receive data vector. It is synchronous with RXC.<br><b>PLLOFF:</b> This pin reads in pin-strapping information during reset.                                                                                                                                                                                                                             |
| 24      | RXD1<br>/TXDLY    | I/O      | PD          | <b>RGMII: Receive Data Bit 1</b><br>This pin carries bit 1 of the RXD[3:0] RGMII receive data vector. It is synchronous with RXC.<br><b>TXDLY:</b> This pin reads in pin-strapping information during reset.                                                                                                                                                                                                                              |
| 25      | RXD0<br>/RXDLY    | I/O      | PD          | <b>RGMII: Receive Data Bit 0</b><br>This pin carries bit 0 of the RXD[3:0] RGMII receive data vector. It is synchronous with RXC.<br><b>RXDLY:</b> This pin reads in pin-strapping information during reset.                                                                                                                                                                                                                              |
| 26      | RX_CTL<br>/PHYAD2 | I/O      | PD          | <b>RGMII: Receive Control</b><br>This is the receive control signal driven by the PHY, and which is synchronous with RXC. The signal encodes the RX_DV and RX_ER signals of the GMII.<br><b>PHYAD2:</b> This pin reads in pin-strapping information during reset.                                                                                                                                                                         |
| 27      | RX_CLK<br>/PHYAD1 | I/O      | PD          | <b>RGMII: Receive Clock</b><br>The RXC signal is a continuous clock signal and provides the timing reference for the transfer of RX_EN_CTL and RXD[3:0]. The nominal frequency of this clock is 125 MHz for 1000 Mbit/s, 25 MHz for 100 Mbit/s and 2.5 MHz for 10 Mbit/s. The frequency deviation is smaller than +/-50 ppm.<br><b>PHYAD1:</b> This pin reads in pin-strapping information during reset.                                  |

### 2.2.3.3 LED Interface

**Table 5** describes the LED interface-related pins which allow external LEDs to be connected to the MxL86110C/MxL86110I to indicate the status of the Ethernet PHY interfaces. The LED interface uses pins 32-34.

**Table 5 LED Interface Signals**

| Pin No.            | Name                       | Pin Type | Buffer Type | Function                                                                                                                                           |
|--------------------|----------------------------|----------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>LED Signals</b> |                            |          |             |                                                                                                                                                    |
| 32                 | <b>GPHY_LED0 /CFG_EXT</b>  | I/O      | PU          | <b>GPHY LED0</b><br>The LED control output drives single color LEDs.<br><b>CFG_EXT:</b> This pin reads in pin-strapping information during reset.  |
| 33                 | <b>GPHY_LED1 /CFG_LDO0</b> | I/O      | PU          | <b>GPHY LED1</b><br>The LED control output drives single color LEDs.<br><b>CFG_LDO0:</b> This pin reads in pin-strapping information during reset. |
| 34                 | <b>GPHY_LED2 /CFG_LDO1</b> | O        | PD          | <b>GPHY LED2</b><br>The LED control output drives single color LEDs.<br><b>CFG_LDO1:</b> This pin reads in pin-strapping information during reset. |

## 2.2.3.4 Management Interfaces

**Table 6** describes the MIDO slave interface pins which uses pins 13, 14, and 31.

**Table 6 Management Interface Signals**

| Pin No.                     | Name         | Pin Type | Buffer Type | Function                                                                                                                                                                    |
|-----------------------------|--------------|----------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>MDIO Slave Interface</b> |              |          |             |                                                                                                                                                                             |
| 13                          | <b>MDC</b>   | I        | PD          | <b>MDIO Slave Clock</b><br>The external controller host, also called STA by the IEEE, acts as clock master and provides the serial clock of up to 12.5 MHz on this input.   |
| 14                          | <b>MDIO</b>  | I/O      | PU          | <b>MDIO Slave Data Input/Output</b><br>The external controller host uses this signal to address internal registers and to transfer data to and from the internal registers. |
| 31                          | <b>MDINT</b> | O        | OD          | <b>MDIO Interrupt</b><br>The MDINT signal is used to send an interrupt to an external MAC SoC acting as station manager (STA).                                              |

### 2.2.3.5 Miscellaneous Signals

**Table 7** lists miscellaneous signals required by the device.

**Table 7 Miscellaneous Signals**

| Pin No.                   | Name  | Pin Type | Buffer Type | Function                                                                                                                                                                                                                                                |
|---------------------------|-------|----------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Reset and Clocking</b> |       |          |             |                                                                                                                                                                                                                                                         |
| 12                        | HRSTN | I        | PU          | <b>Hardware Reset</b><br>Asynchronous active low device reset.                                                                                                                                                                                          |
| 35                        | GPC   | O        | –           | <b>General Purpose Clock</b><br>1. This is the reference clock generated from the internal PLL. This pin must be kept floating when the clock is not used by the MAC.<br>2. UTP recovery receive clock for Sync Ethernet.<br>3. 25 MHz reference clock. |
| 36                        | XTAL1 | AI       | A           | <b>Oscillator Input</b><br>A crystal must be connected between XTAL1 and XTAL2. Additional load capacitances must also tie both pins to GND.                                                                                                            |
| 37                        | XTAL2 | AO       | A           | <b>Oscillator Output</b><br>A crystal must be connected between XTAL1 and XTAL2. Additional load capacitances must also tie both pins to GND.                                                                                                           |
|                           | CLK   | I        | –           | <b>Clock Input</b><br>The clock must have a frequency accuracy of $\pm 50$ ppm. When connecting an external 25 MHz oscillator or clock from another device to XTAL2 pin, XTAL1 must be tied to GND.                                                     |

### 2.2.3.6 Power Supply

This section specifies the power supply pins. The device is supplied by two supply rails,  $V_{\text{HIGH}}$  (3.3 V) and  $V_{\text{LOW}}$  (1.1 V). The  $V_{\text{LOW}}$  domain is able to be either be supplied externally, or self-generated by the internal DC/DC Selecting Voltage Regulator (SVR) converter, which converts the VDD3V3 supply into DCDC\_REGO output. In the external supply configuration, the DCDC\_REGO output pins are not connected (NC). In the internal DC/DC SVR converter configuration, the DCDC\_REGO output pins are connected back to the  $V_{\text{LOW}}$  supply inputs.

**Table 8 Power Supply Pins**

| Pin No.                  | Name      | Pin Type | Buffer Type | Function                                                                                                                                                                                                                                                                                                                                                                     |
|--------------------------|-----------|----------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Power Supply Pins</b> |           |          |             |                                                                                                                                                                                                                                                                                                                                                                              |
| 11, 40                   | VDDA3V3   | PWR      | —           | <b>High Voltage Domain Supply <math>V_{\text{HIGH}}</math></b><br>These are the input power pins for the analog front end in the high voltage domain. They must be supplied with a nominal voltage of $V_{\text{DDA3V3}} = 3.3 \text{ V}$ .                                                                                                                                  |
| 3, 8, 38                 | VDDA1V1   | PWR      | —           | <b>Low Voltage Domain Supply <math>V_{\text{LOW}}</math></b><br>These are the input power supply pins for the low voltage domain. These pins must be supplied with a nominal voltage of 1.1 V. When the internal DC/DC SVR converter is used, they must be connected to the output of the converter DCDC_REGO.                                                               |
| 28                       | VDDP      | PWR      | —           | <b>Configurable MDIO Pin Voltage Domain Supply</b><br>The voltage domains for the digital RGMII I/O and MDC/MDIO are controlled by the pins CFG_EXT, CFG_LDO0, and CFG_LDO1. See <a href="#">Section 3.16</a> for the settings.<br>No matter whether the I/O pin power form external or internal, a bulk capacitor and a decoupling capacitor must be connected to this pin. |
| 21                       | VDD       | PWR      | —           | <b>Core Voltage Domain Supply <math>V_{\text{LOW}}</math></b><br>This is the group of supply pins for the core digital voltage domain. This pin must be supplied with a nominal voltage of $V_{\text{DD}} = 1.1 \text{ V}$ . When the internal DC/DC SVR converter is used, these pins must be connected to the output of the converter DCDC_REGO.                           |
| 29                       | VDD3V3    | PWR      | —           | <b>Power Supply <math>V_{\text{HIGH}}</math></b><br>This pin must be supplied with a nominal voltage of $V_{\text{DD3V3}} = 3.3 \text{ V}$ .                                                                                                                                                                                                                                 |
| 30                       | DCDC_REGO | PWR      | —           | <b>Switch Regulator 1.1 V Output</b><br>The connection circuitry for the internal DCDC SVR $V_{\text{LOW}}$ supply option and the external $V_{\text{LOW}}$ supply option are described in <a href="#">Figure 4</a> .                                                                                                                                                        |

**Table 9** Device Ground

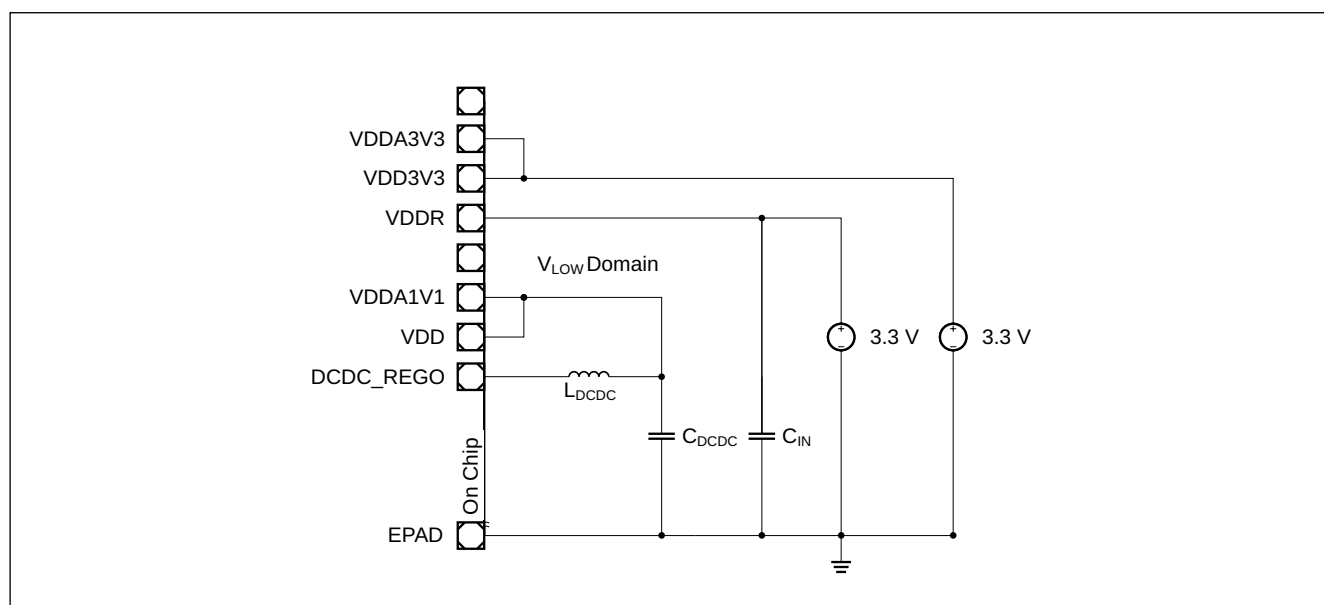
| Pin No.            | Name | Pin Type | Buffer Type | Function              |
|--------------------|------|----------|-------------|-----------------------|
| EPAD <sup>1)</sup> | VSS  | GND      | –           | General device ground |

1) The EPAD is the exposed pin on the bottom of the package. This pin must be properly connected to the ground plane of the PCB.

### 2.2.3.6.1 Power Supply Using Integrated DC/DC SVR Converter

The MxL86110 is capable of being powered using a single 3.3 V supply when the integrated DC/DC converter is used. As long as the applied nominal voltage remains within the operating range specified in [Section 8.2](#), the device operates automatically and without the need for additional settings to be applied. Only minor external circuitry is required to enable this feature. [Figure 4](#) shows an example schematic. The electrical characteristics of the power supply are defined in [Section 8.2](#).

The required values for the external components are listed in [Table 10](#).



**Figure 4** External Circuitry Using the Integrated DC/DC Converter

**Table 10** External Component Values for DC/DC Converter

| Parameter                   | Symbol     | Values |                |      | Unit          | Note / Test Condition                        |
|-----------------------------|------------|--------|----------------|------|---------------|----------------------------------------------|
|                             |            | Min.   | Typ.           | Max. |               |                                              |
| DC/DC Buck Inductance       | $L_{DCDC}$ | –      | 2.2            | –    | $\mu\text{H}$ | $\text{DCR}_{\text{max}} = 0.07 \text{ ohm}$ |
| DC/DC Smoothing Capacitance | $C_{DCDC}$ | –      | 4.7            | –    | $\mu\text{F}$ | –                                            |
|                             |            | –      | 0.1            | –    | $\mu\text{F}$ | –                                            |
| DC/DC Input Capacitance     | $C_{IN}$   | –      | 4.7            | –    | $\mu\text{F}$ | –                                            |
|                             |            | –      | $2 \times 0.1$ | –    | $\mu\text{F}$ | –                                            |

## 3 Functional Description

This chapter describes the functions available to the MxL86110.

### 3.1 Management Interface

The status and control registers of the device are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3, Section 22 and also support MDC clock rates up to 12.5 MHz.

### 3.2 Auto-Negotiation (ANEG)

The MxL86110 negotiates its operation mode using the ANEG mechanism according to IEEE 802.3 Clause 28 over copper media. ANEG supports choosing the mode of operation automatically by comparing its own abilities and received abilities from link partner. The advertised abilities include:

- Speed: 10/100/1000Mbps
- Duplex mode: full-duplex and/or half-duplex

ANEG is initialized when these scenarios occur:

- Power-up/Hardware/Software reset
- ANEG restart
- Transition from power down to normal operation of the port
- Link down

ANEG is enabled for MxL86110 by default, and is disabled by software control.

### 3.3 Polarity Detection and Auto Correction

The MxL86110 is capable of detecting and correcting two types of cable errors automatically.

- Swapped pairs within the UTP cable:
  - Pair 0 and 1, and/or pair 2 and 3.
- Swapped wires within a pair.

### 3.4 Loopback Mode

The MxL86110 supports several test loops to support system integration.

#### 3.4.1 Near-End Test Loops

Digital loopback provides the ability to loop transmitted data back to the receiver using digital circuitry in the MxL86110.

The near-end test loops are used to verify system integration of an MxL86110 device. They allow for closed loopback of data and signals at different Open Systems Interconnection (OSI) reference layers. [Section 3.4.2](#) and [Section 3.4.3](#) describe these loopback functions in descending order of OSI abstraction layer. Digital loopback is set via `STD_CTRL.LB = 1B`. See [Section 5.1.1](#).

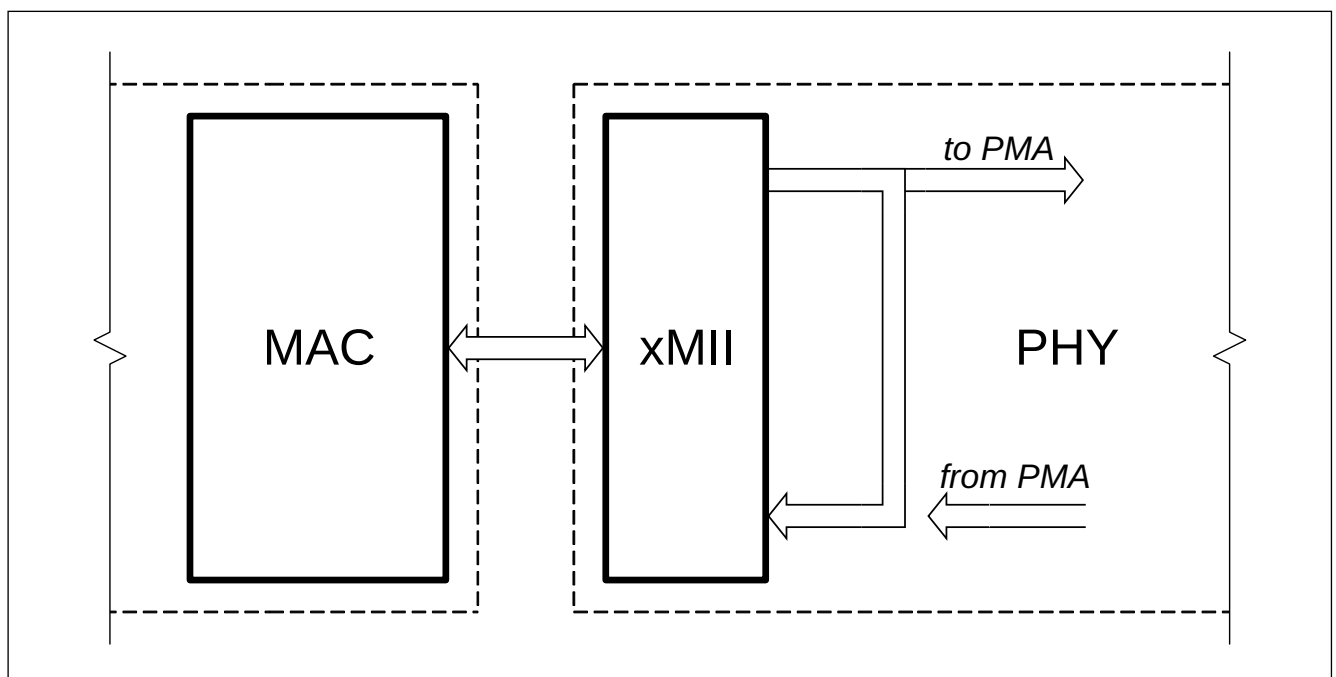


Figure 5 Near-End Loopback

#### 3.4.2 External Loopback

The MxL86110 supports an external loopback with help of a physical connection at the RJ45 connector as shown in [Figure 6](#). This allows a complete Tx -> Rx cable loopback.

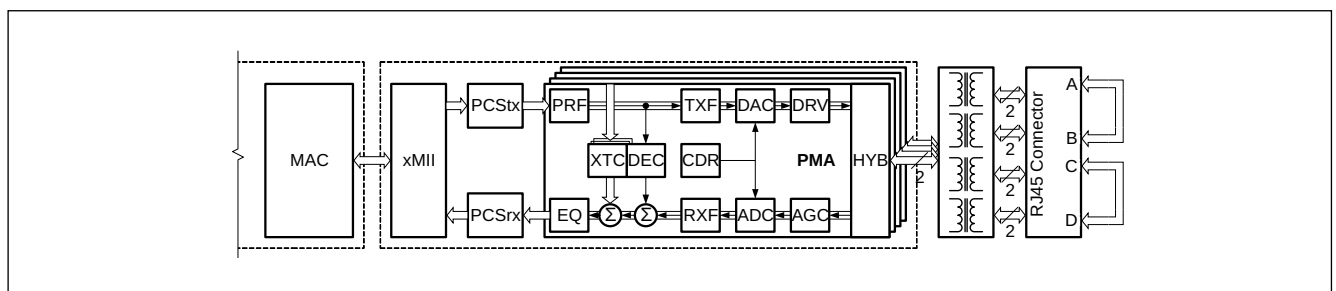
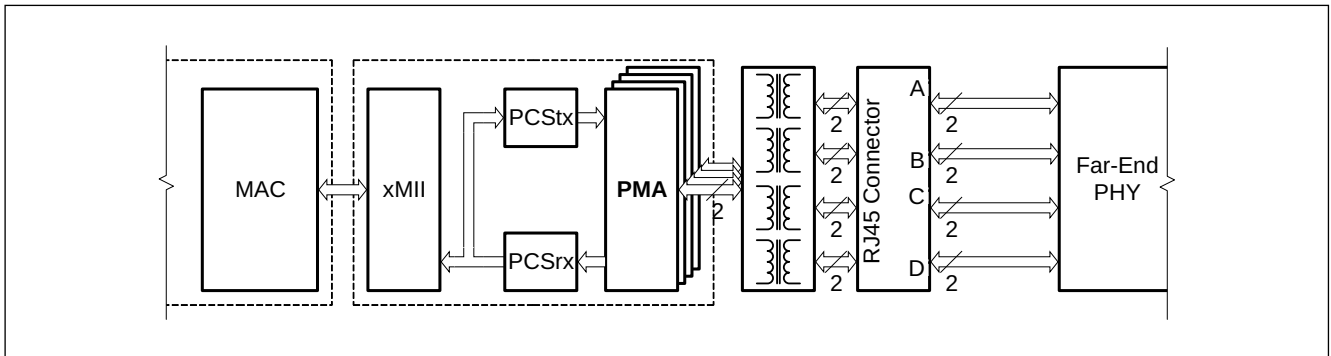


Figure 6 External Loopback

Note: External loopback is set via `UTP_EXT_10BT_DBG.ELB`. See [Section 7.2](#).

### 3.4.3 Far-End PHY Loopback

The Far-End loopback mode connects the MDI Rx path to the MDI Tx path close to RGMII interface as shown in [Figure 7](#). With this function, it is possible for the Far-End PHY to detect the proper connectivity.

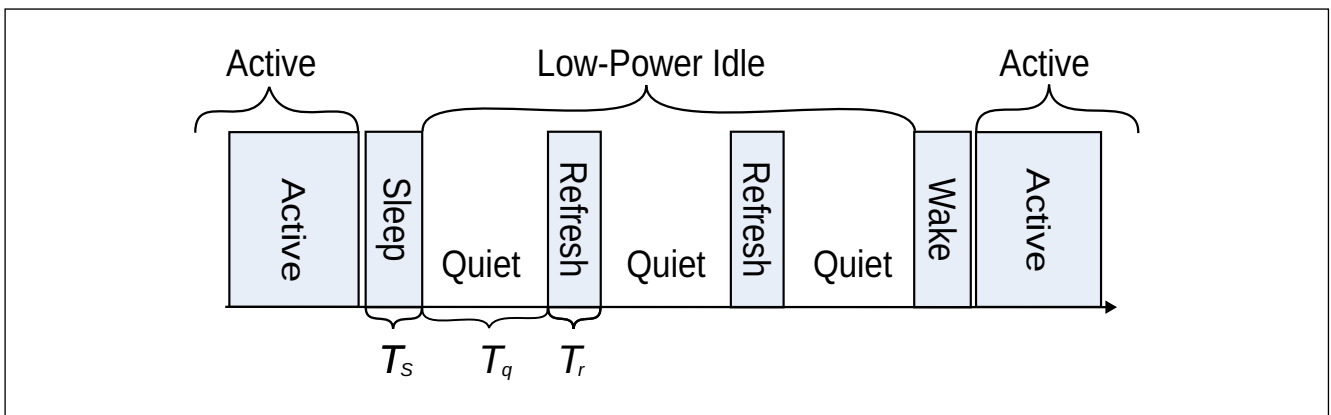


**Figure 7** Far-End PHY Loopback

Note: Remote PHY loopback is set via `COM_EXT_MISC_CFG.RLBP`. See [Section 7.2](#).

## 3.5 Energy Efficient Ethernet (EEE)

The IEEE 802.3 standard [\[1\]](#) describes the EEE operation that is supported by the MxL86110. EEE is supported in the various speeds of 100BASE-TX and 1000BASE-T. The general idea of EEE is to save power during periods of low link utilization. Instead of sending active idle data, the transmitters are switched off for a short period of time. This is called the quiet period in the standard. The link is kept active by means of a frequent refresh cycle initiated by the PHY itself while in the low power state. This sequence is repeated until a wake request is generated by one of the link partner MACs.



**Figure 8** EEE Low Power Idle Sequence

## 3.6 Synchronous Ethernet (SyncE)

The MxL86110 provides Synchronous Ethernet (SyncE) support when the device is operating in 1000BASE-T and 100BASE-TX on the transmission media. It is possible to assign the GPC pin to output the recovered clock. The MxL86110 allows a SyncE interface to support transportation of a source-referable clock from a clock master to clock clients. This is supported in 1000BASE-T and 100BASE-T mode on the TPI.

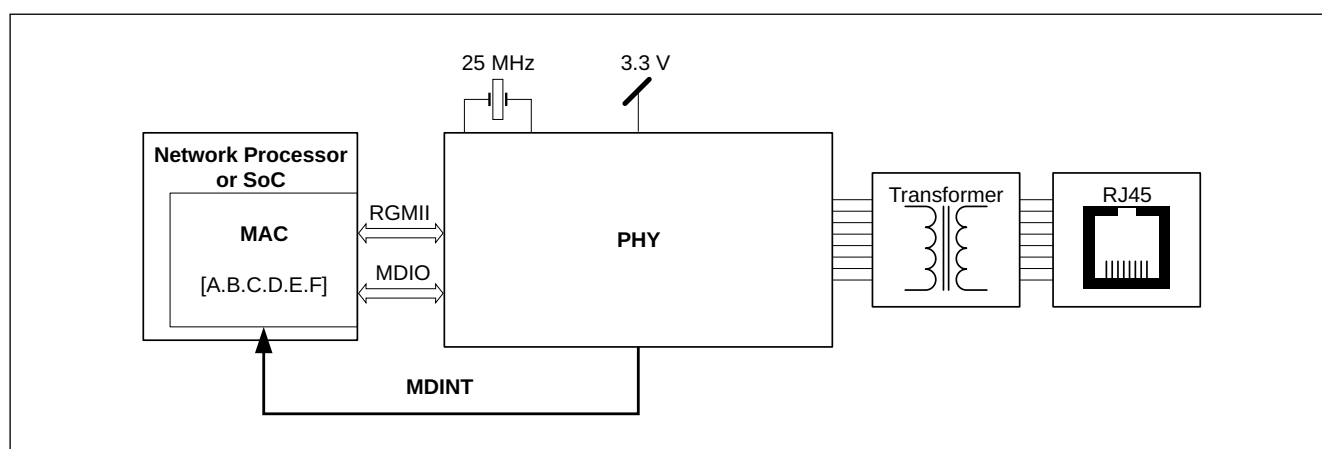
- In 1000BASE-T, the GPC outputs the recovered clock from PHY<->PHY.
- In slave mode, the GPC outputs the recovered clock from MDI.
- In master mode, the GPC outputs the clock from local free running PLL.

When the GPC pin is assigned to output the recovered clock from the PHY and the PHY is configured for 1000BASE-T mode, the function of the GPC varies depending upon the current PHY mode.

- When the PHY is in slave mode, the GPC outputs the recovered clock from the MDI.
- When the device is in master mode, the GPC outputs the clock based on the local free run PLL.

### 3.7 Wake-On-LAN (WoL)

The MxL86110 supports WoL. The MxL86110 generates an interrupt to an external controller when it detects special WoL Ethernet packets. This allows the controller to enter into sleep mode when there is no Ethernet traffic to process, and be woken up when traffic starts. WoL packets are detected at all link speeds. [Figure 9](#) shows this scenario. The specific frame contains a specific data sequence located anywhere inside the packet. The 48-bit address is set using the COM\_EXT\_MAC\_ADDR\_CFG1, COM\_EXT\_MAC\_ADDR\_CFG2, and COM\_EXT\_MAC\_ADDR\_CFG3 registers. See [Section 7.1](#).



**Figure 9 WoL Application Block Diagram**

The most commonly used WoL packet is called a magic packet. A magic packet contains the MAC address of the device to be woken up.

### 3.8 Link Down Power Saving (Sleep Mode)

The MxL86110 supports link down power saving, also called sleep mode. The MxL86110 enters sleep mode after around 40 seconds if no signals are received over the Ethernet cable.

In sleep mode, the MxL86110 disables almost all circuits, nevertheless access by MDC/MDIO interface remains available.

Once signals are detected on an Ethernet cable, the MxL86110 exits sleep mode automatically.

### 3.9 Interrupt

The MxL86110 provides an active low interrupt output signal (MDINT) based on change of the PHY status. Every interrupt condition is mapped to the read-only general interrupt status register by the read-only general interrupt status register. See [Section 5.2](#) for more information.

The interrupts are individually enabled or disabled by setting or clearing bits in the interrupt enable register [Section 5.2](#). See PHY\_IMASK [Section 5.2.3](#).

The MDINT signal is used to send an interrupt to an external MAC SoC acting as station manager (STA). The STA is able to program its sensitivity to specific events using the PHY\_IMASK register. The MDINT event is then raised when the event occurs. It is possible for the STA to read which type of event occurred in the PHY\_ISTAT register. Upon reading of PHY\_ISTAT by the STA, the MDINT is deasserted by the MxL86110.

Note: The interrupt of the MxL86110 is a level-triggered mechanism.

### 3.10 Reset

The MxL86110 has a hardware reset (HRSTN) pin. The HRSTN signal must be active for at least 10 ms after power-up. After the HRSTN is released, the MxL86110 latches the input values on the strapping pins to configure the device settings. This is useful for configuring the device in applications where MDIO access is unavailable. After a hardware reset, there is a 100 ms MDIO access delay to complete MxL86110 internal initialization.

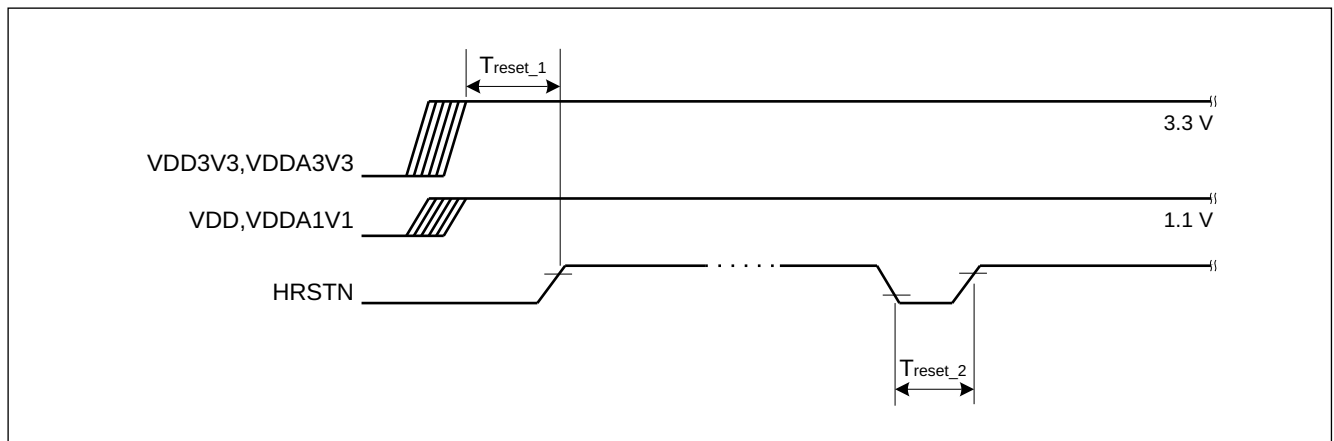


Figure 10 Reset Timing Diagram

Table 11 Reset Timing Characteristics

| Symbol               | Description                                                                              | Min. | Typ. | Max. | Units |
|----------------------|------------------------------------------------------------------------------------------|------|------|------|-------|
| T <sub>reset_1</sub> | The amount of time to allow all power rails to stabilize before releasing HRSTN to high. | 10   | -    | -    | ms    |
| T <sub>reset_2</sub> | The minimum amount of time for a reset signal to be recognized.                          | 10   | -    | -    | ms    |

### 3.11 PHY Address

The MxL86110 offers the ability to configure the PHY address from the pins PHYAD0/PHYAD1/PHYAD2. In addition, MxL86110 supports broadcast address 0 on the MDIO bus. This feature enables PHY to always respond to MDIO access. It is controlled via the COM\_EXT\_RGMII\_MDIO\_CFG register. See [Section 7.1](#) for more information.

The MxL86110 supports the option to configure a dedicated broadcast PHY address.

### 3.12 RGMII Interface

The RGMII interface implements a MAC interface which is usable for all supported speeds (10/100/1000 Mbit/s). The transfer of data between the MAC and PHY devices is handled via a clock signal, a control signal, and a four bit data vector in both the transmit and receive directions. The clock signal is always driven by the signal source, which is the MAC in the transmit direction and PHY in the receive direction. The control and data signals change with both the rising and falling edges of the driving clock.

The nominal driving clock frequency at 1000 Mbit/s data speeds is 125 MHz. Lower speeds of 100 Mbit/s and 10 Mbit/s use a clock frequency of 25 MHz and 2.5 MHz respectively. At these lower speeds, the higher half of the data octet is empty and the signals on TXD[3:0] and RXD[3:0] are duplicated.

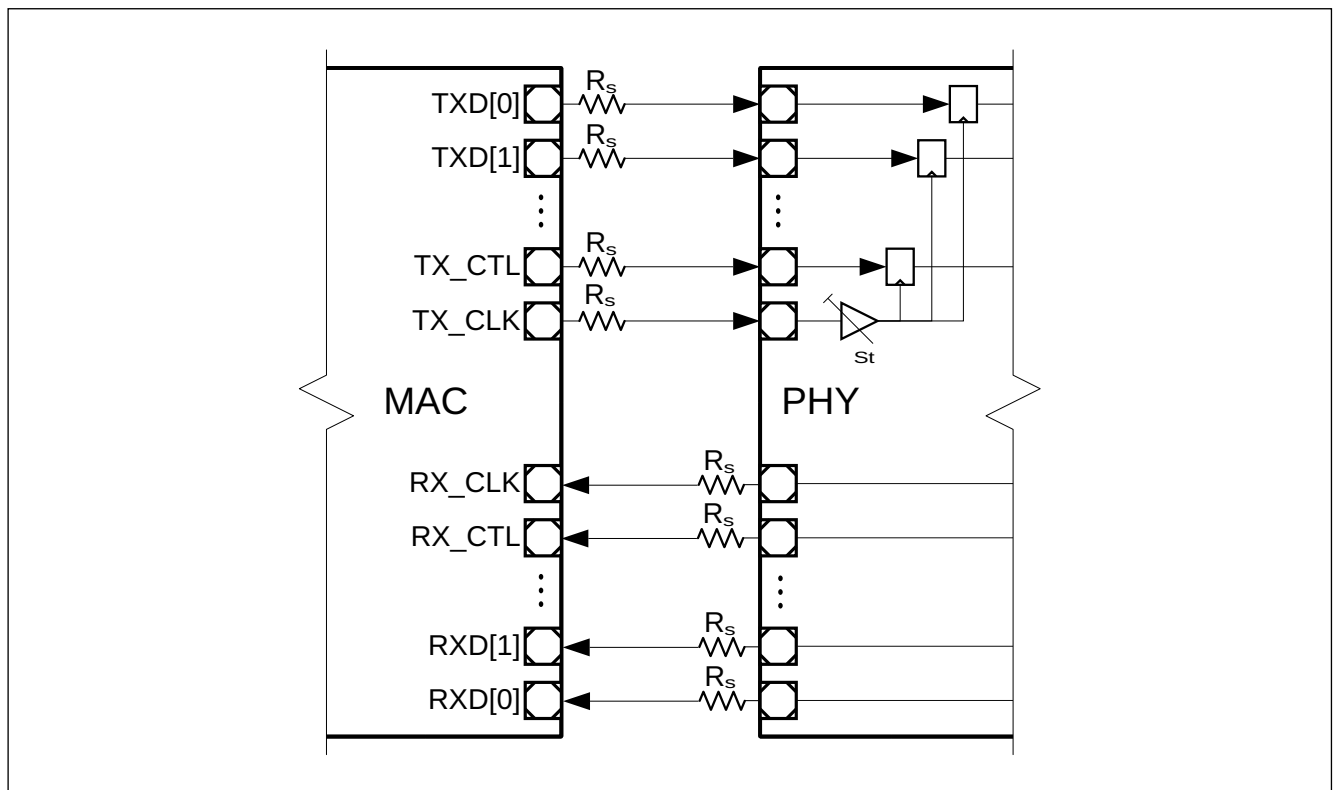


Figure 11 RGMII Connection Diagram

### 3.13 LED Interface

The LED interface is controllable by two methods: by the PHY or manually controlled. The LED interface provides up to three LEDs to provide visual indication of the link speed, duplex, and link status. The LEDs are programmable by the MDIO interface via direct register access. [Figure 12](#) shows the LED circuit design.

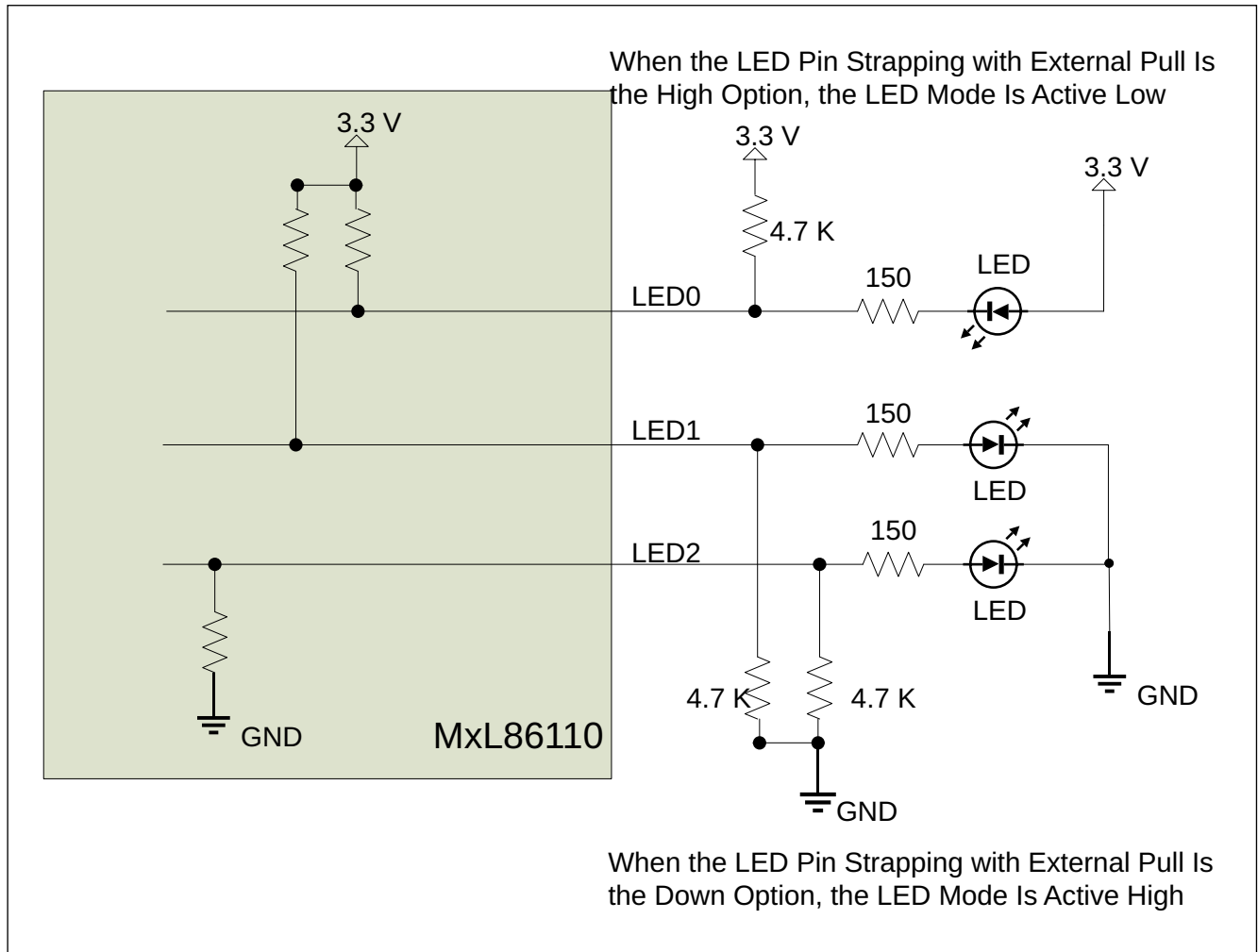


Figure 12 LED Circuit Design

### 3.14 MDINT Pin Usage

The MDINT pin is used to notify the network processor, or SoC, of both interrupt and WoL events. For general use, indication of a WoL event is also integrated into one of the interrupt events which is triggered when any specified WoL event occurs.

### 3.15 Power Supply Rails

The MxL86110 requires only one external supply rail of 3.3 V. The device has an integrated SVR which generates the 1.1 V rail, as well as an LDO to adapt to different RGMII levels (either 2.5 / 1.8 V).

The RGMII I/O voltage level is set via external strapping.

When the integrated SVR is not used, the MxL86110 must be powered by a 3.3 V and 1.1 V dual power supply. See [Section 8.2](#) for more information on the electrical characteristics of the power supply. In external supply mode, the DCDC\_REGO output pins are left unconnected. The integrated SVR converter is able to be switched off after power up.

### 3.16 Configuration by Pin Strapping

The MxL86110 device is configured by means of pin strapping several pins. The pin strapping configurations are captured during the chip power-on sequence, until the reset initialization is complete. The pin strap values are set to logical high or low by connecting the corresponding pin via an external 1 kΩ resistor to either ground or the VDD domain supply for the pin strapping pins. For example, GPHY\_LED0/1/2 connects to either ground or 3.3 V and RXD3/2/1/0/RX\_CLK/RXCTL connects to either ground or the VDDP domain.

The pin strap mapping is described in [Table 12](#) and [Table 13](#).

**Table 12 Pin Names Used for Pin Strapping**

| Pin Name  | Pin Number | Configuration Item Description |
|-----------|------------|--------------------------------|
| RXD3      | 22         | PS_PHY_MADDR(0)                |
| RXD2      | 23         | PLLOFF                         |
| RXD1      | 24         | TXDLY                          |
| RXD0      | 25         | RXDLY                          |
| RX_CTL    | 26         | PS_PHY_MADDR(2)                |
| RX_CLK    | 27         | PS_PHY_MADDR(1)                |
| GPHY_LED0 | 32         | CFG_EXT                        |
| GPHY_LED1 | 33         | CFG_LDO0                       |
| GPHY_LED2 | 34         | CFG_LDO1                       |

**Table 13 Pin Strapping Configuration Description**

| Pin Strapping Signals | Description                                                                                                                                                                                                             |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PS_PHY_MADDR(2:0)     | <b>MDIO PHY Address</b><br>A high level means a logical 1 and low level means a logical 0.                                                                                                                              |
| PLLOFF                | <b>PLL off Configuration During Sleep Mode</b><br>0 <sub>B</sub> PLL is on during sleep mode.<br>1 <sub>B</sub> PLL is off during sleep mode.                                                                           |
| TXDLY                 | <b>RGMII Transmit Clock Timing Control</b><br>0 <sub>B</sub> No additional delay on TX_CLK.<br>1 <sub>B</sub> Enable 2 ns delay on TX_CLK when TX_CLK is 125 MHz or 8 ns delay on TX_CLK when TX_CLK is 25 MHz/2.5 MHz. |
| RXDLY                 | <b>RGMII Receiver Clock Timing Control</b><br>0 <sub>B</sub> No additional delay on RX_CLK.<br>1 <sub>B</sub> Enable 2 ns delay on RX_CLK when RX_CLK is 125 MHz or 8 ns delay on RX_CLK when RX_CLK is 25 MHz/2.5 MHz. |

Functional Description

**Table 13** Pin Strapping Configuration Description (continued)

| Pin Strapping Signals | Description                                                                                                                                                                                                                                                 |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFG_EXT               | <b>External Power Source Mode Configuration</b><br>0 <sub>B</sub> Use the integrated LDO to supply the RGMII/MDIO I/O pin.<br>1 <sub>B</sub> Use an external power source on VDDP for the RGMII/MDIO I/O pin.                                               |
| CFG_LDO(1:0)          | <b>Configuration of Integrated LDO voltage</b><br>This is the voltage level configuration for supplying the RGMII/MDIO I/O pin.<br>00 <sub>B</sub> Reserved<br>01 <sub>B</sub> <b>2.5 V</b><br>10 <sub>B</sub> <b>1.8 V</b><br>1x <sub>B</sub> <b>1.8 V</b> |

## 4 MDIO and MMD Register Interface Description

This chapter describes the MDIO and MMD registers, which are standardized by IEEE 802.3 [\[1\]](#), and available to support the MxL86110 feature set. After power-on, the MxL86110 resets the MDIO and MMD registers to default values that are sufficient to operate without specific programming.

All the register definitions, behaviors, and fields are strictly compliant with the IEEE 802.3 [\[1\]](#). There are PHY specific registers which are not referenced in IEEE 802.3, which are found in [Section 5.2](#). These allow custom functions related to the MxL86110.

### 4.1 Definitions

These acronyms are used in the IEEE 802.3 standard and commonly used in the Ethernet technical domain:

- **STA:** Station Management. A host connected to the MDIO interface. STAs are generally Media Access Controllers (MACs). The STA drives the MDIO bus as a clock master and the MxL86110 is MDIO slave.
- **Host:** Used as a synonym of STA in this document.
- **PHY:** Physical Layer. In the MxL86110 this encompasses Analog Signal Processing, Digital Signal Processing, and Physical Coding Sublayer (PCS). The PHY contains several sub-layers that are individually manageable entities known as MDIO manageable devices (MMDs).
- **MMD:** MDIO Manageable Device. The list of MMDs available in the MxL86110 is in [Section 4.3](#).
- **Device:** In the context of MDIO/MMD registers, a device is a register bank grouped by logical sub-layers of the PHY layer.
- **Clause:** Refers to a particular section of the IEEE 802.3 standard [\[1\]](#). In particular Clause 22 describes MDIO device 0, and Clause 45 describes the other MMDs.
- **MII:** Media Independent Interface. This encompasses the MDIO as well as the (G)MII as described in Clause 22. STD registers in device 0 are also called MII registers.

## 4.2 Register Naming and Numbering

The register numbering convention in this document is similar to that of IEEE 802.3:

The numbering syntax uses 3 numbers “a.b.c” as specified in IEEE 802.3 paragraph 45.1, and the notation is generalized to Clause 22 registers in device 0 “STD”. The alphanumeric syntax also uses the same structure and uses the names of the MMD devices, registers and register fields separated by underscore and dot as described below.

### 4.2.1 Register Numbering

The syntax is as follows, with a, b, c written as decimal numbers:

a.b.c = <DEVICE\_NUMBER>.<REGISTER\_NUMBER>.<FIELD\_NUMBER>

When the last indicator (c) is omitted, the register numbering refers to the full register.

When a field is more than a single bit, the bit range is indicated using a semicolon (e.g. 1:3 is the field of bits 1 to 3). In an MDIO register, the least significant bit is bit 0 and most significant bit is bit 15. All MDIO registers are 16 bit wide.

### 4.2.2 Register Naming

The syntax is as follows, with AA, BB, CC written as alphanumeric strings:

AA.BB.CC = <DEVICE\_NAME>\_<REGISTER\_NAME>.<FIELD\_NAME>

When the last indicator (CC) is omitted, the register naming refers to the full register.

The fields named RES refer to reserved fields as per IEEE 802.3 documents.

### 4.2.3 Examples

STD\_STAT.ANOK is the name of the field 0.1.5, which indicates auto-negotiation complete.

ANEG\_CTRL.ANEG\_RESTART is the name of the field 7.0.9, which allows the STA to restart the Ethernet ANEG procedure.

ANEG\_PHYID1 is the complete 16-bit register number 7.2, for the PHY identifier 1 number.

### 4.3 MMD Devices Present in MxL86110

[Table 14](#) lists the devices present in the MxL86110.

**Table 14 MMD Devices Present in MxL86110**

| MDIO / MMD Name | Device Number (decimal) | Description                                                           |
|-----------------|-------------------------|-----------------------------------------------------------------------|
| PCS             | 3                       | Control and status registers related to PCS encoding/decoding device. |
| ANEG            | 7                       | Control and status registers related to auto-negotiation device.      |

### 4.4 Responsibilities of the STA

The MMD devices implement groups of standardized registers under the management of the STA. They are defined in IEEE 802.3.

As per IEEE 802.3 guidelines, it is the responsibility of the STA entity to ensure that mutually acceptable speeds are applied consistently across all the MMDs of the MxL86110.

### 4.5 MDIO Access Protocols to Read / Write Registers

All the MDIO/MMD registers are accessible from an external chip connected to the MDIO bus on the MDIO and MDC pins. The MxL86110 supports several MDIO frame protocols:

- Clause 22: To access Device 0
- Clause 22 Extended: To access other devices (Dev 3: PCS, Dev 7: ANEG,) using the indirection scheme specified by IEEE 802.3.
- Clause 45: to access device as [Table 14](#).

Both Clause 22 Extended and Clause 45 are usable to access MMD devices. However, the mechanism implemented in the MxL86110 provides faster speeds using Clause 45, so there are some differences in latencies in the MDIO reply:

- Protocol "Clause 22 Extended" involves the MxL86110 an indirection mechanism.
- Protocol "Clause 45" provides faster replies.

The Clause 22 registers are accessible using the Clause 45 electrical interface and the Clause 22 management frame structure (IEEE 802.3 section 45.2).

## 5 MDIO Registers Detailed Description

**Table 15** MDIO Register Access Type

| Mode                                                                                             | Symbol |
|--------------------------------------------------------------------------------------------------|--------|
| Status Register (Status, or Ability Register)                                                    | RO     |
| Read-Write Register (e.g. MDIO Register)                                                         | RW     |
| Read-Write, Self-Clearing Register. The bit is cleared after being read from the MDIO interface. | RWSC   |

**Attention:** Since the MxL86110 is a 1000 Mbit/s product, the maximum speed capability available in the registers is 1000 Mbit/s. Any speed higher than 1000 Mbit/s, such as 2.5 Gbit/s, 5 Gbit/s, or 10 Gbit/s, defaults to 1000 Mbit/s.

## MDIO Registers Detailed Description

### 5.1 Standard Management Registers

This section describes the IEEE 802.3 standard management registers corresponding to Clause 22.

**Table 16 Registers Overview - Standard Management**

| Register Short Name         | Register Long Name                                                     | Reset Value                     |
|-----------------------------|------------------------------------------------------------------------|---------------------------------|
| <a href="#">STD_CTRL</a>    | STD Control (Register 0)                                               | 1140 <sub>H</sub>               |
| <a href="#">STD_STAT</a>    | Status Register (Register 1)                                           | 7949 <sub>H</sub>               |
| <a href="#">STD_PHYID1</a>  | PHY Identifier 1 (Register 2)                                          | C133 <sub>H</sub>               |
| <a href="#">STD_PHYID2</a>  | PHY Identifier 2 (Register 3)                                          | 5580 <sub>H</sub> <sup>1)</sup> |
| <a href="#">STD_AN_ADV</a>  | Auto-Negotiation Advertisement (Register 4)                            | 11E1 <sub>H</sub>               |
| <a href="#">STD_AN_LPA</a>  | Auto-Negotiation Link Partner Ability (Register 5)                     | 0000 <sub>H</sub>               |
| <a href="#">STD_AN_EXP</a>  | Auto-Negotiation Expansion (Register 6)                                | 0004 <sub>H</sub>               |
| <a href="#">STD_AN_NPTX</a> | Auto-Negotiation Next Page Transmit Register (Register 7)              | 2001 <sub>H</sub>               |
| <a href="#">STD_AN_NPRX</a> | Auto-Negotiation Link Partner Received Next Page Register (Register 8) | 0000 <sub>H</sub>               |
| <a href="#">STD_GCTRL</a>   | Gigabit Control Register (Register 9)                                  | 0200 <sub>H</sub>               |
| <a href="#">STD_GSTAT</a>   | Gigabit Status Register (Register 10)                                  | 0000 <sub>H</sub>               |
| <a href="#">STD_MMDCTRL</a> | MMD Access Control Register (Register 13)                              | 0000 <sub>H</sub>               |
| <a href="#">STD_MMDDATA</a> | MMD Access Data Register (Register 14)                                 | 0000 <sub>H</sub>               |
| <a href="#">STD_XSTAT</a>   | Extended Status Register (Register 15)                                 | 2000 <sub>H</sub>               |

1) For the device specific reset value, see [Table 37](#) in [Section 9.2](#).

## MDIO Registers Detailed Description

### 5.1.1 Standard Management Registers

This chapter describes all registers of STD in detail.

#### STD Control (Register 0)

This register controls the main functions of the PHY.

IEEE Standard Register=0

#### STD\_CTRL

Reset Value

#### STD Control (Register 0)

1140<sub>H</sub>

|      |    |     |      |    |      |      |      |     |     |   |  |  |  |     |   |
|------|----|-----|------|----|------|------|------|-----|-----|---|--|--|--|-----|---|
| 15   | 14 | 13  | 12   | 11 | 10   | 9    | 8    | 7   | 6   | 5 |  |  |  |     | 0 |
| RST  | LB | SSL | ANEN | PD | ISOL | ANRS | DPLX | COL | SSM |   |  |  |  | RES |   |
| RWSC | RW | RW  | RW   | RW | RW   | RWSC | RW   | RW  | RW  |   |  |  |  | RO  |   |

| Field | Bits | Type | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RST   | 15   | RWSC | <b>Reset</b><br>Resets the PHY to its default state. Active links are terminated. Note that this is a self-clearing bit which is set to zero by the hardware after reset has been done.<br>0 <sub>B</sub> <b>NORMAL</b> Normal operational mode<br>1 <sub>B</sub> <b>RESET</b> Resets the device                                                                                                                                                                   |
| LB    | 14   | RW   | <b>Loopback on GMII</b><br>This mode enables looping back of MII data from the transmit to the receive direction. No data is transmitted to the Ethernet PHY. The device operates at the selected speed. The collision signal remains de-asserted unless otherwise forced by the collision test.<br>0 <sub>B</sub> <b>NORMAL</b> Normal operational mode<br>1 <sub>B</sub> <b>ENABLE</b> Closes the loopback from Tx to Rx at xMII                                 |
| SSL   | 13   | RW   | <b>Forced Speed Selection LSB</b><br>This bit only takes effect with the auto-negotiation process is disabled (STD_CTRL.ANEN bit is set to 0 <sub>B</sub> ). This is the lower bit (LSB) of the forced speed selection. In conjunction with the higher bit (MSB), this encoding is valid:<br>MSB LSB bit values:<br>00 <sub>B</sub> <b>10 Mbit/s</b><br>01 <sub>B</sub> <b>100 Mbit/s</b><br>10 <sub>B</sub> <b>1000 Mbit/s</b><br>11 <sub>B</sub> <b>Reserved</b> |
| ANEN  | 12   | RW   | <b>Auto-Negotiation Enable</b><br>Allows enabling and disabling of the auto-negotiation process capability of the PHY. If enabled, the force bits for duplex mode (STD_CTRL.DPLX) and the speed selection (STD_CTRL.SSM, STD_CTRL.SSL) become inactive. Otherwise, the force bits define the PHY operation.<br>0 <sub>B</sub> <b>DISABLE</b> Disable the auto-negotiation protocol<br>1 <sub>B</sub> <b>ENABLE</b> Enable the auto-negotiation protocol            |

## MDIO Registers Detailed Description

| Field | Bits | Type | Description (continued)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PD    | 11   | RW   | <b>Power Down</b><br>Forces the device into a power down state (SLEEP) in which power consumption is the minimum required to still maintain the MII management interface communication. When activating the power down functionality, the PHY terminates active data links. The MII interface is also stopped in power down mode.<br>0 <sub>B</sub> <b>NORMAL</b> Normal operational mode<br>1 <sub>B</sub> <b>POWERDOWN</b> Forces the device into power down mode                                                                               |
| ISOL  | 10   | RW   | <b>Isolate</b><br>The isolation mode isolates the PHY from the MAC. MAC interface inputs are ignored, whereas MAC interface outputs are set to tristate (high-impedance).<br>0 <sub>B</sub> <b>NORMAL</b> Normal operational mode<br>1 <sub>B</sub> <b>ISOLATE</b> Isolates the PHY from the MAC                                                                                                                                                                                                                                                  |
| ANRS  | 9    | RWSC | <b>Restart Auto-Negotiation</b><br>Restarts the auto-negotiation process on the MDI. This bit does not take any effect when auto-negotiation is disabled using (STD_CTRL.ANEN). Note that this bit is self-clearing after the auto-negotiation process is initiated.<br>0 <sub>B</sub> <b>NORMAL</b> Stay in current mode<br>1 <sub>B</sub> <b>RESTART</b> Restart auto-negotiation                                                                                                                                                               |
| DPLX  | 8    | RW   | <b>Forced Duplex Mode</b><br>This bit controls forced duplex mode. It forces the PHY into full or half-duplex mode for 10BASE-T and 100BASE-T modes. This field is ignored for higher speeds.<br>Note(s): <ul style="list-style-type: none"> <li>This bit only takes effect when the auto-negotiation process (STD_CTRL.ANEN) is set to 0<sub>B</sub>.</li> <li>This bit does not take effect in loopback mode, when STD_CTRL.LB is set to 1<sub>B</sub>.</li> </ul> 0 <sub>B</sub> <b>HD</b> Half-duplex<br>1 <sub>B</sub> <b>FD</b> Full-duplex |
| COL   | 7    | RW   | <b>Collision Test</b><br>Allows testing of the COL signal at the xMII interface. When the collision test is enabled, the state of the TX_EN signal is looped back to the COL signal within a minimum latency.<br>0 <sub>B</sub> <b>DISABLE</b> Normal operational mode<br>1 <sub>B</sub> <b>ENABLE</b> Activates the collision test                                                                                                                                                                                                               |
| SSM   | 6    | RW   | <b>Forced Speed Selection MSB</b><br>This bit only takes effect when the auto-negotiation process is disabled, that is, bit ANEN is set to zero.<br>This is the most significant bit (MSB) of the forced speed selection. In conjunction with the lower bit, (LSB), the following encoding is valid: PHY mirrors 1.0.6, 1.0.13 and 0.0.6, 0.0.13<br>MSB LSB:<br>00 <sub>B</sub> <b>10 Mbit/s</b><br>01 <sub>B</sub> <b>100 Mbit/s</b><br>10 <sub>B</sub> <b>1000 Mbit/s</b><br>11 <sub>B</sub> <b>Reserved</b>                                    |

## MDIO Registers Detailed Description

| Field | Bits | Type | Description (continued)                           |
|-------|------|------|---------------------------------------------------|
| RES   | 5:0  | RO   | <b>Reserved</b><br>Write as zero, ignore on read. |

## MDIO Registers Detailed Description

### Status Register (Register 1)

This register contains status and capability information about the device. All bits are read-only. A write access by the MAC does not have any effect.

IEEE Standard Register=1

#### STD\_STAT

Reset Value

#### Status Register (Register 1)

7949<sub>H</sub>

| 15   | 14        | 13        | 12   | 11   | 10    | 9         | 8   | 7   | 6    | 5    | 4  | 3    | 2    | 1    | 0    |
|------|-----------|-----------|------|------|-------|-----------|-----|-----|------|------|----|------|------|------|------|
| CBT4 | CBTX<br>F | CBTX<br>H | XBTF | XBTH | CBT2F | CBT2<br>H | EXT | RES | MFPS | ANOK | RF | ANAB | LS   | JD   | XCAP |
| ro   | ro        | ro        | ro   | ro   | ro    | ro        | ro  | ro  | ro   | ro   | ro | ro   | roll | roll | ro   |

| Field | Bits | Type | Description                                                                                                                                                                                                  |
|-------|------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CBT4  | 15   | RO   | <b>IEEE 100BASE-T4</b><br>Specifies the 100BASE-T4 ability.<br>0 <sub>B</sub> <b>DISABLED</b> PHY does not support this mode<br>1 <sub>B</sub> <b>ENABLED</b> PHY supports this mode                         |
| CBTXF | 14   | RO   | <b>IEEE 100BASE-TX Full-Duplex</b><br>Specifies the 100BASE-TX full-duplex ability.<br>0 <sub>B</sub> <b>DISABLED</b> PHY does not support this mode<br>1 <sub>B</sub> <b>ENABLED</b> PHY supports this mode |
| CBTXH | 13   | RO   | <b>IEEE 100BASE-TX Half-Duplex</b><br>Specifies the 100BASE-TX half-duplex ability.<br>0 <sub>B</sub> <b>DISABLED</b> PHY does not support this mode<br>1 <sub>B</sub> <b>ENABLED</b> PHY supports this mode |
| XBTF  | 12   | RO   | <b>IEEE 10BASE-T Full-Duplex</b><br>Specifies the 10BASE-T full-duplex ability.<br>0 <sub>B</sub> <b>DISABLED</b> PHY does not support this mode<br>1 <sub>B</sub> <b>ENABLED</b> PHY supports this mode     |
| XBTH  | 11   | RO   | <b>IEEE 10BASE-T Half-Duplex</b><br>Specifies the 10BASE-T half-duplex ability.<br>0 <sub>B</sub> <b>DISABLED</b> PHY does not support this mode<br>1 <sub>B</sub> <b>ENABLED</b> PHY supports this mode     |
| CBT2F | 10   | RO   | <b>IEEE 100BASE-T2 Full-Duplex</b><br>Specifies the 100BASE-T2 full-duplex ability.<br>0 <sub>B</sub> <b>DISABLED</b> PHY does not support this mode<br>1 <sub>B</sub> <b>ENABLED</b> PHY supports this mode |
| CBT2H | 9    | RO   | <b>IEEE 100BASE-T2 Half-Duplex</b><br>Specifies the 100BASE-T2 half-duplex ability.<br>0 <sub>B</sub> <b>DISABLED</b> PHY does not support this mode<br>1 <sub>B</sub> <b>ENABLED</b> PHY supports this mode |

## MDIO Registers Detailed Description

| Field | Bits | Type | Description (continued)                                                                                                                                                                                                                                                                                               |
|-------|------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EXT   | 8    | RO   | <b>Extended Status</b><br>The extended status registers are used to specify 1000 Mbit/s speed capabilities in the STD_XSTAT register.<br>0 <sub>B</sub> <b>DISABLED</b> No extended status information available in register 15<br>1 <sub>B</sub> <b>ENABLED</b> Extended status information available in register 15 |
| RES   | 7    | RO   | <b>Reserved</b><br>Ignore when read.                                                                                                                                                                                                                                                                                  |
| MFPS  | 6    | RO   | <b>Management Preamble Suppression</b><br>Specifies the MF preamble suppression ability.<br>0 <sub>B</sub> <b>DISABLED</b> PHY requires management frames with preamble<br>1 <sub>B</sub> <b>ENABLED</b> PHY accepts management frames without preamble                                                               |
| ANOK  | 5    | RO   | <b>Auto-Negotiation Completed</b><br>Indicates whether the auto-negotiation process is completed or in progress.<br>0 <sub>B</sub> <b>RUNNING</b> Auto-Negotiation process is in progress<br>1 <sub>B</sub> <b>COMPLETED</b> Auto-Negotiation process is completed                                                    |
| RF    | 4    | ROLH | <b>Remote Fault</b><br>Indicates the detection of a remote fault event.<br>0 <sub>B</sub> <b>INACTIVE</b> No remote fault condition detected<br>1 <sub>B</sub> <b>ACTIVE</b> Remote fault condition detected                                                                                                          |
| ANAB  | 3    | RO   | <b>Auto-Negotiation Ability</b><br>Specifies the auto-negotiation ability.<br>0 <sub>B</sub> <b>DISABLED</b> PHY is not able to perform auto-negotiation<br>1 <sub>B</sub> <b>ENABLED</b> PHY is able to perform auto-negotiation                                                                                     |
| LS    | 2    | ROLL | <b>Link Status</b><br>Indicates the link status of the PHY to the link partner.<br>0 <sub>B</sub> <b>INACTIVE</b> The link is down. No communication with link partner possible.<br>1 <sub>B</sub> <b>ACTIVE</b> The link is up. Data communication with link partner is possible.                                    |
| JD    | 1    | ROLH | <b>Jabber Detect</b><br>Indicates that a jabber event has been detected.<br>0 <sub>B</sub> <b>NONE</b> No jabber condition detected<br>1 <sub>B</sub> <b>DETECTED</b> Jabber condition detected                                                                                                                       |
| XCAP  | 0    | RO   | <b>Extended Capability</b><br>Indicates the availability and support of extended capability registers.<br>0 <sub>B</sub> <b>DISABLED</b> Only base registers are supported<br>1 <sub>B</sub> <b>ENABLED</b> Extended capability registers are supported                                                               |

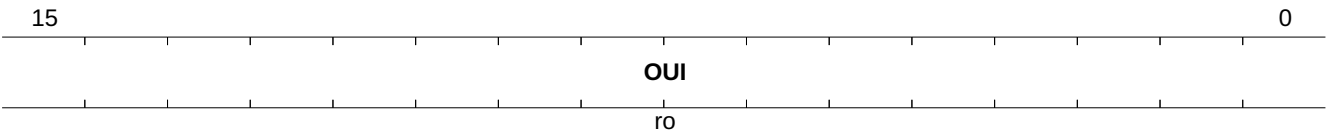
MDIO Registers Detailed Description

PHY Identifier 1 (Register 2)

This code specifies the Organizationally Unique Identifier (OUI), the vendor's model number, and the model's revision number.

IEEE Standard Register=2

|                               |                   |
|-------------------------------|-------------------|
| STD_PHYID1                    | Reset Value       |
| PHY Identifier 1 (Register 2) | C133 <sub>H</sub> |



| Field | Bits | Type | Description                                  |
|-------|------|------|----------------------------------------------|
| OUI   | 15:0 | RO   | Organizationally Unique Identifier Bits 3:18 |

## MDIO Registers Detailed Description

### PHY Identifier 2 (Register 3)

IEEE Standard Register=3

STD\_PHYID2

Reset Value

PHY Identifier 2 (Register 3)

5580<sub>H</sub>



| Field | Bits  | Type | Description                                                                                                                        |
|-------|-------|------|------------------------------------------------------------------------------------------------------------------------------------|
| OUI   | 15:10 | RO   | <b>Organizationally Unique Identifier Bits 19:24</b>                                                                               |
| LDN   | 9:4   | RO   | <b>Device Number</b><br>Specifies the device number <sup>1)</sup> to distinguish between several products.                         |
| LDRN  | 3:0   | RO   | <b>Device Number</b><br>Specifies the device revision number <sup>1)</sup> to distinguish between several versions of this device. |

1) For the device specific reset value, see [Table 37](#) in [Section 9.2](#).

## MDIO Registers Detailed Description

### Auto-Negotiation Advertisement (Register 4)

This register contains the advertised abilities of the PHY during auto-negotiation.

IEEE Standard Register=4

STD\_AN\_ADV

Reset Value

Auto-Negotiation Advertisement (Register 4)

11E1<sub>H</sub>

|    |     |    |     |    |  |  |  |  |  |     |   |  |  |  |    |
|----|-----|----|-----|----|--|--|--|--|--|-----|---|--|--|--|----|
| 15 | 14  | 13 | 12  | 11 |  |  |  |  |  | 5   | 4 |  |  |  | 0  |
| NP | RES | RF | XNP |    |  |  |  |  |  | TAF |   |  |  |  | SF |
| RW | RO  | RW | RW  |    |  |  |  |  |  | RW  |   |  |  |  | RW |

| Field | Bits | Type | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NP    | 15   | RW   | <b>Next Page</b><br>Next page indication is encoded in bit NP regardless of the selector field value or link code word encoding. The PHY always advertises NP if a 1000BASE-T mode is advertised during auto-negotiation.<br>0 <sub>B</sub> <b>INACTIVE</b> No next page(s) will follow<br>1 <sub>B</sub> <b>ACTIVE</b> Additional next page(s) will follow                                                                                                                                                                                                                                                                                                                                                                                          |
| RES   | 14   | RO   | <b>Reserved</b><br>Write as zero, ignore on read.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| RF    | 13   | RW   | <b>Remote Fault</b><br>The remote fault bit allows indication of a fault to the link partner.<br>0 <sub>B</sub> <b>NONE</b> No remote fault is indicated<br>1 <sub>B</sub> <b>FAULT</b> A remote fault is indicated                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| XNP   | 12   | RW   | <b>Extended Next Page</b><br>Indicates that the PHY supports transmission of extended next pages (XNP).<br>0 <sub>B</sub> <b>UNABLE</b> PHY is XNP unable<br>1 <sub>B</sub> <b>ABLE</b> PHY is XNP able                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| TAF   | 11:5 | RW   | <b>Technology Ability Field</b><br>The technology ability field is an 8-bit wide field containing information indicating supported technologies. This field indicates PHY support for 10BASE-T (half- and full-duplex), 100BASE-T (half- and full-duplex), and PAUSE (asymmetric and symmetric).<br>40 <sub>H</sub> <b>PS_ASYM</b> Advertise asymmetric pause<br>20 <sub>H</sub> <b>PS_SYM</b> Advertise symmetric pause<br>10 <sub>H</sub> <b>DBT4</b> Advertise 100BASE-T4<br>08 <sub>H</sub> <b>DBT_FDX</b> Advertise 100BASE-TX full-duplex<br>04 <sub>H</sub> <b>DBT_HDX</b> Advertise 100BASE-TX half-duplex<br>02 <sub>H</sub> <b>XBT_FDX</b> Advertise 10BASE-T full-duplex<br>01 <sub>H</sub> <b>XBT_HDX</b> Advertise 10BASE-T half-duplex |
| SF    | 4:0  | RW   | <b>Selector Field</b><br>The selector field is a 5-bit wide field for encoding 32 possible messages. Combinations not specified are reserved for future use. Reserved combinations of the selector field are not to be transmitted.<br>00001 <sub>B</sub> <b>IEEE802DOT3</b> Select the IEEE 802.3 technology                                                                                                                                                                                                                                                                                                                                                                                                                                        |

## MDIO Registers Detailed Description

### Auto-Negotiation Link Partner Ability (Register 5)

IEEE Standard Register=5

When the auto-negotiation is complete, this register contains the advertised ability of the link partner. The bit definitions are a direct representation of the received link code word.

STD\_AN\_LPA

Reset Value

Auto-Negotiation Link Partner Ability (Register 5)

0000<sub>H</sub>

|    |     |    |     |    |  |  |  |  |  |     |   |  |  |    |   |
|----|-----|----|-----|----|--|--|--|--|--|-----|---|--|--|----|---|
| 15 | 14  | 13 | 12  | 11 |  |  |  |  |  | 5   | 4 |  |  |    | 0 |
| NP | ACK | RF | XNP |    |  |  |  |  |  | TAF |   |  |  | SF |   |
| ro | ro  | ro | rw  |    |  |  |  |  |  | rw  |   |  |  | ro |   |

| Field | Bits | Type | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NP    | 15   | RO   | <b>Next Page</b><br>Next page request indication from the link partner.<br>0 <sub>B</sub> <b>INACTIVE</b> No next page(s) will follow<br>1 <sub>B</sub> <b>ACTIVE</b> Additional next pages will follow                                                                                                                                                                                                                                                                             |
| ACK   | 14   | RO   | <b>Acknowledge</b><br>Acknowledgment indication from the link partner's link code word.<br>0 <sub>B</sub> <b>INACTIVE</b> The device did not successfully receive its link partner's link code word<br>1 <sub>B</sub> <b>ACTIVE</b> The device has successfully received its link partner's link code word                                                                                                                                                                          |
| RF    | 13   | RO   | <b>Remote Fault</b><br>Remote fault indication from the link partner.<br>0 <sub>B</sub> <b>NONE</b> Remote fault is not indicated by the link partner<br>1 <sub>B</sub> <b>FAULT</b> Remote fault is indicated by the link partner                                                                                                                                                                                                                                                  |
| XNP   | 12   | RW   | <b>Extended Next Page</b><br>Indicates that PHY supports transmission of extended next pages (XNP).<br>0 <sub>B</sub> <b>UNABLE</b> Link partner is XNP unable<br>1 <sub>B</sub> <b>ABLE</b> Link partner is XNP able                                                                                                                                                                                                                                                               |
| TAF   | 11:5 | RW   | <b>Technology Ability Field</b><br>40 <sub>H</sub> <b>PS_ASYM</b> Advertise asymmetric pause<br>20 <sub>H</sub> <b>PS_SYM</b> Advertise symmetric pause<br>10 <sub>H</sub> <b>DBT4</b> Advertise 100BASE-T4<br>08 <sub>H</sub> <b>DBT_FDX</b> Advertise 100BASE-TX full-duplex<br>04 <sub>H</sub> <b>DBT_HDX</b> Advertise 100BASE-TX half-duplex<br>02 <sub>H</sub> <b>XBT_FDX</b> Advertise 10BASE-T full-duplex<br>01 <sub>H</sub> <b>XBT_HDX</b> Advertise 10BASE-T half-duplex |
| SF    | 4:0  | RO   | <b>Selector Field</b><br>00001 <sub>B</sub> <b>IEEE802DOT3</b> Select the IEEE 802.3 technology                                                                                                                                                                                                                                                                                                                                                                                     |

## MDIO Registers Detailed Description

### Auto-Negotiation Expansion (Register 6)

This is the auto-negotiation expansion register indicating the status of the link partner's auto-negotiation. This register is valid only after the auto-negotiation is completed.

IEEE Standard Register=6

## STD\_AN\_EXP

### Reset Value

### Auto-Negotiation Expansion (Register 6)

0004<sub>H</sub>[illegible]

| Field | Bits | Type | Description                                                                                                                                                                                                                  |
|-------|------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RES   | 15:5 | RO   | <b>Reserved</b><br>Write as zero, ignore on read.                                                                                                                                                                            |
| PDF   | 4    | ROLH | <b>Parallel Detection Fault</b><br>0 <sub>B</sub> <b>NONE</b> A fault has not been detected via the parallel detection function<br>1 <sub>B</sub> <b>FAULT</b> A fault has been detected via the parallel detection function |
| LPNPC | 3    | RO   | <b>Link Partner Next Page Capable</b><br>0 <sub>B</sub> <b>UNABLE</b> Link partner is unable to exchange next pages<br>1 <sub>B</sub> <b>CAPABLE</b> Link partner is capable of exchanging next pages                        |
| NPC   | 2    | RO   | <b>Next Page Capable</b><br>0 <sub>B</sub> <b>UNABLE</b> PHY is unable to exchange next pages<br>1 <sub>B</sub> <b>CAPABLE</b> PHY is capable of exchanging next pages                                                       |
| PR    | 1    | ROLH | <b>Page Received</b><br>0 <sub>B</sub> <b>NONE</b> A new page has not been received<br>1 <sub>B</sub> <b>RECEIVED</b> A new page has been received                                                                           |
| LPANC | 0    | RO   | <b>Link Partner Auto-Negotiation Capable</b><br>0 <sub>B</sub> <b>UNABLE</b> Link partner is unable to auto-negotiate<br>1 <sub>B</sub> <b>CAPABLE</b> Link partner is auto-negotiation capable                              |

## MDIO Registers Detailed Description

### Auto-Negotiation Next Page Transmit Register (Register 7)

The auto-negotiation next page transmit register contains the next page link code word to be transmitted when next page ability is supported.

IEEE Standard Register=7

**STD\_AN\_NPTX**

### Reset Value

### Auto-Negotiation Next Page Transmit Register (Register 7)

2001<sub>H</sub>

|    |     |    |      |      |     |  |  |  |  |  |  |  |  |  |  |   |
|----|-----|----|------|------|-----|--|--|--|--|--|--|--|--|--|--|---|
| 15 | 14  | 13 | 12   | 11   | 10  |  |  |  |  |  |  |  |  |  |  | 0 |
| NP | RES | MP | ACK2 | TOGG | MCF |  |  |  |  |  |  |  |  |  |  |   |
| rw | ro  | rw | rw   | ro   | rw  |  |  |  |  |  |  |  |  |  |  |   |

| Field | Bits | Type | Description                                                                                                                                                                                                                                                                                                                          |
|-------|------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NP    | 15   | RW   | <b>Next Page</b><br>0 <sub>B</sub> <b>INACTIVE</b> Last page<br>1 <sub>B</sub> <b>ACTIVE</b> Additional next page(s) will follow                                                                                                                                                                                                     |
| RES   | 14   | RO   | <b>Reserved</b><br>Write as zeros, ignore on read.                                                                                                                                                                                                                                                                                   |
| MP    | 13   | RW   | <b>Message Page</b><br>Indicates that the content of STD_AN_NPTX.MCF is either an unformatted page or a formatted message.<br>0 <sub>B</sub> <b>UNFOR</b> Unformatted page<br>1 <sub>B</sub> <b>MESSG</b> Message page                                                                                                               |
| ACK2  | 12   | RW   | <b>Acknowledge 2</b><br>0 <sub>B</sub> <b>INACTIVE</b> Device cannot comply with message<br>1 <sub>B</sub> <b>ACTIVE</b> Device will comply with message                                                                                                                                                                             |
| TOGG  | 11   | RO   | <b>Toggle</b><br>This bit always takes the opposite value of the STD_AN_NPTX.TOGG bit in the previously exchanged link code word.<br>0 <sub>B</sub> <b>ZERO</b> Previous value of the transmitted link code word was 1 <sub>B</sub><br>1 <sub>B</sub> <b>ONE</b> Previous value of the transmitted link code word was 0 <sub>B</sub> |

MDIO Registers Detailed Description

| Field | Bits | Type | Description (continued)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MCF   | 10:0 | RW   | <p><b>Message or Unformatted Code Field</b></p> <p>When Message Page STD_AN_NPTX.MP bit is set to 1<sub>B</sub> (0.7.13), this field is the Message Code Field of a message page used in next page exchange. The message codes are described in IEEE802.3 Appendix 28C.</p> <p>It is used to indicate the type of message in UCF1 and UCF2.</p> <p>00<sub>H</sub> Reserved</p> <p>01<sub>H</sub> Null message</p> <p>02<sub>H</sub> One Unformatted Page (UP) with TAF follows</p> <p>03<sub>H</sub> Two UPs with TAF follows</p> <p>04<sub>H</sub> Remote fault details message</p> <p>05<sub>H</sub> OUI message</p> <p>06<sub>H</sub> PHY ID message</p> <p>07<sub>H</sub> 100BASE-T2 message</p> <p>08<sub>H</sub> 1000BASE-T message</p> <p>09<sub>H</sub> MULTIGBASE-T message</p> <p>0A<sub>H</sub> EEE technology capability follows in next UP</p> <p>0B<sub>H</sub> OUI XNP</p> |

### Auto-Negotiation Link Partner Received Next Page Register (Register 8)

IEEE Standard Register=8

### Reset Value

0000<sub>H</sub>

|    |     |    |      |      |     |  |  |  |  |  |  |  |  |  |  |   |
|----|-----|----|------|------|-----|--|--|--|--|--|--|--|--|--|--|---|
| 15 | 14  | 13 | 12   | 11   | 10  |  |  |  |  |  |  |  |  |  |  | 0 |
| NP | ACK | MP | ACK2 | TOGG | MCF |  |  |  |  |  |  |  |  |  |  |   |
| ro | ro  | ro | ro   | ro   | rw  |  |  |  |  |  |  |  |  |  |  |   |

| Field | Bits | Type | Description                                                                                                                                                                                                                                                                                                           |
|-------|------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NP    | 15   | RO   | <b>Next Page</b><br>0 <sub>B</sub> <b>INACTIVE</b> No next pages to follow<br>1 <sub>B</sub> <b>ACTIVE</b> Additional next page(s) will follow                                                                                                                                                                        |
| ACK   | 14   | RO   | <b>Acknowledge</b><br>0 <sub>B</sub> <b>INACTIVE</b> The device did not successfully receive its link partner's link code word<br>1 <sub>B</sub> <b>ACTIVE</b> The device has successfully received its link partner's link code word                                                                                 |
| MP    | 13   | RO   | <b>Message Page</b><br>Indicates that the content of STD_AN_NPTX.MCF is either an unformatted page or a formatted message.<br>0 <sub>B</sub> <b>UNFOR</b> Unformatted page<br>1 <sub>B</sub> <b>MESSG</b> Message page                                                                                                |
| ACK2  | 12   | RO   | <b>Acknowledge 2</b><br>0 <sub>B</sub> <b>INACTIVE</b> Device cannot comply with message<br>1 <sub>B</sub> <b>ACTIVE</b> Device will comply with message                                                                                                                                                              |
| TOGG  | 11   | RO   | <b>Toggle</b><br>This bit always takes the opposite value of the TOGG bit in the previously exchanged link code word.<br>0 <sub>B</sub> <b>ZERO</b> Previous value of the transmitted link code word was equal to ONE<br>1 <sub>B</sub> <b>ONE</b> Previous value of the transmitted link code word was equal to ZERO |

MDIO Registers Detailed Description

| Field | Bits | Type | Description (continued)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MCF   | 10:0 | RW   | <p><b>Message or Unformatted Code Field</b></p> <p>This field is the Message Code Field of a message page used in next page exchange.</p> <p>The message codes are described in IEEE802.3 Appendix 28C.</p> <p>It is used to indicate the type of message in UCF1 and UCF2.</p> <p>00<sub>H</sub> Reserved</p> <p>01<sub>H</sub> Null message</p> <p>02<sub>H</sub> One Unformatted Page (UP) with TAF follows</p> <p>03<sub>H</sub> Two UPs with TAF follows</p> <p>04<sub>H</sub> Remote fault details message</p> <p>05<sub>H</sub> OUI message</p> <p>06<sub>H</sub> PHY ID message</p> <p>07<sub>H</sub> 100BASE-T2 message</p> <p>08<sub>H</sub> 1000BASE-T message</p> <p>09<sub>H</sub> MULTIGBASE-T message</p> <p>0A<sub>H</sub> EEE technology capability follows in next UP</p> <p>0B<sub>H</sub> OUI XNP</p> |

## MDIO Registers Detailed Description

### Gigabit Control Register (Register 9)

This is the control register used to configure the Gigabit Ethernet behavior of the PHY.

IEEE Standard Register=9

STD\_GCTRL

Reset Value

Gigabit Control Register (Register 9)

0200<sub>H</sub>

|    |    |      |    |      |           |           |     |  |  |  |  |  |  |  |  |   |
|----|----|------|----|------|-----------|-----------|-----|--|--|--|--|--|--|--|--|---|
| 15 | 13 | 12   | 11 | 10   | 9         | 8         | 7   |  |  |  |  |  |  |  |  | 0 |
| TM |    | MSEN | MS | MSPT | MBTF<br>D | MBTH<br>D | RES |  |  |  |  |  |  |  |  |   |
| rw |    | rw   | rw | rw   | rw        | rw        | ro  |  |  |  |  |  |  |  |  |   |

| Field | Bits  | Type | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|-------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TM    | 15:13 | RW   | <b>Transmitter Test Mode</b><br>This register field allows enabling of the standard transmitter test modes.<br>000 <sub>B</sub> <b>NOP</b> Normal operation<br>001 <sub>B</sub> <b>WAV</b> Test mode 1 transmit waveform test<br>010 <sub>B</sub> <b>JITM</b> Test mode 2 transmit jitter test in master mode<br>011 <sub>B</sub> <b>JITS</b> Test mode 3 transmit jitter test in slave mode<br>100 <sub>B</sub> <b>DIST</b> Test mode 4 transmitter distortion test |
| MSEN  | 12    | RW   | <b>Master/Slave Manual Configuration Enable</b><br>0 <sub>B</sub> <b>DISABLED</b> Disable master/slave manual configuration value<br>1 <sub>B</sub> <b>ENABLED</b> Enable master/slave manual configuration value                                                                                                                                                                                                                                                    |
| MS    | 11    | RW   | <b>Master/Slave Config Value</b><br>Allows forcing of master or slave mode manually when STD_GCTRL.MSEN is set to logical one.<br>0 <sub>B</sub> <b>SLAVE</b> Configure PHY as slave during master/slave negotiation<br>1 <sub>B</sub> <b>MASTER</b> Configure PHY as master during master/slave negotiation                                                                                                                                                         |
| MSPT  | 10    | RW   | <b>Master/Slave Port Type</b><br>Defines whether the PHY advertises itself as a multi- or single-port device, which in turn impacts the master/slave resolution function.<br>0 <sub>B</sub> <b>SPD</b> Single-port device<br>1 <sub>B</sub> <b>MPD</b> Multi-port device                                                                                                                                                                                             |
| MBTFD | 9     | RW   | <b>1000BASE-T Full-Duplex</b><br>Advertises the 1000BASE-T full-duplex capability; always forced to 1 <sub>B</sub> in converter mode.<br>0 <sub>B</sub> <b>DISABLED</b> Advertise PHY as not 1000BASE-T full-duplex capable<br>1 <sub>B</sub> <b>ENABLED</b> Advertise PHY as 1000BASE-T full-duplex capable                                                                                                                                                         |
| MBTHD | 8     | RW   | <b>1000BASE-T Half-Duplex</b><br>Always advertises the 1000BASE-T half-duplex capability as disabled; PHY does not support 1000BASE-T Half-Duplex capability<br>0 <sub>B</sub> <b>DISABLED</b> Advertise PHY as not 1000BASE-T half-duplex capable<br>1 <sub>B</sub> <b>ENABLED</b> Advertise PHY as 1000BASE-T half-duplex capable                                                                                                                                  |

## MDIO Registers Detailed Description

| Field | Bits | Type | Description (continued)                           |
|-------|------|------|---------------------------------------------------|
| RES   | 7:0  | RO   | <b>Reserved</b><br>Write as zero, ignore on read. |

## MDIO Registers Detailed Description

### Gigabit Status Register (Register 10)

This is the status register used to reflect the Gigabit Ethernet status of the PHY.

IEEE Standard Register=10

#### STD\_GSTAT

Reset Value

### Gigabit Status Register (Register 10)

0000<sub>H</sub>

|             |           |             |             |           |           |     |   |   |  |  |  |  |  |  |  |      |   |
|-------------|-----------|-------------|-------------|-----------|-----------|-----|---|---|--|--|--|--|--|--|--|------|---|
| 15          | 14        | 13          | 12          | 11        | 10        | 9   | 8 | 7 |  |  |  |  |  |  |  |      | 0 |
| MSFA<br>ULT | MSRE<br>S | LRXS<br>TAT | RRXS<br>TAT | MBTF<br>D | MBTH<br>D | RES |   |   |  |  |  |  |  |  |  | IEC  |   |
| RWSC        | ro        | ro          | ro          | ro        | ro        | ro  |   |   |  |  |  |  |  |  |  | RWSC |   |

| Field   | Bits | Type | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|---------|------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MSFAULT | 15   | RWSC | <b>Master/Slave Manual Configuration Fault</b><br>This bit is set if the number of attempts to set the master/slave configuration reaches 7.<br>It is cleared upon each read of the STD_GSTAT register.<br>This bit self clears on auto-negotiation enable or auto-negotiation complete.<br>0 <sub>B</sub> <b>OK</b> Master/slave manual configuration resolved successfully<br>1 <sub>B</sub> <b>NOK</b> Master/slave manual configuration resolved with a fault |
| MSRES   | 14   | RO   | <b>Master/Slave Configuration Resolution</b><br>0 <sub>B</sub> <b>SLAVE</b> Local PHY configuration resolved to slave<br>1 <sub>B</sub> <b>MASTER</b> Local PHY configuration resolved to master                                                                                                                                                                                                                                                                  |
| LRXSTAT | 13   | RO   | <b>Local Receiver Status</b><br>Indicates the status of the local receiver.<br>0 <sub>B</sub> <b>NOK</b> Local receiver not OK<br>1 <sub>B</sub> <b>OK</b> Local receiver OK                                                                                                                                                                                                                                                                                      |
| RRXSTAT | 12   | RO   | <b>Remote Receiver Status</b><br>Indicates the status of the remote receiver.<br>0 <sub>B</sub> <b>NOK</b> Remote receiver not OK<br>1 <sub>B</sub> <b>OK</b> Remote receiver OK                                                                                                                                                                                                                                                                                  |
| MBTFD   | 11   | RO   | <b>Link Partner Capable of Operating 1000BASE-T Full-Duplex</b><br>0 <sub>B</sub> <b>DISABLED</b> Link partner is not capable of operating 1000BASE-T full-duplex<br>1 <sub>B</sub> <b>ENABLED</b> Link partner is capable of operating 1000BASE-T full-duplex                                                                                                                                                                                                    |
| MBTHD   | 10   | RO   | <b>Link Partner Capable of Operating 1000BASE-T Half-Duplex</b><br>0 <sub>B</sub> <b>DISABLED</b> Link partner is not capable of operating 1000BASE-T half-duplex<br>1 <sub>B</sub> <b>ENABLED</b> Link partner is capable of operating 1000BASE-T half-duplex                                                                                                                                                                                                    |
| RES     | 9:8  | RO   | <b>Reserved</b><br>Write as zero, ignore on read.                                                                                                                                                                                                                                                                                                                                                                                                                 |

## MDIO Registers Detailed Description

| Field | Bits | Type | Description (continued)                                                                                                                                        |
|-------|------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IEC   | 7:0  | RWSC | <b>Idle Error Count</b><br>Indicates the idle error count. This field contains a cumulative count of the errors detected when the receiver is receiving idles. |

## MDIO Registers Detailed Description

### MMD Access Control Register (Register 13)

The MMD access control register is used in conjunction with the MMDDATA register to access the MMD register space. This uses address directing as specified in IEEE802.3 Clause 22 Extended.

IEEE Standard Register=13

STD\_MMDCTRL

Reset Value

MMD Access Control Register (Register 13)

0000<sub>H</sub>

|        |    |     |  |  |  |  |  |  |  |       |   |  |  |  |   |
|--------|----|-----|--|--|--|--|--|--|--|-------|---|--|--|--|---|
| 15     | 14 | 13  |  |  |  |  |  |  |  | 5     | 4 |  |  |  | 0 |
| ACTYPE |    | RES |  |  |  |  |  |  |  | DEVAD |   |  |  |  |   |
| rw     |    | ro  |  |  |  |  |  |  |  | rw    |   |  |  |  |   |

| Field  | Bits  | Type | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|--------|-------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ACTYPE | 15:14 | RW   | <b>Access Type Function</b><br>If the access of the MMDDATA register is an address access (ACTYPE = 00 <sub>B</sub> ) then it is directed to the address register within the MMD associated with the value in the DEVAD field. Otherwise, both the DEVAD field and the MMD's address register direct the register MMDDATA data accesses to the appropriate registers within that MMD.<br>00 <sub>B</sub> <b>ADDRESS</b> Accesses to register MMDDATA access the MMD individual address register<br>01 <sub>B</sub> <b>DATA</b> Accesses to register MMDDATA access the register within the MMD selected<br>10 <sub>B</sub> <b>DATA_PI</b> Accesses to register MMDDATA access the register within the MMD selected<br>11 <sub>B</sub> <b>DATA_PIWR</b> Accesses to register MMDDATA access the register within the MMD selected |
| RES    | 13:8  | RO   | <b>Reserved</b><br>Write as zero, ignored on read.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| RES    | 7:5   | RO   | <b>Reserved</b><br>Write as zero, ignored on read.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| DEVAD  | 4:0   | RW   | <b>Device Address</b><br>The field directs any accesses of register MMDDATA to the appropriate MMD.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

## MDIO Registers Detailed Description

### MMD Access Data Register (Register 14)

The MMD access data register is used in conjunction with the MMD access control (MMDCTRL) register to access the MMD register space.

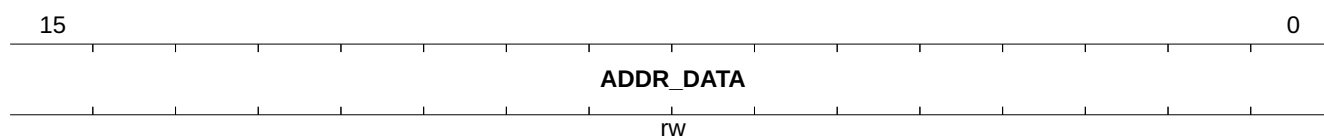
IEEE Standard Register=14

STD\_MMDDATA

Reset Value

MMD Access Data Register (Register 14)

0000<sub>H</sub>



| Field     | Bits | Type | Description                                                                                                                                                                                                                                                   |
|-----------|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ADDR_DATA | 15:0 | RW   | <b>Address or Data Register</b><br>This register accesses either a specific MMD address register or the data content of the MMD register to which this address register points. Which of the functions is currently valid is defined by the MMDCTRL register. |

## MDIO Registers Detailed Description

### Extended Status Register (Register 15)

This register contains extended status and capability information about the PHY. All bits are read-only. A write access does not have any effect.

IEEE Standard Register=15

STD\_XSTAT

Reset Value

Extended Status Register (Register 15)

2000<sub>H</sub>

|             |             |             |             |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |
|-------------|-------------|-------------|-------------|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|
| 15          | 14          | 13          | 12          | 11 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0          |
| <b>MBXF</b> | <b>MBXH</b> | <b>MBTF</b> | <b>MBTH</b> |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  | <b>RES</b> |
| ro          | ro          | ro          | ro          |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  | ro         |

| Field | Bits | Type | Description                                                                                                                                                                                                                                    |
|-------|------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MBXF  | 15   | RO   | <b>1000BASE-X Full-Duplex Capability</b><br>Specifies whether the PHY is capable of operating 1000BASE-X full-duplex.<br>0 <sub>B</sub> <b>DISABLED</b> PHY does not support this mode<br>1 <sub>B</sub> <b>ENABLED</b> PHY supports this mode |
| MBXH  | 14   | RO   | <b>1000BASE-X Half-Duplex Capability</b><br>Specifies whether the PHY is capable of operating 1000BASE-X half-duplex.<br>0 <sub>B</sub> <b>DISABLED</b> PHY does not support this mode<br>1 <sub>B</sub> <b>ENABLED</b> PHY supports this mode |
| MBTF  | 13   | RO   | <b>1000BASE-T Full-Duplex Capability</b><br>Specifies whether the PHY is capable of operating 1000BASE-T full-duplex.<br>0 <sub>B</sub> <b>DISABLED</b> PHY does not support this mode<br>1 <sub>B</sub> <b>ENABLED</b> PHY supports this mode |
| MBTH  | 12   | RO   | <b>1000BASE-T Half-Duplex Capability</b><br>PHY does not support 1000BASE-T Half-Duplex capability.<br>0 <sub>B</sub> <b>DISABLED</b> PHY does not support this mode<br>1 <sub>B</sub> <b>ENABLED</b> PHY supports this mode                   |
| RES   | 11:8 | RO   | <b>Reserved</b><br>Ignore when read.                                                                                                                                                                                                           |
| RES   | 7:0  | RO   | <b>Reserved</b><br>Ignore when read.                                                                                                                                                                                                           |

## 5.2 PHY-specific Management Registers

This section describes the PHY specific management registers.

**Table 17 Registers Overview - PHY-specific Management Registers**

| Register Short Name          | Register Long Name                                        | Reset Value       |
|------------------------------|-----------------------------------------------------------|-------------------|
| <a href="#">PHY_CTL</a>      | PHY Specific Function Control Register (Register 16)      | 0062 <sub>H</sub> |
| <a href="#">PHY_STAT</a>     | PHY Specific Status Register (Register 17)                | 0000 <sub>H</sub> |
| <a href="#">PHY_IMASK</a>    | Interrupt Mask Register (Register 18)                     | 0000 <sub>H</sub> |
| <a href="#">PHY_ISTAT</a>    | Interrupt Status Register (Register 19)                   | 0000 <sub>H</sub> |
| <a href="#">PHY_ADS_CTL</a>  | Speed Auto Downgrade Control Register (Register 20)       | 082C <sub>H</sub> |
| <a href="#">PHY_EXT_ADR</a>  | Extended Register's Address Offset Register (Register 30) | 0000 <sub>H</sub> |
| <a href="#">PHY_EXT_DATA</a> | Extended Register's Data Register (Register 31)           | 1C8D <sub>H</sub> |

## MDIO Registers Detailed Description

### 5.2.1 PHY Specific Function Control Register (Register 16)

This section describes the PHY Specific Function Control Register in detail.

#### PHY Specific Function Control Register (Register 16)

The register controls PHY specific functions.

| PHY_CTL                                              | Offset            | Reset Value       |
|------------------------------------------------------|-------------------|-------------------|
| PHY Specific Function Control Register (Register 16) | 0010 <sub>H</sub> | 0062 <sub>H</sub> |

| 15  |  |  |  |  |  |  | 7 | 6    | 5 | 4   | 3   | 2   | 1   | 0   |
|-----|--|--|--|--|--|--|---|------|---|-----|-----|-----|-----|-----|
| RES |  |  |  |  |  |  |   | MDIX |   | RES | CRS | SQE | POL | JAB |
| ro  |  |  |  |  |  |  |   | rw   |   | rw  | rw  | rw  | rw  | rw  |

| Field | Bits | Type | Description                                                                                                                                                                                                                                                                                                                                                                     |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RES   | 15:7 | RO   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                 |
| MDIX  | 6:5  | RW   | <b>MDI Crossover</b><br>Changes made to these bits disrupt normal operation, thus a software reset is mandatory after the change. The configuration does not take effect until software reset.<br>00 <sub>B</sub> Manual MDI configuration<br>01 <sub>B</sub> Manual MDIX configuration<br>10 <sub>B</sub> Reserved<br>11 <sub>B</sub> Enable automatic crossover for all modes |
| RES   | 4    | RW   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                 |
| CRS   | 3    | RW   | <b>Carrier Sense on Transmitting</b><br>This bit is effective in 10BASE-Te half-duplex mode and 100BASE-TX mode:<br>0 <sub>B</sub> Never assert Carrier Sense (CRS) on transmitting, only assert it on receiving<br>1 <sub>B</sub> Assert CRS on transmitting or receiving                                                                                                      |
| SQE   | 2    | RW   | <b>Enable SQE Testing</b><br>Note: The Signal Quality Errors (SQE) test is automatically disabled in full-duplex mode regardless the setting in this bit.<br>0 <sub>B</sub> SQE test disabled<br>1 <sub>B</sub> SQE test enabled                                                                                                                                                |
| POL   | 1    | RW   | <b>Enable Polarity Reversal</b><br>If polarity reversal is disabled, the polarity is forced to be normal in 10BASE-Te.<br>0 <sub>B</sub> Polarity reversal disabled<br>1 <sub>B</sub> Polarity reversal enabled                                                                                                                                                                 |
| JAB   | 0    | RW   | <b>Disable Jabber</b><br>Jabber takes effect only in 10BASE-Te half-duplex mode.<br>0 <sub>B</sub> Enable the jabber function<br>1 <sub>B</sub> Disable the jabber function                                                                                                                                                                                                     |

## MDIO Registers Detailed Description

### 5.2.2 PHY Specific Status Register (Register 17)

This section describes the PHY Specific Status register in detail.

#### PHY Specific Status Register (Register 17)

The register reports PHY link, MDI crossover, polarity, ADS, and PAUSE status.

| PHY_STAT                                   | Offset            | Reset Value       |
|--------------------------------------------|-------------------|-------------------|
| PHY Specific Status Register (Register 17) | 0011 <sub>H</sub> | 0000 <sub>H</sub> |

| 15    | 14  | 13   | 12  | 11   | 10  | 9 | 7 | 6     | 5   | 4   | 3   | 2   | 1         | 0         |
|-------|-----|------|-----|------|-----|---|---|-------|-----|-----|-----|-----|-----------|-----------|
| SPEED | DPX | PAGE | SDR | LSRT | RES |   |   | MDIXS | ADS | RES | TPS | RPS | POLR<br>T | JABR<br>T |
| ro    | ro  | ro   | ro  | ro   | ro  |   |   | ro    | ro  | ro  | ro  | ro  | ro        | ro        |

| Field | Bits  | Type | Description                                                                                                                                                                                                                                                                                                                                             |
|-------|-------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SPEED | 15:14 | RO   | <b>Speed Mode</b><br>This register contains the speed mode status. These status bits are only valid when PHY_STAT.SDR is 1 <sub>B</sub> . PHY_STAT.SDR is set when auto-negotiation is completed or auto-negotiation is disabled.<br>00 <sub>B</sub> 10 Mbit/s<br>01 <sub>B</sub> 100 Mbit/s<br>10 <sub>B</sub> 1000 Mbit/s<br>11 <sub>B</sub> Reserved |
| DPX   | 13    | RO   | <b>Duplex</b><br>This register contains the duplex mode status. These status bits are only valid when PHY_STAT.SDR is 1 <sub>B</sub> . PHY_STAT.SDR is set when auto-negotiation is completed or auto-negotiation is disabled.<br>0 <sub>B</sub> Half-duplex<br>1 <sub>B</sub> Full-duplex                                                              |
| PAGE  | 12    | RO   | <b>Page Received Real-Time</b><br>0 <sub>B</sub> Page not received<br>1 <sub>B</sub> Page received                                                                                                                                                                                                                                                      |
| SDR   | 11    | RO   | <b>Speed and Duplex Resolved</b><br>This field contains the status of whether the speed and duplex has been resolved. This bit is set when auto-negotiation is completed or disabled. When auto-negotiation is disabled (force-speed mode), this bit is set to 1 <sub>B</sub> .<br>0 <sub>B</sub> Not resolved<br>1 <sub>B</sub> Resolved               |
| LSRT  | 10    | RO   | <b>Link Status Real-Time</b><br>0 <sub>B</sub> Link down<br>1 <sub>B</sub> Link up                                                                                                                                                                                                                                                                      |
| RES   | 9:7   | RO   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                         |

## MDIO Registers Detailed Description

| Field | Bits | Type | Description (continued)                                                                                                                                                                                                                                                                                                                       |
|-------|------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MDIXS | 6    | RO   | <b>MDI Crossover Status</b><br>This field contains the MDI Crossover status. This bit value depends upon the PHY_CTL.MDIX configuration.<br>This status bit is only valid when PHY_STAT.SPEED is 1 <sub>B</sub> .<br>0 <sub>B</sub> MDI<br>1 <sub>B</sub> MDIX                                                                                |
| ADS   | 5    | RO   | <b>Wirespeed Downgrade</b><br>0 <sub>B</sub> No Downgrade<br>1 <sub>B</sub> Downgrade                                                                                                                                                                                                                                                         |
| RES   | 4    | RO   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                               |
| TPS   | 3    | RO   | <b>Transmit Pause</b><br>This field contains the MAC pause resolution status. This bit is for information purposes only.<br>When in forced mode, this bit is set to 0 <sub>B</sub> . This status bit is only valid when PHY_STAT.SPEED is 1 <sub>B</sub> .<br>0 <sub>B</sub> Transmit pause disabled<br>1 <sub>B</sub> Transmit pause enabled |
| RPS   | 2    | RO   | <b>Receive Pause</b><br>This field contains the MAC pause resolution status. This bit is for information purposes only.<br>When in forced mode, this bit is set to 0 <sub>B</sub> . This status bit is only valid when PHY_STAT.SPEED is 1 <sub>B</sub> .<br>0 <sub>B</sub> Receive pause disabled<br>1 <sub>B</sub> Receive pause enabled    |
| POLRT | 1    | RO   | <b>Polarity Real Time</b><br>0 <sub>B</sub> Normal polarity<br>1 <sub>B</sub> Reverted polarity                                                                                                                                                                                                                                               |
| JABRT | 0    | RO   | <b>Jabber Real Time</b><br>0 <sub>B</sub> No jabber<br>1 <sub>B</sub> Jabber                                                                                                                                                                                                                                                                  |

## MDIO Registers Detailed Description

### 5.2.3 Interrupt Mask Register (Register 18)

This section describes the Interrupt Mask Register in detail.

#### Interrupt Mask Register (Register 18)

This register defines the mask for the Interrupt Status Register, which contains the event source for INT\_N sent from the PHY to an external device.

| PHY_IMASK                             |      |      |      |      |      | Offset            |   | Reset Value       |      |     |   |       |     |
|---------------------------------------|------|------|------|------|------|-------------------|---|-------------------|------|-----|---|-------|-----|
| Interrupt Mask Register (Register 18) |      |      |      |      |      | 0012 <sub>H</sub> |   | 0000 <sub>H</sub> |      |     |   |       |     |
| 15                                    | 14   | 13   | 12   | 11   | 10   | 9                 | 7 | 6                 | 5    | 4   | 2 | 1     | 0   |
| ANE                                   | LSPC | DXMC | NPRX | LFST | LSTC | RES               |   | WOL               | ADSC | RES |   | MDIPC | JAB |
| RW                                    | RW   | RW   | RW   | RW   | RW   | RW                |   | RW                | RW   | RW  |   | RW    | RW  |

| Field | Bits | Type | Description                                                                                                         |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------|
| ANE   | 15   | RW   | <b>Auto-Negotiation Error INT Mask</b><br>0 <sub>B</sub> Interrupt disable<br>1 <sub>B</sub> Interrupt enable       |
| LSPC  | 14   | RW   | <b>Speed Changed INT Mask</b><br>0 <sub>B</sub> Interrupt disable<br>1 <sub>B</sub> Interrupt enable                |
| DXMC  | 13   | RW   | <b>Duplex Changed INT Mask</b><br>0 <sub>B</sub> Interrupt disable<br>1 <sub>B</sub> Interrupt enable               |
| NPRX  | 12   | RW   | <b>Page Received INT Mask</b><br>0 <sub>B</sub> Interrupt disable<br>1 <sub>B</sub> Interrupt enable                |
| LFST  | 11   | RW   | <b>Link Failed INT Mask</b><br>0 <sub>B</sub> Interrupt disable<br>1 <sub>B</sub> Interrupt enable                  |
| LSTC  | 10   | RW   | <b>Link Succeed INT Mask</b><br>0 <sub>B</sub> Interrupt disable<br>1 <sub>B</sub> Interrupt enable                 |
| RES   | 9:7  | RW   | <b>Reserved</b><br>Not used.                                                                                        |
| WOL   | 6    | RW   | <b>WOL INT Mask</b><br>0 <sub>B</sub> Interrupt disable<br>1 <sub>B</sub> Interrupt enable                          |
| ADSC  | 5    | RW   | <b>Link Speed Auto-Downspeed Detect Mask</b><br>0 <sub>B</sub> Interrupt disable<br>1 <sub>B</sub> Interrupt enable |
| RES   | 4    | RW   | <b>Reserved</b><br>Not used.                                                                                        |
| RES   | 3    | RW   | <b>Reserved</b>                                                                                                     |

MDIO Registers Detailed Description

| Field | Bits | Type | Description (continued)                                                                                 |
|-------|------|------|---------------------------------------------------------------------------------------------------------|
| RES   | 2    | RW   | <b>Reserved</b>                                                                                         |
| MDIPC | 1    | RW   | <b>Polarity Changed INT Mask</b><br>0 <sub>B</sub> Interrupt disable<br>1 <sub>B</sub> Interrupt enable |
| JAB   | 0    | RW   | <b>Jabber Occurred INT Mask</b><br>0 <sub>B</sub> Interrupt disable<br>1 <sub>B</sub> Interrupt enable  |

## MDIO Registers Detailed Description

### 5.2.4 Interrupt Status Register (Register 19)

This section describes the Interrupt Status Register in detail.

#### Interrupt Status Register (Register 19)

This register defines the event source for the MDINT interrupt sent from the PHY to an external device. The register is a cleared on read by the STA.

| PHY_ISTAT                               |       |       |       |       |       | Offset            |   | Reset Value       |       |       |   |       |       |
|-----------------------------------------|-------|-------|-------|-------|-------|-------------------|---|-------------------|-------|-------|---|-------|-------|
| Interrupt Status Register (Register 19) |       |       |       |       |       | 0013 <sub>H</sub> |   | 0000 <sub>H</sub> |       |       |   |       |       |
| 15                                      | 14    | 13    | 12    | 11    | 10    | 9                 | 7 | 6                 | 5     | 4     | 2 | 1     | 0     |
| ANE                                     | LSPC  | DXMC  | NPRX  | LFST  | LSTC  | RES               |   | WOL               | ADSC  | RES   |   | MDIPC | JAB   |
| ro rc                                   | ro rc | ro rc | ro rc | ro rc | ro rc | ro rc             |   | ro rc             | ro rc | ro rc |   | ro rc | ro rc |

| Field | Bits | Type  | Description                                                                                                                                                                                          |
|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ANE   | 15   | RO RC | <b>Auto-Negotiation Error INT</b><br>This field indicates errors occurring during ANEG.<br>0 <sub>B</sub> No auto-negotiation error takes place<br>1 <sub>B</sub> Auto-Negotiation error takes place |
| LSPC  | 14   | RO RC | <b>Speed Changed INT</b><br>0 <sub>B</sub> Speed not changed<br>1 <sub>B</sub> Speed changed                                                                                                         |
| DXMC  | 13   | RO RC | <b>Duplex Changed INT</b><br>0 <sub>B</sub> Duplex not changed<br>1 <sub>B</sub> Duplex changed                                                                                                      |
| NPRX  | 12   | RO RC | <b>Page Received INT</b><br>0 <sub>B</sub> Page not received<br>1 <sub>B</sub> Page received                                                                                                         |
| LFST  | 11   | RO RC | <b>Link Failed INT</b><br>0 <sub>B</sub> No link down takes place<br>1 <sub>B</sub> PHY link down takes place                                                                                        |
| LSTC  | 10   | RO RC | <b>Link Succeed INT</b><br>0 <sub>B</sub> No link up takes place<br>1 <sub>B</sub> PHY link up takes place                                                                                           |
| RES   | 9    | RO RC | <b>Reserved</b>                                                                                                                                                                                      |
| RES   | 8    | RO RC | <b>Reserved</b>                                                                                                                                                                                      |
| RES   | 7    | RO RC | <b>Reserved</b>                                                                                                                                                                                      |
| WOL   | 6    | RO RC | <b>WOL INT</b><br>0 <sub>B</sub> PHY did not receive WOL magic frame<br>1 <sub>B</sub> PHY received WOL magic frame.                                                                                 |
| ADSC  | 5    | RO RC | <b>Link Speed Auto-Downspeed Detect Interrupt Status</b><br>0 <sub>B</sub> Speed did not downgrade<br>1 <sub>B</sub> Speed downgraded                                                                |
| RES   | 4    | RO RC | <b>Reserved</b>                                                                                                                                                                                      |

MDIO Registers Detailed Description

| Field | Bits | Type  | Description (continued)                                                                                                                            |
|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| RES   | 3    | RO RC | <b>Reserved</b>                                                                                                                                    |
| RES   | 2    | RO RC | <b>Reserved</b>                                                                                                                                    |
| MDIPC | 1    | RO RC | <b>Polarity Changed INT</b><br>0 <sub>B</sub> PHY did not revert MDI polarity<br>1 <sub>B</sub> PHY reversed MDI polarity                          |
| JAB   | 0    | RO RC | <b>Jabber Occurred INT</b><br>Refer to STD_STAT.JD.<br>0 <sub>B</sub> 10BaseT Tx jabber did not occur<br>1 <sub>B</sub> 10BaseT Tx jabber occurred |

## MDIO Registers Detailed Description

### 5.2.5 Speed Auto Downgrade Control Register (Register 20)

This section describes the Speed Auto Downgrade Control Register in detail.

#### Speed Auto Downgrade Control Register (Register 20)

The register is used for speed downshift control.

| PHY_ADS_CTL                                         | Offset            | Reset Value       |
|-----------------------------------------------------|-------------------|-------------------|
| Speed Auto Downgrade Control Register (Register 20) | 0014 <sub>H</sub> | 082C <sub>H</sub> |

| 15   | 12 | 11   | 10   | 9    | 5 | 4     | 2 | 1   | 0    |
|------|----|------|------|------|---|-------|---|-----|------|
| RES0 |    | RES1 | RES2 | RES3 |   | ADSRT |   | BAT | RES4 |
| ro   |    | ro   | rwsc | rw   |   | rw    |   | rw  | ro   |

| Field | Bits  | Type | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|-------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RES0  | 15:12 | RO   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| RES1  | 11    | RO   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| RES2  | 10    | RWSC | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| RES3  | 9:5   | RW   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| ADSRT | 4:2   | RW   | <b>Autoneg Retry Limit Pre-downgrade</b><br>This field sets the number of link-up attempts before performing an Automatic-Downspeed (ADS) of the link. For example, with a 000 <sub>B</sub> setting, the PHY makes two attempts to link-up before trying a lower speed. (N+2).<br>000 <sub>B</sub> ADS after 2 consecutive link-up failures.<br>001 <sub>B</sub> ADS after 3 consecutive link-up failures.<br>010 <sub>B</sub> ADS after 4 consecutive link-up failures.<br>011 <sub>B</sub> ADS after 5 consecutive link-up failures.<br>100 <sub>B</sub> ADS after 6 consecutive link-up failures.<br>101 <sub>B</sub> ADS after 7 consecutive link-up failures.<br>110 <sub>B</sub> ADS after 8 consecutive link-up failures.<br>111 <sub>B</sub> ADS after 9 consecutive link-up failures. |
| BAT   | 1     | RW   | <b>Bypass Autospeed Timer</b><br>A link up that does not hold for 2.5 seconds is counted as a link fail, and the Auto-Downspeed retry counter increases by 1. The field only takes effect after a software reset.<br>0 <sub>B</sub> Do not bypass the timer<br>1 <sub>B</sub> Bypass the timer                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| RES4  | 0     | RO   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

## MDIO Registers Detailed Description

### 5.2.6 Extended Register's Address Offset Register (Register 30)

This section describes the Extended Register's Address Offset Register in detail.

#### Extended Register's Address Offset Register (Register 30)

The register is used in conjunction with the MDIO access to the extended register address field. This uses address directing as specified in the extended register chapter. See [Section 7.1](#) for more information.

| PHY_EXT_ADR                                                  | Offset            | Reset Value       |
|--------------------------------------------------------------|-------------------|-------------------|
| Extended Register's Address Offset Register<br>(Register 30) | 001E <sub>H</sub> | 0000 <sub>H</sub> |
| 15                                                           |                   | 0                 |
| EXTA                                                         |                   |                   |
| rw                                                           |                   |                   |

| Field | Bits | Type | Description                                                                                                             |
|-------|------|------|-------------------------------------------------------------------------------------------------------------------------|
| EXTA  | 15:0 | RW   | <b>Extended Register Address Offset</b><br>This is the address offset of the extended register that is read or written. |

### 5.2.7 Extended Register's Data Register (Register 31)

This section describes the Extended Register's Data Register in detail.

#### Extended Register's Data Register (Register 31)

The register is used in conjunction with the MDIO access to the extended data field. The data format is defined as specified in the extended register chapter. This register holds the data to be written or read to the extended register (indicated in [Section 5.2.6](#)). See [Section 7.1](#) for more information.

| PHY_EXT_DATA                                       | Offset            | Reset Value       |
|----------------------------------------------------|-------------------|-------------------|
| Extended Register's Data Register<br>(Register 31) | 001F <sub>H</sub> | 1C8D <sub>H</sub> |
| 15                                                 |                   | 0                 |
| EXTD                                               |                   |                   |
| rw                                                 |                   |                   |

| Field | Bits | Type | Description                                                                                                                                        |
|-------|------|------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| EXTD  | 15:0 | RW   | <b>Extended Register Data</b><br>This field contains the data to be written to, or read from, the extended register indicated by PHY_EXT_ADR.EXTA. |

## 6 MMD Registers Detailed Description

**Table 18** MMD Register Access Type

| Mode                                                                                             | Symbol |
|--------------------------------------------------------------------------------------------------|--------|
| Status Register (Status, or Ability Register)                                                    | RO     |
| Read-Write Register (e.g. MDIO Register)                                                         | RW     |
| Read-Write, Self-Clearing Register. The bit is cleared after being read from the MDIO interface. | RWSC   |

## 6.1 Standard PCS Registers for MMD=0003<sub>H</sub>

This section describes the PCS registers for MMD device 0003<sub>H</sub>.

**Table 19 Registers Overview - Standard PCS Registers**

| Register Short Name         | Register Long Name                 | Reset Value       |
|-----------------------------|------------------------------------|-------------------|
| <a href="#">PCS_STAT1</a>   | PCS Status 1 (Register 3.1)        | 0000 <sub>H</sub> |
| <a href="#">PCS_EEE_CAP</a> | PCS EEE Capability (Register 3.20) | 0006 <sub>H</sub> |

## MMD Registers Detailed Description

### 6.1.1 Standard PCS Registers for MMD=0003<sub>H</sub>

This chapter describes all registers of PCS in detail.

#### PCS Status 1 (Register 3.1)

IEEE Standard Register=3.1

#### PCS\_STAT1

Reset Value

#### PCS Status 1 (Register 3.1)

0000<sub>H</sub>

|     |              |              |              |              |       |            |     |             |             |     |    |    |
|-----|--------------|--------------|--------------|--------------|-------|------------|-----|-------------|-------------|-----|----|----|
| 15  | 12           | 11           | 10           | 9            | 8     | 7          | 6   | 5           | 3           | 2   | 1  | 0  |
| RES | TX_LP<br>I_* | RX_LP<br>I_* | TX_LP<br>I_* | RX_LP<br>I_* | FAULT | TXCK<br>ST | RES | PCS<br>RX_* | LOW<br>POW* | RES |    |    |
| ro  | ro           | ro           | ro           | ro           | ro    | ro         | ro  | ro          | ro          | ro  | ro | ro |

| Field              | Bits  | Type | Description                                                                                                                            |
|--------------------|-------|------|----------------------------------------------------------------------------------------------------------------------------------------|
| RES                | 15:12 | RO   | <b>Reserved</b>                                                                                                                        |
| TX_LPI_RXD         | 11    | RO   | <b>Tx Low Power Idle (LPI) Received</b><br>0 <sub>B</sub> LPI not received<br>1 <sub>B</sub> Tx PCS has received LPI                   |
| RX_LPI_RXD         | 10    | RO   | <b>Rx LPI received</b><br>0 <sub>B</sub> LPI not received Rx<br>1 <sub>B</sub> PCS has received LPI                                    |
| TX_LPI_INDICATION  | 9     | RO   | <b>Tx LPI Indication</b><br>0 <sub>B</sub> PCS is not currently receiving LPI<br>1 <sub>B</sub> Tx PCS is currently receiving LPI      |
| RX_LPI_INDICATION  | 8     | RO   | <b>Rx LPI Indication</b><br>0 <sub>B</sub> PCS is not currently receiving LPI<br>1 <sub>B</sub> Rx PCS is currently receiving LPI      |
| FAULT              | 7     | RO   | <b>Fault</b><br>0 <sub>B</sub> No fault condition detected<br>1 <sub>B</sub> Fault condition detected                                  |
| TXCKST             | 6     | RO   | <b>Clock Stop Capable</b><br>0 <sub>B</sub> Clock not stoppable<br>1 <sub>B</sub> The MAC has the ability to stop the clock during LPI |
| RES                | 5:3   | RO   | <b>Reserved</b>                                                                                                                        |
| PCS_RX_LINK_STATUS | 2     | RO   | <b>PCS Receive Link Status</b><br>0 <sub>B</sub> PCS receive link down<br>1 <sub>B</sub> PCS receive link up                           |
| LOW_POWER_ABILITY  | 1     | RO   | <b>Low-Power Ability</b><br>0 <sub>B</sub> PCS does not support low-power mode<br>1 <sub>B</sub> PCS supports low-power mode           |
| RES                | 0     | RO   | <b>Reserved</b>                                                                                                                        |

MMD Registers Detailed Description

PCS EEE Capability (Register 3.20)

IEEE Standard Register=3.20

PCS\_EEE\_CAP

PCS EEE Capability (Register 3.20)

Reset Value

0006<sub>H</sub>

|    |  |  |  |  |  |  |  |   |              |              |              |              |              |              |     |
|----|--|--|--|--|--|--|--|---|--------------|--------------|--------------|--------------|--------------|--------------|-----|
| 15 |  |  |  |  |  |  |  | 7 | 6            | 5            | 4            | 3            | 2            | 1            | 0   |
|    |  |  |  |  |  |  |  |   | R10G<br>BAS* | R10G<br>BAS* | R1000<br>BA* | R10G<br>BAS* | R1000<br>BA* | R100B<br>AS* | RES |
|    |  |  |  |  |  |  |  |   | ro           | ro           | ro           | ro           | ro           | ro           | ro  |

| Field                | Bits | Type | Description                                                                                                                      |
|----------------------|------|------|----------------------------------------------------------------------------------------------------------------------------------|
| RES                  | 15:7 | RO   | <b>Reserved</b>                                                                                                                  |
| R10GBASE_K<br>R_EEE  | 6    | RO   | <b>10GBASE-KR EEE</b><br>0 <sub>B</sub> EEE is not supported for 10GBASE-KR<br>1 <sub>B</sub> EEE is supported for 10GBASE-KR    |
| R10GBASE_K<br>X4_EEE | 5    | RO   | <b>10GBASE-KX4 EEE</b><br>0 <sub>B</sub> EEE is not supported for 10GBASE-KX4<br>1 <sub>B</sub> EEE is supported for 10GBASE-KX4 |
| R1000BASE_K<br>X_EEE | 4    | RO   | <b>1000BASE-KX EEE</b><br>0 <sub>B</sub> EEE is not supported for 1000BASE-KX<br>1 <sub>B</sub> EEE is supported for 1000BASE-KX |
| R10GBASE_T<br>_EEE   | 3    | RO   | <b>10GBASE-T EEE</b><br>0 <sub>B</sub> EEE is not supported for 10GBASE-T<br>1 <sub>B</sub> EEE is supported for 10GBASE-T       |
| R1000BASE_T<br>_EEE  | 2    | RO   | <b>1000BASE-T EEE</b><br>0 <sub>B</sub> EEE is not supported for 1000BASE-T<br>1 <sub>B</sub> EEE is supported for 1000BASE-T    |
| R100BASE_T<br>X_EEE  | 1    | RO   | <b>100BASE-TX EEE</b><br>0 <sub>B</sub> EEE is not supported for 100BASE-TX<br>1 <sub>B</sub> EEE is supported for 100BASE-TX    |
| RES                  | 0    | RO   | <b>Reserved</b>                                                                                                                  |

## 6.2 Standard Auto-Negotiation Registers for MMD=0007<sub>H</sub>

This register file contains the auto-negotiation registers for MMD device 0007<sub>H</sub>.

**Table 20 Registers Overview - Standard Auto-Negotiation Registers**

| Register Short Name               | Register Long Name                         | Reset Value       |
|-----------------------------------|--------------------------------------------|-------------------|
| <a href="#">ANEG_EEE_AN_ADV1</a>  | EEE Advertisement 1 (Register 7.60)        | 0000 <sub>H</sub> |
| <a href="#">ANEG_EEE_AN_LPAB1</a> | EEE Link Partner Ability 1 (Register 7.61) | 0000 <sub>H</sub> |

## MMD Registers Detailed Description

### 6.2.1 Standard Auto-Negotiation Registers for MMD=0007<sub>H</sub>

This section describes all registers of ANEG in detail.

#### EEE Advertisement 1 (Register 7.60)

IEEE Standard Register=7.60

ANEG\_EEE\_AN\_ADV1

#### EEE Advertisement 1 (Register 7.60)

Reset Value

0000<sub>H</sub>

| 15  | 7 | 6 | 5 | 4 | 3 | 2 | 1            | 0   |
|-----|---|---|---|---|---|---|--------------|-----|
| RES |   |   |   |   |   |   | EEE_1<br>0G* | RES |
| ro  |   |   |   |   |   |   | ro           | ro  |

| Field           | Bits | Type | Description                                                                                                                                                                   |
|-----------------|------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RES             | 15:7 | RO   | <b>Reserved</b>                                                                                                                                                               |
| EEE_10GBKR      | 6    | RO   | <b>Support of 10GBASE-KR EEE</b><br>0 <sub>B</sub> <b>DISABLED</b> This PHY mode is not supported for EEE<br>1 <sub>B</sub> <b>ENABLE</b> This PHY mode is supported for EEE  |
| EEE_10GBKX<br>4 | 5    | RO   | <b>Support of 10GBASE-KX4 EEE</b><br>0 <sub>B</sub> <b>DISABLED</b> This PHY mode is not supported for EEE<br>1 <sub>B</sub> <b>ENABLE</b> This PHY mode is supported for EEE |
| EEE_1000BKX     | 4    | RO   | <b>Support of 1000BASE-KX EEE</b><br>0 <sub>B</sub> <b>DISABLED</b> This PHY mode is not supported for EEE<br>1 <sub>B</sub> <b>ENABLE</b> This PHY mode is supported for EEE |
| EEE_10GBT       | 3    | RO   | <b>Support of 10GBASE-T EEE</b><br>0 <sub>B</sub> <b>DISABLED</b> This PHY mode is not supported for EEE<br>1 <sub>B</sub> <b>ENABLE</b> This PHY mode is supported for EEE   |
| EEE_1000BT      | 2    | RW   | <b>Support of 1000BASE-T EEE</b><br>0 <sub>B</sub> <b>DISABLED</b> This PHY mode is not supported for EEE<br>1 <sub>B</sub> <b>ENABLE</b> This PHY mode is supported for EEE  |
| EEE_100BTX      | 1    | RW   | <b>Support of 100BASE-TX EEE</b><br>0 <sub>B</sub> <b>DISABLED</b> This PHY mode is not supported for EEE<br>1 <sub>B</sub> <b>ENABLE</b> This PHY mode is supported for EEE  |
| RES             | 0    | RO   | <b>Reserved</b>                                                                                                                                                               |

## MMD Registers Detailed Description

### EEE Link Partner Ability 1 (Register 7.61)

After the ANEG process is completed, this register reflects the contents of the link partner's EEE advertisement register. The definitions are the same as the ANEG\_EEE\_AN\_ADV1 register.

IEEE Standard Register=7.61

All of the bits in the EEE LP ability 1 register are read-only. A write operation to the EEE LP advertisement register has no effect.

ANEG EEE AN LPAB1

### Reset Value

### EEE Link Partner Ability 1 (Register 7.61)

0000<sub>H</sub>

|     |  |  |  |  |  |  |  |   |              |              |              |              |              |              |     |
|-----|--|--|--|--|--|--|--|---|--------------|--------------|--------------|--------------|--------------|--------------|-----|
| 15  |  |  |  |  |  |  |  | 7 | 6            | 5            | 4            | 3            | 2            | 1            | 0   |
| RES |  |  |  |  |  |  |  |   | EEE_1<br>0G* | EEE_1<br>0G* | EEE_1<br>00* | EEE_1<br>0G* | EEE_1<br>00* | EEE_1<br>00* | RES |
| ro  |  |  |  |  |  |  |  |   | ro           | ro           | ro           | ro           | ro           | ro           | ro  |

| Field           | Bits | Type | Description                                                                                                                                                                   |
|-----------------|------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RES             | 15:7 | RO   | <b>Reserved</b>                                                                                                                                                               |
| EEE_10GBKR      | 6    | RO   | <b>Support of 10GBASE-KR EEE</b><br>0 <sub>B</sub> <b>DISABLED</b> This PHY mode is not supported for EEE<br>1 <sub>B</sub> <b>ENABLE</b> This PHY mode is supported for EEE  |
| EEE_10GBKX<br>4 | 5    | RO   | <b>Support of 10GBASE-KX4 EEE</b><br>0 <sub>B</sub> <b>DISABLED</b> This PHY mode is not supported for EEE<br>1 <sub>B</sub> <b>ENABLE</b> This PHY mode is supported for EEE |
| EEE_1000BKX     | 4    | RO   | <b>Support of 1000BASE-KX EEE</b><br>0 <sub>B</sub> <b>DISABLED</b> This PHY mode is not supported for EEE<br>1 <sub>B</sub> <b>ENABLE</b> This PHY mode is supported for EEE |
| EEE_10GBT       | 3    | RO   | <b>Support of 10GBASE-T EEE</b><br>0 <sub>B</sub> <b>DISABLED</b> This PHY mode is not supported for EEE<br>1 <sub>B</sub> <b>ENABLE</b> This PHY mode is supported for EEE   |
| EEE_1000BT      | 2    | RO   | <b>Support of 1000BASE-T EEE</b><br>0 <sub>B</sub> <b>DISABLED</b> This PHY mode is not supported for EEE<br>1 <sub>B</sub> <b>ENABLE</b> This PHY mode is supported for EEE  |
| EEE_100BTX      | 1    | RO   | <b>Support of 100BASE-TX EEE</b><br>0 <sub>B</sub> <b>DISABLED</b> This PHY mode is not supported for EEE<br>1 <sub>B</sub> <b>ENABLE</b> This PHY mode is supported for EEE  |
| RES             | 0    | RO   | <b>Reserved</b>                                                                                                                                                               |

## 7 Extended Register Detailed Description

**Table 21** Extended Register Access Type

| Mode                                                                                             | Symbol |
|--------------------------------------------------------------------------------------------------|--------|
| Status Register (Status, or Ability Register)                                                    | RO     |
| Read-Write Register (e.g. MDIO Register)                                                         | RW     |
| Read-Write, Self-Clearing Register. The bit is cleared after being read from the MDIO interface. | RWSC   |

## Extended Register Detailed Description

### 7.1 Common Extended Register

This section describes the common extended registers.

**Table 22 Registers Overview - Common Extended Register**

| Register Short Name                    | Register Long Name                                                                 | Reset Value       |
|----------------------------------------|------------------------------------------------------------------------------------|-------------------|
| <a href="#">COM_EXT_CHIP_CFG</a>       | Chip Configuration Register (Register A001 <sub>H</sub> )                          | 8140 <sub>H</sub> |
| <a href="#">COM_EXT_RGMII_CFG1</a>     | RGMII Configuration Register 1 (Register A003 <sub>H</sub> )                       | 00F1 <sub>H</sub> |
| <a href="#">COM_EXT_RGMII_CFG2</a>     | RGMII Configuration Register 2 (Register A004 <sub>H</sub> )                       | 0000 <sub>H</sub> |
| <a href="#">COM_EXT_RGMII_MDIO_CFG</a> | RGMII In-Band Status and MDIO Configuration Register (Register A005 <sub>H</sub> ) | 00C0 <sub>H</sub> |
| <a href="#">COM_EXT_MISC_CFG</a>       | Miscellaneous Control Register (Register A006 <sub>H</sub> )                       | 000D <sub>H</sub> |
| <a href="#">COM_EXT_MAC_ADDR_CFG1</a>  | Wake on LAN Address Byte 5 and 4 (Register A007 <sub>H</sub> )                     | 0000 <sub>H</sub> |
| <a href="#">COM_EXT_MAC_ADDR_CFG2</a>  | Wake on LAN Address Byte 3 and 2 (Register A008 <sub>H</sub> )                     | 0000 <sub>H</sub> |
| <a href="#">COM_EXT_MAC_ADDR_CFG3</a>  | Wake on LAN Address Byte 1 and 0 (Register A009 <sub>H</sub> )                     | 0000 <sub>H</sub> |
| <a href="#">COM_EXT_WOL_CFG</a>        | Wake on LAN Control Register (Register A00A <sub>H</sub> )                         | 0002 <sub>H</sub> |
| <a href="#">COM_EXT_LED_GEN_CFG</a>    | LED General Configuration Register (Register A00B <sub>H</sub> )                   | E000 <sub>H</sub> |
| <a href="#">COM_EXT_LED0_CFG</a>       | LED0 Configuration Register (Register A00C <sub>H</sub> )                          | 0610 <sub>H</sub> |
| <a href="#">COM_EXT_LED1_CFG</a>       | LED1 Configuration Register (Register A00D <sub>H</sub> )                          | 0620 <sub>H</sub> |
| <a href="#">COM_EXT_LED2_CFG</a>       | LED2 Configuration Register (Register A00E <sub>H</sub> )                          | 0640 <sub>H</sub> |
| <a href="#">COM_EXT_LED_BLINK_CFG</a>  | LED Blinking Configuration Register (Register A00F <sub>H</sub> )                  | 0006 <sub>H</sub> |
| <a href="#">COM_EXT_PAD_STR_CFG</a>    | Pin Driving Strength Configuration Register (Register A010 <sub>H</sub> )          | 6BFF <sub>H</sub> |
| <a href="#">COM_EXT_SYNCE_CFG</a>      | SyncE Configuration Register (Register A012 <sub>H</sub> )                         | 00C8 <sub>H</sub> |

## Extended Register Detailed Description

### 7.1.1 Chip Configuration Register (Register A001<sub>H</sub>)

This section describes the Chip Configuration Register in detail.

#### Chip Configuration Register (Register A001<sub>H</sub>)

This register is used to control chip mode and configuration.

| COM_EXT_CHIP_CFG                                             | Offset            | Reset Value       |
|--------------------------------------------------------------|-------------------|-------------------|
| Chip Configuration Register<br>(Register A001 <sub>H</sub> ) | A001 <sub>H</sub> | 8140 <sub>H</sub> |

|      |    |     |    |       |       |     |      |   |      |   |     |   |
|------|----|-----|----|-------|-------|-----|------|---|------|---|-----|---|
| 15   | 14 |     | 10 | 9     | 8     | 7   | 6    | 5 | 4    | 3 |     | 0 |
| MCR  |    | RES |    | GERXC | RXDLY | RES | ELDO |   | CLDO |   | RES |   |
| rwsc |    | rw  |    | rw    | rw    | ro  | rw   |   | rw   |   | ro  |   |

| Field | Bits  | Type | Description                                                                                                                                                                                                                                                                                                                                |
|-------|-------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MCR   | 15    | RWSC | <b>Software Reset Mode</b><br>This MCR field resets the chip to change the mode. The bit is active low and self clearing.<br>0 <sub>B</sub> Reset<br>1 <sub>B</sub> No Reset (Default)                                                                                                                                                     |
| RES   | 14:10 | RW   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                            |
| GERXC | 9     | RW   | <b>RGMII Rx Clock Enable</b><br>This GERXC field controls the RGMII Rx clock gating when the link is down.<br>0 <sub>B</sub> Do not close RXC when the link is down. (Default)<br>1 <sub>B</sub> Close RXC when the link is down.                                                                                                          |
| RXDLY | 8     | RW   | <b>RGMII Rx Clock Delay</b><br>This RXDLY field enables or disables the RGMII Rx clock delay. When enabled the delay is 2 ns for 125 MHz or 8 ns for 25 MHz and 2.5 MHz. The initial setting is defined by pin strapping.<br>0 <sub>B</sub> Disable the RGMII Rx clock delay.<br>1 <sub>B</sub> Enable the RGMII Rx clock delay. (Default) |
| RES   | 7     | RO   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                            |
| ELDO  | 6     | RW   | <b>LDO Enable</b><br>This ELDO field controls the RGMII LDO. The default value is 0 and is set to 1 after power-on pin strapping is completed.<br>0 <sub>B</sub> LDO Disabled (Default)<br>1 <sub>B</sub> LDO Enabled                                                                                                                      |
| CLDO  | 5:4   | RW   | <b>LDO Configuration</b><br>This CLDO field sets the RGMII LDO voltage and RGMII/MDC/MDIO pin's level shifter control. The initial setting is defined by pin strapping.<br>00 <sub>B</sub> 3.3 V - Not regulated from 3.3 V. (Default)<br>01 <sub>B</sub> 2.5 V<br>10 <sub>B</sub> 1.8 V<br>11 <sub>B</sub> 1.8 V                          |

## Extended Register Detailed Description

| Field | Bits | Type | Description (continued) |
|-------|------|------|-------------------------|
| RES   | 3    | RO   | Reserved                |
| RES   | 2:0  | RO   | Reserved                |

## Extended Register Detailed Description

### 7.1.2 RGMII Configuration Register 1 (Register A003<sub>H</sub>)

This section describes the RGMII Configuration Register 1 in detail.

#### RGMII Configuration Register 1 (Register A003<sub>H</sub>)

This register controls the RGMII interface settings.

| COM_EXT_RGMII_CFG1                                              | Offset            | Reset Value       |
|-----------------------------------------------------------------|-------------------|-------------------|
| RGMII Configuration Register 1<br>(Register A003 <sub>H</sub> ) | A003 <sub>H</sub> | 00F1 <sub>H</sub> |

|     |    |       |    |      |     |   |      |   |     |
|-----|----|-------|----|------|-----|---|------|---|-----|
| 15  | 14 | 13    | 10 | 9    | 8   | 7 | 4    | 3 | 0   |
| RES |    | RDLYS |    | ERFC | ERC |   | TDSF |   | TDS |
| rw  |    | rw    |    | rw   | rw  |   | rw   |   | rw  |

| Field | Bits  | Type | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|-------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RES   | 15:14 | RW   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| RDLYS | 13:10 | RW   | <b>RGMII Rx Delay Select</b><br>This register controls the RGMII Rx clock delay training configuration. Each step adds approximately 150 ps of delay.<br>0000 <sub>B</sub> Disabled (Default)<br>0001 <sub>B</sub> 150 ps<br>0010 <sub>B</sub> 300 ps<br>0011 <sub>B</sub> 450 ps<br>0100 <sub>B</sub> 600 ps<br>0101 <sub>B</sub> 750 ps<br>0110 <sub>B</sub> 900 ps<br>0111 <sub>B</sub> 1050 ps<br>1000 <sub>B</sub> 1200 ps<br>1001 <sub>B</sub> 1350 ps<br>1010 <sub>B</sub> 1500 ps<br>1011 <sub>B</sub> 1650 ps<br>1100 <sub>B</sub> 1800 ps<br>1101 <sub>B</sub> 1950 ps<br>1110 <sub>B</sub> 2100 ps<br>1111 <sub>B</sub> 2250 ps |
| ERFC  | 9     | RW   | <b>Enable RGMII In-Band Full Duplex with CRS</b><br>This ERFC field in conjunction with the ERC field controls encoding of the GMII/MII CRS into RGMII in-band status.<br>0 <sub>B</sub> Encoding of GMII/MII CRS into RGMII in-band status is controlled by the ERC field. (Default)<br>1 <sub>B</sub> Encode GMII/MII CRS into RGMII in-band status if the field ERC is set to 1.                                                                                                                                                                                                                                                        |

Extended Register Detailed Description

| Field | Bits | Type | Description (continued)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ERC   | 8    | RW   | <b>Enable RGMII In-Band with CRS</b><br>This ERC field controls encoding of GMII/MII CRS into RGMII in-band status.<br>0 <sub>B</sub> Do not encode GMII/MII CRS into RGMII in-band status. (Default)<br>1 <sub>B</sub> Encode GMII/MII CRS into RGMII in-band status on half-duplex mode or if field ERFC is also set to 1.                                                                                                                                                                                                                                                                                                                                              |
| TDSF  | 7:4  | RW   | <b>Fast Ethernet RGMII Tx Clock Delay Selection</b><br>This TDSF field configures the RGMII TX_CLK delay train for 100 Mbps or 10 Mbps link speed. Each step delays by about 150 ps.<br>0000 <sub>B</sub> Disabled<br>0001 <sub>B</sub> 150 ps<br>0010 <sub>B</sub> 300 ps<br>0011 <sub>B</sub> 450 ps<br>0100 <sub>B</sub> 600 ps<br>0101 <sub>B</sub> 750 ps<br>0110 <sub>B</sub> 900 ps<br>0111 <sub>B</sub> 1050 ps<br>1000 <sub>B</sub> 1200 ps<br>1001 <sub>B</sub> 1350 ps<br>1010 <sub>B</sub> 1500 ps<br>1011 <sub>B</sub> 1650 ps<br>1100 <sub>B</sub> 1800 ps<br>1101 <sub>B</sub> 1950 ps<br>1110 <sub>B</sub> 2100 ps<br>1111 <sub>B</sub> 2250 ps (Default) |
| TDS   | 3:0  | RW   | <b>Gigabit Ethernet RGMII Tx Clock Delay Selection</b><br>This TDS field configures the RGMII TX_CLK delay train for 1000 Mbps link speed. Each step delays by about 150 ps.<br>0000 <sub>B</sub> Disabled<br>0001 <sub>B</sub> 150 ps (Default)<br>0010 <sub>B</sub> 300 ps<br>0011 <sub>B</sub> 450 ps<br>0100 <sub>B</sub> 600 ps<br>0101 <sub>B</sub> 750 ps<br>0110 <sub>B</sub> 900 ps<br>0111 <sub>B</sub> 1050 ps<br>1000 <sub>B</sub> 1200 ps<br>1001 <sub>B</sub> 1350 ps<br>1010 <sub>B</sub> 1500 ps<br>1011 <sub>B</sub> 1650 ps<br>1100 <sub>B</sub> 1800 ps<br>1101 <sub>B</sub> 1950 ps<br>1110 <sub>B</sub> 2100 ps<br>1111 <sub>B</sub> 2250 ps         |

## Extended Register Detailed Description

### 7.1.3 RGMII Configuration Register 2 (Register A004<sub>H</sub>)

This section describes the RGMII Configuration Register 2 in detail.

#### RGMII Configuration Register 2 (Register A004<sub>H</sub>)

This register is used for RGMII in-band status.

|                                                                 |                   |                   |
|-----------------------------------------------------------------|-------------------|-------------------|
| COM_EXT_RGMII_CFG2                                              | Offset            | Reset Value       |
| RGMII Configuration Register 2<br>(Register A004 <sub>H</sub> ) | A004 <sub>H</sub> | 0000 <sub>H</sub> |

|      |    |      |      |      |    |           |            |     |  |  |  |  |  |  |  |  |   |
|------|----|------|------|------|----|-----------|------------|-----|--|--|--|--|--|--|--|--|---|
| 15   | 14 | 13   | 12   | 11   | 10 | 9         | 8          | 7   |  |  |  |  |  |  |  |  | 0 |
| SPDP |    | DUPP | LNKP | PAUP |    | EEEC<br>P | EEEC<br>CP | RES |  |  |  |  |  |  |  |  |   |
| ro   |    | ro   | ro   | ro   |    | ro        | ro         | rw  |  |  |  |  |  |  |  |  |   |

| Field | Bits  | Type | Description                                                                                                                                                                                                                                                                                                              |
|-------|-------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SPDP  | 15:14 | RO   | <b>RGMII PHY Speed Status</b><br>This SPDP field reports the RGMII interface speed information when configured as an RGMII PHY. This is also the source of RGMII in-band status communication.<br>00 <sub>B</sub> 10 Mbps (Default)<br>01 <sub>B</sub> 100 Mbps<br>10 <sub>B</sub> 1000 Mbps<br>11 <sub>B</sub> Reserved |
| DUPP  | 13    | RO   | <b>RGMII PHY Duplex Status</b><br>This DUPP field reports the RGMII interface duplex information when configured as an RGMII PHY. This is also the source of RGMII in-band status.<br>0 <sub>B</sub> Half-duplex (Default)<br>1 <sub>B</sub> Full-duplex                                                                 |
| LNKP  | 12    | RO   | <b>RGMII PHY Link-up Status</b><br>This LNKP field reports the RGMII interface linkup information when configured as an RGMII PHY. This is also the source of RGMII in-band status.<br>0 <sub>B</sub> Link down (Default)<br>1 <sub>B</sub> Link up                                                                      |
| PAUP  | 11:10 | RO   | <b>RGMII PHY Pause Information</b><br>This PAUP field reports the RGMII interface pause information when configured as an RGMII PHY.<br>00 <sub>B</sub> No asymmetric pause (Default)<br>10 <sub>B</sub> Asymmetric pause<br>01 <sub>B</sub> No Pause symmetric pause<br>11 <sub>B</sub> Symmetric pause                 |

Extended Register Detailed Description

| Field | Bits | Type | Description (continued)                                                                                                                                                                                                                                                                                                   |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EEEC  | 9    | RO   | <b>RGMII PHY EEE Capability</b><br>This EEECP field reports the capability of the RGMII interface for EEE when configured as RGMII PHY.<br>0 <sub>B</sub> The RGMII interface is not capable of EEE. (Default)<br>1 <sub>B</sub> The RGMII interface is capable of EEE.                                                   |
| EEEC  | 8    | RO   | <b>RGMII PHY EEE Clock Stopping</b><br>This EEECCP field reports the capability of the RGMII interface for EEE clock stopping when configured as RGMII PHY.<br>0 <sub>B</sub> The RGMII interface is not capable of EEE clock stopping. (Default)<br>1 <sub>B</sub> The RGMII interface is capable of EEE clock stopping. |
| RES   | 7:0  | RW   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                           |

## Extended Register Detailed Description

### 7.1.4 RGMII In-Band Status and MDIO Configuration Register (Register A005<sub>H</sub>)

This section describes the RGMII In-Band Status and MDIO Configuration Register in detail.

#### RGMII In-Band Status and MDIO Configuration Register (Register A005<sub>H</sub>)

This register shows the RGMII in-band status and MDIO settings.

|                                                                                    |                   |                   |
|------------------------------------------------------------------------------------|-------------------|-------------------|
| COM_EXT_RGMII_MDIO_CFG                                                             | Offset            | Reset Value       |
| RGMII In-Band Status and MDIO Configuration Register (Register A005 <sub>H</sub> ) | A005 <sub>H</sub> | 00C0 <sub>H</sub> |

|      |    |      |   |   |      |     |    |
|------|----|------|---|---|------|-----|----|
| 15   | 12 | 11   | 7 | 6 | 5    | 4   | 0  |
| RES0 |    | RES1 |   |   | EPA0 | EBA | BA |
| rw   |    | ro   |   |   | rw   | rw  | rw |

| Field | Bits  | Type | Description                                                                                                                                                                                                                    |
|-------|-------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RES0  | 15:12 | RW   | <b>Reserved</b>                                                                                                                                                                                                                |
| RES1  | 11:7  | RO   | <b>Reserved</b><br>The default is 0 <sub>B</sub> .                                                                                                                                                                             |
| EPA0  | 6     | RW   | <b>Enable PHY Address 0 Broadcast Responses</b><br>This field controls whether the PHY responds to the MDIO interface's broadcasts access from PHY address 0.<br>0 <sub>B</sub> Disabled<br>1 <sub>B</sub> Enabled (Default)   |
| EBA   | 5     | RW   | <b>Enable PHY BA Broadcast Responses</b><br>This field controls whether the PHY responds to broadcasts from a PHY address defined in COM_ETX_RGMII_MIDO_CFG.BA.<br>0 <sub>B</sub> Disabled (Default)<br>1 <sub>B</sub> Enabled |
| BA    | 4:0   | RW   | <b>Broadcast Address</b><br>This BA field defines the address for accepting broadcast access response.<br>The default is 0 <sub>B</sub> .                                                                                      |

### Miscellaneous Control Register (Register A006<sub>H</sub>)

This register controls miscellaneous PHY settings.

|                                                                       |                         |                         |
|-----------------------------------------------------------------------|-------------------------|-------------------------|
| <b>COM_EXT_MISC_CFG</b>                                               | <b>Offset</b>           | <b>Reset Value</b>      |
| <b>Miscellaneous Control Register<br/>(Register A006<sub>H</sub>)</b> | <b>A006<sub>H</sub></b> | <b>000D<sub>H</sub></b> |

|     |  |  |  |  |  |  |   |    |     |      |     |      |     |  |   |
|-----|--|--|--|--|--|--|---|----|-----|------|-----|------|-----|--|---|
| 15  |  |  |  |  |  |  | 8 | 7  | 6   | 5    | 4   | 3    | 2   |  | 0 |
| RES |  |  |  |  |  |  |   | JE | RES | RLBP | RES | BGFR | RES |  |   |
| rw  |  |  |  |  |  |  |   | rw | rw  | rw   | rw  | rw   | rw  |  |   |

| Field | Bits | Type | Description                                                                                                                                                                                                                                                                                                       |
|-------|------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RES   | 15:8 | RW   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                   |
| JE    | 7    | RW   | <b>Jumbo Frame Enable</b><br>This JE field controls the use of jumbo frames.<br>0 <sub>B</sub> Jumbo frames are disabled (Default)<br>1 <sub>B</sub> Jumbo frames are enabled                                                                                                                                     |
| RES   | 6    | RW   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                   |
| RLBP  | 5    | RW   | <b>PHY Remote Loopback</b><br>This RLBP field controls setting of remote loopback for PHY.<br>0 <sub>B</sub> Disabled (Default)<br>1 <sub>B</sub> Enabled                                                                                                                                                         |
| RES   | 4    | RW   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                   |
| BGFR  | 3    | RW   | <b>Bypass GMII Overflow and Reset</b><br>This BGFR field controls whether to bypass the GMII FIFO overflow and underflow RST.<br>0 <sub>B</sub> Enable to reset GMII FIFO automatic when overflow or underflow happens.<br>1 <sub>B</sub> Disable to reset GMII FIFO when overflow or underflow happen. (Default) |
| RES   | 2:0  | RW   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                   |

Extended Register Detailed Description

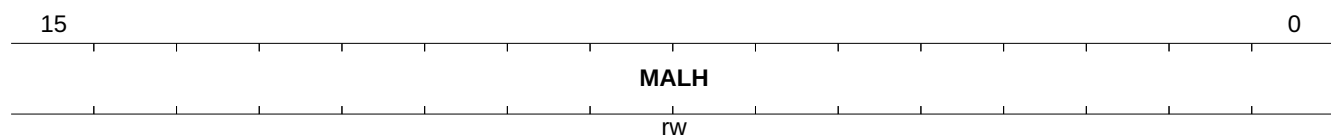
### 7.1.6 Wake on LAN Address Byte 5 and 4 (Register A007<sub>H</sub>)

This section describes the Wake on LAN Address Byte 5 and 4 registers in detail.

#### Wake on LAN Address Byte 5 and 4 (Register A007<sub>H</sub>)

This register holds the WoL MAC address's bytes 4 and 5.

| COM_EXT_MAC_ADDR_CFG1                                             | Offset            | Reset Value       |
|-------------------------------------------------------------------|-------------------|-------------------|
| Wake on LAN Address Byte 5 and 4<br>(Register A007 <sub>H</sub> ) | A007 <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type | Description                                                                                                                                         |
|-------|------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| MALH  | 15:0 | RW   | <b>MAC Address Location 47-32</b><br>This MALH field holds the first two octets of the MAC address used for WOL.<br>The default is 0 <sub>B</sub> . |

## Extended Register Detailed Description

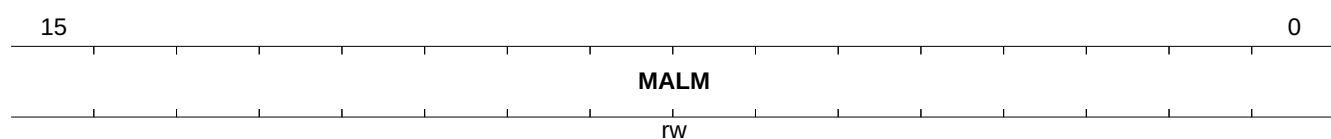
### 7.1.7 Wake on LAN Address Byte 3 and 2 (Register A008<sub>H</sub>)

This section describes the Wake on LAN Address Byte 3 and 2 registers in detail.

#### Wake on LAN Address Byte 3 and 2 (Register A008<sub>H</sub>)

This register holds the WoL MAC address's bytes 3 and 2.

| COM_EXT_MAC_ADDR_CFG2                                             | Offset            | Reset Value       |
|-------------------------------------------------------------------|-------------------|-------------------|
| Wake on LAN Address Byte 3 and 2<br>(Register A008 <sub>H</sub> ) | A008 <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type | Description                                                                                                                                          |
|-------|------|------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| MALM  | 15:0 | RW   | <b>MAC Address Location 31-16</b><br>This MALM field holds the middle two octets of the MAC address used for WOL.<br>The default is 0 <sub>B</sub> . |

Extended Register Detailed Description

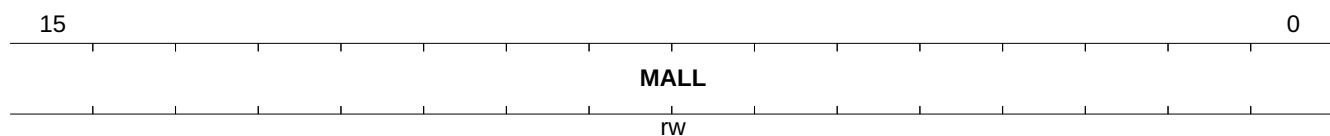
### 7.1.8 Wake on LAN Address Byte 1 and 0 (Register A009<sub>H</sub>)

This section describes the Wake on LAN Address Byte 1 and 0 registers in detail.

#### Wake on LAN Address Byte 1 and 0 (Register A009<sub>H</sub>)

This register holds the WoL MAC address's bytes 1 and 0.

| COM_EXT_MAC_ADDR_CFG3                                             | Offset            | Reset Value       |
|-------------------------------------------------------------------|-------------------|-------------------|
| Wake on LAN Address Byte 1 and 0<br>(Register A009 <sub>H</sub> ) | A009 <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type | Description                                                                                                                                       |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| MALL  | 15:0 | RW   | <b>MAC Address Location 15-0</b><br>This MALL field holds the last two octets of the MAC address used for WOL.<br>The default is 0 <sub>B</sub> . |

## Extended Register Detailed Description

### 7.1.9 Wake on LAN Control Register (Register A00A<sub>H</sub>)

This section describes the Wake on LAN Control Register in detail.

#### Wake on LAN Control Register (Register A00A<sub>H</sub>)

This register configures the WoL function.

|                                                               |                   |                   |
|---------------------------------------------------------------|-------------------|-------------------|
| COM_EXT_WOL_CFG                                               | Offset            | Reset Value       |
| Wake on LAN Control Register<br>(Register A00A <sub>H</sub> ) | A00A <sub>H</sub> | 0002 <sub>H</sub> |

|     |  |  |  |  |  |  |   |     |     |    |   |      |     |  |    |  |
|-----|--|--|--|--|--|--|---|-----|-----|----|---|------|-----|--|----|--|
| 15  |  |  |  |  |  |  | 8 | 7   | 6   |    | 4 | 3    | 2   |  | 0  |  |
| RES |  |  |  |  |  |  |   | SCR | RES |    |   | WOLE | RES |  |    |  |
| ro  |  |  |  |  |  |  |   | rw  |     | rw |   |      | rw  |  | rw |  |

| Field | Bits | Type | Description                                                                                                                                                                           |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RES   | 15:8 | RO   | <b>Reserved</b><br>The default is 0 <sub>B</sub>                                                                                                                                      |
| SCR   | 7    | RW   | <b>RGMII Enable</b><br>This SCR field enables or disables the RGMII interface.<br>0 <sub>B</sub> Enable the RGMII interface. (Default)<br>1 <sub>B</sub> Disable the RGMII interface. |
| RES   | 6:4  | RW   | <b>Reserved</b>                                                                                                                                                                       |
| WOLE  | 3    | RW   | <b>WOL Enable</b><br>This WOLE field controls the operation mode of the Wake-on-LAN feature.<br>0 <sub>B</sub> WOL is disabled. (Default)<br>1 <sub>B</sub> WOL is enabled.           |
| RES   | 2:0  | RW   | <b>Reserved</b>                                                                                                                                                                       |

## Extended Register Detailed Description

### 7.1.10 LED General Configuration Register (Register A00B<sub>H</sub>)

This section describes the LED General Configuration Register in detail.

#### LED General Configuration Register (Register A00B<sub>H</sub>)

This register controls the LED general configuration.

| COM_EXT_LED_GEN_CFG                                                 | Offset            | Reset Value       |
|---------------------------------------------------------------------|-------------------|-------------------|
| LED General Configuration Register<br>(Register A00B <sub>H</sub> ) | A00B <sub>H</sub> | E000 <sub>H</sub> |

| 15    | 14    | 13   | 12  | 11  | 9 | 8    | 7    | 6    | 5    | 4    | 3    | 2  | 1 | 0 |
|-------|-------|------|-----|-----|---|------|------|------|------|------|------|----|---|---|
| COLBS | JABLD | LPLD | DLD | RES |   | L2FE | L2FM | L1FE | L1FM | L0FE | L0FM |    |   |   |
| RW    | RW    | RW   | RW  | RO  |   | RW   | RW   | RW   | RW   | RW   | RW   | RW |   |   |

| Field | Bits | Type | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| COLBS | 15   | RW   | <b>LED Collision Blink Frequency</b><br>This COLBS field controls the collision LED blinking frequency. The blink function is only valid if COM_EXT_LED0_CFG.LCBE0, COM_EXT_LED1_CFG.LCBE0, or COM_EXT_LED0_CFG.LCBE0 is set to 1 <sub>B</sub> .<br>0 <sub>B</sub> When a collision occurs, blink with the frequency defined in COM_EXT_LED_BLINK_CFG.LFEQ1.<br>1 <sub>B</sub> When a collision occurs, blink with the frequency defined in COM_EXT_LED_BLINK_CFG.LFEQ2. (Default) |
| JABLD | 14   | RW   | <b>LED Jabber Blink</b><br>This JABLD field controls LED blinking on a jabber condition.<br>0 <sub>B</sub> Blinking under jabber conditions.<br>1 <sub>B</sub> No blinking under jabber conditions. (Default)                                                                                                                                                                                                                                                                      |
| LPLD  | 13   | RW   | <b>LED Loopback Display</b><br>This LPLD field controls whether the LED indicates an internal loopback condition.<br>0 <sub>B</sub> Blinking under loopback conditions.<br>1 <sub>B</sub> No blinking under loopback conditions. (Default)                                                                                                                                                                                                                                         |
| DLD   | 12   | RW   | <b>Auto-Negotiation Display</b><br>This DLD field controls whether the LED indicates the auto-negotiation state.<br>0 <sub>B</sub> Blinking when auto-negotiation is at LINK_GOOD_CHECK condition. It means the link is not yet ready. (Default)<br>1 <sub>B</sub> No blinking to indicate auto-negotiation state.                                                                                                                                                                 |
| RES   | 11:9 | RO   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| L2FE  | 8    | RW   | <b>LED2 Force Enable</b><br>This L2FE field controls the enable of LED2 force mode defined in the L2FM field.<br>0 <sub>B</sub> Disable LED2 force mode. (Default)<br>1 <sub>B</sub> Enable LED2 force mode.                                                                                                                                                                                                                                                                       |

Extended Register Detailed Description

| Field | Bits | Type | Description (continued)                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| L2FM  | 7:6  | RW   | <b>LED2 Force Mode</b><br>This L2FM field controls the LED2 blink pattern in force mode. Force mode is enabled with the L2FE bit.<br>00 <sub>B</sub> Force the LED off. (Default)<br>01 <sub>B</sub> Force the LED on.<br>10 <sub>B</sub> Force the LED to blink with the frequency defined in COM_EXT_LED_BLINK_CFG.LFEQ1.<br>11 <sub>B</sub> Force the LED to blink with the frequency defined in COM_EXT_LED_BLINK_CFG.LFEQ2. |
| L1FE  | 5    | RW   | <b>LED1 Force Enable</b><br>This L1FE field controls the enable of LED1 force mode defined in the L1FM field.<br>0 <sub>B</sub> Disable LED1 force mode. (Default)<br>1 <sub>B</sub> Enable LED1 force mode.                                                                                                                                                                                                                     |
| L1FM  | 4:3  | RW   | <b>LED1 Force Mode</b><br>This L1FM field controls the LED1 blink pattern in force mode. Force mode is enabled with the L1FE bit.<br>00 <sub>B</sub> Force the LED off. (Default)<br>01 <sub>B</sub> Force the LED on.<br>10 <sub>B</sub> Force the LED to blink with the frequency defined in COM_EXT_LED_BLINK_CFG.LFEQ1.<br>11 <sub>B</sub> Force the LED to blink with the frequency defined in COM_EXT_LED_BLINK_CFG.LFEQ2. |
| L0FE  | 2    | RW   | <b>LED0 Force Enable</b><br>This L0FE field controls the enable of LED0 force mode defined in the L0FM field.<br>0 <sub>B</sub> Disable LED0 force mode. (Default)<br>1 <sub>B</sub> Enable LED0 force mode.                                                                                                                                                                                                                     |
| L0FM  | 1:0  | RW   | <b>LED0 Force Mode</b><br>This L0FM field controls the LED0 blink pattern in force mode. Force mode is enabled with the L0FE bit.<br>00 <sub>B</sub> Force the LED off. (Default)<br>01 <sub>B</sub> Force the LED on.<br>10 <sub>B</sub> Force the LED to blink with the frequency defined in COM_EXT_LED_BLINK_CFG.LFEQ1.<br>11 <sub>B</sub> Force the LED to blink with the frequency defined in COM_EXT_LED_BLINK_CFG.LFEQ2. |

Extended Register Detailed Description

### 7.1.11 LED0 Configuration Register (Register A00C<sub>H</sub>)

This section describes the LED0 Configuration Register in detail.

#### LED0 Configuration Register (Register A00C<sub>H</sub>)

This register configures LED0.

| COM_EXT_LED0_CFG                                             | Offset            | Reset Value       |
|--------------------------------------------------------------|-------------------|-------------------|
| LED0 Configuration Register<br>(Register A00C <sub>H</sub> ) | A00C <sub>H</sub> | 0610 <sub>H</sub> |

| 15  | 14   | 13    | 12    | 11     | 10     | 9     | 8     | 7    | 6    | 5    | 4     | 3     | 2     | 1     | 0  |
|-----|------|-------|-------|--------|--------|-------|-------|------|------|------|-------|-------|-------|-------|----|
| RES | LAB0 | LFDE0 | LHDE0 | LTABE0 | LRABE0 | LTAE0 | LRAE0 | LGE0 | LFE0 | LBE0 | LCBE0 | LGBE0 | LFBE0 | LBBE0 |    |
| rw  | rw   | rw    | rw    | rw     | rw     | rw    | rw    | rw   | rw   | rw   | rw    | rw    | rw    | rw    | rw |

| Field  | Bits  | Type | Description                                                                                                                                                                                                                                                                                                                                     |
|--------|-------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RES    | 15:14 | RW   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                 |
| LAB0   | 13    | RW   | <b>LED0 Activity Blink Indicator</b><br>This field configures LED blinking when there is traffic activity no matter LED under constant on or off state.<br>0 <sub>B</sub> LED0 only blinks when the link LED0 is in the ON state. (Default)<br>1 <sub>B</sub> LED0 blinks no matter whether the LED0 is in the ON or OFF state.                 |
| LFDE0  | 12    | RW   | <b>LED0 Full-Duplex Status</b><br>This LFDE0 field controls the LED to show full-duplex status.<br>0 <sub>B</sub> No full-duplex status support. (Default)<br>1 <sub>B</sub> When the PHY link is up and the duplex mode is full-duplex, the LED0 is ON. When the LED also has a blink setting, the blink setting has a higher priority.        |
| LHDE0  | 11    | RW   | <b>LED0 Half-Duplex Status</b><br>This LHDE0 field controls how LED0 indicates half-duplex status.<br>0 <sub>B</sub> Half-duplex mode is not indicated. (Default)<br>1 <sub>B</sub> When the PHY link is up and the duplex mode is half-duplex, LED0 is ON. If the LED also has blink setting, the Blink setting has a higher priority.         |
| LTABE0 | 10    | RW   | <b>LED0 Tx Activity Blink</b><br>This LTABE0 field controls how LED0 indicates Tx activity status.<br>0 <sub>B</sub> Tx activity is not indicated.<br>1 <sub>B</sub> When the PHY link is up and Tx activity occurs, LED0 blinks at the frequency defined in field COM_EXT_LED_BLINK_CFG.LFEQ2 in the COM_EXT_LED_BLINK_CFG register. (Default) |
| LRABE0 | 9     | RW   | <b>LED0 Rx Activity Blink</b><br>This LRABE0 field controls how LED0 indicates Rx activity status.<br>0 <sub>B</sub> Rx activity is not indicated.<br>1 <sub>B</sub> When the PHY link is up and Rx activity occurs LED0 blinks at the frequency defined in field COM_EXT_LED_BLINK_CFG.LFEQ2 in the COM_EXT_LED_BLINK_CFG register. (Default)  |

Extended Register Detailed Description

| Field | Bits | Type | Description (continued)                                                                                                                                                                                                                                                                                                                                                               |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LTAEO | 8    | RW   | <b>LED0 Tx Activity Minimum On Time</b><br>This LTAEO field controls a minimum ON time for LED0 when Tx is active.<br>0 <sub>B</sub> No minimum ON time for LED0 when Tx is active. (Default)<br>1 <sub>B</sub> When the PHY link is up and Tx is active, LED0 is ON for at least 10 ms. If the LED also has a blink setting for Tx activity the blink setting has a higher priority. |
| LRAEO | 7    | RW   | <b>LED0 Rx Activity Minimum On Time</b><br>This LRAEO field controls a minimum ON time for LED0 when Rx is active.<br>0 <sub>B</sub> No minimum ON time for LED0 when Rx is active. (Default)<br>1 <sub>B</sub> When the PHY link is up and Rx is active, LED0 is ON for at least 10 ms. If the LED also has a blink setting for Rx activity the blink setting has a higher priority. |
| LGE0  | 6    | RW   | <b>LED0 1000Base-T Ethernet Link Behavior</b><br>This LGE0 field controls how LED0 indicates 1000 Mbps link speed.<br>0 <sub>B</sub> No change to LED0 behavior. (Default)<br>1 <sub>B</sub> When the PHY link up is and the speed mode is 1000 Mbps, LED0 is ON. If the LED also has a blink setting the blink setting has a higher priority.                                        |
| LFE0  | 5    | RW   | <b>LED0 100Base-T Ethernet Link Behavior</b><br>This LFE0 field controls how LED0 indicates 100 Mbps link speed.<br>0 <sub>B</sub> No change to LED0 behavior. (Default)<br>1 <sub>B</sub> When the PHY link is up and the speed mode is 100 Mbps, LED0 is ON. If the LED also has blink setting the blink setting has a higher priority.                                             |
| LBE0  | 4    | RW   | <b>LED0 10Base-T Ethernet Link Behavior</b><br>This LBE0 field controls how LED0 indicates 10 Mbps link speed.<br>0 <sub>B</sub> No change to LED0 behavior.<br>1 <sub>B</sub> When the PHY link up and the speed mode is 10 Mbps, LED0 is ON. If the LED also has blink setting the blink setting has a higher priority. (Default)                                                   |
| LCBE0 | 3    | RW   | <b>LED0 Collision Behavior</b><br>This LCBE0 field controls how LED0 indicates collisions.<br>0 <sub>B</sub> No change to LED0 behavior. (Default)<br>1 <sub>B</sub> When the PHY link is up and a collision occurs, blink LED0.                                                                                                                                                      |
| LGBE0 | 2    | RW   | <b>LED0 1000Base-T Ethernet Link Blink</b><br>This LGBE0 field controls how LED0 indicates 1000 Mbps link speed.<br>0 <sub>B</sub> No change to LED0 behavior. (Default)<br>1 <sub>B</sub> When the PHY link is up and the speed mode is 1000 Mbps, blink LED0.                                                                                                                       |
| LFBE0 | 1    | RW   | <b>LED0 100Base-T Ethernet Link Blink</b><br>This LFBE0 field controls how LED0 indicates 100 Mbps link speed.<br>0 <sub>B</sub> No change to LED0 behavior. (Default)<br>1 <sub>B</sub> When the PHY link is up and the speed mode is 100 Mbps, blink LED0.                                                                                                                          |

Extended Register Detailed Description

| Field | Bits | Type | Description (continued)                                                                                                                                                                                                                                   |
|-------|------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LBBE0 | 0    | RW   | <b>LED0 10Base-T Ethernet Link Blink</b><br>This LBBE0 field controls how LED0 indicates 10 Mbps link speed.<br>0 <sub>B</sub> No change to LED0 behavior. (Default)<br>1 <sub>B</sub> When the PHY link is up and the speed mode is 10 Mbps, blink LED0. |

## Extended Register Detailed Description

### 7.1.12 LED1 Configuration Register (Register A00D<sub>H</sub>)

This section describes the LED1 Configuration Register in detail.

#### LED1 Configuration Register (Register A00D<sub>H</sub>)

This register configures LED1.

|                                                              |                   |                   |
|--------------------------------------------------------------|-------------------|-------------------|
| COM_EXT_LED1_CFG                                             | Offset            | Reset Value       |
| LED1 Configuration Register<br>(Register A00D <sub>H</sub> ) | A00D <sub>H</sub> | 0620 <sub>H</sub> |

|     |      |       |       |        |        |       |       |      |      |      |       |       |       |       |    |
|-----|------|-------|-------|--------|--------|-------|-------|------|------|------|-------|-------|-------|-------|----|
| 15  | 14   | 13    | 12    | 11     | 10     | 9     | 8     | 7    | 6    | 5    | 4     | 3     | 2     | 1     | 0  |
| RES | LAB1 | LFDE1 | LHDE1 | LTABE1 | LRABE1 | LTAE1 | LRAE1 | LGE1 | LFE1 | LBE1 | LCBE1 | LGBE1 | LFBE1 | LBBE1 |    |
| rw  | rw   | rw    | rw    | rw     | rw     | rw    | rw    | rw   | rw   | rw   | rw    | rw    | rw    | rw    | rw |

| Field  | Bits  | Type | Description                                                                                                                             |
|--------|-------|------|-----------------------------------------------------------------------------------------------------------------------------------------|
| RES    | 15:14 | RW   | <b>Reserved</b>                                                                                                                         |
| LAB1   | 13    | RW   | <b>LED1 Activity Blink Indicator</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> .          |
| LFDE1  | 12    | RW   | <b>LED1 Full-Duplex Status</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> .                |
| LHDE1  | 11    | RW   | <b>LED1 Half-Duplex Status</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> .                |
| LTABE1 | 10    | RW   | <b>LED1 Tx Activity Blink</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 1 <sub>B</sub> .                 |
| LRABE1 | 9     | RW   | <b>LED1 Rx Activity Blink</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 1 <sub>B</sub> .                 |
| LTAE1  | 8     | RW   | <b>LED0 Tx Activity Minimum On Time</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> .       |
| LRAE1  | 7     | RW   | <b>LED1 Rx Activity Minimum On Time</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> .       |
| LGE1   | 6     | RW   | <b>LED1 1000Base-T Ethernet Link Behavior</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> . |
| LFE1   | 5     | RW   | <b>LED1 100Base-T Ethernet Link Behavior</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 1 <sub>B</sub> .  |

Extended Register Detailed Description

| Field | Bits | Type | Description (continued)                                                                                                               |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------------------------|
| LBE1  | 4    | RW   | <b>LED1 10Base-T Ethernet Link Behavior</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> . |
| LCBE1 | 3    | RW   | <b>LED1 Collision Behavior</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> .              |
| LGBE1 | 2    | RW   | <b>LED1 1000Base-T Ethernet Link Blink</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> .  |
| LFBE1 | 1    | RW   | <b>LED1 100Base-T Ethernet Link Blink</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> .   |
| LBBE1 | 0    | RW   | <b>LED1 10Base-T Ethernet Link Blink</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> .    |

## Extended Register Detailed Description

### 7.1.13 LED2 Configuration Register (Register A00E<sub>H</sub>)

This section describes the LED2 Configuration Register in detail.

#### LED2 Configuration Register (Register A00E<sub>H</sub>)

The register controls the LED2 configuration.

|                                                              |                   |                   |
|--------------------------------------------------------------|-------------------|-------------------|
| COM_EXT_LED2_CFG                                             | Offset            | Reset Value       |
| LED2 Configuration Register<br>(Register A00E <sub>H</sub> ) | A00E <sub>H</sub> | 0640 <sub>H</sub> |

|     |      |       |       |        |        |       |       |      |      |      |       |       |       |       |    |
|-----|------|-------|-------|--------|--------|-------|-------|------|------|------|-------|-------|-------|-------|----|
| 15  | 14   | 13    | 12    | 11     | 10     | 9     | 8     | 7    | 6    | 5    | 4     | 3     | 2     | 1     | 0  |
| RES | LAB2 | LFDE2 | LHDE2 | LTABE2 | LRABE2 | LTAE2 | LRAE2 | LGE2 | LFE2 | LBE2 | LCBE2 | LGBE2 | LFBE2 | LBBE2 |    |
| rw  | rw   | rw    | rw    | rw     | rw     | rw    | rw    | rw   | rw   | rw   | rw    | rw    | rw    | rw    | rw |

| Field  | Bits  | Type | Description                                                                                                                             |
|--------|-------|------|-----------------------------------------------------------------------------------------------------------------------------------------|
| RES    | 15:14 | RW   | <b>Reserved</b>                                                                                                                         |
| LAB2   | 13    | RW   | <b>LED2 Activity Blink Indicator</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> .          |
| LFDE2  | 12    | RW   | <b>LED2 Full-Duplex Status</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> .                |
| LHDE2  | 11    | RW   | <b>LED2 Half-Duplex Status</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> .                |
| LTABE2 | 10    | RW   | <b>LED2 Tx Activity Blink</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 1 <sub>B</sub> .                 |
| LRABE2 | 9     | RW   | <b>LED2 Rx Activity Blink</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 1 <sub>B</sub> .                 |
| LTAE2  | 8     | RW   | <b>LED2 Tx Activity Minimum On Time</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> .       |
| LRAE2  | 7     | RW   | <b>LED2 Rx Activity Minimum On Time</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> .       |
| LGE2   | 6     | RW   | <b>LED2 1000Base-T Ethernet Link Behavior</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 1 <sub>B</sub> . |
| LFE2   | 5     | RW   | <b>LED2 100Base-T Ethernet Link Behavior</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> .  |

Extended Register Detailed Description

| Field | Bits | Type | Description (continued)                                                                                                               |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------------------------|
| LBE2  | 4    | RW   | <b>LED2 10Base-T Ethernet Link Behavior</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> . |
| LCBE2 | 3    | RW   | <b>LED2 Collision Behavior</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> .              |
| LGBE2 | 2    | RW   | <b>LED2 1000Base-T Ethernet Link Blink</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> .  |
| LFBE2 | 1    | RW   | <b>LED2 100Base-T Ethernet Link Blink</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> .   |
| LBBE2 | 0    | RW   | <b>LED2 10Base-T Ethernet Link Blink</b><br>Same as LED0. See the COM_EXT_LED0_CFG description.<br>The default is 0 <sub>B</sub> .    |

Extended Register Detailed Description

### 7.1.14 LED Blinking Configuration Register (Register A00F<sub>H</sub>)

This section describes the LED Blinking Configuration Register in detail.

#### LED Blinking Configuration Register (Register A00F<sub>H</sub>)

This register configures the LED blink frequency.

|                                                                      |                   |                   |
|----------------------------------------------------------------------|-------------------|-------------------|
| COM_EXT_LED_BLINK_CFG                                                | Offset            | Reset Value       |
| LED Blinking Configuration Register<br>(Register A00F <sub>H</sub> ) | A00F <sub>H</sub> | 0006 <sub>H</sub> |

|     |  |  |  |  |  |  |   |      |  |       |   |       |   |   |
|-----|--|--|--|--|--|--|---|------|--|-------|---|-------|---|---|
| 15  |  |  |  |  |  |  | 7 | 6    |  | 4     | 3 | 2     | 1 | 0 |
| RES |  |  |  |  |  |  |   | LDTY |  | LFEQ2 |   | LFEQ1 |   |   |
| ro  |  |  |  |  |  |  |   | rw   |  | rw    |   | rw    |   |   |

| Field | Bits | Type | Description                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RES   | 15:7 | RO   | <b>Reserved</b><br>The default is 0 <sub>B</sub> .                                                                                                                                                                                                                                                                                                                                                                  |
| LDTY  | 6:4  | RW   | <b>LED Duty Cycle</b><br>This LDTY field configures the blink duty cycle.<br>000 <sub>B</sub> 50% on and 50% off. (Default)<br>001 <sub>B</sub> 67% on and 33% off.<br>010 <sub>B</sub> 75% on and 25% off.<br>011 <sub>B</sub> 83% on and 17% off.<br>100 <sub>B</sub> 50% on and 50% off.<br>101 <sub>B</sub> 33% on and 67% off.<br>110 <sub>B</sub> 25% on and 75% off.<br>111 <sub>B</sub> 17% on and 83% off. |
| LFEQ2 | 3:2  | RW   | <b>LED Blink Mode 2 Frequency</b><br>This LFEQ2 field configures the blink frequency for blink mode 2.<br>00 <sub>B</sub> 2 Hz<br>01 <sub>B</sub> 4 Hz (Default)<br>10 <sub>B</sub> 8 Hz<br>11 <sub>B</sub> 16 Hz                                                                                                                                                                                                   |
| LFEQ1 | 1:0  | RW   | <b>LED Blink Mode 1 Frequency</b><br>This LFEQ1 field configures the blink frequency for blink mode 1.<br>00 <sub>B</sub> 2 Hz<br>01 <sub>B</sub> 4 Hz<br>10 <sub>B</sub> 8 Hz (Default)<br>11 <sub>B</sub> 16 Hz                                                                                                                                                                                                   |

Extended Register Detailed Description

### 7.1.15 Pin Driving Strength Configuration Register (Register A010<sub>H</sub>)

This section describes the Pin Driving Strength Configuration Register in detail.

#### Pin Driving Strength Configuration Register (Register A010<sub>H</sub>)

This register sets the pin interface's I/O drive strength.

| COM_EXT_PAD_STR_CFG                                                       | Offset            | Reset Value       |
|---------------------------------------------------------------------------|-------------------|-------------------|
| Pin Driving Strength Configuration Register (Register A010 <sub>H</sub> ) | A010 <sub>H</sub> | 6BFF <sub>H</sub> |

|      |    |      |      |      |     |   |    |   |       |   |     |   |    |   |
|------|----|------|------|------|-----|---|----|---|-------|---|-----|---|----|---|
| 15   | 13 | 12   | 11   | 10   | 9   | 8 | 7  | 6 | 5     | 4 | 3   | 2 | 1  | 0 |
| RSDR |    | RSD2 | IODE | IAHL | DSE |   | DM |   | RSD10 |   | DII |   | DL |   |
| rw   |    | rw   | rw   | rw   | rw  |   | rw |   | rw    |   | rw  |   | rw |   |

| Field | Bits  | Type | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|-------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RSDR  | 15:13 | RW   | <b>RGMII Rx Clock Pin Drive Strength</b><br>This RSDR field configures the output drive strength of the RX_CLK pin. Values range from 0 (weakest setting) to 7 (strongest setting).<br>000 <sub>B</sub> Weakest<br>001 <sub>B</sub> Weaker<br>010 <sub>B</sub> Weak<br>011 <sub>B</sub> Default<br>101 <sub>B</sub> Strong<br>110 <sub>B</sub> Stronger<br>111 <sub>B</sub> Strongest                                                                                                                                                                                               |
| RSD2  | 12    | RW   | <b>Drive Strength of RGMII Data and Control</b><br>This RGMII_SW_DR2 field holds bit 2 of the drive strength of the RXD/RX_CTL pin. See COM_EXT_PAD_STR_CFG.RGMII_SW_DR10. The RSD value is formed by combining 1 bit from this field as MSB with the 2 bits from the RSD10 field as LSB into a 3-bit wide value. Values range from 0 (weakest setting) to 7 (strongest setting).<br>000 <sub>B</sub> Weakest<br>001 <sub>B</sub> Weaker<br>010 <sub>B</sub> Weak<br>011 <sub>B</sub> Default<br>101 <sub>B</sub> Strong<br>110 <sub>B</sub> Stronger<br>111 <sub>B</sub> Strongest |
| IODE  | 11    | RW   | <b>Interrupt Output Open Drain Enable</b><br>This IODE field controls the interrupt pin output mode.<br>0 <sub>B</sub> This interrupt pin acts as a push-pull output.<br>1 <sub>B</sub> This interrupt pin acts as open drain.                                                                                                                                                                                                                                                                                                                                                      |
| IAHL  | 10    | RW   | <b>Interrupt Polarity Active High</b><br>This IAHL field configures the interrupt line polarity sensitivity.<br>0 <sub>B</sub> The interrupt line is low-active.<br>1 <sub>B</sub> The interrupt line is high-active.                                                                                                                                                                                                                                                                                                                                                               |

Extended Register Detailed Description

| Field | Bits | Type | Description (continued)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DSE   | 9:8  | RW   | <b>SyncE Pin Drive Strength</b><br>This DSE field configures the output driver strength of the SyncE pin. Values range from 0 (weakest setting) to 3 (strongest setting).<br>00 <sub>B</sub> Weakest<br>01 <sub>B</sub> Weak<br>10 <sub>B</sub> Strong<br>11 <sub>B</sub> Strongest (Default)                                                                                                                                                                                                                                                                                                                                    |
| DM    | 7:6  | RW   | <b>MDIO Pin Drive Strength</b><br>This DM field configures the output driver strength of the MDIO pin. Values range from 0 (weakest setting) to 3 (strongest setting).<br>00 <sub>B</sub> Weakest<br>01 <sub>B</sub> Weak<br>10 <sub>B</sub> Strong<br>11 <sub>B</sub> Strongest (Default)                                                                                                                                                                                                                                                                                                                                       |
| RSD10 | 5:4  | RW   | <b>Drive Strength of RGMII Data and Control</b><br>This RGMII_SW_DR10 field sets the drive strength of the RXD/RX_CTL pin.<br>This field holds bit 1 and bit 0. Bit 2 is held in COM_EXT_PAD_STR_CFG.RGMII_SW_DR2.<br>The RSD value is formed by combining 1 bit from the RSD2 field as MSB with the 2 bits from this field as LSB into a 3-bit wide value.<br>Values range from 0 (weakest setting) to 7 (strongest setting).<br>000 <sub>B</sub> Weakest<br>001 <sub>B</sub> Weaker<br>010 <sub>B</sub> Weak<br>011 <sub>B</sub> Default<br>101 <sub>B</sub> Strong<br>110 <sub>B</sub> Stronger<br>111 <sub>B</sub> Strongest |
| DII   | 3:2  | RW   | <b>Interrupt Pin Drive Strength</b><br>This DII field configures the output drive strength of the interrupt pin. Values range from 0 (weakest setting) to 3 (strongest setting).<br>00 <sub>B</sub> Weakest<br>01 <sub>B</sub> Weak<br>10 <sub>B</sub> Strong<br>11 <sub>B</sub> Strongest (Default)                                                                                                                                                                                                                                                                                                                             |
| DL    | 1:0  | RW   | <b>LED Pin Drive Strength</b><br>Sets the drive strength of GPHY_LED0, GPHY_LED1, and GPHY_LED2.<br>Values range from 0 (weakest setting) to 3 (strongest setting).<br>00 <sub>B</sub> Weakest<br>01 <sub>B</sub> Weak<br>10 <sub>B</sub> Strong<br>11 <sub>B</sub> Strongest (Default)                                                                                                                                                                                                                                                                                                                                          |

Extended Register Detailed Description

### 7.1.16 SyncE Configuration Register (Register A012<sub>H</sub>)

This section describes the SyncE Configuration Register in detail.

#### SyncE Configuration Register (Register A012<sub>H</sub>)

This register controls the SyncE setting.

| COM_EXT_SYNCE_CFG                                             | Offset            | Reset Value       |   |   |   |   |   |    |     |           |     |     |     |
|---------------------------------------------------------------|-------------------|-------------------|---|---|---|---|---|----|-----|-----------|-----|-----|-----|
| SyncE Configuration Register<br>(Register A012 <sub>H</sub> ) | A012 <sub>H</sub> | 00C8 <sub>H</sub> |   |   |   |   |   |    |     |           |     |     |     |
| 15                                                            | 8                 | 7                 | 6 | 5 | 4 | 3 | 1 | 0  |     |           |     |     |     |
| RES                                                           |                   |                   |   |   |   |   |   | PF | ESE | ESED<br>N | CFS | CSS | RES |
| ro                                                            |                   |                   |   |   |   |   |   | rw | rw  | rw        | rw  | rw  | ro  |

| Field | Bits | Type | Description                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RES   | 15:8 | RO   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                       |
| PF    | 7    | RW   | <b>PHY to Fiber</b><br>This PF field controls UTP activation.<br>0 <sub>B</sub> Always enable UTP.<br>1 <sub>B</sub> In UTP to FIBER mode, do not enable UTP until the fiber link is up. (Default)                                                                                                                                                                                                                    |
| ESE   | 6    | RW   | <b>SyncE Output Control</b><br>This ESE field controls the SyncE clock output.<br>0 <sub>B</sub> Disable SyncE clock output.<br>1 <sub>B</sub> Enable SyncE clock output. (Default)                                                                                                                                                                                                                                   |
| ESEDN | 5    | RW   | <b>Enable SyncE Clock Output under No Link</b><br>This ESEDN field controls SyncE clock output behavior in link down state.<br>0 <sub>B</sub> No SyncE clock output when the link is down. (Default)<br>1 <sub>B</sub> Force SyncE clock output when the link is down.                                                                                                                                                |
| CFS   | 4    | RW   | <b>SyncE Clock Frequency Select</b><br>This CFS field selects the clock frequency.<br>0 <sub>B</sub> 25 MHz. (Default)<br>1 <sub>B</sub> 125 MHz.                                                                                                                                                                                                                                                                     |
| CSS   | 3:1  | RW   | <b>SyncE Clock Source Select</b><br>This CSS field selects the clock source for generating SyncE clock output.<br>000 <sub>B</sub> Use the internal 125 MHz PLL as the output clock.<br>001 <sub>B</sub> Use the TPI recovered clock.<br>010 <sub>B</sub> Reserved<br>011 <sub>B</sub> Use the RGMII Tx clock.<br>100 <sub>B</sub> Use the reference 25 MHz clock. (Default)<br>101 <sub>B</sub> Use 25 MHz with SSC. |
| RES   | 0    | RO   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                       |

## Extended Register Detailed Description

### 7.2 UTP Extended Register

This section describes the UTP extended register.

**Table 23 Registers Overview - UTP Extended Register**

| Register Short Name                     | Register Long Name                                              | Reset Value       |
|-----------------------------------------|-----------------------------------------------------------------|-------------------|
| <a href="#">UTP_EXT_10BT_DBG</a>        | 10 M Base-Tc Debug Mode Register (Register 000A <sub>H</sub> )  | 1000 <sub>H</sub> |
| <a href="#">UTP_EXT_SLEEP_CTRL</a>      | Sleep Mode Control Register (Register 0027 <sub>H</sub> )       | E812 <sub>H</sub> |
| <a href="#">UTP_EXT_PKG_RX_VALID_0</a>  | Packet Rx Valid High Register (Register 00A3 <sub>H</sub> )     | 0000 <sub>H</sub> |
| <a href="#">UTP_EXT_PKG_RX_VALID_1</a>  | Packet Rx Valid Low Register (Register 00A4 <sub>H</sub> )      | 0000 <sub>H</sub> |
| <a href="#">UTP_EXT_PKG_RX_OS_0</a>     | Packet Rx Oversize High Register (Register 00A5 <sub>H</sub> )  | 0000 <sub>H</sub> |
| <a href="#">UTP_EXT_PKG_RX_OS_1</a>     | Packet Rx Oversize Low Register (Register 00A6 <sub>H</sub> )   | 0000 <sub>H</sub> |
| <a href="#">UTP_EXT_PKG_RX_US_0</a>     | Packet Rx Undersize High Register (Register 00A7 <sub>H</sub> ) | 0000 <sub>H</sub> |
| <a href="#">UTP_EXT_PKG_RX_US_1</a>     | Packet Rx Undersize Low Register (Register 00A8 <sub>H</sub> )  | 0000 <sub>H</sub> |
| <a href="#">UTP_EXT_PKG_RX_ERR</a>      | Packet Rx CRC Register (Register 00A9 <sub>H</sub> )            | 0000 <sub>H</sub> |
| <a href="#">UTP_EXT_PKG_RX_OS_BAD</a>   | Packet Rx CRC Oversize Register (Register 00AA <sub>H</sub> )   | 0000 <sub>H</sub> |
| <a href="#">UTP_EXT_PKG_RX_FRAGMENT</a> | Packet Rx Fragment Register (Register 00AB <sub>H</sub> )       | 0000 <sub>H</sub> |
| <a href="#">UTP_EXT_PKG_RX_NOSFD</a>    | Packet Rx No SFD Register (Register 00AC <sub>H</sub> )         | 0000 <sub>H</sub> |
| <a href="#">UTP_EXT_PKG_TX_VALID_0</a>  | Packet Tx High Register (Register 00AD <sub>H</sub> )           | 0000 <sub>H</sub> |
| <a href="#">UTP_EXT_PKG_TX_VALID_1</a>  | Packet Tx Low Register (Register 00AE <sub>H</sub> )            | 0000 <sub>H</sub> |
| <a href="#">UTP_EXT_PKG_TX_OS_0</a>     | Packet Tx Oversize High Register (Register 00AF <sub>H</sub> )  | 0000 <sub>H</sub> |
| <a href="#">UTP_EXT_PKG_TX_OS_1</a>     | Packet Tx Oversize Low Register (Register 00B0 <sub>H</sub> )   | 0000 <sub>H</sub> |
| <a href="#">UTP_EXT_PKG_TX_US_0</a>     | Packet Tx Undersize High Register (Register 00B1 <sub>H</sub> ) | 0000 <sub>H</sub> |
| <a href="#">UTP_EXT_PKG_TX_US_1</a>     | Packet Tx Undersize Low Register (Register 00B2 <sub>H</sub> )  | 0000 <sub>H</sub> |
| <a href="#">UTP_EXT_PKG_TX_ERR</a>      | Packet Tx CRC Register (Register 00B3 <sub>H</sub> )            | 0000 <sub>H</sub> |
| <a href="#">UTP_EXT_PKG_TX_OS_BAD</a>   | Packet Tx CRC Oversize Register (Register 00B4 <sub>H</sub> )   | 0000 <sub>H</sub> |
| <a href="#">UTP_EXT_PKG_TX_FRAGMENT</a> | Packet Tx Fragment Register (Register 00B5 <sub>H</sub> )       | 0000 <sub>H</sub> |
| <a href="#">UTP_EXT_PKG_TX_NOSFD</a>    | Packet Tx No SFD Register (Register 00B6 <sub>H</sub> )         | 0000 <sub>H</sub> |

Extended Register Detailed Description

## 7.2.1 10 M Base-Tc Debug Mode Register (Register 000A<sub>H</sub>)

This section describes the 10 M Base-Tc Debug Mode Register in detail.

### 10 M Base-Tc Debug Mode Register (Register 000A<sub>H</sub>)

This register is used for 10 M Base-Tc mode IEEE compliance and external loopback testing.

|                                                                   |                   |                   |
|-------------------------------------------------------------------|-------------------|-------------------|
| UTP_EXT_10BT_DBG                                                  | Offset            | Reset Value       |
| 10 M Base-Tc Debug Mode Register<br>(Register 000A <sub>H</sub> ) | 000A <sub>H</sub> | 1000 <sub>H</sub> |

|      |    |      |  |  |  |  |   |     |      |        |  |   |
|------|----|------|--|--|--|--|---|-----|------|--------|--|---|
| 15   | 14 | 13   |  |  |  |  | 5 | 4   | 3    | 2      |  | 0 |
| RES0 |    | RES1 |  |  |  |  |   | ELB | RES2 | TM10   |  |   |
| ro   |    | rw   |  |  |  |  |   | rw  | rw   | rw SWC |  |   |

| Field | Bits  | Type      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|-------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RES0  | 15:14 | RO        | <b>Reserved</b><br>The default is 0 <sub>B</sub> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| RES1  | 13:5  | RW        | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| ELB   | 4     | RW        | <b>External Loopback Control</b><br>This field enables/disables the external loopback.<br>1 <sub>B</sub> Enable the external loopback.<br>0 <sub>B</sub> Disable the external loopback. (Default)                                                                                                                                                                                                                                                                                                                                                                    |
| RES2  | 3     | RW        | <b>Reserved</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| TM10  | 2:0   | RW<br>SWC | <b>10Base-Tc Ethernet Test Mode</b><br>This field configures the 10Base-Tc test modes.<br>000 <sub>B</sub> Normal operation (Default)<br>101 <sub>B</sub> Normal operation<br>110 <sub>B</sub> Normal operation<br>111 <sub>B</sub> Normal operation<br>001 <sub>B</sub> Used for IEEE harmonic test with 10 MHz sine wave and packets with "all ones".<br>010 <sub>B</sub> Enables a pseudo random packet for TP_IDLE/Jitter/Differential Voltage testing.<br>011 <sub>B</sub> Enables a "normal" link pulse<br>110 <sub>B</sub> Used to generate a 5 MHz sine wave |

Extended Register Detailed Description

## 7.2.2 Sleep Mode Control Register (Register 0027<sub>H</sub>)

This section describes the Sleep Mode Control Register in detail.

### Sleep Mode Control Register (Register 0027<sub>H</sub>)

This register configures the power saving mode.

|                                                              |                   |                   |
|--------------------------------------------------------------|-------------------|-------------------|
| UTP_EXT_SLEEP_CTRL                                           | Offset            | Reset Value       |
| Sleep Mode Control Register<br>(Register 0027 <sub>H</sub> ) | 0027 <sub>H</sub> | E812 <sub>H</sub> |

|     |      |     |      |    |      |   |     |   |      |
|-----|------|-----|------|----|------|---|-----|---|------|
| 15  | 14   | 13  | 12   | 11 | 10   | 6 | 5   | 4 | 0    |
| ESS | PLIS | SPS | RES0 |    | RES1 |   | SLP |   | RES2 |
| rw  | rw   | rw  | rw   |    | ro   |   | ro  |   | ro   |

| Field | Bits  | Type | Description                                                                                                                                                                                                                                                                                                           |
|-------|-------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ESS   | 15    | RW   | <b>Sleep Mode Control</b><br>This field enables/disables the sleep mode feature of the PHY. In sleep mode, the PHY automatically disables AFE when the TPI has no link after a amount of certain time.<br>0 <sub>B</sub> Disables the sleep mode feature.<br>1 <sub>B</sub> Enables the sleep mode feature. (Default) |
| PLIS  | 14    | RW   | <b>Sleep Mode PLL Control</b><br>This field configures the PLL in the sleep mode of the PHY.<br>0 <sub>B</sub> PLL stops in sleep mode. (Default)<br>1 <sub>B</sub> PLL remains active in sleep mode.                                                                                                                 |
| SPS   | 13    | RW   | <b>Sleep Mode Periodic Pulse Control</b><br>This field configures the PHY sending periodic pulse signal in sleep mode.<br>0 <sub>B</sub> Disables sending periodic pulses.<br>1 <sub>B</sub> Enables sending periodic pulses. (Default)                                                                               |
| RES0  | 12:11 | RW   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                       |
| RES1  | 10:6  | RO   | <b>Reserved</b><br>The default is 0 <sub>B</sub> .                                                                                                                                                                                                                                                                    |
| SLP   | 5     | RO   | <b>Sleep Status</b><br>This SLP field reports the status of the PHY.<br>0 <sub>B</sub> PHY is enabled. (Default)<br>1 <sub>B</sub> PHY is in sleep mode.                                                                                                                                                              |
| RES2  | 4:0   | RO   | <b>Reserved</b>                                                                                                                                                                                                                                                                                                       |

## Extended Register Detailed Description

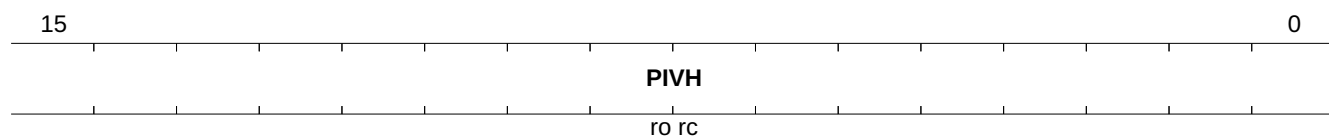
### 7.2.3 Packet Rx Valid High Register (Register 00A3<sub>H</sub>)

This section describes the Packet Rx Valid High Register in detail.

#### Packet Rx Valid High Register (Register 00A3<sub>H</sub>)

This register is used for debugging Rx packets.

| UTP_EXT_PKG_RX_VALID_0                                         | Offset            | Reset Value       |
|----------------------------------------------------------------|-------------------|-------------------|
| Packet Rx Valid High Register<br>(Register 00A3 <sub>H</sub> ) | 00A3 <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type  | Description                                                                                                                                                                                                                                                                                                                     |
|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PIVH  | 15:0 | RO RC | <b>Rx Packet Valid Count High</b><br>This PIVH field reports the number of Rx packets from line to PHY side with correct CRC and a packet length $\geq 64$ bytes and $\leq 1518$ bytes. These are the upper 16-bits of a 32-bit value. The lower 16-bits are in UTP_EXT_PKG_RX_VALID_1.PIVL.<br>The default is 0 <sub>B</sub> . |

## Extended Register Detailed Description

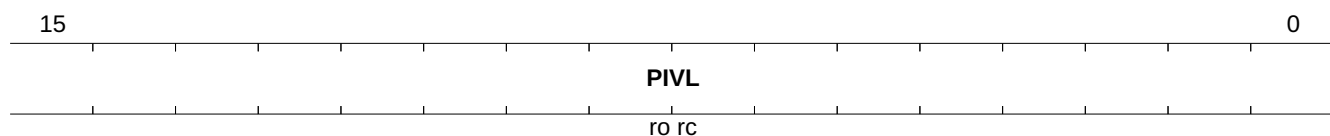
### 7.2.4 Packet Rx Valid Low Register (Register 00A4<sub>H</sub>)

This section describes the Packet Rx Valid Low Register in detail.

#### Packet Rx Valid Low Register (Register 00A4<sub>H</sub>)

This register is used for debugging Rx packets.

|                                                               |                   |                   |
|---------------------------------------------------------------|-------------------|-------------------|
| UTP_EXT_PKG_RX_VALID_1                                        | Offset            | Reset Value       |
| Packet Rx Valid Low Register<br>(Register 00A4 <sub>H</sub> ) | 00A4 <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type  | Description                                                                                                                                                                                                                                                                                                                    |
|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PIVL  | 15:0 | RO RC | <b>Rx Packet Valid Count Low</b><br>This PIVL field reports the number of Rx packets from line to PHY side with correct CRC and a packet length $\geq 64$ bytes and $\leq 1518$ bytes. These are the lower 16-bits of a 32-bit value. The upper 16-bits are in UTP_EXT_PKG_RX_VALID_0.PIVH.<br>The default is 0 <sub>B</sub> . |

## Extended Register Detailed Description

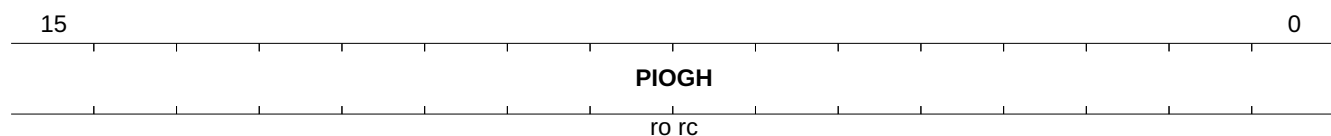
### 7.2.5 Packet Rx Oversize High Register (Register 00A5<sub>H</sub>)

This section describes the Packet Rx Oversize High Register in detail.

#### Packet Rx Oversize High Register (Register 00A5<sub>H</sub>)

This register is used for debugging Rx packets.

|                                                                   |                   |                   |
|-------------------------------------------------------------------|-------------------|-------------------|
| UTP_EXT_PKG_RX_OS_0                                               | Offset            | Reset Value       |
| Packet Rx Oversize High Register<br>(Register 00A5 <sub>H</sub> ) | 00A5 <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type  | Description                                                                                                                                                                                                                                                                                                 |
|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PIOGH | 15:0 | RO RC | <b>Oversize Rx Packet Count High</b><br>This PIOGH field represents the number of Rx packets from line to PHY side with correct CRC and a packet length > 1518 bytes. These are the upper 16-bits of a 32-bit value. The lower 16-bits are in UTP_EXT_PKG_RX_OS_1.PIOGL.<br>The default is 0 <sub>B</sub> . |

Extended Register Detailed Description

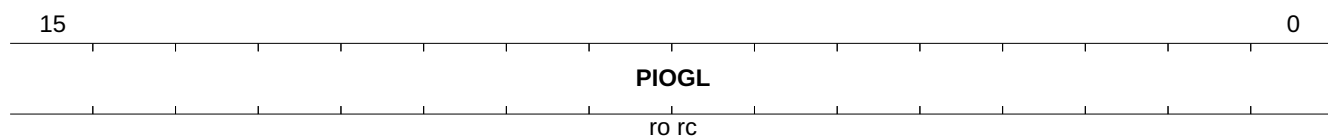
## 7.2.6 Packet Rx Oversize Low Register (Register 00A6<sub>H</sub>)

This section describes the Packet Rx Oversize Low Register in detail.

### Packet Rx Oversize Low Register (Register 00A6<sub>H</sub>)

This register is used for debugging Rx packets.

|                                                                  |                   |                   |
|------------------------------------------------------------------|-------------------|-------------------|
| UTP_EXT_PKG_RX_OS_1                                              | Offset            | Reset Value       |
| Packet Rx Oversize Low Register<br>(Register 00A6 <sub>H</sub> ) | 00A6 <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type  | Description                                                                                                                                                                                                                                                                                                |
|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PIOGL | 15:0 | RO RC | <b>Oversize Rx Packet Count Low</b><br>This PIOGL field represents the number of Rx packets from line to PHY side with correct CRC and a packet length > 1518 bytes. These are the lower 16-bits of a 32-bit value. The upper 16-bits are in UTP_EXT_PKG_RX_OS_0.PIOGH.<br>The default is 0 <sub>B</sub> . |

## Extended Register Detailed Description

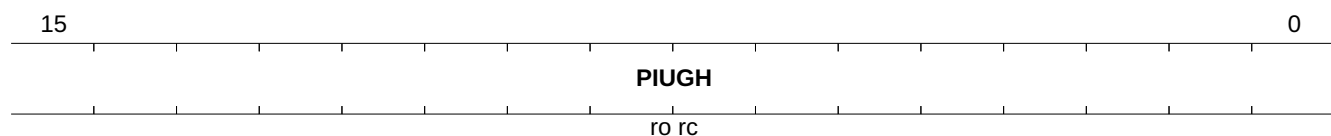
### 7.2.7 Packet Rx Undersize High Register (Register 00A7<sub>H</sub>)

This section describes the Packet Rx Undersize High Register in detail.

#### Packet Rx Undersize High Register (Register 00A7<sub>H</sub>)

This register is used for debugging Rx packets.

| UTP_EXT_PKG_RX_US_0                                                | Offset            | Reset Value       |
|--------------------------------------------------------------------|-------------------|-------------------|
| Packet Rx Undersize High Register<br>(Register 00A7 <sub>H</sub> ) | 00A7 <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type  | Description                                                                                                                                                                                                                                                                                                      |
|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PIUGH | 15:0 | RO RC | <b>Rx Undersize Packet Count High</b><br>This PIUGH field represents the number of Rx packets from line to PHY side with correct CRC and a packet length < 64 bytes. These bytes are the upper 16-bits of a 32-bit value. The lower 16-bits are in UTP_EXT_PKG_RX_US_1.PIUGL.<br>The default is 0 <sub>B</sub> . |

Extended Register Detailed Description

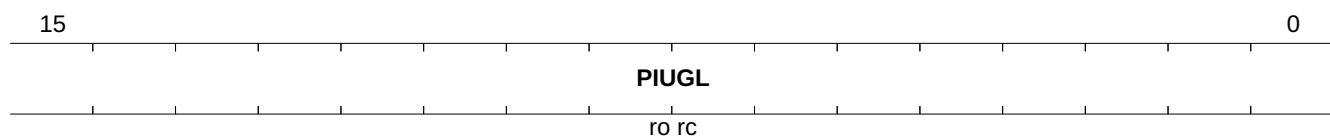
## 7.2.8 Packet Rx Undersize Low Register (Register 00A8<sub>H</sub>)

This section describes the Packet Rx Undersize Low Register in detail.

### Packet Rx Undersize Low Register (Register 00A8<sub>H</sub>)

This register is used for debugging Rx packets.

| UTP_EXT_PKG_RX_US_1                                               | Offset            | Reset Value       |
|-------------------------------------------------------------------|-------------------|-------------------|
| Packet Rx Undersize Low Register<br>(Register 00A8 <sub>H</sub> ) | 00A8 <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type  | Description                                                                                                                                                                                                                                                                                               |
|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PIUGL | 15:0 | RO RC | <b>Rx Undersize Packet Count Low</b><br>This PIUGL field represents the number of Rx packets from line to PHY side with correct CRC and a packet length < 64 bytes. These are the lower 16-bits of a 32-bit value. The upper 16-bits are in UTP_EXT_PKG_RX_US_0.PIUGH.<br>The default is 0 <sub>B</sub> . |

Extended Register Detailed Description

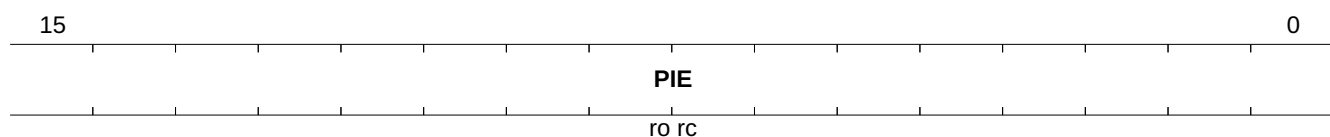
### 7.2.9 Packet Rx CRC Register (Register 00A9<sub>H</sub>)

This section describes the Packet Rx CRC Register in detail.

#### Packet Rx CRC Register (Register 00A9<sub>H</sub>)

This register is used for debugging Rx packets.

| UTP_EXT_PKG_RX_ERR                                   | Offset            | Reset Value       |
|------------------------------------------------------|-------------------|-------------------|
| Packet Rx CRC Register (Register 00A9 <sub>H</sub> ) | 00A9 <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type  | Description                                                                                                                                                                                                            |
|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PIE   | 15:0 | RO RC | <b>Rx Packet Error Count</b><br>This PIE field represents the number of Rx packets from line to PHY side with corrupted CRC and a packet length $\geq 64$ bytes and $\leq 1518$ bytes. The default is 0 <sub>B</sub> . |

## Extended Register Detailed Description

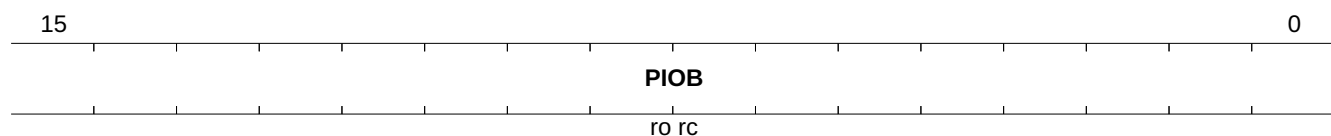
### 7.2.10 Packet Rx CRC Oversize Register (Register 00AA<sub>H</sub>)

This section describes the Packet Rx CRC Oversize Register in detail.

#### Packet Rx CRC Oversize Register (Register 00AA<sub>H</sub>)

This register is used for debugging Rx packets.

|                                                                  |                   |                   |
|------------------------------------------------------------------|-------------------|-------------------|
| UTP_EXT_PKG_RX_OS_BAD                                            | Offset            | Reset Value       |
| Packet Rx CRC Oversize Register<br>(Register 00AA <sub>H</sub> ) | 00AA <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type  | Description                                                                                                                                                                                               |
|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PIOB  | 15:0 | RO RC | <b>Rx Oversize Packet CRC Error Count</b><br>This field represents the number of Rx packets from line to PHY side with corrupted CRC and a packet length > 1518 bytes.<br>The default is 0 <sub>B</sub> . |

Extended Register Detailed Description

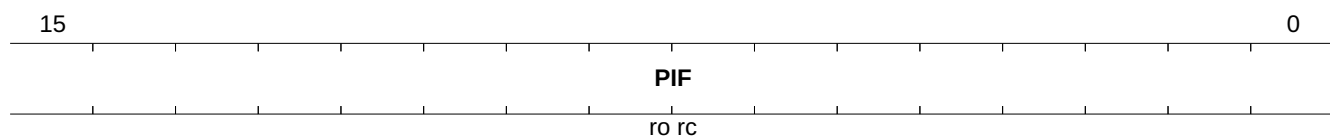
### 7.2.11 Packet Rx Fragment Register (Register 00AB<sub>H</sub>)

This section describes the Packet Rx Fragment Register in detail.

#### Packet Rx Fragment Register (Register 00AB<sub>H</sub>)

This register is used for debugging Rx packets.

|                                                              |                   |                   |
|--------------------------------------------------------------|-------------------|-------------------|
| UTP_EXT_PKG_RX_FRAGMENT                                      | Offset            | Reset Value       |
| Packet Rx Fragment Register<br>(Register 00AB <sub>H</sub> ) | 00AB <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type  | Description                                                                                                                                                                                         |
|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PIF   | 15:0 | RO RC | <b>Rx Fragment Packet Error Count</b><br>This field represents the number of Rx packets from line to PHY side with corrupted CRC and a packet length < 64 bytes.<br>The default is 0 <sub>B</sub> . |

Extended Register Detailed Description

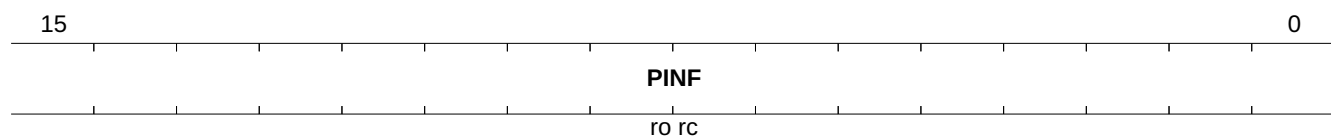
## 7.2.12 Packet Rx No SFD Register (Register 00AC<sub>H</sub>)

This section describes the Packet Rx No SFD Register in detail.

### Packet Rx No SFD Register (Register 00AC<sub>H</sub>)

This register is used for debugging Rx packets.

| UTP_EXT_PKG_RX_NOSFD                                       | Offset            | Reset Value       |
|------------------------------------------------------------|-------------------|-------------------|
| Packet Rx No SFD Register<br>(Register 00AC <sub>H</sub> ) | 00AC <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type  | Description                                                                                                                                                                                                     |
|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PINF  | 15:0 | RO RC | <b>Rx Packet Missing Start Frame Delimiter Count</b><br>This PINF field represents the number of Rx packets from line to PHY side, with missing Start Frame Delimiter (SFD).<br>The default is 0 <sub>B</sub> . |

## Extended Register Detailed Description

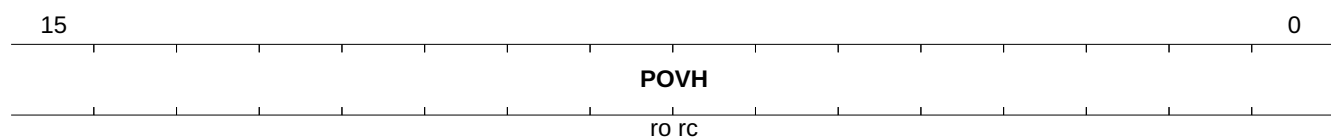
### 7.2.13 Packet Tx High Register (Register 00AD<sub>H</sub>)

This section describes the Packet Tx High Register in detail.

#### Packet Tx High Register (Register 00AD<sub>H</sub>)

This register is used for debugging Tx packets.

| UTP_EXT_PKG_TX_VALID_0                                | Offset            | Reset Value       |
|-------------------------------------------------------|-------------------|-------------------|
| Packet Tx High Register (Register 00AD <sub>H</sub> ) | 00AD <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type  | Description                                                                                                                                                                                                                                                                                                                               |
|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| POVH  | 15:0 | RO RC | <b>Tx Packet Valid Count High</b><br>This POVH field represents the number of Tx packets sending from PHY GMII interface with correct CRC and a packet length $\geq 64$ bytes and $\leq 1518$ bytes. These are the upper 16-bits of a 32-bit value. The lower 16-bits are in UTP_EXT_PKG_TX_VALID_1.POVH. The default is 0 <sub>B</sub> . |

## Extended Register Detailed Description

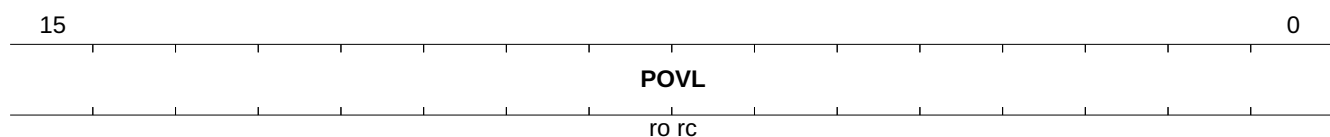
### 7.2.14 Packet Tx Low Register (Register 00AE<sub>H</sub>)

This section describes the Packet Tx Low Register in detail.

#### Packet Tx Low Register (Register 00AE<sub>H</sub>)

This register is used for debugging Tx packets.

| UTP_EXT_PKG_TX_VALID_1                               | Offset            | Reset Value       |
|------------------------------------------------------|-------------------|-------------------|
| Packet Tx Low Register (Register 00AE <sub>H</sub> ) | 00AE <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type  | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| POVL  | 15:0 | RO RC | <b>Tx Packet Valid Count Low</b><br>This POVL field represents the number of Tx packets from PHY GMII interface with correct CRC and a packet length $\geq 64$ bytes and $\leq 1518$ bytes. These are the lower 16-bit of a 32-bit value. The higher 16-bit are in the field UTP_EXT_PKG_TX_VALID_0.POVH.<br>The default is 0 <sub>B</sub> . |

## Extended Register Detailed Description

### 7.2.15 Packet Tx Oversize High Register (Register 00AF<sub>H</sub>)

This section describes the Packet Tx Oversize High Register in detail.

#### Packet Tx Oversize High Register (Register 00AF<sub>H</sub>)

This register is used for debugging Tx packets.

| UTP_EXT_PKG_TX_OS_0                                               | Offset            | Reset Value       |
|-------------------------------------------------------------------|-------------------|-------------------|
| Packet Tx Oversize High Register<br>(Register 00AF <sub>H</sub> ) | 00AF <sub>H</sub> | 0000 <sub>H</sub> |
| 15                                                                |                   | 0                 |
| POOGH                                                             |                   |                   |
| ro rc                                                             |                   |                   |

| Field | Bits | Type  | Description                                                                                                                                                                                                                                                                                                   |
|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| POOGH | 15:0 | RO RC | <b>Oversize Tx Packet Count High</b><br>This POOGH field represents the number of Tx packets from PHY GMII interface with correct CRC and a packet length > 1518 bytes. These are the upper 16-bits of a 32-bit value. The lower 16-bits are in UTP_EXT_PKG_TX_OS_1.POUGL.<br>The default is 0 <sub>B</sub> . |

Extended Register Detailed Description

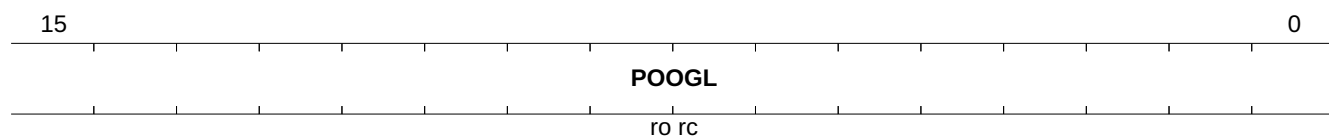
## 7.2.16 Packet Tx Oversize Low Register (Register 00B0<sub>H</sub>)

This section describes the Packet Tx Oversize Low Register in detail.

### Packet Tx Oversize Low Register (Register 00B0<sub>H</sub>)

This register is used for debugging Tx packets.

|                                                                  |                   |                   |
|------------------------------------------------------------------|-------------------|-------------------|
| UTP_EXT_PKG_TX_OS_1                                              | Offset            | Reset Value       |
| Packet Tx Oversize Low Register<br>(Register 00B0 <sub>H</sub> ) | 00B0 <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type  | Description                                                                                                                                                                                                                                                                                                  |
|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| POOGL | 15:0 | RO RC | <b>Oversize Tx Packet Count Low</b><br>This POOGL field represents the number of Tx packets from PHY GMII interface with correct CRC and a packet length > 1518 bytes. These are the lower 16-bits of a 32-bit value. The upper 16-bits are in UTP_EXT_PKG_TX_OS_0.POOGH.<br>The default is 0 <sub>B</sub> . |

Extended Register Detailed Description

## 7.2.17 Packet Tx Undersize High Register (Register 00B1<sub>H</sub>)

This section describes the Packet Tx Undersize High Register in detail.

### Packet Tx Undersize High Register (Register 00B1<sub>H</sub>)

This register is used for debugging Tx packets.

| UTP_EXT_PKG_TX_US_0                                                | Offset            | Reset Value       |
|--------------------------------------------------------------------|-------------------|-------------------|
| Packet Tx Undersize High Register<br>(Register 00B1 <sub>H</sub> ) | 00B1 <sub>H</sub> | 0000 <sub>H</sub> |
| 15                                                                 |                   | 0                 |
| POUGH                                                              |                   |                   |
| ro rc                                                              |                   |                   |

| Field | Bits | Type  | Description                                                                                                                                                                                                                                                                                                  |
|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| POUGH | 15:0 | RO RC | <b>Tx Undersize Packet Count High</b><br>This POUGH field represents the number of Tx packets from PHY GMII interface with correct CRC and a packet length < 64 bytes. These are the upper 16-bits of a 32-bit value. The lower 16-bits are in UTP_EXT_PKG_TX_US_1.POUGL.<br>The default is 0 <sub>B</sub> . |

Extended Register Detailed Description

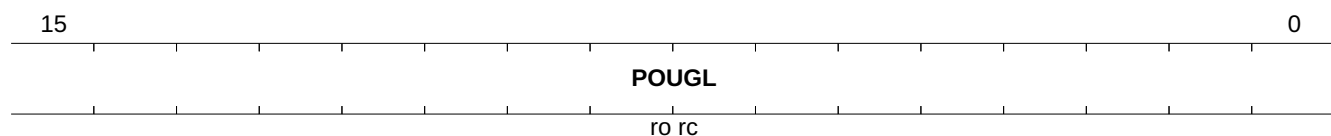
## 7.2.18 Packet Tx Undersize Low Register (Register 00B2<sub>H</sub>)

This section describes the Packet Tx Undersize Low Register in detail.

### Packet Tx Undersize Low Register (Register 00B2<sub>H</sub>)

This register is used for debugging Tx packets.

| UTP_EXT_PKG_TX_US_1                                               | Offset            | Reset Value       |
|-------------------------------------------------------------------|-------------------|-------------------|
| Packet Tx Undersize Low Register<br>(Register 00B2 <sub>H</sub> ) | 00B2 <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type  | Description                                                                                                                                                                                                                                                                                                 |
|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| POUGL | 15:0 | RO RC | <b>Tx Undersize Packet Count Low</b><br>This POUGL field represents the number of Tx packets from PHY GMII interface with correct CRC and a packet length < 64 bytes. These are the lower 16-bits of a 32-bit value. The upper 16-bits are in UTP_EXT_PKG_TX_US_0.POUGH.<br>The default is 0 <sub>B</sub> . |

Extended Register Detailed Description

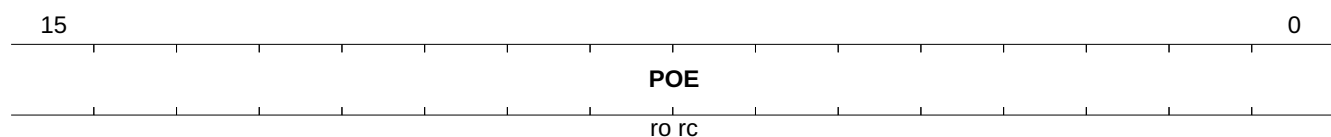
### 7.2.19 Packet Tx CRC Register (Register 00B3<sub>H</sub>)

This section describes the Packet Tx CRC Register in detail.

#### Packet Tx CRC Register (Register 00B3<sub>H</sub>)

This register is used for debugging Tx packets.

| UTP_EXT_PKG_TX_ERR                                   | Offset            | Reset Value       |
|------------------------------------------------------|-------------------|-------------------|
| Packet Tx CRC Register (Register 00B3 <sub>H</sub> ) | 00B3 <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type  | Description                                                                                                                                                                                                             |
|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| POE   | 15:0 | RO RC | <b>Tx Packet Error Count</b><br>This POE field represents the number of Tx packets from PHY GMII interface with wrong CRC and a packet length $\geq 64$ bytes and $\leq 1518$ bytes.<br>The default is 0 <sub>B</sub> . |

Extended Register Detailed Description

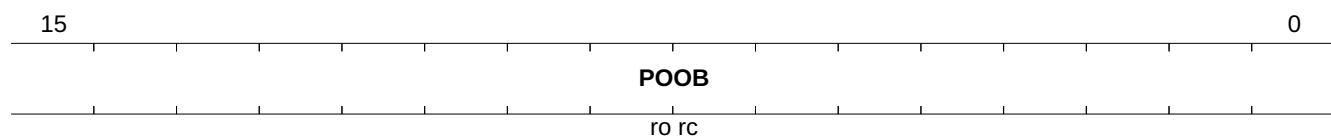
## 7.2.20 Packet Tx CRC Oversize Register (Register 00B4<sub>H</sub>)

This section describes the Packet Tx CRC Oversize Register in detail.

### Packet Tx CRC Oversize Register (Register 00B4<sub>H</sub>)

This register is used for debugging Tx packets.

|                                                                  |                   |                   |
|------------------------------------------------------------------|-------------------|-------------------|
| UTP_EXT_PKG_TX_OS_BAD                                            | Offset            | Reset Value       |
| Packet Tx CRC Oversize Register<br>(Register 00B4 <sub>H</sub> ) | 00B4 <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type  | Description                                                                                                                                                                                                  |
|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| POOB  | 15:0 | RO RC | <b>Tx Oversize Packet CRC Error Count</b><br>This POOB field represents the number of Tx packets from PHY GMII interface with wrong CRC and a packet length > 1518 bytes.<br>The default is 0 <sub>B</sub> . |

Extended Register Detailed Description

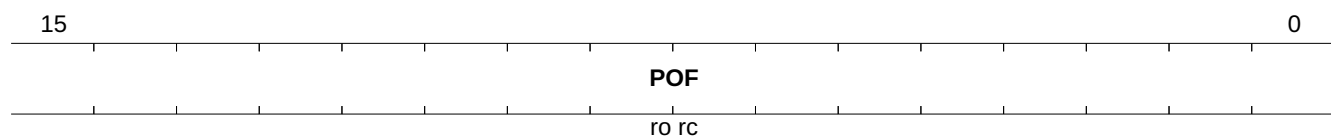
## 7.2.21 Packet Tx Fragment Register (Register 00B5<sub>H</sub>)

This section describes the Packet Tx Fragment Register in detail.

### Packet Tx Fragment Register (Register 00B5<sub>H</sub>)

This register is used for debugging Tx packets.

| UTP_EXT_PKG_TX_FRAGMENT                                      | Offset            | Reset Value       |
|--------------------------------------------------------------|-------------------|-------------------|
| Packet Tx Fragment Register<br>(Register 00B5 <sub>H</sub> ) | 00B5 <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type  | Description                                                                                                                                                                             |
|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| POF   | 15:0 | RO RC | <b>Tx Fragment Packet Error Count</b><br>This POF field represents the number of Tx packets from PHY GMII interface with a packet length < 64 bytes.<br>The default is 0 <sub>B</sub> . |

## Extended Register Detailed Description

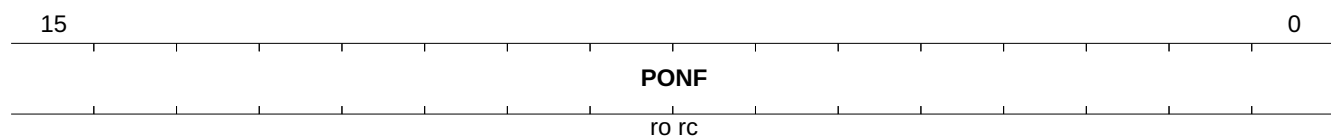
### 7.2.22 Packet Tx No SFD Register (Register 00B6<sub>H</sub>)

This section describes the Packet Tx No SFD Register in detail.

#### Packet Tx No SFD Register (Register 00B6<sub>H</sub>)

This register is used for debugging Tx packets.

| UTP_EXT_PKG_TX_NOSFD                                       | Offset            | Reset Value       |
|------------------------------------------------------------|-------------------|-------------------|
| Packet Tx No SFD Register<br>(Register 00B6 <sub>H</sub> ) | 00B6 <sub>H</sub> | 0000 <sub>H</sub> |



| Field | Bits | Type  | Description                                                                                                                                                                               |
|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PONF  | 15:0 | RO RC | <b>Tx Packet Missing Start Frame Delimiter Count</b><br>This PONF field represents the number of Tx packets from PHY GMII interface, with missing SFD.<br>The default is 0 <sub>B</sub> . |

## 8 Electrical Characteristics

This chapter provides the electrical characteristics for the MxL86110.

### 8.1 Absolute Maximum Ratings

**Table 24** provides the absolute maximum ratings.

**Table 24 Absolute Maximum Ratings**

| Parameter                           | Symbol            | Values |      | Unit | Note / Test Condition                                                                                                                                                                                                                                                                                            |
|-------------------------------------|-------------------|--------|------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                     |                   | Min.   | Max. |      |                                                                                                                                                                                                                                                                                                                  |
| Storage Temperature Limits          | T <sub>STG</sub>  | –      | 40   | °C   | Devices must be stored according to these criteria: <ul style="list-style-type: none"> <li>The temperature must be less than 40 °C.</li> <li>The relative humidity must be less than 90%. Before removing the devices from the moisture barrier bag, ensure that there is no condensation in the air.</li> </ul> |
| Soldering Temperature               | T <sub>SOL</sub>  | –      | 260  | °C   | Solder the devices with lead-free (Pb) solder that complies with J-STD-020D                                                                                                                                                                                                                                      |
| Moisture Level 3 Temperature Limits | T <sub>ML3</sub>  | –      | 260  | °C   | According to IPS J-STD 020                                                                                                                                                                                                                                                                                       |
| Absolute Junction Temperature       | T <sub>JABS</sub> | –      | 125  | °C   | –                                                                                                                                                                                                                                                                                                                |
| VDD3V3/VDDDAV3                      | V <sub>max</sub>  | -0.3   | 3.7  | V    | –                                                                                                                                                                                                                                                                                                                |
| VDDA1V1/VDD                         | V <sub>max</sub>  | -0.2   | 1.4  | V    | –                                                                                                                                                                                                                                                                                                                |
| 2.5 V RGMII                         | V <sub>max</sub>  | -0.3   | 2.8  | V    | –                                                                                                                                                                                                                                                                                                                |
| 1.8 V RGMII                         | V <sub>max</sub>  | -0.3   | 2.3  | V    | –                                                                                                                                                                                                                                                                                                                |
| 3.3 V DC Input                      | V <sub>max</sub>  | -0.3   | 3.7  | V    | –                                                                                                                                                                                                                                                                                                                |
| VDD/VDDA1V1 DC Input                | V <sub>max</sub>  | -0.3   | 1.4  | V    | –                                                                                                                                                                                                                                                                                                                |

**Attention:** Stresses above the maximum values listed in this table may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the device.

## 8.2 Operating Range

**Table 25** defines the maximum values of voltages and temperature that must be applied to guarantee proper operation of the Gigabit Ethernet PHY. The values are relative to a ground voltage source supply (VSS) of 0.0 V.

**Table 25 Supply Voltage and Temperature**

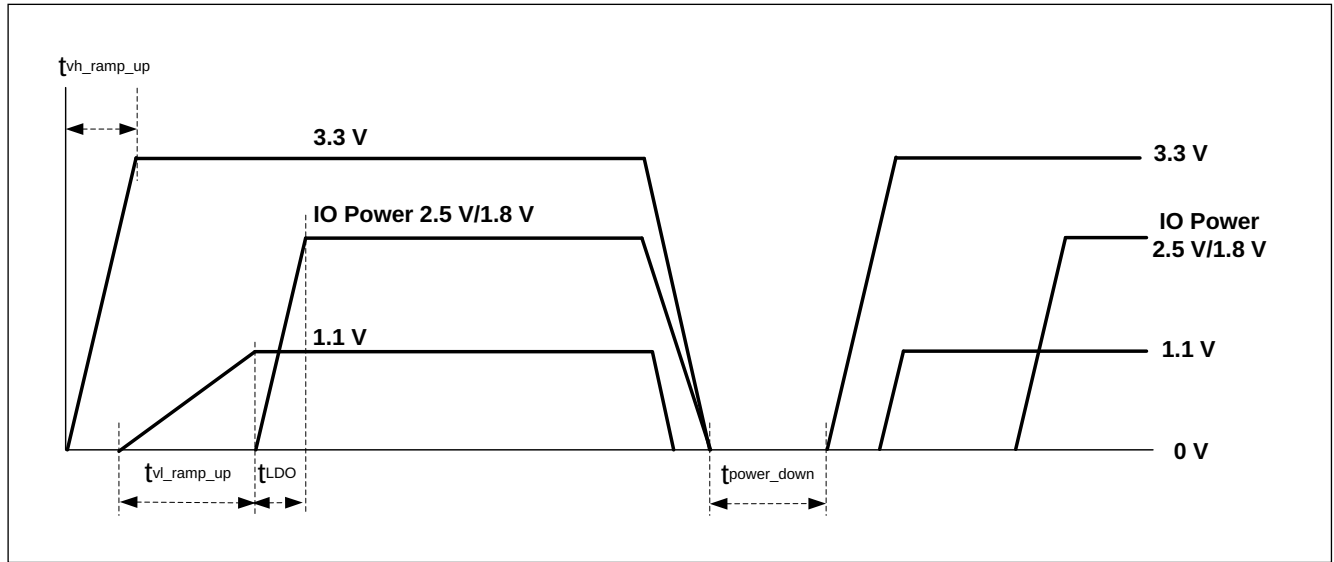
| Parameter                               | Symbol            | Values |      |      | Unit | Note / Test Condition |
|-----------------------------------------|-------------------|--------|------|------|------|-----------------------|
|                                         |                   | Min.   | Typ. | Max. |      |                       |
| VDD3V3/VDDDAV3                          | V <sub>max</sub>  | 3.14   | 3.3  | 3.63 | V    | —                     |
| VDDA1V1/VDD                             | V <sub>max</sub>  | 1.045  | 1.1  | 1.32 | V    | —                     |
| 2.5 V RGMII                             | V <sub>max</sub>  | 2.25   | 2.5  | 2.75 | V    | —                     |
| 1.8 V RGMII                             | V <sub>max</sub>  | 1.62   | 1.8  | 1.98 | V    | —                     |
| Maximum Operating Junction Temperature  | T <sub>JMAX</sub> | —      | —    | 125  | °C   | —                     |
| 3.3 V Minimum High Level Output Voltage | V <sub>OH</sub>   | 2.4    | —    | 3.63 | V    | —                     |
| 3.3 V Maximum Low Level Output Voltage  | V <sub>OL</sub>   | -0.3   | —    | 0.4  | V    | —                     |
| 2.5 V Minimum High Level Output Voltage | V <sub>OH</sub>   | 2      | —    | 2.8  | V    | —                     |
| 2.5 V Maximum Low Level Output Voltage  | V <sub>OL</sub>   | -0.3   | —    | 0.4  | V    | —                     |
| 1.8 V Minimum High Level Output Voltage | V <sub>OH</sub>   | 1.62   | —    | 2.1  | V    | —                     |
| 1.8 V Maximum Low Level Output Voltage  | V <sub>OL</sub>   | -0.3   | —    | 0.4  | V    | —                     |
| 3.3 V Minimum High Level Input Voltage  | V <sub>IH</sub>   | 2      | —    | —    | V    | —                     |
| 3.3 V Maximum Low Level Input Voltage   | V <sub>IL</sub>   | —      | —    | 0.8  | V    | —                     |
| 2.5 V Minimum High Level Input Voltage  | V <sub>IH</sub>   | 1.7    | —    | —    | V    | —                     |
| 2.5 V Maximum Low Level Input Voltage   | V <sub>IL</sub>   | —      | —    | 0.7  | V    | —                     |
| 1.8 V Minimum High Level Input Voltage  | V <sub>IH</sub>   | 1.2    | —    | —    | V    | —                     |
| 1.8 V Maximum Low Level Input Voltage   | V <sub>IL</sub>   | —      | —    | 0.5  | V    | —                     |

## 8.3 AC Characteristics

The following sections describe the AC characteristics of the external interfaces as well as the power up and power down sequence.

### 8.3.1 Power Up and Power Down Sequence

Figure 13 shows the power up and power down sequence.



**Figure 13** Power Up and Power Down Sequence

*Note: When 1.1 V in external supply mode, the sequence for 3.3 V and 1.1 V are able to be powered up at the same time. The 1.1 V power supply must always be lower than 3.3 V power supply.*

**Table 26** Sequence Timing Parameters

| Parameter                           | Symbol      | Values |      |      | Unit | Note / Test Condition |
|-------------------------------------|-------------|--------|------|------|------|-----------------------|
|                                     |             | Min.   | Typ. | Max. |      |                       |
| 3.3 V Rising Time                   | Tvh_ramp_up | 0.5    | —    | —    | ms   | —                     |
| 3.3 V and 1.1 V Power-Down Duration | Tpower_down | 100    | —    | —    | ms   | —                     |
| Core Power 1.1 V Ready Time         | Tvl_ramp_up | —      | —    | 2.5  | ms   | —                     |
| Internal LDO Ready Time             | TLDO        | —      | —    | 100  | us   | —                     |

### 8.3.2 Power Supply Rail Requirements

The maximum noise per power rail must be under these limits:

- 3.3 V: < 100 mV peak-to-peak
- VDD (1.1 V): < 80 mV peak-to-peak
- VDDA (1.1 V): < 50 mV peak-to-peak

### 8.3.3 Device Power Consumption

Table 27 and Table 28 show the power consumption for the MxL86110.

Power consumption at 25 °C ambient temperature is indicated in Table 27 for the different modes. The link-up conditions are full-speed, bidirectional, and full-duplex. Power numbers are indicated for internal DCDC SVR.

**Table 27 Device Power Consumption**

| Condition<br>25 °C<br>100 m Cable | VDDP3V3<br>(mA) | VDD3V3<br>(mA) | VDDA3V3<br>(mA) | Power Consumption<br>(mW) |
|-----------------------------------|-----------------|----------------|-----------------|---------------------------|
| Link Down                         | 1               | 7              | 21              | 95.7                      |
| Link Up at 1000 Mbps              | 13              | 51             | 61              | 412.5                     |
| Traffic at 1000 Mbps              | 28              | 57             | 61              | 481.8                     |

Note: Test by typical corner chip with VDDP3V3/VDD3V3/VDDA3V3 = 3.3 V and VDD/VDDA1V1 = 1.1 V under room temperature.

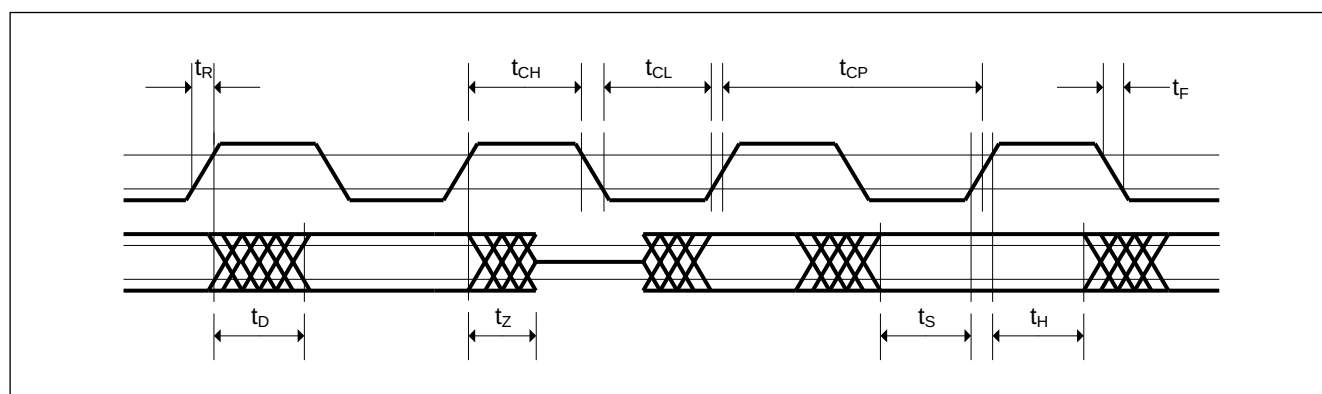
**Table 28 Maximum Device Power Consumption**

| Condition<br>85 °C<br>100 m Cable | VDDP3V3<br>(mA) | VDD3V3<br>(mA) | VDDA3V3<br>(mA) | Power Consumption<br>(mW) |
|-----------------------------------|-----------------|----------------|-----------------|---------------------------|
| Traffic at 1000 Mbps              | 30.8            | 62.7           | 67.1            | 530                       |

Note: Test by fast corner chip with VDDP3V3/VDD3V3/VDDA3V3 = 3.3 V and VDD/VDDA1V1 = 1.1 V at 85 °C.

### 8.3.4 MDIO Interface

Figure 14 shows a timing diagram of the slave MDIO interface for a clock cycle in the read, write, and turnaround modes. The timing measurements are annotated. The defined absolute values are summarized in Table 29.



**Figure 14 Timing Diagram for the MDIO Interface**

Electrical Characteristics

**Table 29** Timing Characteristics of the MDIO Interface

| Parameter                         | Symbol   | Values |      |      | Unit | Note / Test Condition                                                                  |
|-----------------------------------|----------|--------|------|------|------|----------------------------------------------------------------------------------------|
|                                   |          | Min.   | Typ. | Max. |      |                                                                                        |
| MDC High Time                     | $t_{CH}$ | 32.0   | –    | –    | ns   | All provided timings were captured from a probe attached to the MDC pin of the device. |
| MDC Low Time                      | $t_{CL}$ | 32.0   | –    | –    | ns   |                                                                                        |
| MDC Clock Period                  | $t_{CP}$ | 80.0   | –    | –    | ns   |                                                                                        |
| MDC Clock Frequency <sup>1)</sup> | $t_{CP}$ | –      | 2.5  | 12.5 | MHz  |                                                                                        |
| MDC Rise Time                     | $t_R$    | –      | –    | 10.0 | ns   |                                                                                        |
| MDC Fall Time                     | $t_F$    | –      | –    | 10.0 | ns   |                                                                                        |
| MDIO Input Setup Time             | $t_S$    | 10.0   | –    | –    | ns   | Gigabit Ethernet PHY receive                                                           |
| MDIO Input Hold Time              | $t_H$    | 10.0   | –    | –    | ns   | Gigabit Ethernet PHY receive                                                           |
| MDIO Output Delay Time            | $t_D$    | 0.0    | –    | 20   | ns   | Gigabit Ethernet PHY transmit                                                          |
| MDIO Output Setup Time            | $t_S$    | 10.0   | –    | –    | ns   | MAC transmit                                                                           |
| MDIO Output Hold Time             | $t_H$    | 10.0   | –    | –    | ns   | MAC transmit                                                                           |

1) MDC clock supports range of frequencies up to 12.5 MHz. The typical (and default) frequency is 2.5 MHz.

### 8.3.5 RGMII Interface

This section describes the AC characteristics of the RGMII interface on the MxL86110. This interface conforms to the RGMII specification version 1.3 and version 2.0, as defined in [2] and [3] respectively. The RGMII interface operates at speeds of 10 Mbit/s, 100 Mbit/s, or 1000 Mbit/s.

#### 8.3.5.1 Transmit Timing Characteristics

Figure 15 shows the timing diagram of the transmit RGMII interface on the MxL86110. Table 30 provides the RGMII timing requirements. Note the data and control signals are clocked in using the internal delayed version of the TX\_CLK which is the external clock delayed by the integrated delay. The delay is adjustable in steps of 0.15 ns. This amount is configurable using the COM\_EXT\_RGMII\_CFG1 register. See Section 7.1. An additional 2 ns of delay is available via pin strapping. See Section 3.16.

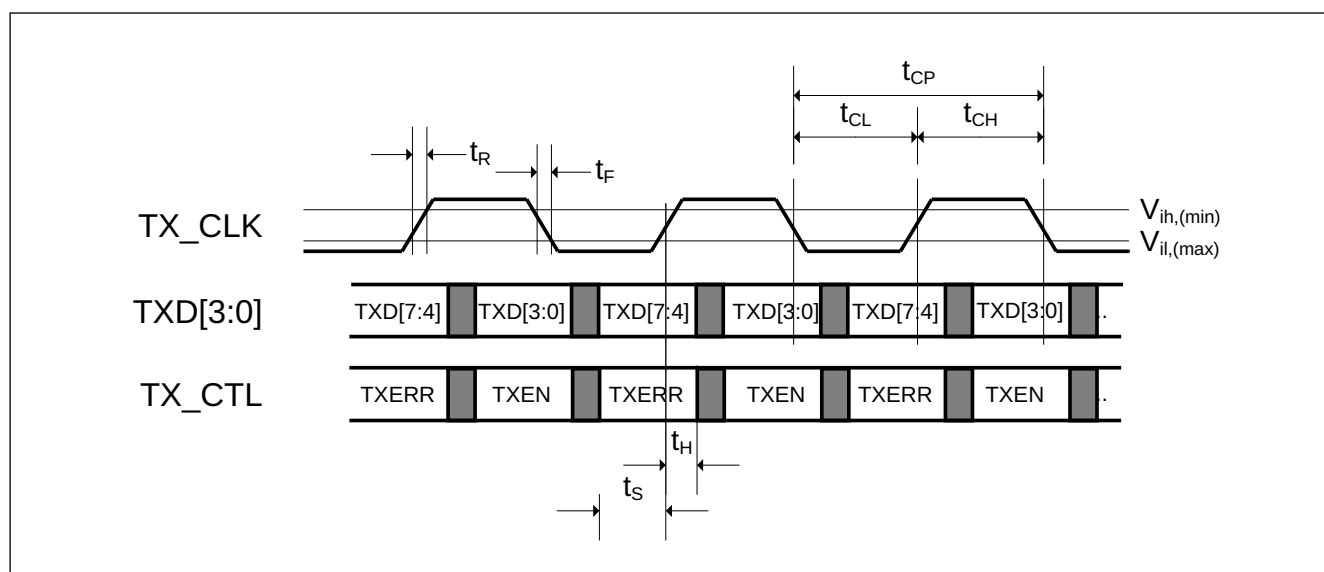


Figure 15 RGMII Transmit Timing Diagram

Table 30 RGMII Transmit Timing Characteristics

| Parameter                                 | Symbol                               | Values  |       |         | Unit | Note / Test Condition |
|-------------------------------------------|--------------------------------------|---------|-------|---------|------|-----------------------|
|                                           |                                      | Min.    | Typ.  | Max.    |      |                       |
| Transmit Clock Frequency (TX_CLK)         | $f_{TX\_CLK}$                        | -50 ppm | 125.0 | +50 ppm | MHz  | For 1000 Mbit/s speed |
|                                           |                                      |         | 25.0  |         | MHz  | For 100 Mbit/s speed  |
|                                           |                                      |         | 2.5   |         | MHz  | For 10 Mbit/s speed   |
| Transmit Clock Period (TX_CLK)            | $t_{CP}$                             | 7.2     | 8.0   | 8.8     | ns   | For 1000 Mbit/s speed |
|                                           |                                      | 36.0    | 40.0  | 44.0    | ns   | For 100 Mbit/s speed  |
|                                           |                                      | 360.0   | 400.0 | 440.0   | ns   | For 10 Mbit/s speed   |
| Duty Cycle                                | $t_{CH}/t_{CP}$ ,<br>$t_{CL}/t_{CP}$ | 45.0    | 50.0  | 55.0    | %    | Speed-independent     |
| Transmit Clock Rise Time (TX_CLK)         | $t_R$                                | —       | —     | 750.0   | ps   | 20%→80%               |
| Transmit Clock Fall Time (TX_CLK)         | $t_F$                                | —       | —     | 750.0   | ps   | 80%→20%               |
| Setup Time to $\uparrow\downarrow$ TX_CLK | $t_S$                                | 1.0     | —     | —       | ns   | —                     |
| Hold Time to $\uparrow\downarrow$ TX_CLK  | $t_H$                                | 1.0     | —     | —       | ns   | —                     |

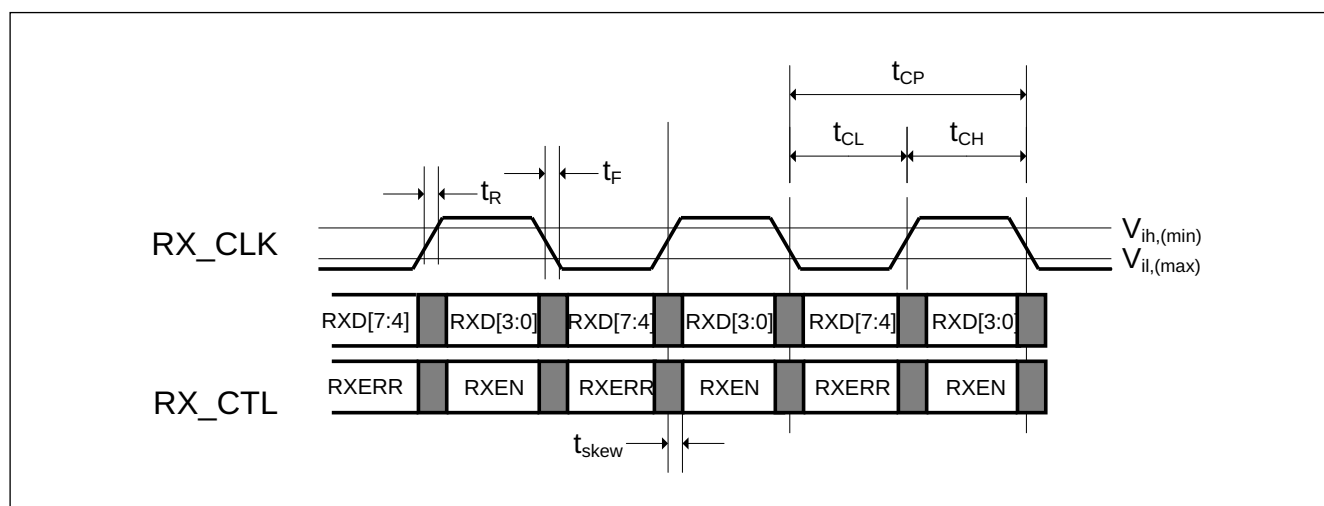
## Electrical Characteristics

**Table 30 RGMII Transmit Timing Characteristics** (continued)

| Parameter                       | Symbol   | Values |        |      | Unit | Note / Test Condition             |
|---------------------------------|----------|--------|--------|------|------|-----------------------------------|
|                                 |          | Min.   | Typ.   | Max. |      |                                   |
| Integrated Transmit Clock Delay | $t_{ID}$ | 0.0    | k*0.15 | 4.25 | ns   | Adjustable via COM_EXT_RGMII_CFG1 |

### 8.3.5.2 Receive Timing Characteristics

**Figure 16** shows the timing diagram of the receive RGMII interface on the MxL86110. It is referred to by **Table 31**, which specifies the timing requirements. The external clock on the pin is delayed by the integrated delay, which is adjustable in steps of 0.15 ns. This amount is configurable using the COM\_EXT\_RGMII\_CFG1 register. See **Section 7.1**. An additional 2 ns of delay is available via pin strapping. See **Section 3.16**. If the integrated delay is not used it must be set to zero, in which case all the timings are related directly to the RX\_CLK on the pin.



**Figure 16 RGMII Receive Timing Diagram**

**Table 31 RGMII Receive Timing Characteristics**

| Parameter                        | Symbol                         | Values  |       |         | Unit | Note / Test Condition |
|----------------------------------|--------------------------------|---------|-------|---------|------|-----------------------|
|                                  |                                | Min.    | Typ.  | Max.    |      |                       |
| Receive Clock Frequency (RX_CLK) | $f_{RX\_CLK}$                  | -50 ppm | 125.0 | +50 ppm | MHz  | For 1000 Mbit/s speed |
|                                  |                                |         | 25.0  |         | MHz  | For 100 Mbit/s speed  |
|                                  |                                |         | 2.5   |         | MHz  | For 10 Mbit/s speed   |
| Receive Clock Period (RX_CLK)    | $t_{CP}$                       | 7.2     | 8.0   | 8.8     | ns   | For 1000 Mbit/s speed |
|                                  |                                | 36      | 40.0  | 46      | ns   | For 100 Mbit/s speed  |
|                                  |                                | 360     | 400.0 | 460     | ns   | For 10 Mbit/s speed   |
| Duty Cycle                       | $t_{CH}/t_{CP}, t_{CL}/t_{CP}$ | 45.0    | 50.0  | 55.0    | %    | Speed-independent     |
| Receive Clock Rise Time (TX_CLK) | $t_R$                          | —       | —     | 750.0   | ps   | 20% → 80%             |
| Receive Clock Fall Time (TX_CLK) | $t_F$                          | —       | —     | 750.0   | ps   | 80% → 20%             |

Electrical Characteristics

**Table 31** RGMII Receive Timing Characteristics (continued)

| Parameter                      | Symbol            | Values |        |      | Unit | Note / Test Condition                                            |
|--------------------------------|-------------------|--------|--------|------|------|------------------------------------------------------------------|
|                                |                   | Min.   | Typ.   | Max. |      |                                                                  |
| Clock-to-Data Skew             | $t_{\text{skew}}$ | -0.5   | 0.0    | 0.5  | ns   | The skew between the RXC and RXC/RX_CTL must be less than 500 ps |
| Integrated Receive Clock Delay | $t_{\text{ID}}$   | 0.0    | k*0.15 | 4.25 | ns   | Adjustable via COM_EXT_RGMII_CF G1 and the RXDLY pin strapping   |

### 8.3.6 Crystal Specification

The 25 MHz crystal must follow the specification given in [Table 32](#).

**Table 32** Specification of the Crystal

| Parameter                               | Symbol      | Values |      |      | Unit     | Note / Test Condition |
|-----------------------------------------|-------------|--------|------|------|----------|-----------------------|
|                                         |             | Min.   | Typ. | Max. |          |                       |
| Frequency with 25 MHz Input             | $f_{clk25}$ | –      | 25.0 | –    | MHz      | –                     |
| Total Frequency Stability <sup>1)</sup> | –           | -50    | –    | +50  | ppm      | –                     |
| Series Resonant Resistance              | –           | –      | –    | 50   | $\Omega$ | –                     |
| Drive Level                             | –           | –      | –    | 0.5  | mW       | –                     |
| Crystal Output High Level               | $V_{ih}$    | 1.4    | –    | –    | V        | –                     |
| Crystal Output Low Level                | $V_{il}$    | –      | –    | 0.7  | V        | –                     |

1) Total frequency stability refers to the sum all effects, not limited to general tolerance, aging, and temperature influences.

### 8.3.7 External Clock Requirements

**Table 33** shows the external clock requirements.

**Table 33** Specification of the External Clock

| Parameter                   | Symbol      | Values |      |                 | Unit | Note / Test Condition |
|-----------------------------|-------------|--------|------|-----------------|------|-----------------------|
|                             |             | Min.   | Typ. | Max.            |      |                       |
| Frequency with 25 MHz Input | $f_{clk25}$ | –      | 25.0 | –               | MHz  | –                     |
| Total Frequency Stability   | –           | -50    | –    | +50             | ppm  | –                     |
| Duty Cycle                  | –           | 40     | –    | 60              | %    | –                     |
| Clock Output High           | $V_{ih}$    | 1.4    | –    | VDDA3V<br>3+0.3 | V    | –                     |
| Clock Output Low            | $V_{il}$    | –      | –    | 0.7             | V    | –                     |
| Rise Time (10% - 90%)       | –           | –      | –    | 10              | ns   | –                     |
| Fall Time (10% - 90%)       | –           | –      | –    | 10              | ns   | –                     |

## 9 Package Outline

The MxL86110 device is available in a 40-pin QFN package with an exposed pin (EPAD). The pin pitch is 0.4 mm and the size of the EPAD is 3.7 x 3.7 mm. The EPAD is used as the common ground and must be connected to the PCB ground plane. The package is a lead-free “green package”, and its exact name for reference purposes is PG-QFN-40.

**Table 34** provides the mechanical dimensions of the PG-QFN-40 package. **Figure 17** shows the top, side, and bottom dimension drawings of the package.

**Table 34 PG-QFN-40 Mechanical Dimensions**

| Parameter       | Symbol | Minimum   | Nominal | Maximum |
|-----------------|--------|-----------|---------|---------|
| Total Thickness | A      | 0.80      | 0.85    | 0.95    |
| Stand Off       | A1     | 0         | 0.02    | 0.05    |
| Mold Thickness  | A2     | -         | 0.65    | -       |
| L/F Thickness   | A3     | 0.203 Ref |         |         |
| Lead Width      | b      | 0.15      | 0.20    | 0.25    |
| Body Size       | X D    | 5.00 BSC  |         |         |
|                 | Y E    | 5.00 BSC  |         |         |
| Lead Pitch      | e      | 0.40 BSC  |         |         |
| EP Size         | X D2   | 3.60      | 3.70    | 3.80    |
|                 | Y E2   | 3.60      | 3.70    | 3.80    |
| Lead Length     | L      | 0.30      | 0.40    | 0.50    |

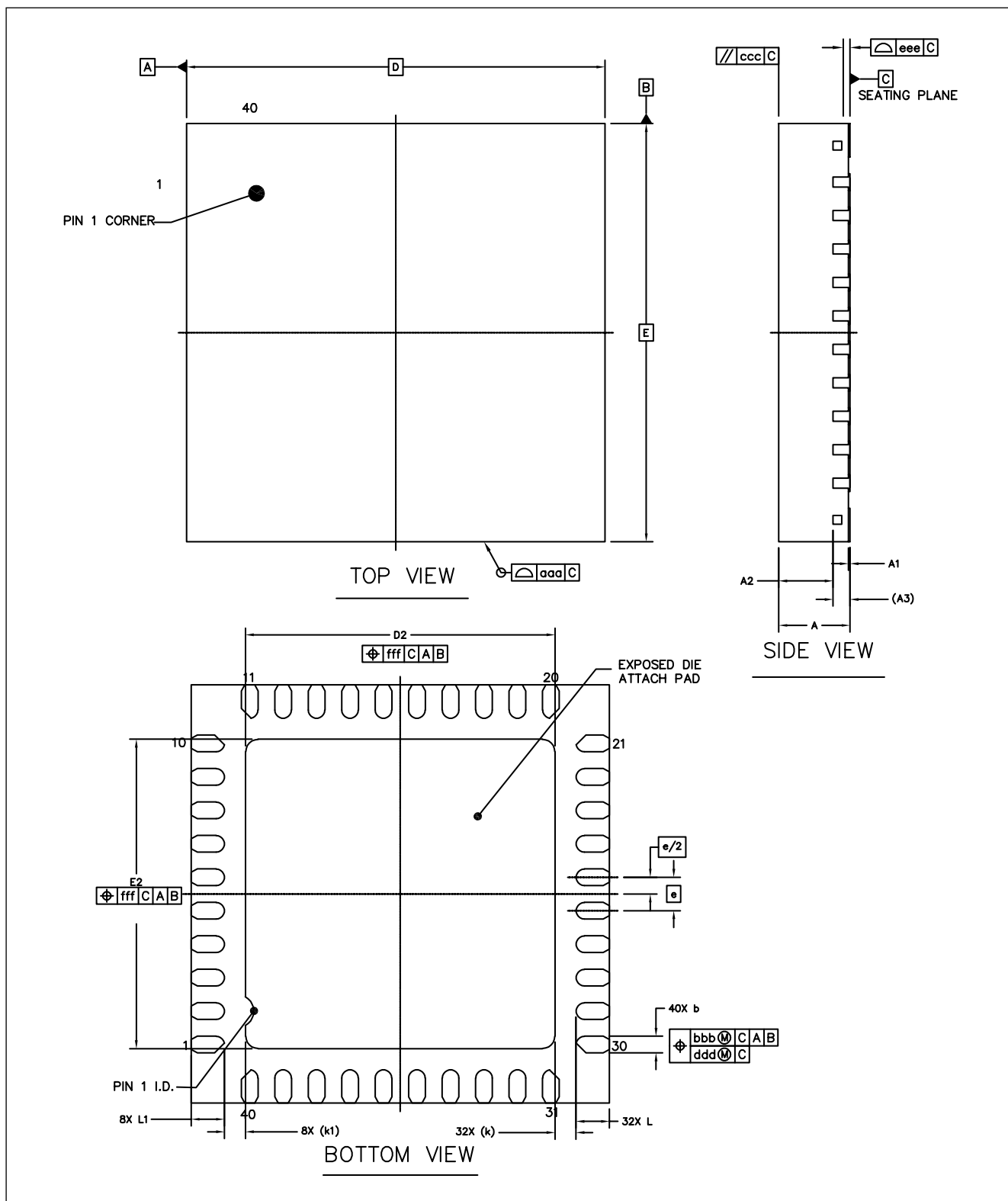


Figure 17 PG-QFN-40 Mechanical Drawing

## 9.1 Thermal Resistance

**Table 35** shows the package thermal resistance values.

**Table 35 Thermal Resistance**

| Symbol            | Parameter                                                                                                                                                                                 | Condition                                                                                | Typ  | Units                |
|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------|------|----------------------|
| $\theta_{JA}$     | Thermal resistance - junction to ambient<br>$\theta_{JA} = (T_J - T_A) / P$<br>$P$ = Total power dissipation                                                                              | JEDEC 3 inch x 4.5 inch 4-layer<br>PCB with no air flow $T_A=25\text{ }^{\circ}\text{C}$ | 33.4 | $^{\circ}\text{C/W}$ |
|                   |                                                                                                                                                                                           | JEDEC 3 inch x 4.5 inch 4-layer<br>PCB with no air flow $T_A=85\text{ }^{\circ}\text{C}$ | 31   | $^{\circ}\text{C/W}$ |
| $\theta_{JB}$     | Thermal resistance - junction to board<br>$\theta_{JB} = (T_J - T_B) / P_{\text{bottom}}$<br>$P_{\text{bottom}}$ = Power dissipation from the bottom of<br>the package to the PCB surface | JEDEC with no air flow                                                                   | 12.3 | $^{\circ}\text{C/W}$ |
| $\theta_{JC-Top}$ | Thermal resistance - junction to case<br>$\theta_{JC} = (T_J - T_C) / P_{\text{top}}$<br>$P_{\text{top}}$ = Power dissipation from the top of the<br>package                              | JEDEC with no air flow                                                                   | 28.4 | $^{\circ}\text{C/W}$ |

## 9.2 Chip Identification and Ordering Information

Figure 18 shows an example of the marking pattern on the MxL86110 device.

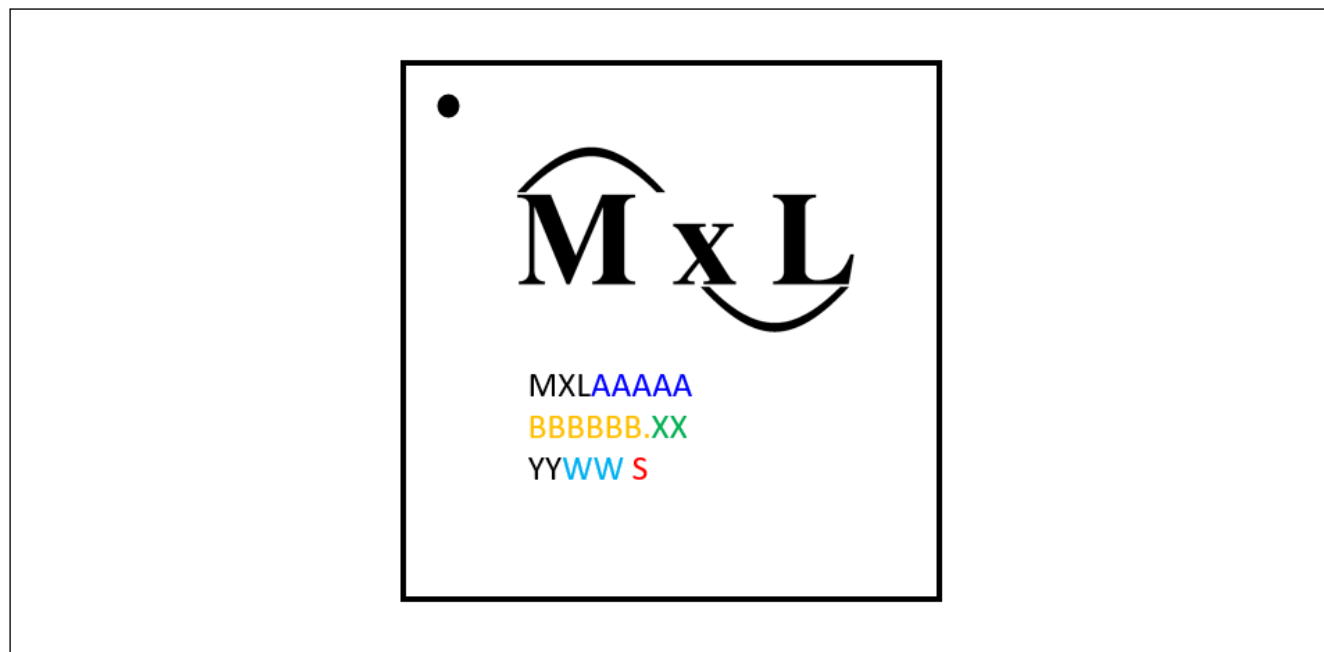


Figure 18 Chip Marking

Table 36 explains the chip marking information.

Table 36 Chip Marking Pattern

| Marking | Description                                    |
|---------|------------------------------------------------|
| MxL     | MaxLinear Logo                                 |
| AAAAA   | MaxLinear Part Number                          |
| BBBBBB  | Wafer Lot Number                               |
| XX      | First wafer number in assembly lot, such as 01 |
| YY      | Year                                           |
| WW      | Work Week                                      |
| S       | Supplier Manufacturing Code                    |

Table 37 provides the chip ordering information.

Table 37 Chip Ordering Information

| Marketing Part Number | Ordering Part Number | Temperature Range | Package (X x Y mm) | MAC Interface | Description                     |
|-----------------------|----------------------|-------------------|--------------------|---------------|---------------------------------|
| MxL86110C             | MXL86110C-A QB-R     | 0 °C to 70 °C     | QFN40 (5 x 5)      | RGMII         | Ethernet Gigabit PHY with RGMII |
| MxL86110I             | MXL86110I-AQ B-R     | -40 °C to 85 °C   | QFN40 (5 x 5)      | RGMII         |                                 |

Note: For more information about part numbers, as well as the most up-to-date information and additional information on environmental rating, go to <https://www.maxlinear.com/support/product-change-notification>.

**Table 38** provides the chip specific information.

**Table 38    Chip Specific Information**

| <b>RGMI Interface</b> | <b>MxL86110</b>   |
|-----------------------|-------------------|
| OUI                   | F04CD5            |
| Device ID             | 0018 <sub>H</sub> |
| Revision              | 0000 <sub>H</sub> |
| Register 2 PHY ID1    | C133 <sub>H</sub> |
| Register 3 PHY ID2    | 5580 <sub>H</sub> |

## Standards References

- [1] IEEE 802.3-2018: "IEEE Standard for Ethernet", IEEE Computer Society
- [2] Hewlett Packard, "Reduced Gigabit Media Independent Interface (RGMII)", Version 1.3, 12.10.2000
- [3] Hewlett Packard, "Reduced Gigabit Media Independent Interface (RGMII)", Version 2.0, 04.01.2002

## Terminology

### A

ADS Auto-Downspeed

ANEG Auto-Negotiation

### B

BER Bit Error Rate

### C

CAT5 Category 5 Cabling

CDR Clock and Data Recovery

CRS Carrier Sense

### D

DEC Digital Echo Canceler

### E

EEE Energy-Efficient Ethernet

EMI Electromagnetic Interference

### G

GbE Gigabit Ethernet

GMII Gigabit Media-Independent Interface

### H

HCD Highest Common Denominator

### I

I<sup>2</sup>C Internally Integrated Circuit Interface (also I2C)

IEEE Institute of Electrical and Electronics Engineers

### L

LAN Local Area Network

LED Light Emitting Diode

LPI Low Power Idle

LQFP Low-Profile Quad Flat Package

LSB Least Significant Bit

### M

MAC Media Access Controller

MBIST Memory Built In Self Test

MDI Media-Dependent Interface

MDIO Management Data Input/Output

MDIX Media-Dependent Interface Crossover

MII Media-Independent Interface

MMD MDIO Manageable Device

MSB Most Significant Bit

|          |                                                            |
|----------|------------------------------------------------------------|
| <b>N</b> |                                                            |
| NC       | Not Connected                                              |
| <b>O</b> |                                                            |
| OSI      | Open Systems Interconnection                               |
| OUI      | Organizationally Unique Identifier                         |
| <b>P</b> |                                                            |
| PCB      | Printed Circuit Board                                      |
| PCS      | Physical Coding Sublayer                                   |
| PHY      | Physical Layer (device)                                    |
| <b>Q</b> |                                                            |
| QFN      | Quad Flat Non-leaded                                       |
| <b>R</b> |                                                            |
| RGMII    | Reduced (pin count) Gigabit Media-Independent Interface    |
| RMII     | Reduced (pin count) Media-Independent Interface            |
| Rx       | Receive                                                    |
| <b>S</b> |                                                            |
| SDF      | Start Frame Delimiter                                      |
| SFP      | Small Form-Factor Pluggable                                |
| SoC      | System on Chip                                             |
| SQE      | Signal Quality Errors                                      |
| STA      | Station Management Entity (MAC SoC), defined in IEEE 802.3 |
| SVR      | Selecting Voltage Regulator                                |
| <b>T</b> |                                                            |
| TPI      | Twisted Pair Interface                                     |
| Tx       | Transmit                                                   |
| <b>V</b> |                                                            |
| VSS      | Voltage Source Supply                                      |
| <b>W</b> |                                                            |
| Wi-Fi    | Wireless Local Area Network                                |
| WoL      | Wake-on-LAN                                                |
| <b>X</b> |                                                            |
| XNP      | Extended Next Page                                         |
| XO       | Crystal Oscillator                                         |
| XTC      | Near-End Cross Talk Canceler                               |