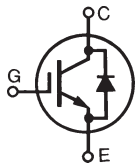
IXYS

High Voltage, High Gain BiMOSFET™

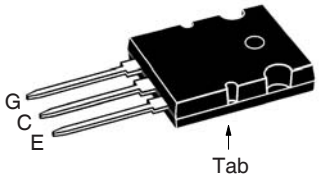
Monolithic Bipolar MOS Transistor

IXBK55N300
IXBX55N300

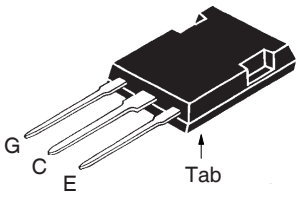
V_{CES} = 3000V
I_{C110} = 55A
$V_{CE(sat)}$ ≤ 3.2V



TO-264 (IXBK)



PLUS247 (IXBX)



G = Gate E = Emitter
C = Collector Tab = Collector

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	3000	V
V_{CGR}	T_J = 25°C to 150°C, R_{GE} = 1MΩ	3000	V
V_{GES}	Continuous	±25	V
V_{GEM}	Transient	±35	V
I_{C25}	T_C = 25°C (Chip Capability)	130	A
I_{LRMS}	T_C = 25°C (Lead RMS Limit)	120	A
I_{C110}	T_C = 110°C	55	A
I_{CM}	T_C = 25°C, 1ms	600	A
SSOA	V_{GE} = 15V, T_{VJ} = 125°C, R_G = 2Ω	I_{CM} = 110	A
(RBSOA)	Clamped Inductive Load	@0.8 • V_{CES}	
T_{SC} **(SCSOA)**	V_{GE} = 15V, T_J = 125°C, R_G = 10Ω, V_{CE} = 1250V, Non-Repetitive	10	μs
P_C	T_C = 25°C	625	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	1.6 mm (0.062 in.) from Case for 10	260	°C
M_d	Mounting Torque (TO-264)	1.13/10	Nm/lb.in.
F_C	Mounting Force (PLUS247)	20..120/4.5..27	N/lb.
Weight	TO-264	10	g
	PLUS247	6	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
BV_{CES}	I_C = 1mA, V_{GE} = 0V	3000			V
$V_{GE(th)}$	I_C = 4mA, V_{CE} = V_{GE}	3.0		5.0	V
I_{CES}	V_{CE} = V_{CES}, V_{GE} = 0V			50	μA
	T_J = 125°C			3	mA
I_{GES}	V_{CE} = 0V, V_{GE} = ± 25V			±200	nA
$V_{CE(sat)}$	I_C = 55A, V_{GE} = 15V, Note 1		2.7	3.2	V
	T_J = 125°C		3.3		V

Features

- High Blocking Voltage
- International Standard Packages
- Low Conduction Losses
- High Current Handling Capability
- MOS Gate Turn-On
  - Drive Simplicity

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- Uninterruptible Power Supplies (UPS)
- Switch-Mode and Resonant-Mode Power Supplies
- Capacitor Discharge Circuits
- Laser Generators

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	I_C = 55A, V_{CE} = 10V, Note 1	32	50		S
C_{ies}	V_{CE} = 25V, V_{GE} = 0V, f = 1MHz		7300		pF
C_{oes}			275		pF
C_{res}			83		pF
Q_g	I_C = 55A, V_{GE} = 15V, V_{CE} = 1000V		335		nC
Q_{ge}			47		nC
Q_{gc}			130		nC
$t_{d(on)}$	**Resistive Switching Times, T_J = 25°C**		54		ns
t_r	I_C = 110A, V_{GE} = 15V		307		ns
$t_{d(off)}$	V_{CE} = 1250V, R_G = 2Ω		230		ns
t_f			268		ns
$t_{d(on)}$	**Resistive Switching Times, T_J = 125°C**		52		ns
t_r	I_C = 110A, V_{GE} = 15V		585		ns
$t_{d(off)}$	V_{CE} = 1250V, R_G = 2Ω		215		ns
t_f			260		ns
R_{thJC}				0.20	°C/W
R_{thCS}			0.15		°C/W

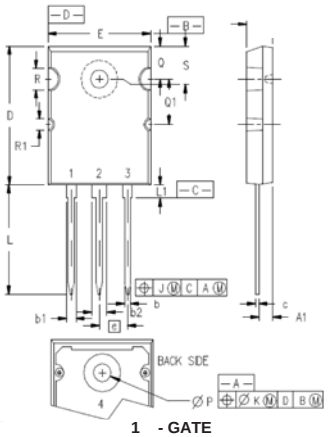
Reverse Diode

Symbol	Test Conditions (T_J = 25°C Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max	
V_F	I_F = 55A, V_{GE} = 0V, Note 1			2.5	V
t_{rr}	I_F = 28A, V_{GE} = 0V, $-di_F/dt$ = 100A/µs		1.9		µs
I_{RM}	V_R = 100V, V_{GE} = 0V		54		A

Note 1: Pulse Test, t ≤ 300µs, Duty Cycle, d ≤ 2%.

Additional provisions for lead-to-lead isolation are required at V_{CE} >1200V.

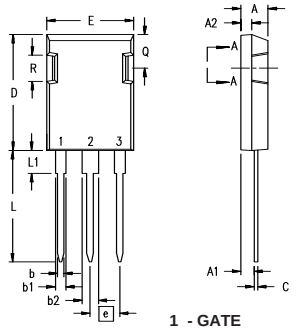
TO-264 Outline



1 - GATE
2,4 - COLLECTOR
3 - EMITTER

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.209	4.70	5.31
A1	.102	.118	2.59	3.00
b	.037	.055	0.94	1.40
b1	.087	.102	2.21	2.59
b2	.110	.126	2.79	3.20
c	.017	.029	0.43	0.74
D	1.007	1.047	25.58	26.59
E	.760	.799	19.30	20.29
e	.215BSC		5.46 BSC	
J	.000	.010	0.00	0.25
K	.000	.010	0.00	0.25
L	.779	.842	19.79	21.39
L1	.087	.102	2.21	2.59
ØP	.122	.138	3.10	3.51
Q	.240	.256	6.10	6.50
Q1	.330	.346	8.38	8.79
ØR	.155	.187	3.94	4.75
ØR1	.085	.093	2.16	2.36
S	.243	.253	6.17	6.43

PLUS 247™ Outline



1 - GATE
2 - COLLECTOR
3 - EMITTER

Dim.	Millimeter Min.	Millimeter Max.	Inches Min.	Inches Max.
A	4.83	5.21	.190	.205
A_1	2.29	2.54	.090	.100
A_2	1.91	2.16	.075	.085
b	1.14	1.40	.045	.055
b_1	1.91	2.13	.075	.084
b_2	2.92	3.12	.115	.123
C	0.61	0.80	.024	.031
D	20.80	21.34	.819	.840
E	15.75	16.13	.620	.635
e	5.45 BSC		.215 BSC	
L	19.81	20.32	.780	.800
L1	3.81	4.32	.150	.170
Q	5.59	6.20	.220	0.244
R	4.32	4.83	.170	.190

Fig. 1. Output Characteristics @ T_J = 25ºC

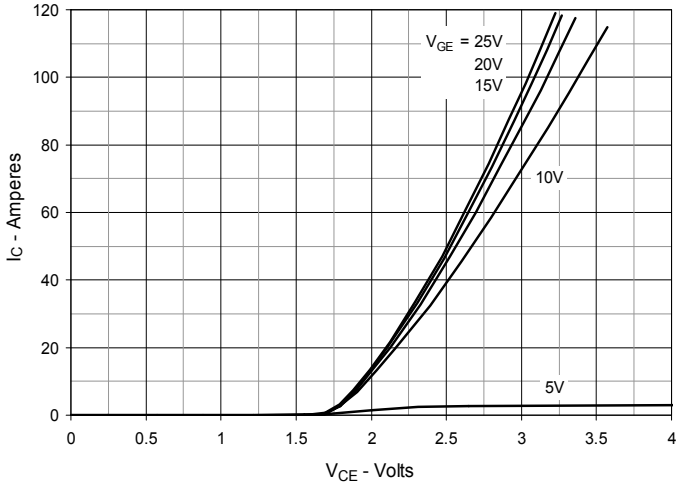


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

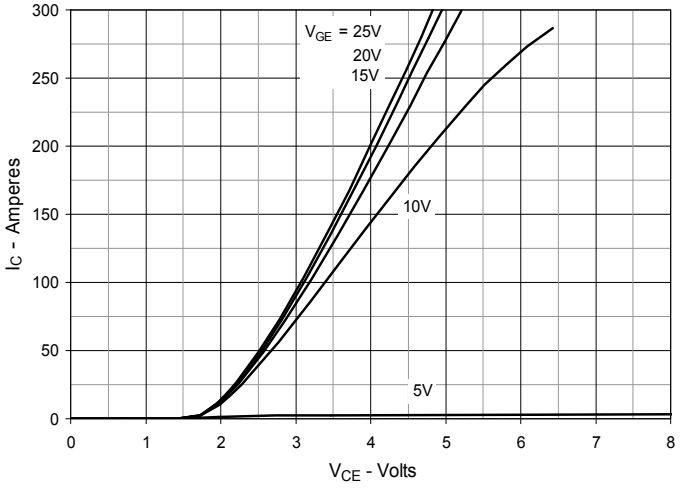


Fig. 3. Output Characteristics @ T_J = 125ºC

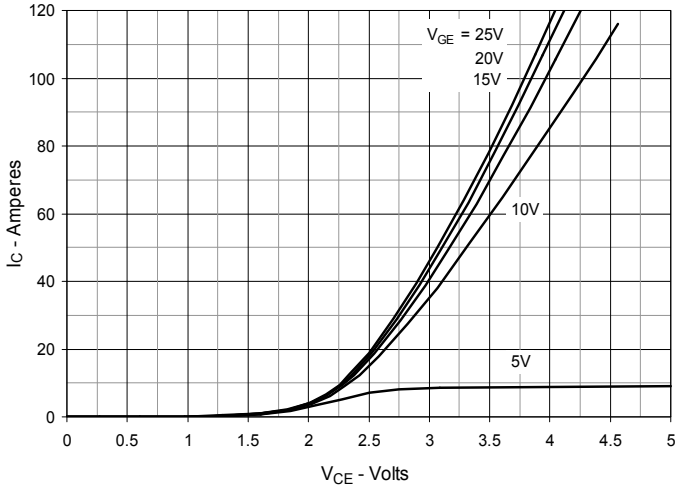


Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

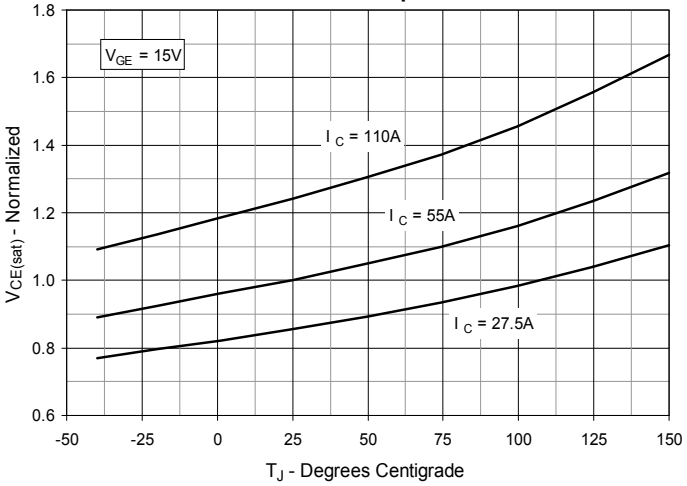


Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

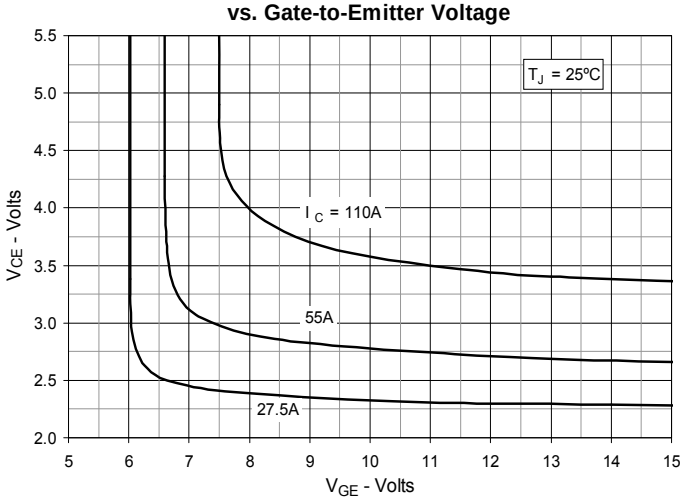


Fig. 6. Input Admittance

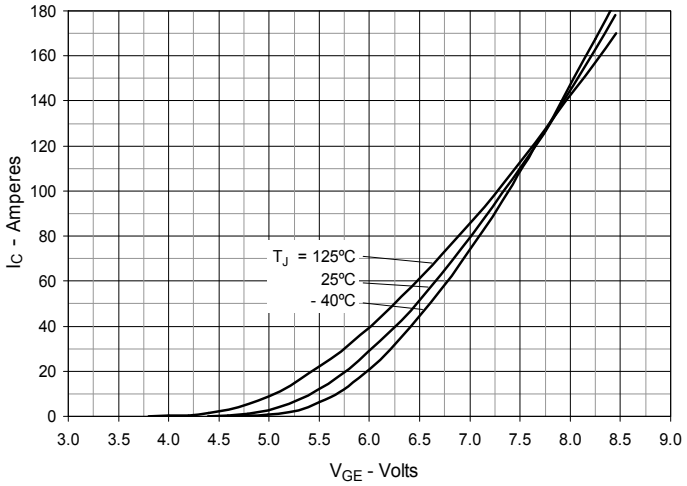


Fig. 7. Transconductance

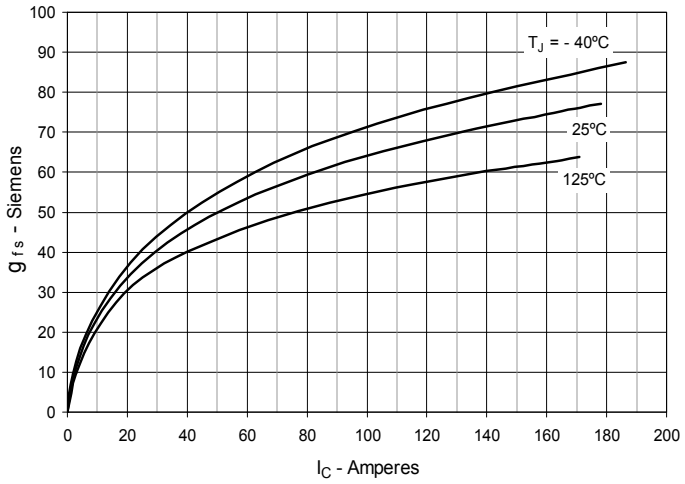


Fig. 8. Forward Voltage Drop of Intrinsic Diode

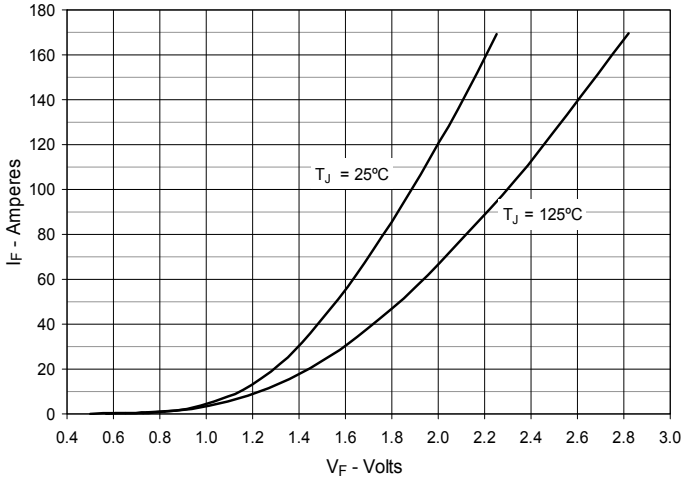


Fig. 9. Gate Charge

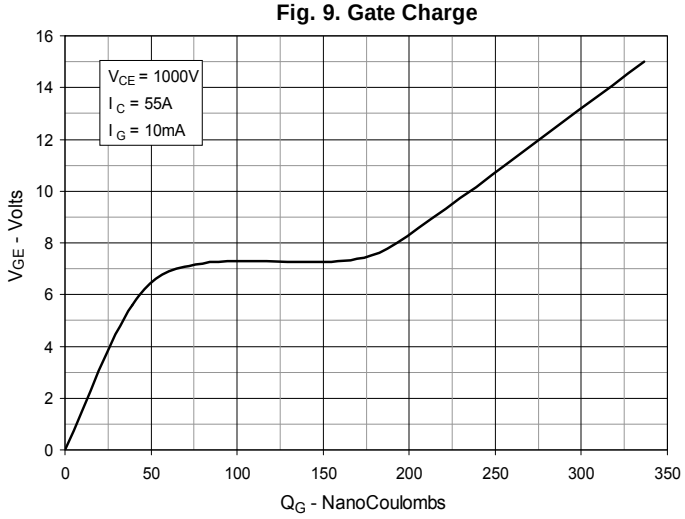


Fig. 10. Capacitance

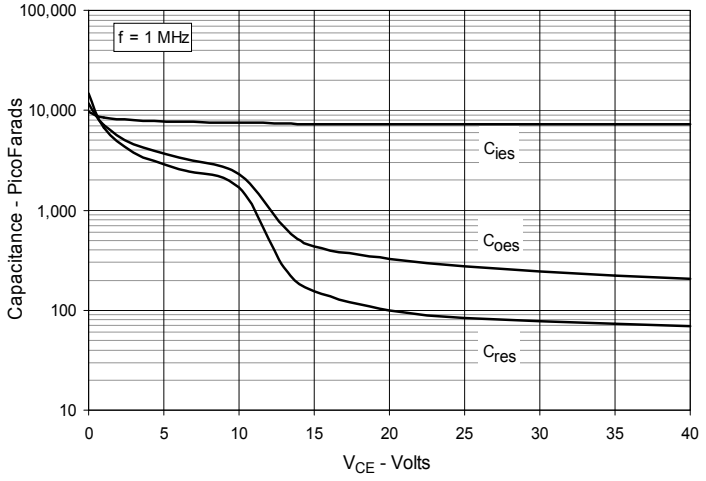


Fig. 11. Reverse-Bias Safe Operating Area

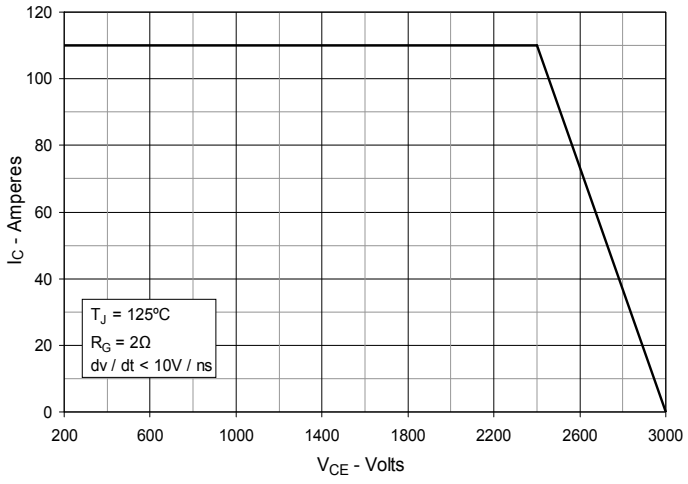


Fig. 12. Maximum Transient Thermal Impedance

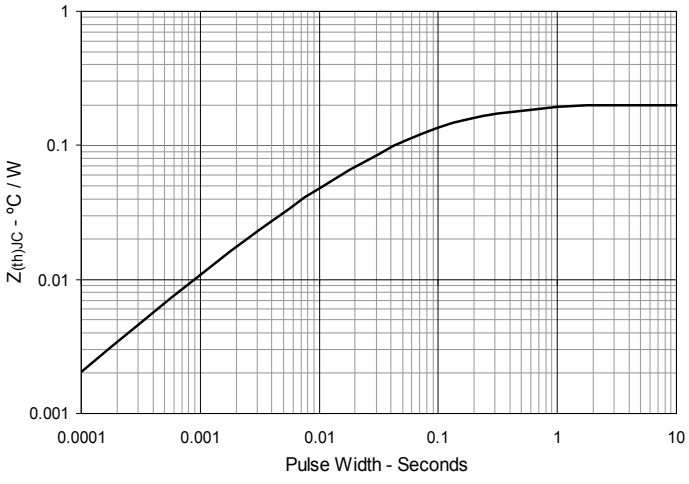


Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature

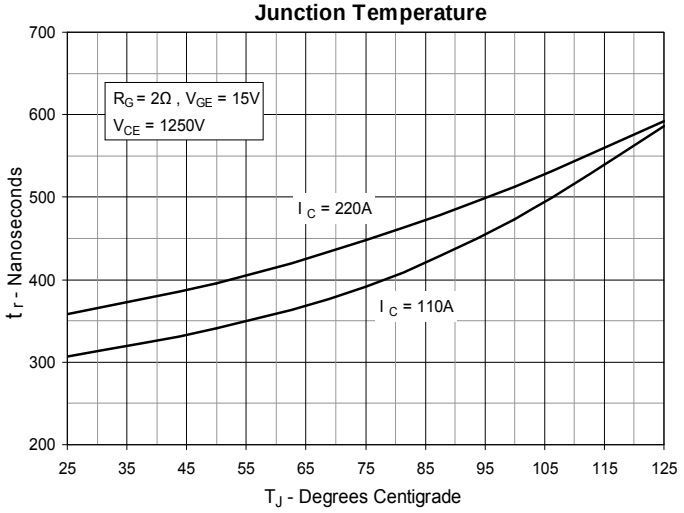


Fig. 14. Resistive Turn-on Rise Time vs. Collector Current

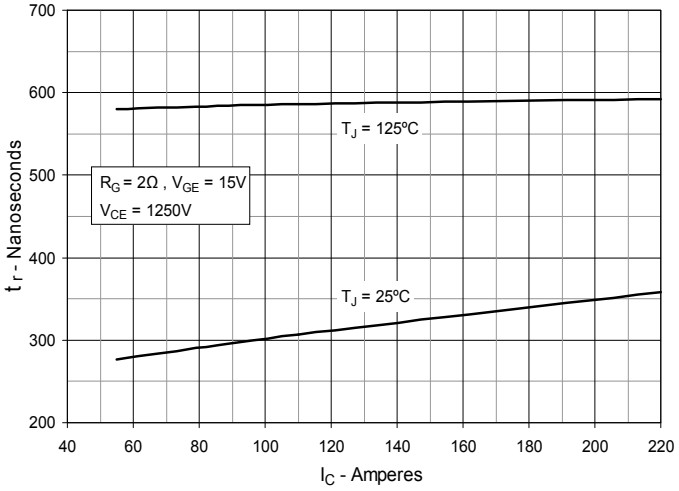


Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance

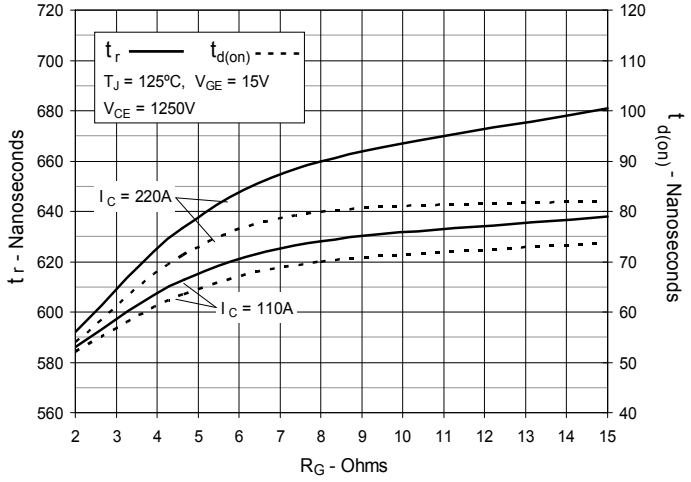


Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature

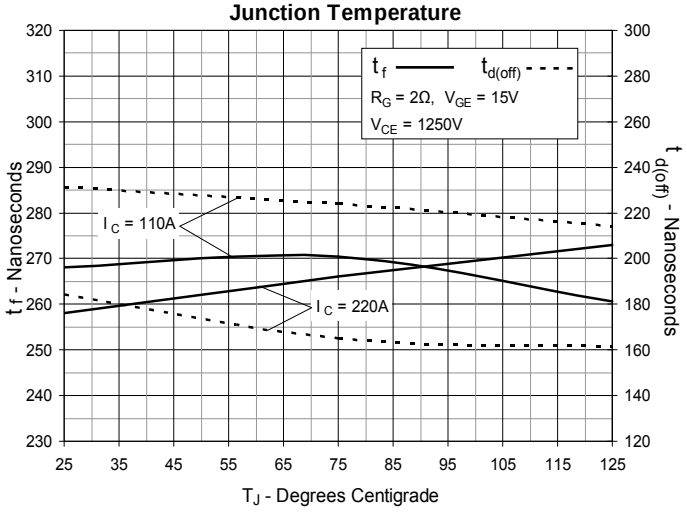


Fig. 17. Resistive Turn-off Switching Times vs. Collector Current

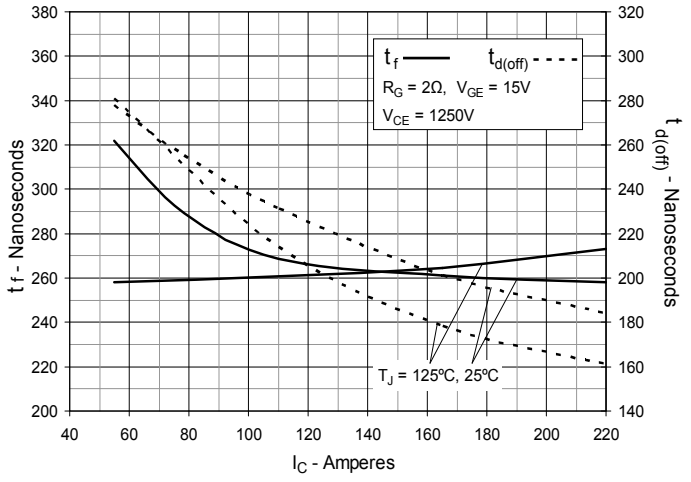


Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance

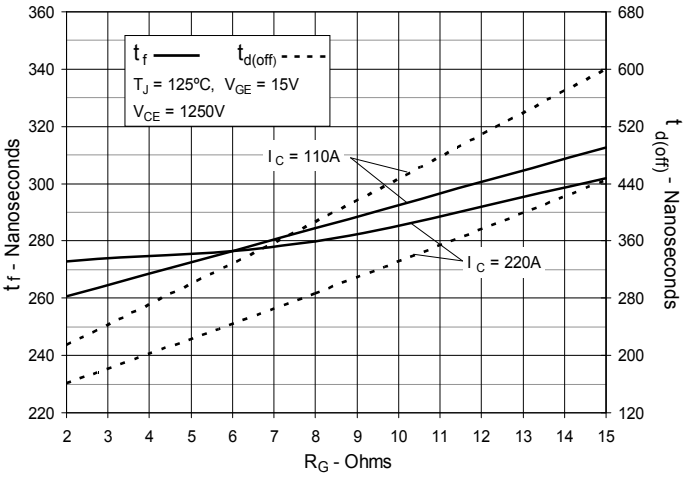


Fig. 19. Forward-Bias Safe Operating Area @ T_C = 25ºC

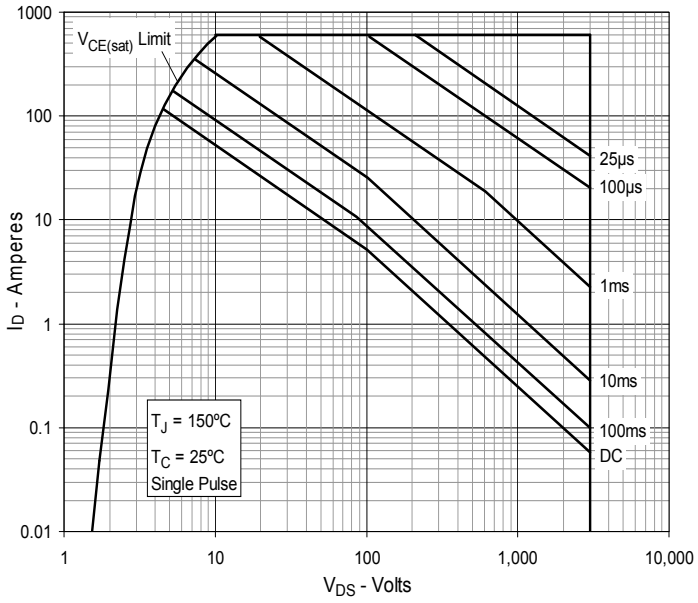


Fig. 20. Forward-Bias Safe Operating Area @ T_C = 75ºC