20V N-Channel Enhancement-Mode MOSFET

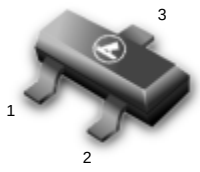
LN2312LT1G

●APPLICATIONS

1)Advanced trench process technology

2)High Density Cell Design For Ultra Low On-Resistance

3)We declare that the material of product compliant with RoHS requirements and Halogen Free



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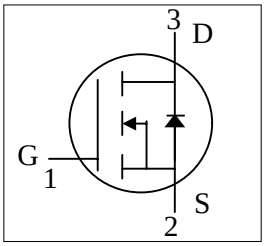

●FEATURES

1)V_{DS}= 20V

2)$R_{DS(ON)}$, Vgs@4.5V, Ids@5.0A = 41mΩ

3)$R_{DS(ON)}$, Vgs@2.5V, Ids@4.5A = 47mΩ

●DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LN2312LT1G	N12	3000/Tape&Reel
LN2312LT3G	N12	10000/Tape&Reel

●MAXIMUM RATINGS(Ta = 25℃)

Parameter		Symbol	Limits	Unit
Drain−to−Source Voltage		V_{DSS}	20	V
Gate−to−Source Voltage		V_{GS}	±8	V
Continuous Drain Current (Note 3),V_{GS}@4.5V	T_A=25℃	I_D	4.9	A
	T_A=70℃		3.4	
Pulsed Drain Current (Note1,2)		I_{DM}	15	A
Maximum Power Dissipation		P_D	0.75	W
Operating and Storage Temperature Range		T_J, Tstg	–55 to +150	°C

●THERMAL DATA

Parameter	Symbol	Limits	Unit
Thermal Resistance Junction-ambient(Note 3)	Rthj-a	140	°C/W

1. Pulse width limited by the Maximum junction temperation

2. 1-in^2 2oz Cu PCB board

3. Surface mounted on 1 in^2 copper PCB board

●ELECTRICAL CHARACTERISTICS (Ta= 25℃)

STATIC

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	20	–	–	V	V_{GS} = 0 V, I_D = 250 μA
Gate Threshold Voltage	$V_{GS(TH)}$	0.4	0.6	1	V	V_{GS} = V_{DS}, I_D = 250 μA
Zero Gate Voltage Drain Current	I_{DSS}	–	–	-1	μA	VDS=20V, VGS=0V
Gate−to−Source Leakage Current	I_{GSS}	–	–	±100	nA	V_{DS} = 0 V, V_{GS} = ±8 V
Drain−to−Source On Resistance	$R_{DS(on)}$	–	31	57	mΩ	V_{GS} = 1.8 V, I_D =4 A
		–	24	47		V_{GS} = 2.5 V, I_D =4.5 A
		–	21	41		V_{GS} = 4.5 V, I_D = 5 A
Forward Diode Voltage	V_{SD}	–	–	1.2	V	V_{GS} = 0 V, I_{SD} = 1.7A
Forward Transconductance	g_{FS}	–	40	–	S	V_{DS} = 10 V, I_D = 5 A

DYNAMIC

Input Capacitance	Ciss	–	500	–	pF	V_{GS} = 0 V, f = 1.0 MHz, V_{DS}= 8 V
Output Capacitance	Coss	–	300	–		
Reverse Transfer Capacitance	Crss	–	140	–		
Total Gate Charge	Q_G	–	11.2	–	nC	V_{GS} =4.5 V,V_{DS} = 10 V I_D = 5 A
Gate−to−Source Gate Charge	Q_{GS}	–	1.4	–		
Gate−to−Drain Charge	Q_{GD}	–	2.2	–		
Turn−On Delay Time	$t_{d(on)}$	–	15	25	ns	V_{DD} = 10V, I_D = 1A, V_{GEN} = 4.5V,R_G = 6 Ω
Rise Time	tr	–	40	60		
Turn−Off Delay Time	$t_{d(off)}$	–	48	70		
Fall Time	tf	–	31	45		

ELECTRICAL CHARACTERISTIC CURVES

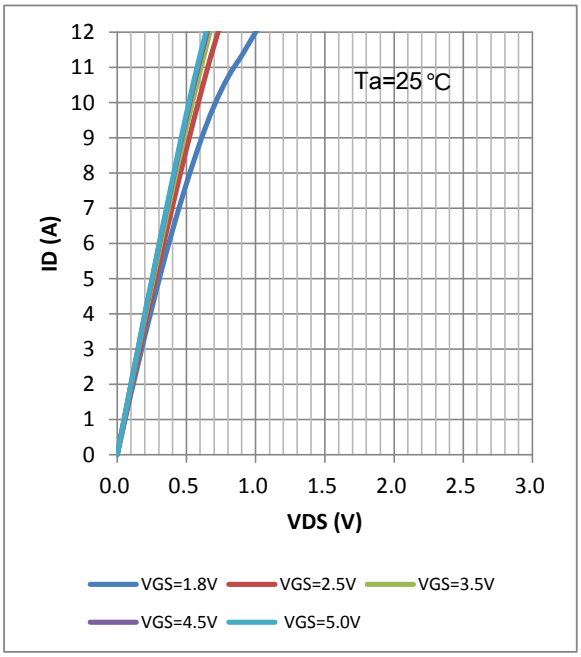

FIG.1 Typical Output Characteristics

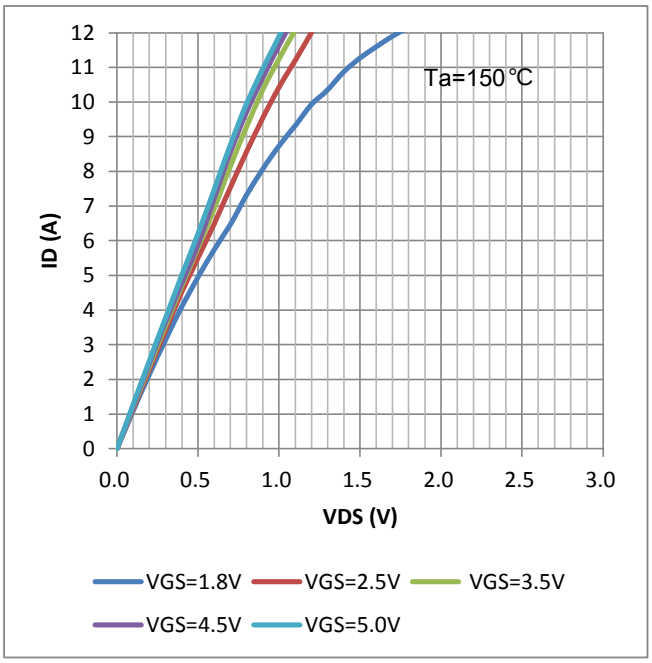

FIG.2 Typical Output Characteristics

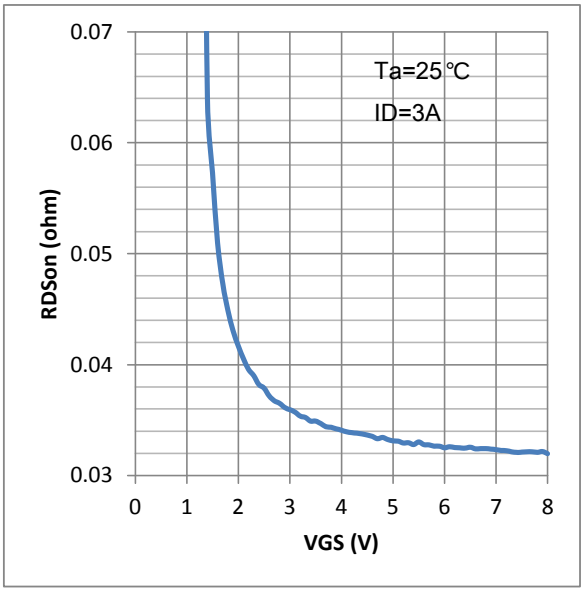

FIG.3 On-Resistance vs. Gate Voltage

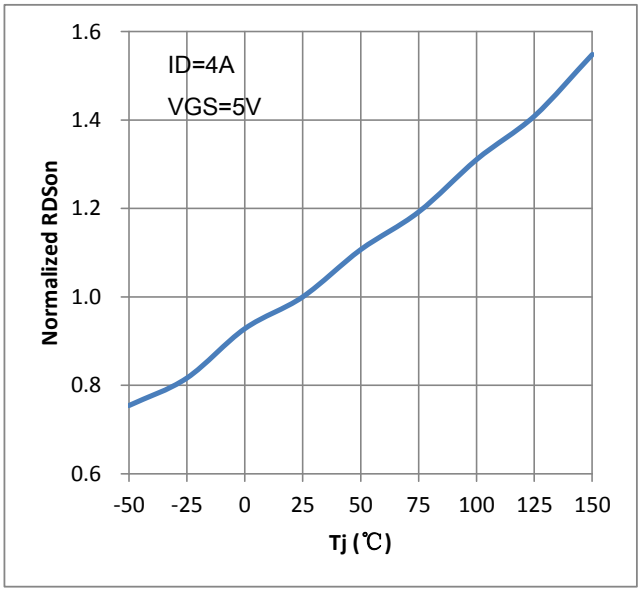

FIG.4 Normalized On-Resistance vs. Junction Temperature

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ELECTRICAL CHARACTERISTIC CURVES

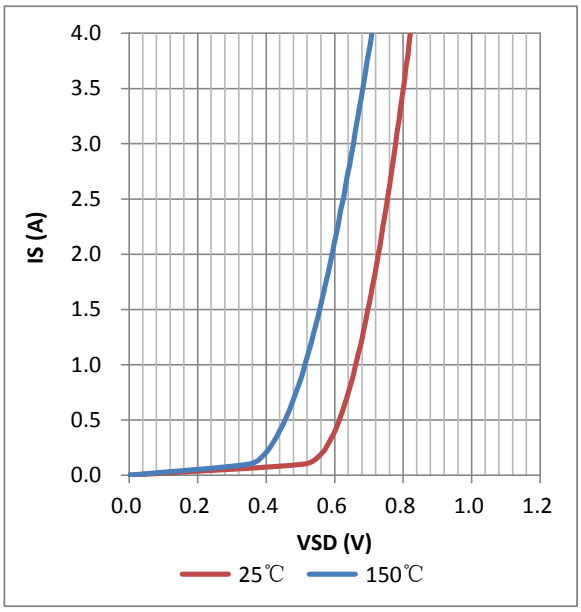

FIG.5 Forward Characteristic of Reverse Diode

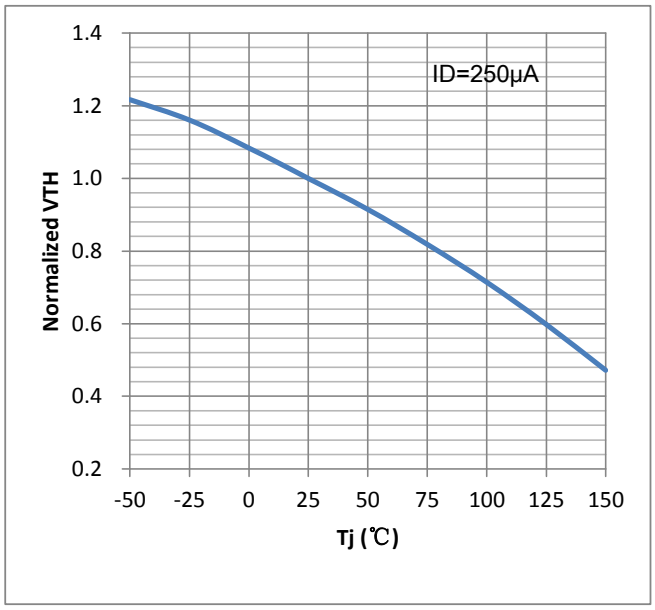

FIG.6 Normalized Gate Threshold Voltage vs. Junction Temperature

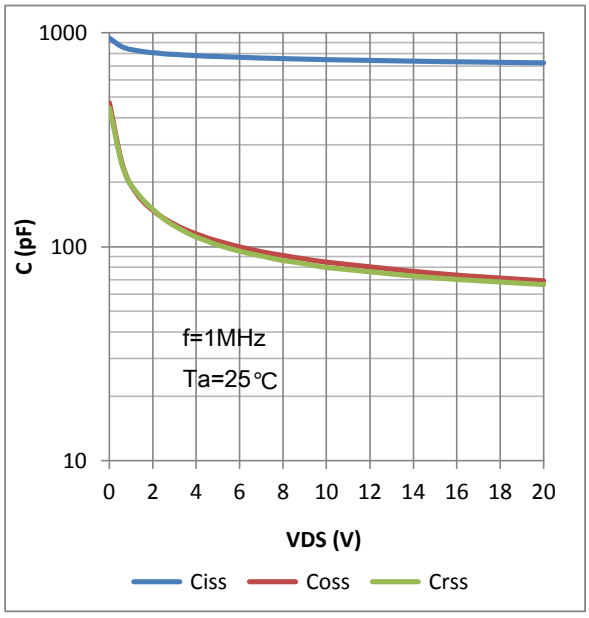

FIG.7 Typical Capacitance Characteristics

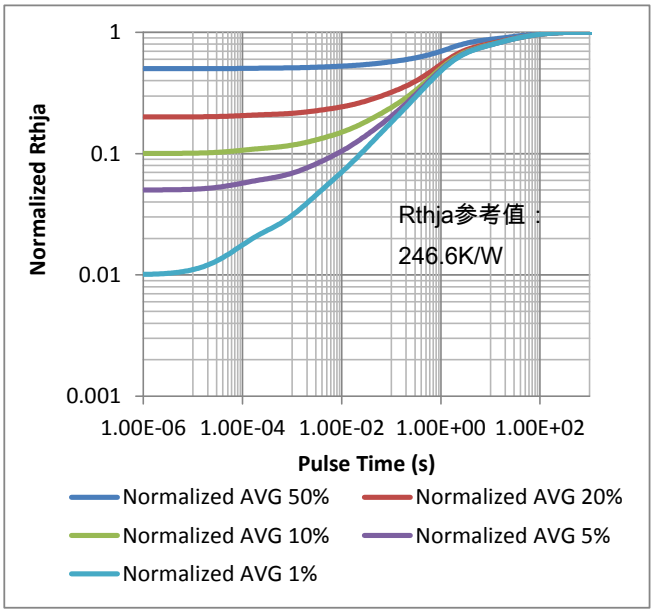

FIG.8 Normalized Effective Transient Thermal Impedance

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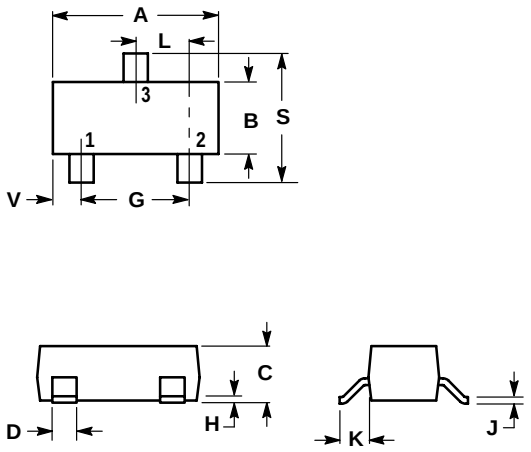

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M,1982
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60