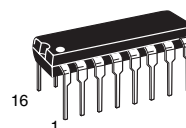


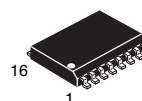
Legacy Device: Motorola/Freescale MC145157-2

The ML145157 has a fully programmable 14-bit reference counter, as well as a fully programmable $\div N$ counter. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

- Operating Temperature Range: $T_A = -40$ to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Fully Programmable Reference and $\div N$ Counters
- $\div R$ Range = 3 to 16383
- $\div N$ Range = 3 to 16383
- f_V and f_R Outputs
- Lock Detect Signal
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- "Linearized" Digital Phase Detector
- Single-Ended (Three-State) or Double-Ended Phase Detector Outputs
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



P DIP 16 = EP
PLASTIC DIP
CASE 648



SOG 16 = -5P
SOG PACKAGE
CASE 751G

CROSS REFERENCE/ORDERING INFORMATION

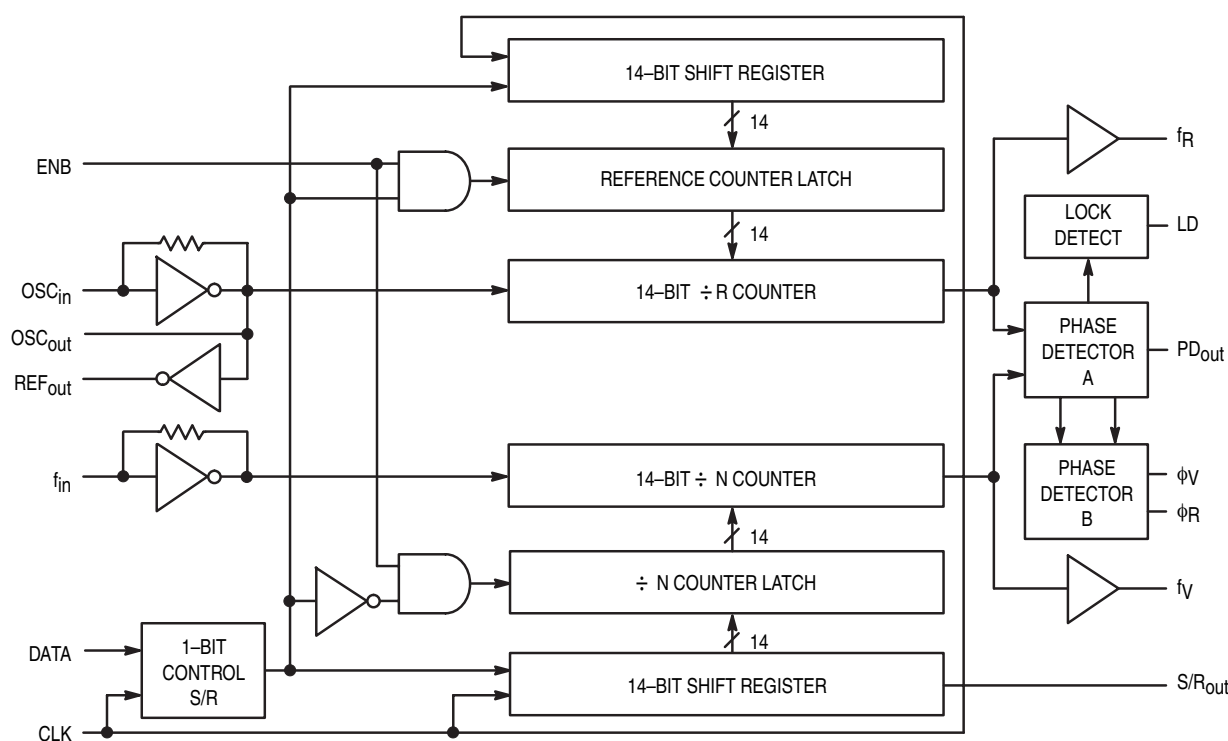
PACKAGE	MOTOROLA	LANSDALE
P DIP 16	MC145157P2	ML145157EP
SOG 20W	MC145157DW2	ML145157-5P

Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

PIN ASSIGNMENT

OSC _{in}	1	16	ϕ_R
OSC _{out}	2	15	ϕ_V
f_V	3	14	REF _{out}
V _{DD}	4	13	f_R
PD _{out}	5	12	S/R _{out}
V _{SS}	6	11	ENB
LD	7	10	DATA
f_{in}	8	9	CLK

ML145157 BLOCK DIAGRAM



PIN DESCRIPTIONS

INPUT PINS

fin**Frequency Input (Pin 8)**

Input frequency from VCO output. A rising edge signal on this input decrements the $\div N$ counter. This input has an inverter biased in the linear region to allow use with AC coupled signals as low as 500 mV p-p. For larger amplitude signals (standard CMOS logic levels), DC coupling may be used.

CLK, DATA**Shift Clock, Serial Data Inputs (Pins 9, 10)**

Each low-to-high transition of the clock shifts one bit of data into the on-chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic 1 selects the reference counter latch and a logic 0 selects the $\div N$ counter latch. The entry format is as follows:

**ENB****Latch Enable Input (Pin 11)**

A logic high on this pin latches the data from the shift register into the reference divider or $\div N$ latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the $\div N$ latches are activated if

the control bit is at a logic low. A logic low on this pin allows the user to change the data in the shift registers without affecting the counters. ENB is normally low and is pulsed high to transfer data to the latches.

OSCin, OSCout**Reference Oscillator Input/Output (Pins 1, 2)**

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSCin to ground and OSCout to ground. OSCin may also serve as the input for an externally-generated reference signal. This signal is typically AC coupled to OSCin, but for larger amplitude signals (standard CMOS logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSCout.

OUTPUT PINS

PDout**Single-Ended Phase Detector A Output (Pin 5)**

This single-ended (three-state) phase detector output produces a loop-error signal that is used with a loop filter to control a VCO.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses

Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses

Frequency $f_V = f_R$ and Phase Coincidence:

High-Impedance State

φR, φV**Double-Ended Phase Detector B Outputs (Pins 16, 15)**

These outputs can be combined externally for a loop-error signal. A single-ended output is also available for this purpose (see **PDout**).

ML145157

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

 f_R, f_V **R Counter Output, N Counter Output (Pins 13, 3)**

Buffered, divided reference and f_{in} frequency outputs. The f_R and f_V outputs are connected internally to the $\div R$ and $\div N$ counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

LD**Lock Detector Output (Pin 7)**

This output is essentially at a high level when the loop is locked (f_R, f_V of same phase and frequency), and pulses low when loop is out of lock.

REF_{out}**Buffered Reference Oscillator Output (Pin 14)**

This output can be used as a second local oscillator, reference oscillator to another frequency synthesizer, or as the system clock to a microprocessor controller.

S/R_{out}**Shift Register Output (Pin 12)**

This output can be connected to an external shift register to provide band switching, control information, and counter programming code checking.

POWER SUPPLY**V_{DD}****Positive Power Supply (Pin 4)**

The positive power supply potential. This pin may range from +3 to +9 V with respect to V_{SS}.

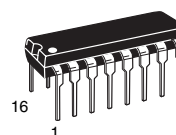
V_{SS}**Negative Power Supply (Pin 6)**

The most negative supply potential. This pin is usually ground.

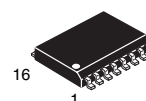
Legacy Device: Motorola/Freescale MC145158-2

The ML145158 has a fully programmable 14-bit reference counter, as well as fully programmable $\div N$ and $\div A$ counters. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

- Operating Temperature Range: $T_A = -40$ to 85°C
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Fully Programmable Reference and $\div N$ Counters
- $\div R$ Range = 3 to 16383
- $\div N$ Range = 3 to 1023
- Dual Modulus Capability; $\div A$ Range = 0 to 127
- f_V and f_R Outputs
- Lock Detect Signal
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- “Linearized” Digital Phase Detector
- Single-Ended (Three-State) or Double-Ended Phase Detector Outputs
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



P DIP 16 = EP
PLASTIC DIP
CASE 648



SOG 16 = -5P
SOG PACKAGE
CASE 751G

CROSS REFERENCE/ORDERING INFORMATION

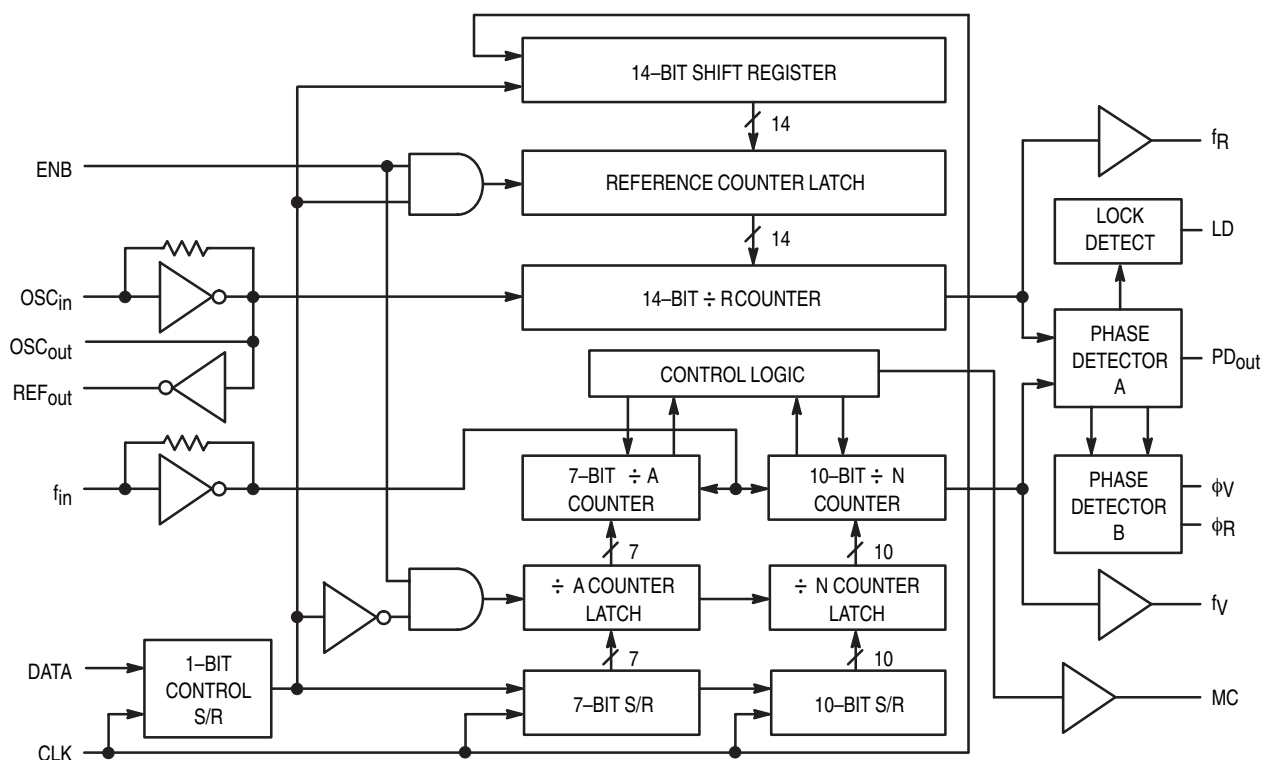
PACKAGE	MOTOROLA	LANSDALE
P DIP 16	MC145158P2	ML145158EP
SOG 16	MC145158DW2	ML145158-5P

Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

PIN ASSIGNMENT

OSC _{in}	1	16	ϕ_R
OSC _{out}	2	15	ϕ_V
f_V	3	14	REF _{out}
V _{DD}	4	13	f_R
PD _{out}	5	12	MC
V _{SS}	6	11	ENB
LD	7	10	DATA
f_{in}	8	9	CLK

ML145158 BLOCK DIAGRAM



PIN DESCRIPTIONS

INPUT PINS

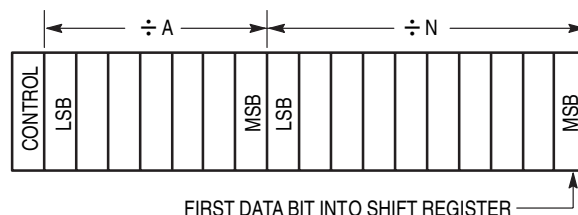
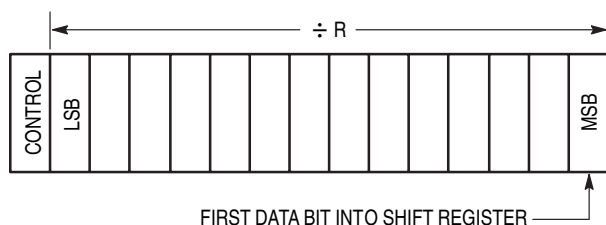
f_{in} Frequency Input (Pin 8)

Input frequency from VCO output. A rising edge signal on this input decrements the $\div A$ and $\div N$ counters. This input has an inverter biased in the linear region to allow use with AC coupled signals as low as 500 mV p-p. For larger amplitude signals (standard CMOS logic levels), DC coupling may be used.

CLK, DATA

Shift Clock, Serial Data Inputs (Pins 9, 10)

Each low-to-high transition of the CLK shifts one bit of data into the on-chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic 1 selects the reference counter latch and a logic 0 selects the $\div A$, $\div N$ counter latch. The data entry format is as follows:



ENB

Latch Enable Input (Pin 11)

A logic high on this pin latches the data from the shift register into the reference divider or $\div N$, $\div A$ latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the $\div N$, $\div A$ latches are activated if the control bit is at a logic low. A logic low on this pin allows the user to change the data in the shift registers without affecting the counters. ENB is normally low and is pulsed high to transfer data to the latches.

OSCin, OSCout

Reference Oscillator Input/Output (Pins 1, 2)

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSCin to ground and OSCout to ground. OSCin may also serve as the input for an externally-generated reference signal. This signal is typically AC coupled to OSCin, but for larger amplitude signals (standard CMOS logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSCout.

OUTPUT PINS

PD_{out}

Phase Detector A Output (Pin 5)

This single-ended (three-state) phase detector output produces a loop-error signal that is used with a loop filter to control a VCO.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses

Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses

Frequency $f_V = f_R$ and Phase Coincidence:

High-Impedance State

ϕ_R, ϕ_V

Phase Detector B Outputs (Pins 16, 15)

Double-ended phase detector outputs. These outputs can be combined externally for a loop-error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

MC

Dual-Modulus Prescaler Control Output (Pin 12)

This output generates a signal by the on-chip control logic circuitry for controlling an external dual-modulus prescaler. The MC level is low at the beginning of a count cycle and remains low until the $\div A$ counter has counted down from its programmed value. At this time, MC goes high and remains high until the $\div N$ counter has counted the rest of the way down from its programmed value ($N - A$ additional counts since both $\div N$ and $\div A$ are counting down during the first portion of the cycle). MC is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = $N \cdot P + A$ where P and $P + 1$ represent the dual-modu-

lus prescaler divide values respectively for high and low modulus control levels, N the number programmed into the $\div N$ counter, and A the number programmed into the $\div A$ counter. Note that when a prescaler is needed, the dual-modulus version offers a distinct advantage. The dual-modulus prescaler allows a higher reference frequency at the phase detector input, increasing system performance capability, and simplifying the loop filter design.

f_R, f_V

R Counter Output, N Counter Output (Pins 13, 3)

Buffered, divided reference and fin frequency outputs. The f_R and f_V outputs are connected internally to the $\div R$ and $\div N$ counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

LD

Lock Detector Output (Pin 7)

This output is essentially at a high level when the loop is locked (f_R, f_V of same phase and frequency), and pulses low when loop is out of lock.

REF_{out}

Buffered Reference Oscillator Output (Pin 14)

This output can be used as a second local oscillator, reference oscillator to another frequency synthesizer, or as the system clock to a microprocessor controller.

POWER SUPPLY

VDD

Positive Power Supply (Pin 4)

The positive power supply potential. This pin may range from +3 to +9 V with respect to VSS.

VSS

Negative Power Supply (Pin 6)

The most negative supply potential. This pin is usually-ground.

ML14515X FAMILY CHARACTERISTICS AND DESCRIPTIONS - CONTINUED

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage	– 0.5 to + 10.0	V
V _{in} , V _{out}	Input or Output Voltage (DC or Transient) except SW1, SW2	– 0.5 to V _{DD} + 0.5	V
V _{out}	Output Voltage (DC or Transient), SW1, SW2 (R _{pull-up} = 4.7 kΩ)	– 0.5 to + 15	V
I _{in} , I _{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
I _{DD} , I _{SS}	Supply Current, V _{DD} or V _{SS} Pins	± 30	mA
P _D	Power Dissipation, per Package†	500	mW
T _{stg}	Storage Temperature	– 65 to + 150	C
T _L	Lead Temperature, 1 mm from Case for 10 seconds	260	C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

† Power Dissipation Temperature Derating:

Plastic DIP: – 12 mW/ C from 65 to 85 C

SOG Package: – 7 mW/ C from 65 to 85 C

These devices contain protection circuitry to protect against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to these high-impedance circuits. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} (V_{in} or V_{out}) V_{DD} except for SW1 and SW2.

SW1 and SW2 can be tied through external resistors to voltages as high as 15 V, independent of the supply voltage.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}), except for inputs with pull-up devices. Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V _{DD} V	– 40 C		25 C		85 C		Unit
				Min	Max	Min	Max	Min	Max	
V _{DD}	Power Supply Voltage Range		–	3	9	3	9	3	9	V
I _{SS}	Dynamic Supply Current	f _{in} = OSC _{in} = 10 MHz, 1 V p-p AC coupled sine wave R = 128, A = 32, N = 128	3 5 9	– – –	3.5 10 30	– – –	3 7.5 24	– – –	3 7.5 24	mA
I _{SS}	Quiescent Supply Current (not including pull-up current component)	V _{in} = V _{DD} or V _{SS} I _{out} = 0 □A	3 5 9	– – –	800 1200 1600	– – –	800 1200 1600	– – –	1600 2400 3200	□A
V _{in}	Input Voltage – f _{in} , OSC _{in}	Input AC coupled sine wave	–	500	–	500	–	500	–	mV p-p
V _{IL}	Low-Level Input Voltage – f _{in} , OSC _{in}	V _{out} 2.1 V Input DC V _{out} 3.5 V coupled V _{out} 6.3 V square wave	3 5 9	– – –	0 0 0	– – –	0 0 0	– – –	0 0 0	V
V _{IH}	High-Level Input Voltage – f _{in} , OSC _{in}	V _{out} 0.9 V Input DC V _{out} 1.5 V coupled V _{out} 2.7 V square wave	3 5 9	3.0 5.0 9.0	– – –	3.0 5.0 9.0	– – –	3.0 5.0 9.0	– – –	V
V _{IL}	Low-Level Input Voltage – except f _{in} , OSC _{in}		3 5 9	– – –	0.9 1.5 2.7	– – –	0.9 1.5 2.7	– – –	0.9 1.5 2.7	V
V _{IH}	High-Level Input Voltage – except f _{in} , OSC _{in}		3 5 9	2.1 3.5 6.3	– – –	2.1 3.5 6.3	– – –	2.1 3.5 6.3	– – –	V
I _{in}	Input Current (f _{in} , OSC _{in})	V _{in} = V _{DD} or V _{SS}	9	± 2	± 50	± 2	± 25	± 2	± 22	□A
I _{IL}	Input Leakage Current (Data, CLK, ENB – without pull-ups)	V _{in} = V _{SS}	9	–	– 0.3	–	– 0.1	–	– 1.0	□A
I _{IH}	Input Leakage Current (all inputs except f _{in} , OSC _{in})	V _{in} = V _{DD}	9	–	0.3	–	0.1	–	1.0	□A

(continued)

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	V _{DD} V	– 40 C		25 C		85 C		Unit
				Min	Max	Min	Max	Min	Max	
I _{IL}	Pull-up Current (all inputs with pull-ups)	V _{in} = V _{SS}	9	– 20	– 400	– 20	– 200	– 20	– 170	μA
C _{in}	Input Capacitance		–	–	10	–	10	–	10	pF
V _{OL}	Low-Level Output Voltage – OSC _{out}	I _{out} = 0 μA V _{in} = V _{DD}	3 5 9	– – –	0.9 1.5 2.7	– – –	0.9 1.5 2.7	– – –	0.9 1.5 2.7	V
V _{OH}	High-Level Output Voltage – OSC _{out}	I _{out} = 0 μA V _{in} = V _{SS}	3 5 9	2.1 3.5 6.3	– – –	2.1 3.5 6.3	– – –	2.1 3.5 6.3	– – –	V
V _{OL}	Low-Level Output Voltage – Other Outputs	I _{out} = 0 μA	3 5 9	– – –	0.05 0.05 0.05	– – –	0.05 0.05 0.05	– – –	0.05 0.05 0.05	V
V _{OH}	High-Level Output Voltage – Other Outputs	I _{out} = 0 μA	3 5 9	2.95 4.95 8.95	– – –	2.95 4.95 8.95	– – –	2.95 4.95 8.95	– – –	V
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage – SW1, SW2	R _{pull-up} = 4.7 kΩ	–	15	–	15	–	15	–	V
I _{OL}	Low-Level Sinking Current – MC	V _{out} = 0.3 V V _{out} = 0.4 V V _{out} = 0.5 V	3 5 9	1.30 1.90 3.80	– – –	1.10 1.70 3.30	– – –	0.66 1.08 2.10	– – –	mA
I _{OH}	High-Level Sourcing Current – MC	V _{out} = 2.7 V V _{out} = 4.6 V V _{out} = 8.5 V	3 5 9	–0.60 –0.90 –1.50	– – –	–0.50 –0.75 –1.25	– – –	–0.30 –0.50 –0.80	– – –	mA
I _{OL}	Low-Level Sinking Current – LD	V _{out} = 0.3 V V _{out} = 0.4 V V _{out} = 0.5 V	3 5 9	0.25 0.64 1.30	– – –	0.20 0.51 1.00	– – –	0.15 0.36 0.70	– – –	mA
I _{OH}	High-Level Sourcing Current – LD	V _{out} = 2.7 V V _{out} = 4.6 V V _{out} = 8.5 V	3 5 9	–0.25 –0.64 –1.30	– – –	–0.20 –0.51 –1.00	– – –	–0.15 –0.36 –0.70	– – –	mA
I _{OL}	Low-Level Sinking Current – SW1, SW2	V _{out} = 0.3 V V _{out} = 0.4 V V _{out} = 0.5 V	3 5 9	0.80 1.50 3.50	– – –	0.48 0.90 2.10	– – –	0.24 0.45 1.05	– – –	mA
I _{OL}	Low-Level Sinking Current – Other Outputs	V _{out} = 0.3 V V _{out} = 0.4 V V _{out} = 0.5 V	3 5 9	0.44 0.64 1.30	– – –	0.35 0.51 1.00	– – –	0.22 0.36 0.70	– – –	mA
I _{OH}	High-Level Sourcing Current – Other Outputs	V _{out} = 2.7 V V _{out} = 4.6 V V _{out} = 8.5 V	3 5 9	–0.44 –0.64 –1.30	– – –	–0.35 –0.51 –1.00	– – –	–0.22 –0.36 –0.70	– – –	mA
I _{OZ}	Output Leakage Current – PD _{out}	V _{out} = V _{DD} or V _{SS} Output in Off State	9	–	± 0.3	–	± 0.1	–	± 1.0	μA
I _{OZ}	Output Leakage Current – SW1, SW2	V _{out} = V _{DD} or V _{SS} Output in Off State	9	–	± 0.3	–	± 0.1	–	± 3.0	μA
C _{out}	Output Capacitance – PD _{out}	PD _{out} – Three-State	–	–	10	–	10	–	10	pF

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 10 ns)

Symbol	Parameter	V _{DD} V	Guaranteed Limit 25°C	Guaranteed Limit – 40 to 85°C	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay, f _{IN} to MC (Figures 1 and 4)	3 5 9	110 60 35	120 70 40	ns
t _{PHL}	Maximum Propagation Delay, ENB to SW1, SW2 (Figures 1 and 5)	3 5 9	160 80 50	180 95 60	ns
t _w	Output Pulse Width, φ _R , φ _V , and LD with f _R in Phase with f _V (Figures 2 and 4)	3 5 9	25 to 200 20 to 100 10 to 70	25 to 260 20 to 125 10 to 80	ns
t _{TLH}	Maximum Output Transition Time, MC (Figures 3 and 4)	3 5 9	115 60 40	115 75 60	ns
t _{THL}	Maximum Output Transition Time, MC (Figures 3 and 4)	3 5 9	60 34 30	70 45 38	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, LD (Figures 3 and 4)	3 5 9	180 90 70	200 120 90	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Other Outputs (Figures 3 and 4)	3 5 9	160 80 60	175 100 65	ns

SWITCHING WAVEFORMS

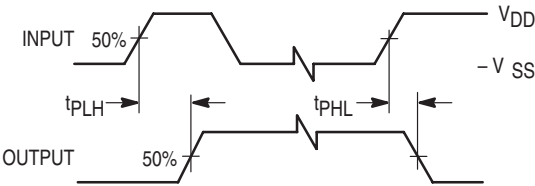


Figure 1.

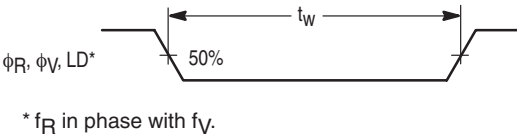


Figure 2.

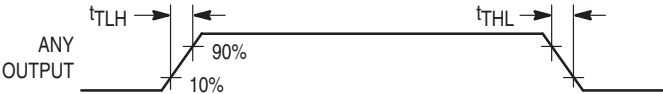
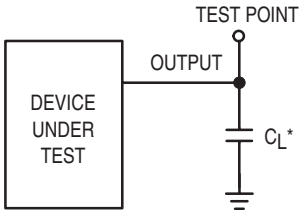
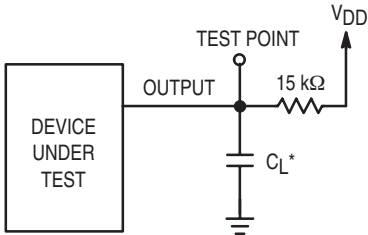


Figure 3.



* Includes all probe and fixture capacitance.

Figure 4. Test Circuit

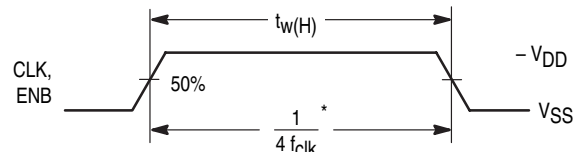


* Includes all probe and fixture capacitance.

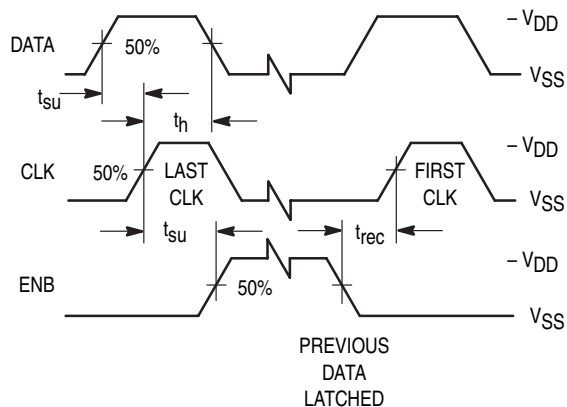
Figure 5. Test Circuit

TIMING REQUIREMENTS (Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	V _{DD} V	Guaranteed Limit 25 C	Guaranteed Limit – 40 to 85 C	Unit
f_{clk}	Serial Data Clock Frequency, Assuming 25% Duty Cycle NOTE: Refer to CLK $t_{w(H)}$ below (Figure 6)	3 5 9	DC to 5.0 DC to 7.1 DC to 10	DC to 3.5 DC to 7.1 DC to 10	MHz
t_{su}	Minimum Setup Time, Data to CLK (Figure 7)	3 5 9	30 20 18	30 20 18	ns
t_h	Minimum Hold Time, CLK to Data (Figure 7)	3 5 9	40 20 15	40 20 15	ns
t_{su}	Minimum Setup Time, CLK to ENB (Figure 7)	3 5 9	70 32 25	70 32 25	ns
t_{rec}	Minimum Recovery Time, ENB to CLK (Figure 7)	3 5 9	5 10 20	5 10 20	ns
$t_{w(H)}$	Minimum Pulse Width, CLK and ENB (Figure 6)	3 5 9	50 35 25	70 35 25	ns
t_r, t_f	Maximum Input Rise and Fall Times – Any Input (Figure 8)	3 5 9	5 4 2	5 4 2	ns

SWITCHING WAVEFORMS

*Assumes 25% Duty Cycle.

Figure 6.**Figure 8.****Figure 7.**

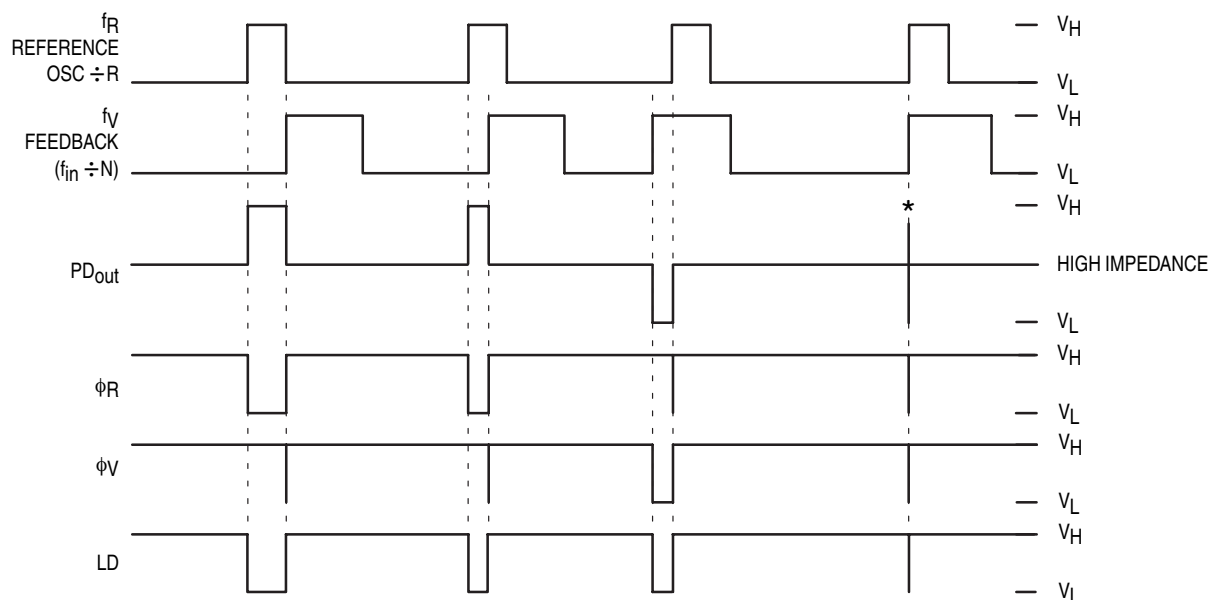
FREQUENCY CHARACTERISTICS (Voltages References to V_{SS} , $C_L = 50$ pF, Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	Test Condition	V_{DD} V	- 40 C		25 C		85 C		Unit
				Min	Max	Min	Max	Min	Max	
f_i	Input Frequency (f_{in} , OSC_{in})	$R \geq 8$, $A \geq 0$, $N \geq 8$ $V_{in} = 500$ mV p-p AC coupled sine wave	3	—	6	—	6	—	6	MHz
			5	—	15	—	15	—	15	
			9	—	15	—	15	—	15	
		$R \geq 8$, $A \geq 0$, $N \geq 8$ $V_{in} = 1$ V p-p AC coupled sine wave	3	—	12	—	12	—	7	MHz
			5	—	22	—	20	—	20	
			9	—	25	—	22	—	22	
		$R \geq 8$, $A \geq 0$, $N \geq 8$ $V_{in} = V_{DD}$ to V_{SS} DC coupled square wave	3	—	13	—	12	—	8	MHz
			5	—	25	—	22	—	22	
			9	—	25	—	25	—	25	

NOTE: Usually, the PLL's propagation delay from f_{in} to MC plus the setup time of the prescaler determines the upper frequency limit of the system.

The upper frequency limit is found with the following formula: $f = P / (t_p + t_{set})$ where f is the upper frequency in Hz, P is the lower of the dual modulus prescaler ratios, t_p is the f_{in} to MC propagation delay in seconds, and t_{set} is the prescaler setup time in seconds.

For example, with a 5 V supply, the f_{in} to MC delay is 70 ns. If the MC12028A prescaler is used, the setup time is 16 ns. Thus, if the 64/65 ratio is utilized, the upper frequency limit is $f = P / (t_p + t_{set}) = 64 / (70 + 16) = 744$ MHz.



V_H = High Voltage Level.

V_L = Low Voltage Level.

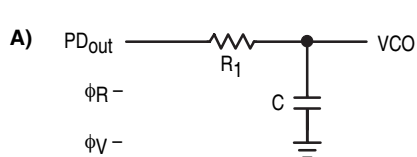
* At this point, when both f_R and f_V are in phase, the output is forced to near mid-supply.

NOTE: The PD_{out} generates error pulses during out-of-lock conditions. When locked in phase and frequency the output is high and the voltage at this pin is determined by the low-pass filter capacitor.

Figure 9. Phase Detector/Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

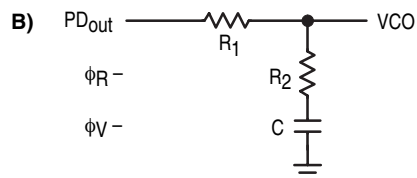
PHASE-LOCKED LOOP – LOW-PASS FILTER DESIGN



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1 C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

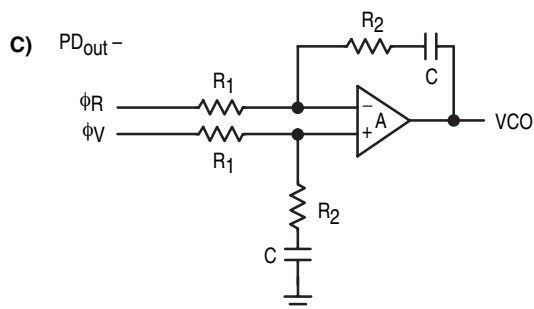
$$F(s) = \frac{1}{R_1 s C + 1}$$



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5 \omega_n \left(R_2 C + \frac{N}{K_\phi K_{VCO}} \right)$$

$$F(s) = \frac{R_2 s C + 1}{(R_1 + R_2) s C + 1}$$



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2 s C + 1}{R_1 s C}$$

NOTE: Sometimes R_1 is split into two series resistors, each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R . The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n . The ϕ_R and ϕ_V outputs swing rail-to-rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used in the combiner/loop filter.

DEFINITIONS:

N = Total Division Ratio in feedback loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ for ϕ_V and ϕ_R

K_{VCO} (VCO Gain) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design ω_n (Natural Frequency) $\frac{2\pi f_r}{10}$ (at phase detector input).

Damping Factor: $\zeta \approx 1$

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition)*. New York, Wiley-Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition)*. New York, Wiley-Interscience, 1980.

Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design*. New York, Wiley-Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock*. New York, Wiley-Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*. Englewood Cliffs, NJ, Prentice-Hall, 1983.

Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments*. Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook*. Blue Ridge Summit, PA, Tab Books, 1980.

AN535, Phase-Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase-Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design*, 1987.

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's or Lansdale's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μ A at CMOS logic levels may be direct or DC coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or AC coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

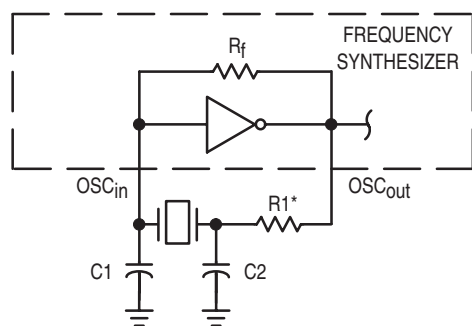
For additional information about TCXOs and data clock oscillators, please consult the latest version of the eem Electronic Engineers Master Catalog, the Gold Book, or similar publications.

Design an Off-Chip Reference

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the ML12061 MECL device. The reference signal from the MECL device is AC coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), DC coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

Use of the On-Chip Oscillator Circuitry

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 10.



* May be deleted in certain cases. See text.

Figure 10. Pierce Crystal Oscillator Circuit

For V_{DD} = 5.0 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8.0 MHz, 20 pF for frequencies in the area of 8.0 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_o + \frac{C_1 \cdot C_2}{C_1 + C_2}$$

where

C_{in} = 5 pF (see Figure 11)

C_{out} = 6 pF (see Figure 11)

C_a = 1 pF (see Figure 11)

C_o = the crystal's holder capacitance (see Figure 12)

C₁ and C₂ = external capacitors (see Figure 10)

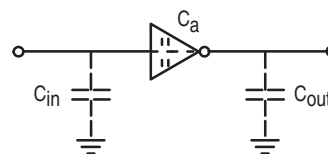
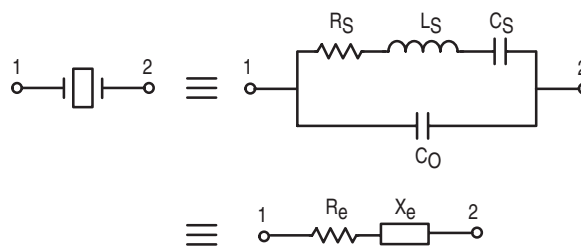


Figure 11. Parasitic Capacitances of the Amplifier



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 12. Equivalent Crystal Networks

The oscillator can be "trimmed" on-frequency by making a portion or all of C₁ variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the value for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 12. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R₁ in Figure 10 limits the drive level. The use of R₁ may not be necessary in some cases (i.e., R₁ = 0 Ω).

To verify that the maximum DC supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the DC supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R₁ must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R₁.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 1).

Table 1. Partial List of Crystal Manufacturers

United States Crystal Corp.
Crystek Crystal
Statek Corp.
Fox Electronics

NOTE: Lansdale and Motorola do not recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

RECOMMENDED READING

- Technical Note TN-24, Statek Corp.
 Technical Note TN-7, Statek Corp.
 E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", Proc. IEEE, Vol. 57, No. 2 Feb., 1969.
 D. Kemper, L. Rosine, "Quartz Crystals for FrequencyControl", Electro-Technology, June, 1969.
 P. J. Ottowitz, "A Guide to Crystal Selection", Electronic Design, May, 1966.

DUAL-MODULUS PRESCALING

OVERVIEW

The technique of dual-modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low-frequency programmable counters to be used as high-frequency programmable counters with speed capability of several hundred MHz. This is possible with out the sacrifice in system resolution and performance that results if a fixed (single-modulus) divider is used for the prescaler.

In dual-modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). Lansdale's dual-modulus frequency synthesizers contain this feature and can be used with a variety of dual-modulus-prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P + 1 divide values in the range of $\div 3/\div 4$ to $\div 128/\div 129$ can be controlled by most Lansdale frequency synthesizers.

Several dual-modulus prescaler approaches suitable for use with the MC145152 (Motorola), ML145156, or ML145158 are:

ML12009	$\div 5/\div 6$	440 MHz
ML12011	$\div 8/\div 9$	500 MHz
ML12013	$\div 10/\div 11$	500 MHz
ML12015	$\div 32/\div 33$	225 MHz
ML12016	$\div 40/\div 41$	225 MHz
ML12017	$\div 64/\div 65$	225 MHz
ML12018	$\div 128/\div 129$	520 MHz
MC12028A	$\div 32/33$ or $\div 64/65$	1.1 GHz
MC12034	$\div 32/33$ or $\div 64/65$	2.0 GHz
MC12038	$\div 127/128$ or $\div 255/256$	1.1 GHz
ML12052	$\div 64/65$ or $\div 128/129$	1.1 GHz
ML12054A	$\div 64/65$ or $\div 128/129$	2.0 GHz

DESIGN GUIDELINES

The system total divide value, N total (N_T) will be dictated by the application:

N is the number programmed into the $\div N$ counter, A is the

$$N_T = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \cdot P + A$$

number programmed into the $\div A$ counter, P and P + 1 are the two selectable divide ratios available in the dual-modulus prescalers. To have a range of N_T values in sequence, the $\div A$ counter is programmed from zero through P – 1 for a particular value N in the $\div N$ counter. N is then incremented to N + 1 and the $\div A$ is sequenced from 0 through P – 1 again.

There are minimum and maximum values that can be achieved for N_T . These values are a function of P and the size of the $\div N$ and $\div A$ counters.

The constraint $N \geq A$ always applies. If $A_{\max} = P - 1$, then $N_{\min} \geq P - 1$. Then $N_T \min = (P - 1) P + A$ or $(P - 1) P$ since A is free to assume the value of 0.

$$N_{T\max} = N_{\max} \cdot P + A_{\max}$$

To maximize system frequency capability, the dual-modulus prescaler output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high and by P + 1 when its MC is low.

For the maximum frequency into the prescaler ($f_{VCO\max}$), the value used for P must be large enough such that:

1. $f_{VCO\max}$ divided by P may not exceed the frequency capability of f_{in} (input to the $\div N$ and $\div A$ counters).
2. The period of f_{VCO} divided by P must be greater than the sum of the times:
 - a. Propagation delay through the dual-modulus prescaler.
 - b. Prescaler setup or release time relative to its MC signal.
 - c. Propagation time from f_{in} to the MC output for the frequency synthesizer device.

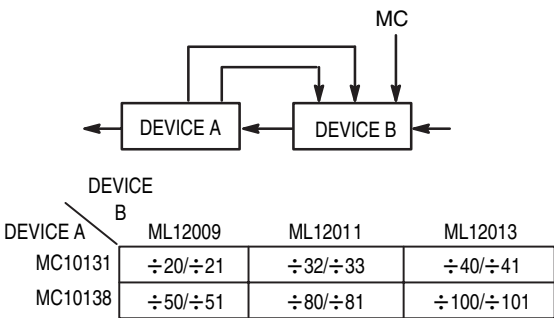
A sometimes useful simplification in the programming code can be achieved by choosing the values for P of 8, 16, 32, or 64. For these cases, the desired value of N_T results when N_T in binary is used as the program code to the $\div N$ and $\div A$ counters treated in the following manner:

1. Assume the $\div A$ counter contains "a" bits where $2^a \geq P$.
2. Always program all higher order $\div A$ counter bits above "a" to 0.

3. Assume the ÷N counter and the ÷A counter (with all the higher order bits above “a” ignored) combined into a single binary counter of n + a bits in length (n = number of divider stages in the ÷N counter). The MSB of this “hypothetical” counter is to correspond to the MSB of ÷ N and the LSB is to

correspond to the LSB of ÷ A. The system divide value, N_T, now results when the value of N_T in binary is used to program the “new” n + a bit counter.

By using the two devices, several dual-modulus values are achievable (shown in Figure 13).

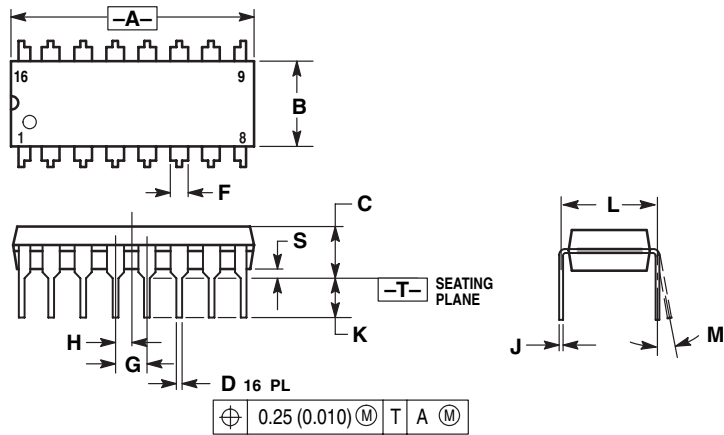


NOTE: ML12009, ML12011, and ML12013 are pin equivalent.
 ML12015, ML12016, and ML12017 are pin equivalent.

Figure 13. Dual-Modulus Values

OUTLINE DIMENSIONS

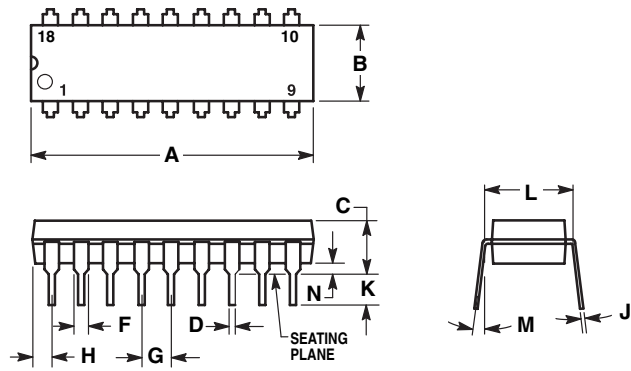
P DIP 16 = EP
PLASTIC DIP
CASE 648-08
(ML145157EP, ML145158EP)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

P DIP 18 = VP
PLASTIC DIP
CASE 707-02
(ML145155VP)

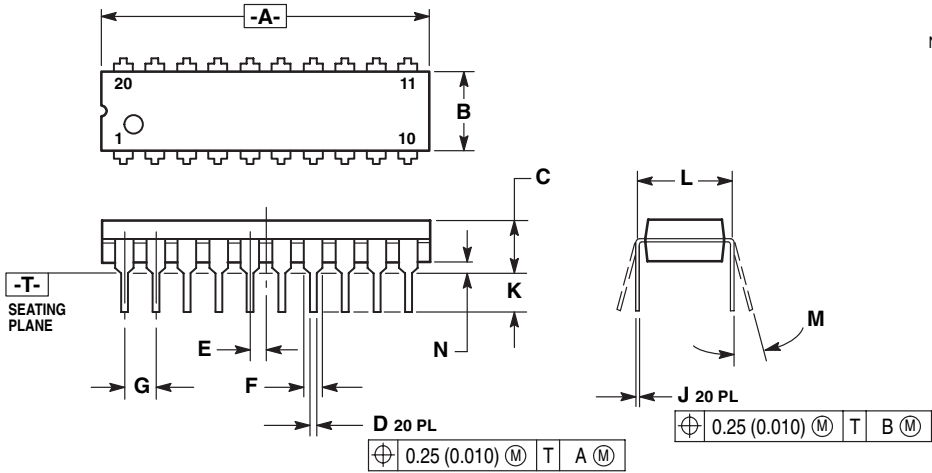


- NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
 2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

OUTLINE DIMENSIONS

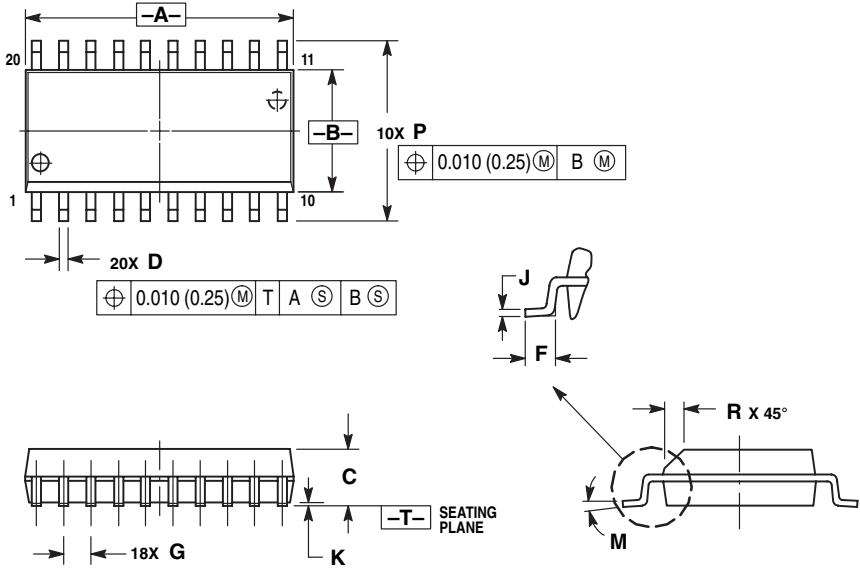
P DIP 20 = RP
 PLASTIC DIP
 CASE 738-03
 (ML145156RP)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

SOG 20 = -6P
 SOG PACKAGE
 CASE 751D-04
 (MC145155-6P, MC145156-6P)

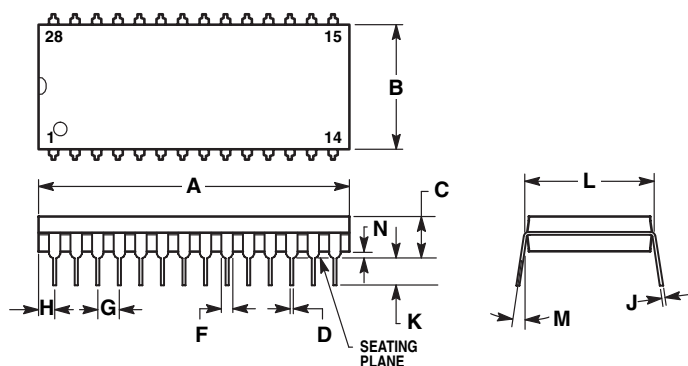


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

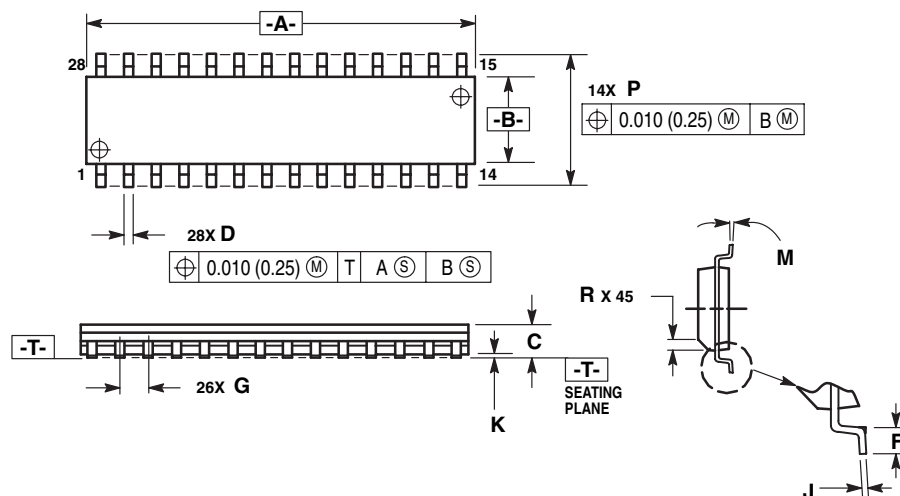
**P DIP 28 = YP
PLASTIC DIP
CASE 710-02
(ML145151YP, ML145152YP)**

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0	15	0	15
N	0.51	1.02	0.020	0.040

SO 28W = -6P
SOG PACKAGE
CASE 751F-04
(ML145151-6P, ML145152-6P)

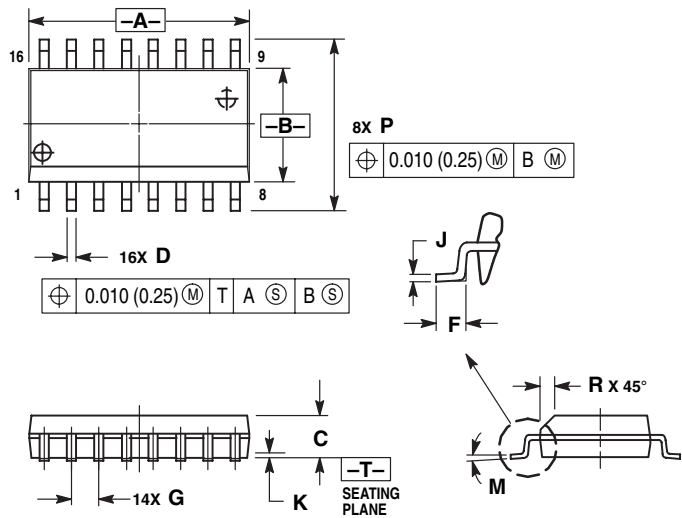


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC	0.050 BSC		
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0	8	0	8
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

OUTLINE DIMENSIONS

SOG 20 = -5P
SOG PACKAGE
CASE 751G-02
(ML145157-5P, ML145158-5P)



- NOTES:
- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - 2. CONTROLLING DIMENSION: MILLIMETER.
 - 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 - 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 - 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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