



Click here for the 3D model.

Dimensions	
D	26.9mm MAX
L	6.35mm MIN
Н	2.54mm +/-0.127mm
F	1.397mm +/-0.25mm
А	5.33mm MAX
В	7.37mm MAX
С	6.35mm +/-0.635mm
E	7.62mm MAX
К	0.5mm +/-0.05mm

Packaging Specifications

Packaging	Waffle, Box
Packaging Quantity	25

General Information		
Series	KPS-MCL Indust COG HT200C	
Style	Leaded Stacked Chip	
Description	Low Loss, Low ESR, Stacked Ceramic Chips	
Features	200C, Low ESR, High Thermal Stability, Bulk Capacitance	
RoHS	With Exemptions	
REACH	SVHC (Pb – CAS 7439-92-1)	
SCIP Number	297427bb-2a48-4853-b594-641304a2cc24	
Termination	Silver	
Lead	Straight Leads	
AEC-Q200	No	
Notes	Number of chips in this stack: 10.	

Specifications	
Capacitance	0.22 uF
Capacitance Tolerance	10%
Voltage DC	630 VDC
Dielectric Withstanding Voltage	819 VDC
Temperature Range	-55/+200°C
Temperature Coefficient	COG
Dissipation Factor	0.1% 1 kHz 25C
Aging Rate	0% Loss/Decade Hour
Insulation Resistance	4.55 GOhms

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