



**IS21TF08G**

**IS22TF08G**

**8GB eMMC**

**With eMMC 5.1 Interface & pSLC Mode NAND**

**DATA SHEET**

## **8GB eMMC with eMMC 5.1 Interface & pSLC Mode NAND**

### **FEATURES**

- Packaged NAND flash memory with eMMC 5.1 interface
  - IS21/22TF08G: 8Gigabyte
- Device is compliant with eMMC Specification Ver.4.3, 4.4, 4.41,4.5, 4.51, 5.0, 5.1
- Bus mode
  - High-speed eMMC protocol
  - Clock frequency: 0-200MHz.
  - Ten-wire bus (clock, 1 bit command, 8 bit data bus) and a hardware reset.
- Supports three different data bus widths : 1 bit(default), 4 bits, 8 bits
  - Data transfer rate: up to 52Mbyte/s (using 8 parallel data lines at 52 MHz)
  - Single data rate: up to 200Mbyte/s @ 200MHz (HS200)
  - Dual data rate: up to 400Mbyte/s @ 200MHz (HS400)
- Operating voltage range:
  - VCCQ = 1.8 V/3.3 V (Automotive A2 Grade only supports 1.8V VCCQ)
  - VCC = 2.7 – 3.6V
- Error free memory access
  - Internal error correction code (ECC) to protect data communication
  - Internal enhanced data management algorithm
  - Solid protection from sudden power failure, safe-update operations for data content
- Security
  - Support secure erase and trim commands
  - Enhanced write protection with permanent and partial protection options
- Key Features:
  - HS400, Field Firmware Update (FFU), Power Off Notification, Pre EOL information, Enhanced Device Life time, Optimal Size
- eMMC 5.1 Features:
  - Command Queuing, Enhanced Strobe, Cache Flushing Report, BKOPS Control, Cache Barrier, RPMB Throughput Improve, Secure Write Protection.
- Temperature range
  - Industrial Grade (I): -40 °C ~ 85 °C
  - Automotive Grade (A1): -40 °C ~ 85 °C
  - Automotive Grade (A2): -40 °C ~ 105 °C (The Surface Temperature of Tc cannot be over 115 °C)
- Package
  - 153 FBGA (11.5mm x 13mm x 1.0mm)
  - 100 FBGA (14.0mm x 18.0mm x 1.4mm)
  - Green Package (RoHS Compliant, Halogen-Free) and TSCA Compliant

## **GENERAL DESCRIPTION**

ISSI *eMMC* products follow the JEDEC *eMMC* 5.1 standard. It is ideal for embedded storage solutions for Industrial application and automotive application, which require high performance across a wide range of operating temperatures.

*eMMC* encloses the pSLC Mode NAND and *eMMC* controller inside as one JEDEC standard package, providing a standard interface to the host. The *eMMC* controller directly manages NAND flash, including ECC, wear-leveling, IOPS optimization and read sensing.

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## 1. PERFORMANCE SUMMARY

### 1.1 Typical Sequential Burst Performance (PSA Pseudo-SLC Burst Status)

| Speed Mode & Operation |                 |       | 8GB | Unit |
|------------------------|-----------------|-------|-----|------|
| HS400                  | Write Cache On  | Read  | 320 | MB/s |
|                        |                 | Write | 135 | MB/s |
|                        | Write Cache Off | Read  | 320 | MB/s |
|                        |                 | Write | 130 | MB/s |
| HS200                  | Write Cache On  | Read  | 175 | MB/s |
|                        |                 | Write | 140 | MB/s |
|                        | Write Cache Off | Read  | 175 | MB/s |
|                        |                 | Write | 120 | MB/s |

**Notes:**

1. Values for an 8-bit bus width, running ISSI proprietary tool,  $V_{CC}=3.3V$ ,  $V_{CCQ}=1.8V$ .
2. Performance numbers might be subject to changes without notice.
3. The write cache size is [192KB](#).

### 1.2 Typical Sequential Sustained Performance (Normal Status)

| Speed Mode & Operation |                 |       | 8GB | Unit |
|------------------------|-----------------|-------|-----|------|
| HS400                  | Write Cache On  | Read  | 320 | MB/s |
|                        |                 | Write | 135 | MB/s |
|                        | Write Cache Off | Read  | 320 | MB/s |
|                        |                 | Write | 125 | MB/s |
| HS200                  | Write Cache On  | Read  | 175 | MB/s |
|                        |                 | Write | 135 | MB/s |
|                        | Write Cache Off | Read  | 175 | MB/s |
|                        |                 | Write | 120 | MB/s |

**Notes:**

1. Values for an 8-bit bus width, running HS400 mode,  $V_{CC}=3.3V$ ,  $V_{CCQ}=1.8V$ .
2. Performance numbers might be subject to changes without notice.
3. The write cache size is [192KB](#).

**1.3 Typical Random Burst Performance (PSA Pseudo SLC Burst Status)**

| Speed Mode & Operation |                 |       | 8GB    | Unit |
|------------------------|-----------------|-------|--------|------|
| HS400                  | Write Cache On  | Read  | 24,000 | IOPS |
|                        |                 | Write | 28,000 | IOPS |
|                        | Write Cache Off | Read  | 24,000 | IOPS |
|                        |                 | Write | 2,400  | IOPS |
| HS200                  | Write Cache On  | Read  | 24,000 | IOPS |
|                        |                 | Write | 28,000 | IOPS |
|                        | Write Cache Off | Read  | 24,000 | IOPS |
|                        |                 | Write | 2,300  | IOPS |

**Notes:**

1. Values for an 8-bit bus width, running ISSI proprietary tool,  $V_{CC}=3.3V$ ,  $V_{CCQ}=1.8V$ .
2. Performance numbers might be subject to changes without notice.
3. The write cache size is [192KB](#).

**1.4 Typical Random Sustained Performance (Normal Status)**

| Speed Mode & Operation |                 |       | 8GB    | Unit |
|------------------------|-----------------|-------|--------|------|
| HS400                  | Write Cache On  | Read  | 24,000 | IOPS |
|                        |                 | Write | 28,400 | IOPS |
|                        | Write Cache Off | Read  | 24,000 | IOPS |
|                        |                 | Write | 2,400  | IOPS |
| HS200                  | Write Cache On  | Read  | 24,000 | IOPS |
|                        |                 | Write | 28,500 | IOPS |
|                        | Write Cache Off | Read  | 24,000 | IOPS |
|                        |                 | Write | 2,300  | IOPS |

**Notes:**

1. Values for an 8-bit bus width, running ISSI proprietary tool,  $V_{CC}=3.3V$ ,  $V_{CCQ}=1.8V$ .
2. Performance numbers might be subject to changes without notice.
3. The write cache size is [192KB](#).

**1.5 Device Power Consumption RMS  $V_{CC}/V_{CCQ}$  ( $T_A = 25^\circ\text{C}$  @ 3.3V/1.8V)**

| Speed Mode & Operation |       |                  | 8GB | Unit |
|------------------------|-------|------------------|-----|------|
| HS400                  | Read  | I <sub>CC</sub>  | 55  | mA   |
|                        |       | I <sub>CCQ</sub> | 220 | mA   |
|                        | Write | I <sub>CC</sub>  | 55  | mA   |
|                        |       | I <sub>CCQ</sub> | 120 | mA   |
| HS200                  | Read  | I <sub>CC</sub>  | 40  | mA   |
|                        |       | I <sub>CCQ</sub> | 220 | mA   |
|                        | Write | I <sub>CC</sub>  | 55  | mA   |
|                        |       | I <sub>CCQ</sub> | 120 | mA   |

**Notes:**

1. The measurement for RMS current is done as average RMS current consumption over a period of 100ms.
2. Current numbers might be subject to changes without notice.

**1.6 Device Power Consumption Standby  $V_{CC}/V_{CCQ}$  ( $T_A = 25^\circ\text{C}$  @ 3.3V/1.8V)**

| Speed Mode & Operation |                          |  | 8GB | Unit |
|------------------------|--------------------------|--|-----|------|
| HS400                  | CMD5 Sleep               |  | 190 | uA   |
|                        | Standby I <sub>CCQ</sub> |  | 240 | uA   |
|                        | Standby I <sub>CC</sub>  |  | 30  | uA   |
| HS200                  | CMD5 Sleep               |  | 190 | uA   |
|                        | Standby I <sub>CCQ</sub> |  | 240 | uA   |
|                        | Standby I <sub>CC</sub>  |  | 30  | uA   |

**Notes:**

1. The current is measured at  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CCQ} = 1.8V \pm 5\%$ , 8-bit bus width without clock frequency..
2. Current numbers might be subject to changes without notice.

**1.7 BOOT PARTITION AND RPMB (REPLAY PROTECTED MEMORY BLOCK)**

| Option   | Boot partition 1 | Boot partition 2 | RPMB     |
|----------|------------------|------------------|----------|
| <b>J</b> | 4,096 KB         | 4,096 KB         | 4,096 KB |
| <b>B</b> | 16,384 KB        | 16,384 KB        | 4,096 KB |

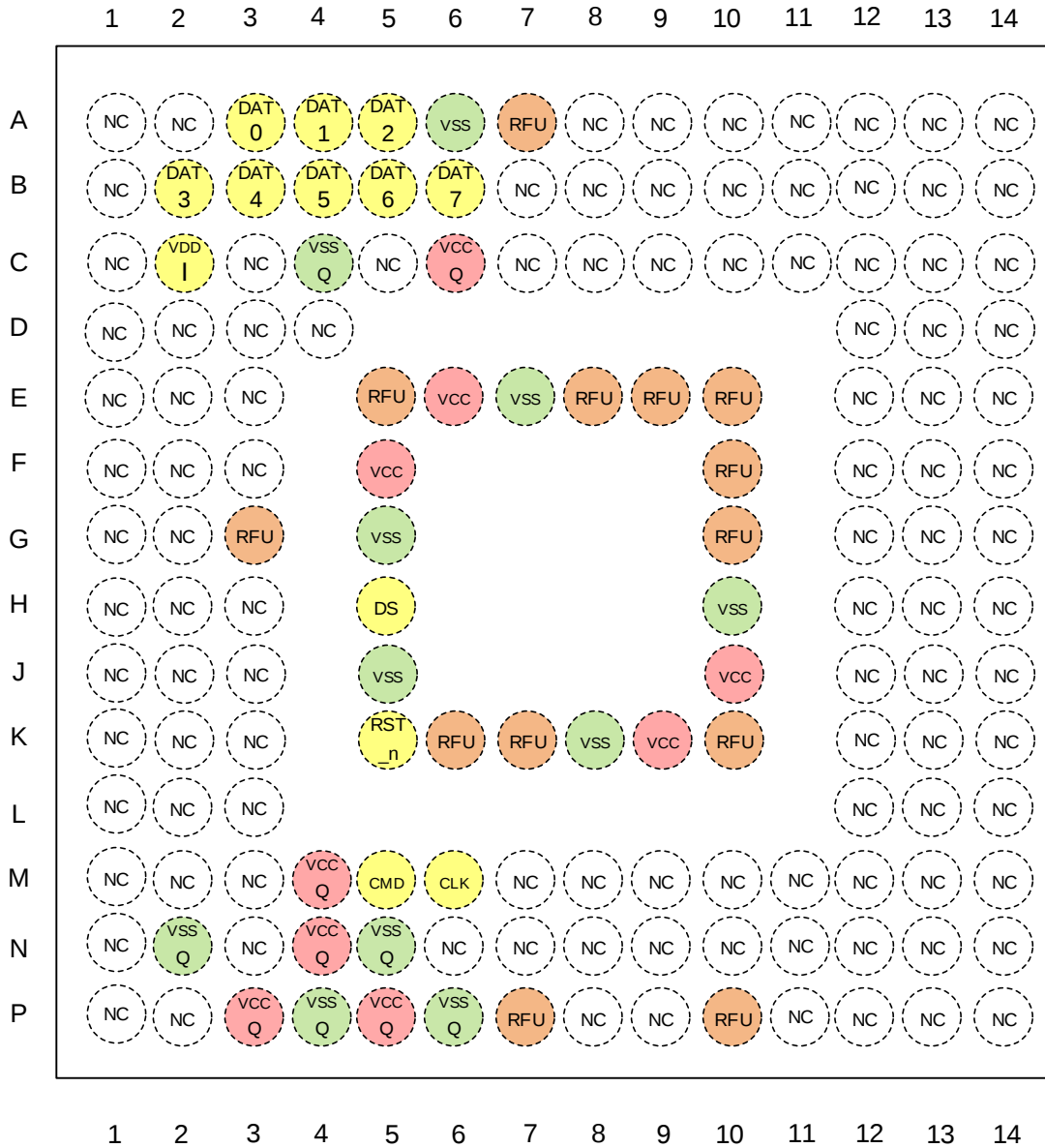
**1.8 USER DENSITY**

Total user density depends on device type (Flash Mode).

| Part Number         | Capacity | Flash Mode | User Density Size   |
|---------------------|----------|------------|---------------------|
| <b>IS/2122TF08G</b> | 8GB      | pSLC       | 7,817,134,080 Bytes |

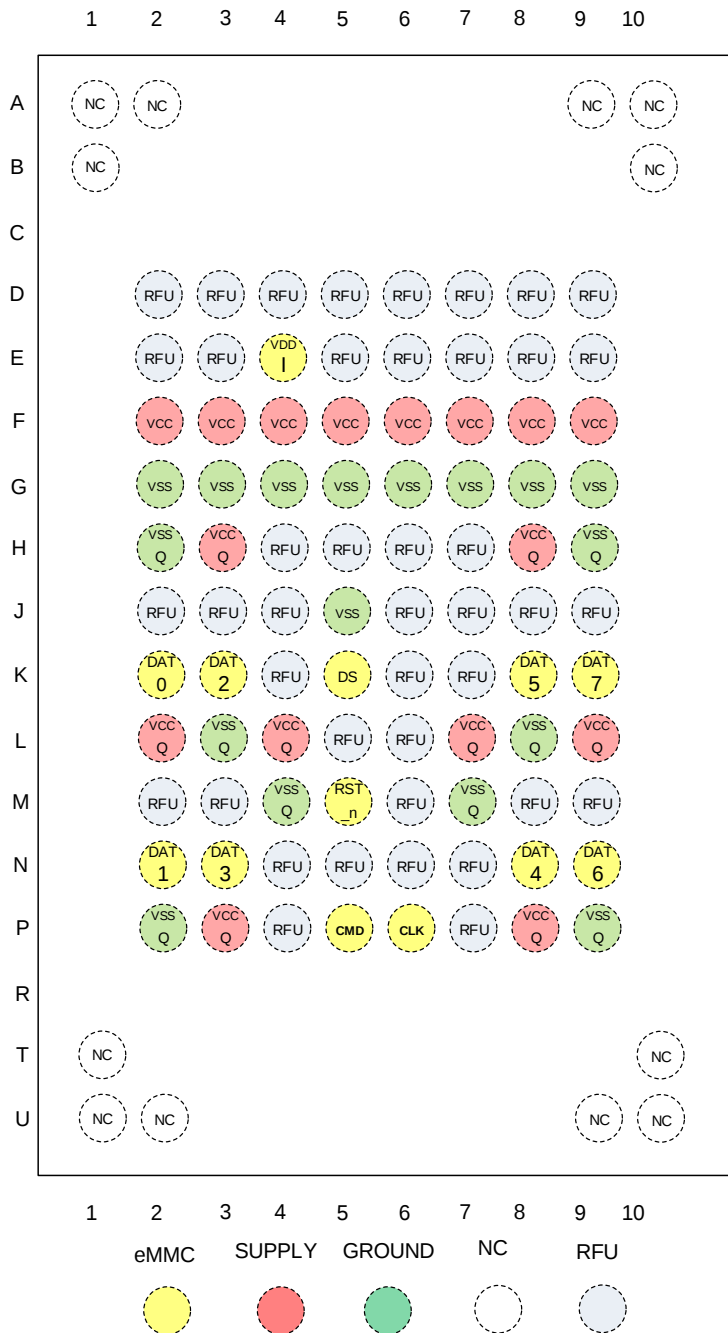
## 2. PIN CONFIGURATION and DDESCRIPTORS

153 FBGA Top View (Ball Down)



**Note:**

1. H5 (DS), A6 (VSS) and J5 (VSS) can be left floating if HS400 mode is not used.

**100 FBGA Top View (Ball Down)**

**Note:**

1. K5 (DS) and J5 (VSS) can be left floating if HS400 mode is not used.

**PIN DESCRIPTIONS**

| Pin Name  | Description                                                                        |
|-----------|------------------------------------------------------------------------------------|
| CLK       | Clock Signal                                                                       |
| DAT0~DAT7 | Data Bus                                                                           |
| CMD       | Command Signal                                                                     |
| RST#      | Hardware Reset Signal                                                              |
| DS        | Data Strobe Signal, used in HS400 mode.                                            |
| VDDI      | Connect capacitor from VDDI to GND for stabilize internal power.                   |
| VCC       | Supply voltage for controller and Flash memory power.                              |
| VCCQ      | Supply voltage for controller and Flash memory I/O power.                          |
| VSS       | Supply voltage ground for controller and Flash memory. Can be short with VSSQ.     |
| VSSQ      | Supply voltage ground for controller and Flash memory I/O. Can be short with VSSQ. |
| RFU       | Reserved For Future Use. Left it floating for future use.                          |
| NC        | In eMMC chip is no connect. Left it floating.                                      |

**Note:**

1. I: input; O: output; PP: push-pull; OD: open-drain; NC: Not connected (or logical high); S: power

### 3. OPERATING and STORAGE TEMPERATURE

| Grade      | Condition                                                    | Temperature      |
|------------|--------------------------------------------------------------|------------------|
| Industrial | Minimum and Maximum Ambient Temperature <sup>(1)</sup>       | -40 °C to 85 °C  |
|            | Maximum Case Temperature <sup>(1)</sup>                      | 95 °C            |
|            | Minimum and Maximum Non-operating Temperature <sup>(2)</sup> | -40 °C to 85 °C  |
| Auto (A1)  | Minimum and Maximum Ambient Temperature <sup>(1)</sup>       | -40 °C to 85 °C  |
|            | Maximum Case Temperature <sup>(1)</sup>                      | 95 °C            |
|            | Minimum and Maximum Non-operating Temperature <sup>(2)</sup> | -40 °C to 85 °C  |
| Auto (A2)  | Minimum and Maximum Ambient Temperature <sup>(1)</sup>       | -40 °C to 105 °C |
|            | Maximum Case Temperature <sup>(1)</sup>                      | 115 °C           |
|            | Minimum and Maximum Non-operating Temperature <sup>(2)</sup> | -40 °C to 105 °C |

**Notes:**

1. To achieve optimized and performance, case temperature should not exceed maximum ambient operating temperature.
2. After being soldered onto PCBA.

#### 4. eMMC Device and System

eMMC consists of a single chip MMC controller and NAND flash memory module. The micro-controller interfaces with a host system allowing data to be written to and read from the NAND flash memory module. The controller allows the host to be independent from details of erasing and programming the flash memory.

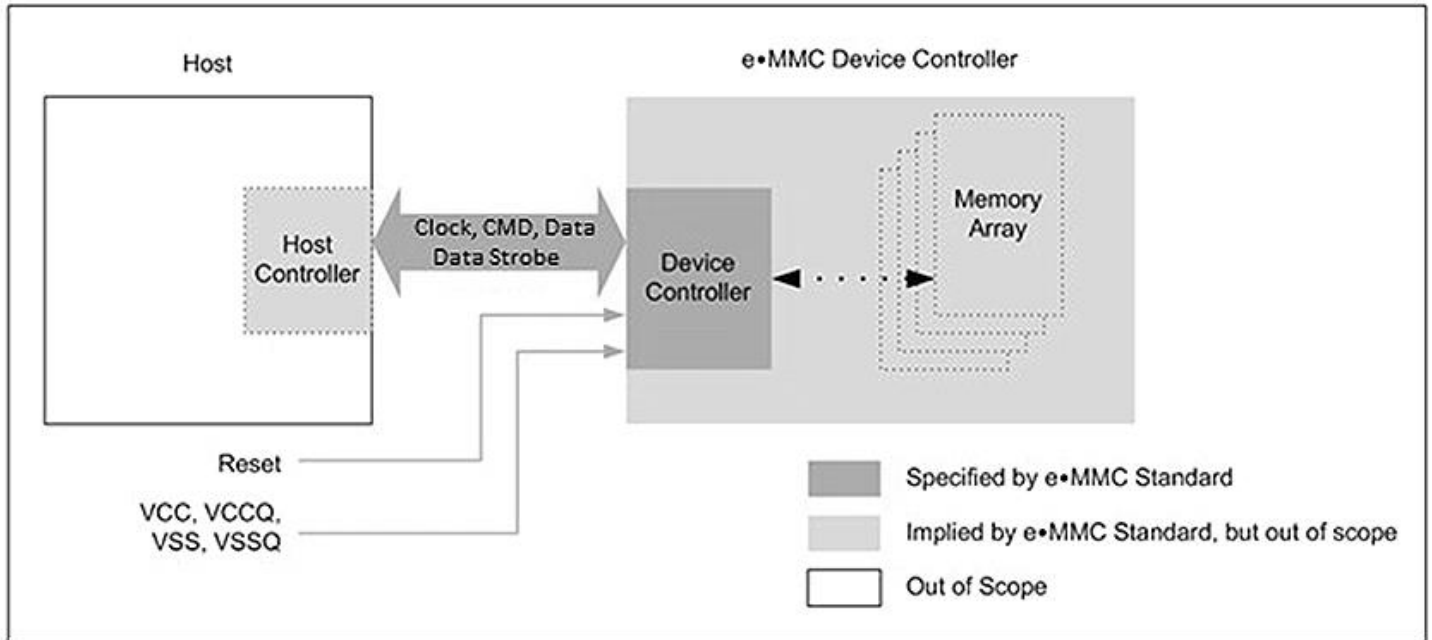


Figure 4.1 eMMC System Overview

##### 4.1 Memory Addressing

Previous implementations of the eMMC specification are following byte addressing with 32-bit field. This addressing mechanism permitted for eMMC densities up to and including 2 GB.

To support larger density, the addressing mechanism was update to support sector addresses (512 B sectors). The sector addresses shall be used for all devices with capacity larger than 2 GB.

To determine the addressing mode, use the host should read bit [30:29] in the OCR register.

## 5. REGISTER SETTINGS

Within the Device interface six registers are defined: OCR, CID, CSD, EXT\_CSD, RCA and DSR. These can be accessed only by corresponding commands (see Section 6.10 of JESD84-B51).

### 5.1 OCR Register

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of the Device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the Device power up procedure has been finished. The OCR register shall be implemented by all Devices.

**Table 5.1 OCR Register**

| VCCQ Voltage Window                              | Width (Bits) | OCR Bit | OCR Value         |
|--------------------------------------------------|--------------|---------|-------------------|
| Device power up status bit (busy) <sup>(1)</sup> | 1            | [31]    | Note 1            |
| Access Mode                                      | 2            | [30:29] | 10b (sector mode) |
| Reserved                                         | 5            | [28:24] | 0 0000b           |
| VCCQ: 2.7 – 3.6V                                 | 9            | [23:15] | 1 1111 1111b      |
| VCCQ: 2.0 – 2.6V                                 | 7            | [14:8]  | 000 0000b         |
| VCCQ: 1.7 – 1.95V                                | 1            | [7]     | 1b                |
| Reserved                                         | 7            | [6:0]   | 000 0000b         |

**Note:**

1. This bit is set to LOW if the device has not finished the power up routine.

### 5.2 CID Register

The Card Identification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase (eMMC protocol).

**Table 5.2 CID Register**

| Name                  | Field |     | Width (Bits) | CID Bits  | CID Value            |
|-----------------------|-------|-----|--------------|-----------|----------------------|
| Manufacturer ID       | MID   |     | 8            | [127:120] | 9Dh                  |
| Reserved              | -     |     | 6            | [119:114] | 0h                   |
| Device/BGA            | CBX   |     | 2            | [113:112] | 1h                   |
| OEM/application ID    | OID   |     | 8            | [111:104] | 1h                   |
| Product name          | PNM   | 8GB | 48           | [103:56]  | IS008G               |
| Product Revision      | PRV   |     | 8            | [55:48]   | 51h                  |
| Product Serial Number | PSN   |     | 32           | [47:16]   | Random by Production |
| Manufacturing Date    | MDT   |     | 8            | [15:8]    | Month, Year          |
| CRC7 Checksum         | CRC   |     | 7            | [7:1]     | - <sup>(1)</sup>     |
| Not used, always "1"  | -     |     | 1            | [0]       | 1h                   |

**Note:**

1. The description is same as e.MMC™ JEDEC standard.

### 5.3 CSD Register

The Card-Specific Data (CSD) register provides information on how to access the contents stored in eMMC. The CSD registers are used to define the error correction type, maximum data access time, data transfer speed, data format...etc. For details, refer to section 7.3 of the JEDEC Standard Specification No.JESD84-B51.

**Table 5.3 CSD Register**

| Name                                             | Field              | Width | Cell Type | CSD-slice | Value |
|--------------------------------------------------|--------------------|-------|-----------|-----------|-------|
| CSD structure                                    | CSD_STRUCTURE      | 2     | R         | [127:126] | 3h    |
| System specification version                     | SPEC_VERS          | 4     | R         | [125:122] | 4h    |
| Reserved                                         | -                  | 2     | R         | [121:120] | 0h    |
| Data read access-time 1                          | TAAC               | 8     | R         | [119:112] | 4Fh   |
| Data read access-time 2 in CLK cycles (NSAC*100) | NSAC               | 8     | R         | [111:104] | 1h    |
| Max. bus clock frequency                         | TRAN_SPEED         | 8     | R         | [103:96]  | 32h   |
| Device command classes                           | CCC                | 12    | R         | [95:84]   | 8F5h  |
| Max. read data block length                      | READ_BL_LEN        | 4     | R         | [83:80]   | 9h    |
| Partial blocks for read allowed                  | READ_BL_PARTIAL    | 1     | R         | [79:79]   | 0h    |
| Write block misalignment                         | WRITE_BLK_MISALIGN | 1     | R         | [78:78]   | 0h    |
| Read block misalignment                          | READ_BLK_MISALIGN  | 1     | R         | [77:77]   | 0h    |
| DSR implemented                                  | DSR_IMP            | 1     | R         | [76:76]   | 0h    |
| Reserved                                         | -                  | 2     | R         | [75:74]   | 0h    |
| Device size                                      | C_SIZE             | 12    | R         | [73:62]   | FFFh  |
| Max. read current @ VDD min                      | VDD_R_CURR_MIN     | 3     | R         | [61:59]   | 7h    |
| Max. read current @ VDD max                      | VDD_R_CURR_MAX     | 3     | R         | [58:56]   | 7h    |
| Max. write current @ VDD min                     | VDD_W_CURR_MIN     | 3     | R         | [55:53]   | 7h    |
| Max. write current @ VDD max                     | VDD_W_CURR_MAX     | 3     | R         | [52:50]   | 7h    |
| Device size multiplier                           | C_SIZE_MULT        | 3     | R         | [49:47]   | 7h    |
| Erase group size                                 | ERASE_GRP_SIZE     | 5     | R         | [46:42]   | 1Fh   |
| Erase group size multiplier                      | ERASE_GRP_MULT     | 5     | R         | [41:37]   | 1Fh   |
| Write protect group size                         | WP_GRP_SIZE        | 5     | R         | [36:32]   | 0Fh   |
| Write protect group enable                       | WP_GRP_ENABLE      | 1     | R         | [31:31]   | 1h    |
| Manufacturer default ECC                         | DEFAULT_ECC        | 2     | R         | [30:29]   | 0h    |
| Write speed factor                               | R2W_FACTOR         | 3     | R         | [28:26]   | 2h    |
| Max. write data block length                     | WRITE_BL_LEN       | 4     | R         | [25:22]   | 9h    |
| Partial blocks for write allowed                 | WRITE_BL_PARTIAL   | 1     | R         | [21:21]   | 0h    |
| Reserved                                         | -                  | 4     | R         | [20:17]   | 0h    |

| Name                           | Field              | Width | Cell Type | CSD-slice | Value |
|--------------------------------|--------------------|-------|-----------|-----------|-------|
| Content protection application | CONTENT_PROT_APP   | 1     | R         | [16:16]   | 0h    |
| File format group              | FILE_FORMAT_GRP    | 1     | R/W       | [15:15]   | 0h    |
| Copy flag (OTP)                | COPY               | 1     | R/W       | [14:14]   | 0h    |
| Permanent write protection     | PERM_WRITE_PROTECT | 1     | R/W       | [13:13]   | 0h    |
| Temporary write protection     | TMP_WRITE_PROTECT  | 1     | R/W/E     | [12:12]   | 0h    |
| File format                    | FILE_FORMAT        | 2     | R/W       | [11:10]   | 0h    |
| ECC code                       | ECC                | 2     | R/W/E     | [9:8]     | 0h    |
| CRC                            | CRC                | 7     | R/W/E     | [7:1]     | 2Eh   |
| Not used, always '1'           | -                  | 1     | -         | [0:0]     | 1h    |

## 5.4 Extended CSD Register

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command.

**Table 5.4 ECSD Register**

| Name                                      | Field                                     | Size (Bytes) | CSD-slice | Value |
|-------------------------------------------|-------------------------------------------|--------------|-----------|-------|
| Properties Segment                        |                                           |              |           |       |
| Reserved                                  | –                                         | 6            | [511:506] | 0h    |
| Extended Security Commands Error          | EXT_SECURITY_ERR                          | 1            | [505]     | 0h    |
| Supported Command Sets                    | S_CMD_SET                                 | 1            | [504]     | 1h    |
| HPI features                              | HPI_FEATURES                              | 1            | [503]     | 1h    |
| Background operations support             | BKOPS_SUPPORT                             | 1            | [502]     | 1h    |
| Max packed read commands                  | MAX_PACKED_READS                          | 1            | [501]     | 20h   |
| Max packed write commands                 | MAX_PACKED_WRITES                         | 1            | [500]     | 20h   |
| Data Tag Support                          | DATA_TAG_SUPPORT                          | 1            | [499]     | 1h    |
| Tag Unit Size                             | TAG_UNIT_SIZE                             | 1            | [498]     | 3h    |
| Tag Resources Size                        | TAG_RES_SIZE                              | 1            | [497]     | 0h    |
| Context management capabilities           | CONTEXT_CAPABILITIES                      | 1            | [496]     | 5h    |
| Large Unit size                           | LARGE_UNIT_SIZE_M1                        | 1            | [495]     | 18h   |
| Extended partitions attribute support     | EXT_SUPPORT                               | 1            | [494]     | 3h    |
| Supported modes                           | SUPPORTED_MODES                           | 1            | [493]     | 3h    |
| FFU features                              | FFU_FEATURES                              | 1            | [492]     | 0h    |
| Operation codes timeout                   | OPERATION_CODE_TIME_OUT                   | 1            | [491]     | 0h    |
| FFU Argument                              | FFU_ARG                                   | 4            | [490:487] | 0h    |
| Barrier support                           | BARRIER_SUPPORT                           | 1            | [486]     | 0h    |
| Reserved                                  | Reserved                                  | 177          | [485:309] | 0h    |
| CMDQ support                              | CMDQ_SUPPORT                              | 1            | [308]     | 1h    |
| CMDQ depth                                | CMDQ_DEPTH                                | 1            | [307]     | 1Fh   |
| Reserved                                  | Reserved                                  | 1            | [306]     | 0h    |
| Number of FW sectors correctly programmed | NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED | 4            | [305:302] | 0h    |
| Vendor proprietary health report          | VENDOR_PROPRIETARY_HEALTH_REPORT          | 32           | [301:270] | –     |
| Device life time estimation type B        | DEVICE_LIFE_TIME_EST_TYP_B                | 1            | [269]     | 1h    |
| Device life time estimation type A        | DEVICE_LIFE_TIME_EST_TYP_A                | 1            | [268]     | 1h    |
| Pre EOL information                       | PRE_EOL_INFO                              | 1            | [267]     | 1h    |
| Optimal read size                         | OPTIMAL_READ_SIZE                         | 1            | [266]     | 1h    |
| Optimal write size                        | OPTIMAL_WRITE_SIZE                        | 1            | [265]     | 8h    |

| Name                                                    | Field                     | Size (Bytes) | CSD-slice | Value      |
|---------------------------------------------------------|---------------------------|--------------|-----------|------------|
| Optimal trim unit size                                  | OPTIMAL_TRIM_UNIT_SIZE    | 1            | [264]     | 1h         |
| Device version                                          | DEVICE_VERSION            | 2            | [263:262] | 0h         |
| Firmware version                                        | FIRMWARE_VERSION          | 8            | [261:254] | – (note 5) |
| Power class for 200MHz, DDR at VCC=3.6V                 | PWR_CL_DDR_200_360        | 1            | [253]     | 0h         |
| Cache size                                              | CACHE_SIZE                | 4            | [252:249] | 600h       |
| Generic CMD6 timeout                                    | GENERIC_CMD6_TIME         | 1            | [248]     | Ah         |
| Power off notification(long) timeout                    | POWER_OFF_LONG_TIME       | 1            | [247]     | 32h        |
| Background operations status                            | BKOPS_STATUS              | 1            | [246]     | 0h         |
| Number of correctly programmed sectors                  | CORRECTLY_PRG_SECTORS_NUM | 4            | [245:242] | 0h         |
| 1st initialization time after partitioning              | INI_TIMEOUT_AP            | 1            | [241]     | 1Eh        |
| Cache Flushing Policy                                   | CACHE_FLUSH_POLICY        | 1            | [240]     | 1h         |
| Power class for 52MHz, DDR at 3.6V                      | PWR_CL_DDR_52_360         | 1            | [239]     | 0h         |
| Power class for 52MHz, DDR at 1.95V                     | PWR_CL_DDR_52_195         | 1            | [238]     | 0h         |
| Power class for 200MHz at 3.6V                          | PWR_CL_200_360            | 1            | [237]     | 0h         |
| Power class for 200MHz, at 1.95V                        | PWR_CL_200_195            | 1            | [236]     | 0h         |
| Minimum Write Performance for 8bit at 52MHz in DDR mode | MIN_PERF_DDR_W_8_52       | 1            | [235]     | 4Bh        |
| Minimum Read Performance for 8bit at 52MHz in DDR mode  | MIN_PERF_DDR_R_8_52       | 1            | [234]     | 0h         |
| Reserved                                                | –                         | 1            | [233]     | 0h         |
| TRIM Multiplier                                         | TRIM_MULT                 | 1            | [232]     | 12h        |
| Secure Feature support                                  | SEC_FEATURE_SUPPORT       | 1            | [231]     | 55h        |
| Secure Erase Multiplier                                 | SEC_ERASE_MULT            | 1            | [230]     | 64h        |
| Secure TRIM Multiplier                                  | SEC_TRIM_MULT             | 1            | [229]     | 64h        |
| Boot information                                        | BOOT_INFO                 | 1            | [228]     | 7h         |
| Reserved                                                | –                         | 1            | [227]     | 0h         |
| Boot partition size                                     | BOOT_SIZE_MULT            | J-option     | [226]     | 20h        |
|                                                         |                           | B-option     |           | 80h        |
| Access size                                             | ACC_SIZE                  | 1            | [225]     | 7h         |
| High-capacity erase unit size                           | HC_ERASE_GRP_SIZE         | 1            | [224]     | 1h         |
| High-capacity erase timeout                             | ERASE_TIMEOUT_MULT        | 1            | [223]     | 12h        |
| Reliable write sector count                             | REL_WR_SEC_C              | 1            | [222]     | 1h         |
| High-capacity write protect group size                  | HC_WP_GRP_SIZE            | 1            | [221]     | 10h        |
| Sleep current (VCC)                                     | S_C_VCC                   | 1            | [220]     | 8h         |

| Name                                                           | Field                              | Size (Bytes) | CSD-slice | Value    |
|----------------------------------------------------------------|------------------------------------|--------------|-----------|----------|
| Sleep current (VCCQ)                                           | S_C_VCCQ                           | 1            | [219]     | 8h       |
| Production state awareness Timeout                             | PRODUCTION_STATE_AWARENESS_TIMEOUT | 1            | [218]     | 0h       |
| Sleep/awake timeout                                            | S_A_TIMEOUT                        | 1            | [217]     | 15h      |
| Sleep Notification timeout                                     | SLEEP_NOTIFICATION_TIME            | 1            | [216]     | Fh       |
| Sector Count                                                   | SEC_COUNT                          | 4            | [215:212] | 15267840 |
| Security write protect information                             | SECURE_WP_INFO                     | 1            | [211]     | 1h       |
| Minimum Write Performance for 8bit at 52MHz                    | MIN_PERF_W_8_52                    | 1            | [210]     | 4Bh      |
| Minimum Read Performance for 8bit at 52MHz                     | MIN_PERF_R_8_52                    | 1            | [209]     | 0h       |
| Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz | MIN_PERF_W_8_26_4_52               | 1            | [208]     | 2Bh      |
| Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz  | MIN_PERF_R_8_26_4_52               | 1            | [207]     | 0h       |
| Minimum Write Performance for 4bit at 26MHz                    | MIN_PERF_W_4_26                    | 1            | [206]     | 1Eh      |
| Minimum Read Performance for 4bit at 26MHz                     | MIN_PERF_R_4_26                    | 1            | [205]     | 0h       |
| Reserved                                                       | –                                  | 1            | [204]     | 0h       |
| Power class for 26MHz at 3.6V 1 R                              | PWR_CL_26_360                      | 1            | [203]     | 0h       |
| Power class for 52MHz at 3.6V 1 R                              | PWR_CL_52_360                      | 1            | [202]     | 0h       |
| Power class for 26MHz at 1.95V 1 R                             | PWR_CL_26_195                      | 1            | [201]     | 0h       |
| Power class for 52MHz at 1.95V 1 R                             | PWR_CL_52_195                      | 1            | [200]     | 0h       |
| Partition switching timing                                     | PARTITION_SWITCH_TIME              | 1            | [199]     | 3h       |
| Out-of-interrupt busy timing                                   | OUT_OF_INTERRUPT_TIME              | 1            | [198]     | Ah       |
| I/O Driver Strength                                            | DRIVER_STRENGTH                    | 1            | [197]     | 1Fh      |
| Device type                                                    | CARD_TYPE                          | 1            | [196]     | 57h      |
| Reserved                                                       | –                                  | 1            | [195]     | 0h       |
| CSD structure version                                          | –                                  | 1            | [194]     | 2h       |
| Reserved                                                       | –                                  | 1            | [193]     | 0h       |
| Extended CSD revision                                          | EXT_CSD_REV                        | 1            | [192]     | 8h       |
| Modes Segment                                                  |                                    |              |           |          |
| Command set                                                    | CMD_SET                            | 1            | [191]     | 0h       |
| Reserved                                                       | –                                  | 1            | [190]     | 0h       |

| Name                                   | Field                       | Size (Bytes) | CSD-slice | Value       |
|----------------------------------------|-----------------------------|--------------|-----------|-------------|
| Command set revision                   | CMD_SET_REV                 | 1            | [189]     | 0h          |
| Reserved                               | –                           | 1            | [188]     | 0h          |
| Power class                            | POWER_CLASS                 | 1            | [187]     | 0h          |
| Reserved                               | –                           | 1            | [186]     | 0h          |
| High-speed interface timing            | HS_TIMING                   | 1            | [185]     | 1h (note 3) |
| Strobe support                         | STROBE_SUPPORT              | 1            | [184]     | 1h          |
| Bus width mode                         | BUS_WIDTH                   | 1            | [183]     | 2h (note 4) |
| Reserved                               | –                           | 1            | [182]     | 0h          |
| Erased memory content                  | ERASED_MEM_CONT             | 1            | [181]     | 0h          |
| Reserved                               | –                           | 1            | [180]     | 0h          |
| Partition configuration                | PARTITION_CONFIG            | 1            | [179]     | 0h          |
| Boot config protection                 | BOOT_CONFIG_PROT            | 1            | [178]     | 0h          |
| Boot bus Conditions                    | BOOT_BUS_CONDITIONS         | 1            | [177]     | 0h          |
| Reserved                               | –                           | 1            | [176]     | 0h          |
| High-density erase group definition    | ERASE_GROUP_DEF             | 1            | [175]     | 0h          |
| Boot write protection status registers | BOOT_WP_STATUS              | 1            | [174]     | 0h          |
| Boot area write protection register    | BOOT_WP                     | 1            | [173]     | 0h          |
| Reserved                               | –                           | 1            | [172]     | 0h          |
| User area write protection register    | USER_WP                     | 1            | [171]     | 0h          |
| Reserved                               | –                           | 1            | [170]     | 1Eh         |
| FW configuration                       | FW_CONFIG                   | 1            | [169]     | 0h          |
| RPMB Size                              | RPMB_SIZE_MULT              | 1            | [168]     | 20h         |
| Write reliability setting register     | WR_REL_SET                  | 1            | [167]     | 1Fh         |
| Write reliability parameter register   | WR_REL_PARAM                | 1            | [166]     | 15h         |
| Start Sanitize operation               | SANITIZE_START              | 1            | [165]     | 0h          |
| Manually start background operations   | BKOPS_START                 | 1            | [164]     | 0h          |
| Enable background operations handshake | BKOPS_EN                    | 1            | [163]     | 2h          |
| H/W reset function                     | RST_n_FUNCTION              | 1            | [162]     | 0h          |
| HPI management                         | HPI_MGMT                    | 1            | [161]     | 0h          |
| Partitioning Support                   | PARTITIONING_SUPPORT        | 1            | [160]     | 7h          |
| Max Enhanced Area Size                 | MAX_ENH_SIZE_MULT           | 3            | [159:157] | 3A8h        |
| Partitions attribute                   | PARTITIONS_ATTRIBUTE        | 1            | [156]     | 1h          |
| Partitioning Setting                   | PARTITION_SETTING_COMPLETED | 1            | [155]     | 1h          |

| Name                                                     | Field                       | Size (Bytes) | CSD-slice | Value |
|----------------------------------------------------------|-----------------------------|--------------|-----------|-------|
| General Purpose Partition Size                           | GP_SIZE_MULT 4              | 3            | [154:152] | 0h    |
| General Purpose Partition Size                           | GP_SIZE_MULT3               | 3            | [151:149] | 0h    |
| General Purpose Partition Size                           | GP_SIZE_MULT2               | 3            | [148:146] | 0h    |
| General Purpose Partition Size                           | GP_SIZE_MULT1               | 3            | [145:143] | 0h    |
| Enhanced User Data Area Size                             | ENH_SIZE_MULT               | 3            | [142:140] | 3A8h  |
| Enhanced User Data Start Address                         | ENH_START_ADDR              | 4            | [139:136] | 0h    |
| Reserved                                                 | –                           | 1            | [135]     | 0h    |
| Bad Block Management mode                                | SEC_BAD_BLK_MGMNT           | 1            | [134]     | 0h    |
| Production state awareness                               | PRODUCTION_STATE_AWARENESS  | 1            | [133]     | 0h    |
| Package Case Temperature is controlled                   | TCASE_SUPPORT               | 1            | [132]     | 0h    |
| Periodic Wake-up                                         | PERIODIC_WAKEUP             | 1            | [131]     | 0h    |
| Program CID/CSD in DDR mode support                      | PROGRAM_CID_CSD_DDR_SUPPORT | 1            | [130]     | 1h    |
| Reserved                                                 | –                           | 2            | [129:128] | 0h    |
| Vendor Specific Fields                                   | VENDOR_SPECIFIC_FIELD       | 61           | [127:67]  | –     |
| Error code                                               | ERROR_CODE                  | 2            | [66:65]   | 0h    |
| Error type                                               | ERROR_TYPE                  | 1            | [64]      | 0h    |
| Native sector size                                       | NATIVE_SECTOR_SIZE          | 1            | [63]      | 0h    |
| Sector size emulation                                    | USE_NATIVE_SECTOR           | 1            | [62]      | 0h    |
| Sector size                                              | DATA_SECTOR_SIZE            | 1            | [61]      | 0h    |
| 1st initialization after disabling sector size emulation | INI_TIMEOUT_EMU             | 1            | [60]      | 0h    |
| Class 6 commands control                                 | CLASS_6_CTRL                | 1            | [59]      | 0h    |
| Number of addressed group to be Released                 | DYNCAP_NEEDED               | 1            | [58]      | 0h    |
| Exception events control                                 | EXCEPTION_EVENTS_CTRL       | 2            | [57:56]   | 0h    |
| Exception events status                                  | EXCEPTION_EVENTS_STATUS     | 2            | [55:54]   | 0h    |
| Extended Partitions Attribute                            | EXT_PARTITIONS_ATTRIBUTE    | 2            | [53:52]   | 0h    |
| Context configuration                                    | CONTEXT_CONF                | 15           | [51:37]   | -     |
| Packed command status                                    | PACKED_COMMAND_STATUS       | 1            | [36]      | 0h    |
| Packed command failure index                             | PACKED_FAILURE_INDEX        | 1            | [35]      | 0h    |
| Power Off Notification                                   | POWER_OFF_NOTIFICATION      | 1            | [34]      | 0h    |
| Control to turn the Cache ON/OFF                         | CACHE_CTRL                  | 1            | [33]      | 0h    |
| Flushing of the cache                                    | FLUSH_CACHE                 | 1            | [32]      | 0h    |
| Reserved                                                 | Reserved                    | 1            | [31]      | 0h    |
| Mode config                                              | MODE_CONFIG                 | 1            | [30:30]   | 0h    |

| Name                               | Field                              | Size (Bytes) | CSD-slice | Value   |
|------------------------------------|------------------------------------|--------------|-----------|---------|
| Mode operation codes               | MODE_OPERATION_CODES               | 1            | [29:29]   | 0h      |
| Reserved                           | Reserved                           | 2            | [28:27]   | 0h      |
| FFU status                         | FFU_STATUS                         | 1            | [26:26]   | 0h      |
| Per loading data size              | PRE_LOADING_DATA_SIZE              | 4            | [25:22]   | 0h      |
| Max pre loading data size          | MAX_PRE_LOADING_DATA_SIZE          | 4            | [21:18]   | 4843520 |
| Product state awareness enablement | PRODUCT_STATE_AWARENESS_ENABLEMENT | 1            | [17:17]   | 1h      |
| Secure removal type                | SECURE_REMOVAL_TYPE                | 1            | [16:16]   | 01h     |
| Command Queue Mode enable          | CMQ_MODE_EN                        | 1            | [15:15]   | 0h      |
| Reserved                           | Reserved                           | 15           | [14:0]    | 0h      |

**Notes:**

1. Reserved bits should read as "0".
2. Obsolete values should be don't care.
3. This field is 0 after power-on, H/W reset or software reset, thus selecting the backwards compatible interface timing for the Device. If the host sets 1 to this field, the Device changes the timing to high speed interface timing (see Section 10.6.1 of JESD84-B50). If the host sets value 2, the Device changes its timing to HS200 interface timing (see Section 10.8.1 of JESD854-B50). If the host sets HS\_TIMING [3:0] to 0x3, the device changes it's timing to HS400 interface timing (see 10.10).
4. It is set to "0" (1bit data bus) after power up and can be changed by a SWITCH command.
5. Could be changed by Firmware release note.

## 6. The eMMC BUS

The eMMC bus has ten communication lines and three supply lines:

- CMD : Command is a bidirectional signal. The host and Device drivers are operating in two modes, open drain and push/pull.
- DAT0-7 : Data lines are bidirectional signals. Host and Device drivers are operating in push-pull mode
- CLK : Clock is a host to Device signal. CLK operates in push-pull mode
- Data Strobe: Data Strobe is a Device to host signal. Data Strobe operates in push-pull mode.

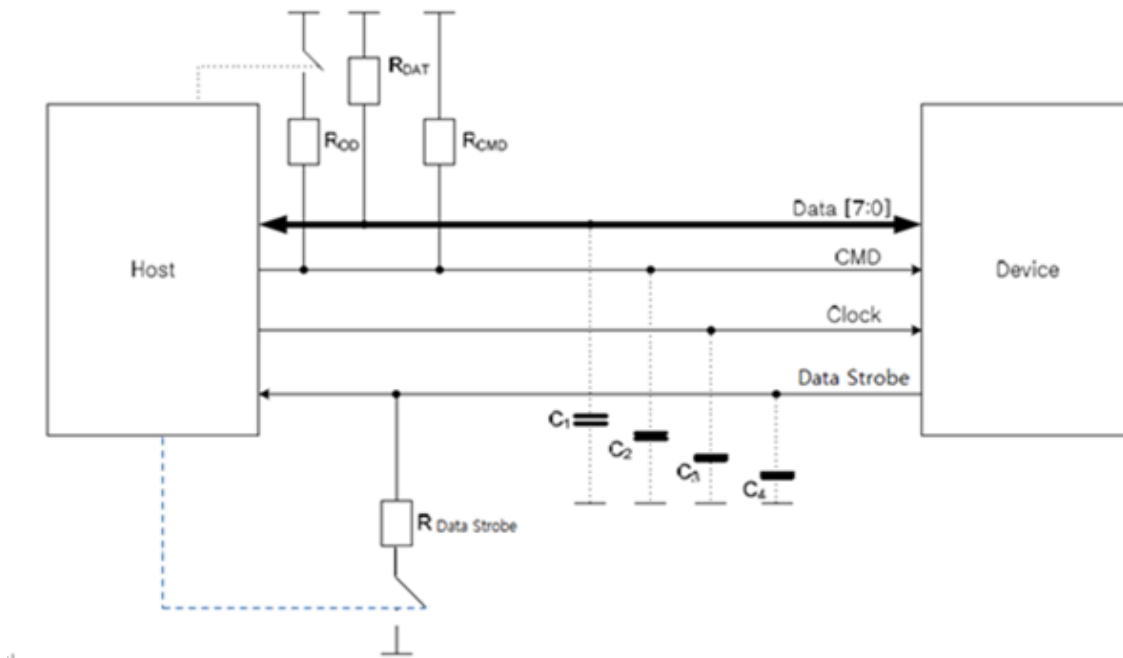


Figure 6.1 BUS Circuitry Diagram

The  $R_{OD}$  is switched on and off by the host synchronously to the open-drain and push-pull mode transitions. The host does not have to have open drain drivers, but must recognize this mode to switch on the  $R_{OD}$ .  $R_{DAT}$  and  $R_{CMD}$  are pull-up resistors protecting the CMD and the DAT lines against bus floating device when all device drivers are in a high-impedance mode.

A constant current source can replace the  $R_{OD}$  by achieving a better performance (constant slopes for the signal rising and falling edges). If the host does not allow the switchable  $R_{OD}$  implementation, a fixed  $R_{CMD}$  can be used). Consequently the maximum operating frequency in the open drain mode has to be reduced if the used  $R_{CMD}$  value is higher than the minimal one given in.

$R_{Data\ strobe}$  is pull-down resistor used in HS400 device.

## 6.1 Power-up

### 6.1.1 eMMC power-up

The power up of the eMMC bus is handled locally in the Device and in the bus master. **Error! Reference source not found.** 6 shows the power-up sequence and is followed by specific instructions regarding the power-up sequence. Refer to section 10.1 of the JEDEC Standard Specification JESD84-B51 for specific instructions regarding the power-up sequence.

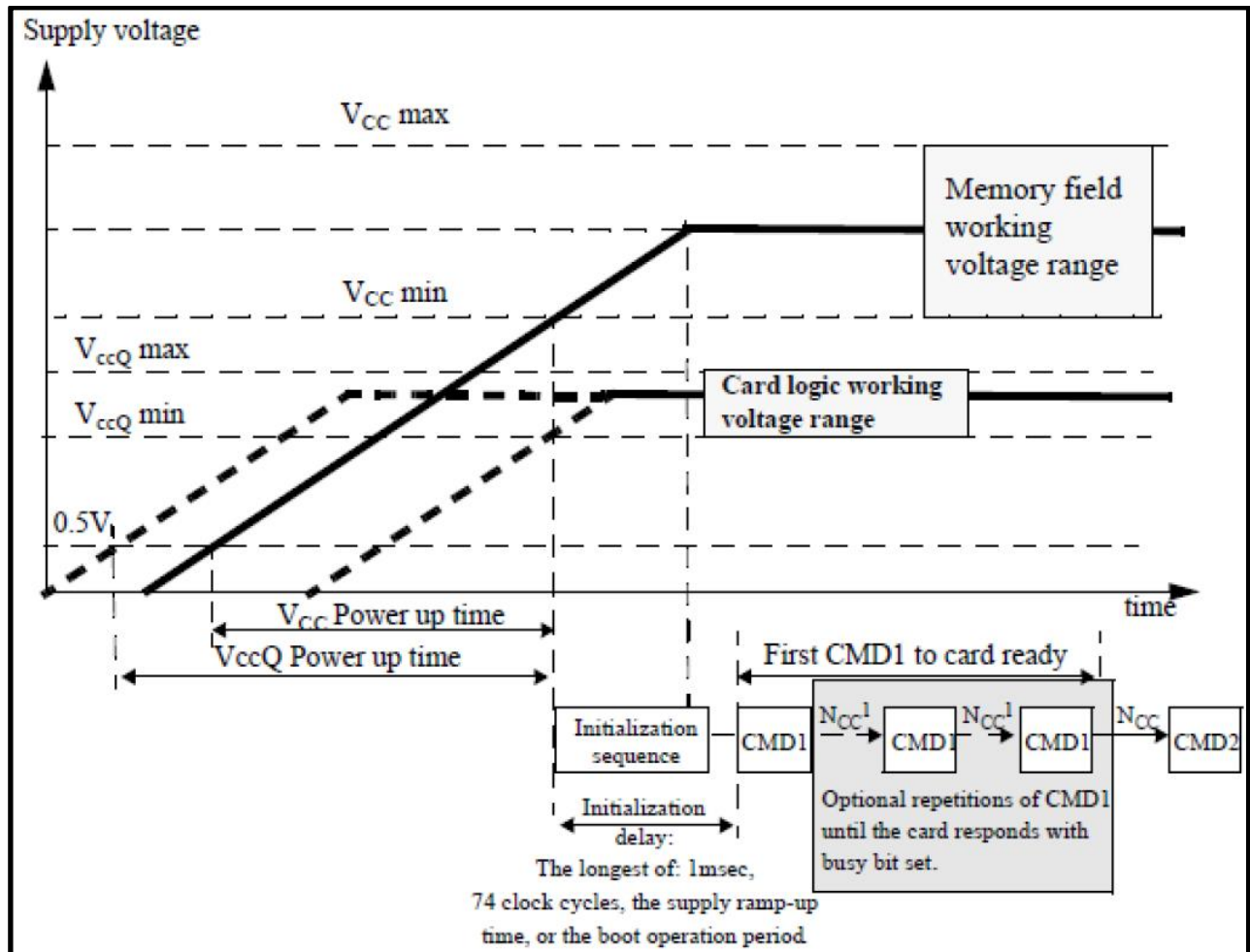


Figure 6.2 eMMC Power-Up Diagram

### 6.1.2 eMMC Power Cycling

The master can execute any sequence of  $V_{CC}$  and  $V_{CCQ}$  power-up/power-down. However, the master must not issue any commands until  $V_{CC}$  and  $V_{CCQ}$  are stable within each operating voltage range. After the slave enters sleep mode, the master can power-down  $V_{CC}$  to reduce power consumption. It is necessary for the slave to be ramped up to  $V_{CC}$  before the host issues CMD5 (SLEEP\_AWAKE) to wake the slave unit. For more information about power cycling see Section 10.1.3 of the JEDEC Standard Specification JESD84-B51.

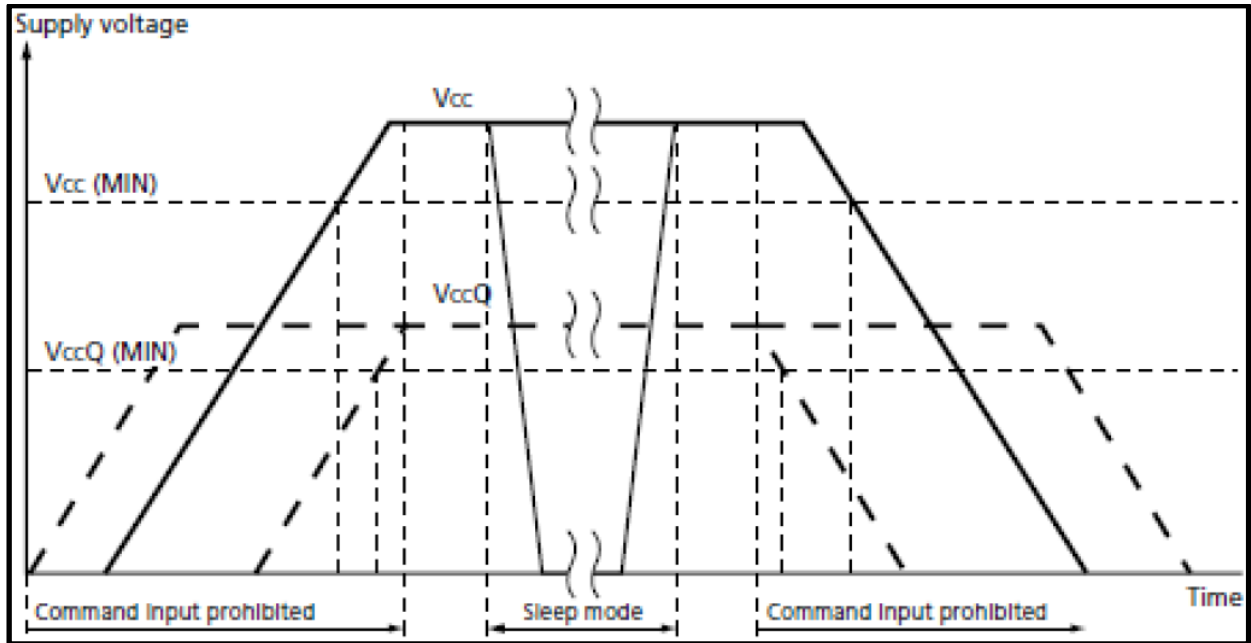


Figure 6.3 – The eMMC Power Cycle

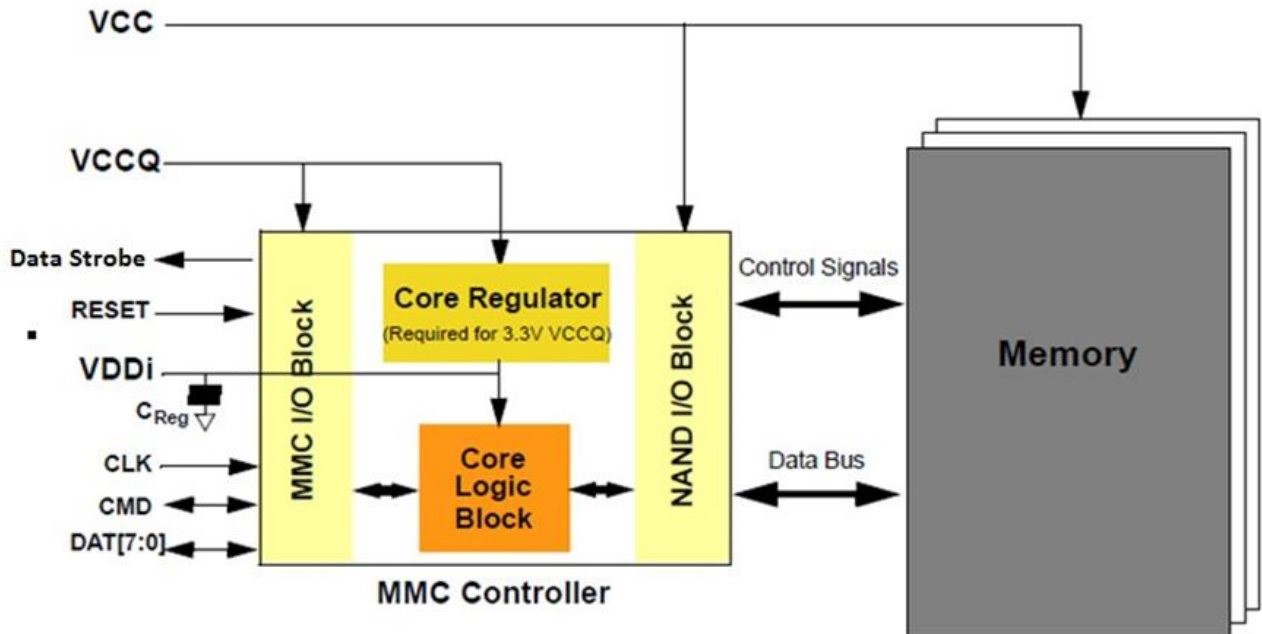
## 6.2 Bus Operating Conditions

**Table 6.1 – General Operating Conditions**

| Parameter                                                                                              | Symbol | Min  | Max.       | Unit | Remark |
|--------------------------------------------------------------------------------------------------------|--------|------|------------|------|--------|
| Peak voltage on all lines                                                                              |        | -0.5 | VCCQ + 0.5 | V    |        |
| All Inputs                                                                                             |        |      |            |      |        |
| Input Leakage Current (before initialization sequence and/or the internal pull up resistors connected) |        | -100 | 100        | μA   |        |
| Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)  |        | -2   | 2          | μA   |        |
| All Outputs                                                                                            |        |      |            |      |        |
| Output Leakage Current (before initialization sequence)                                                |        | -100 | 100        | μA   |        |
| Output Leakage Current (after initialization sequence)                                                 |        | -2   | 2          | μA   |        |

### 6.2.1 Power supply: eMMC

In the *eMMC*,  $V_{CC}$  is used for the NAND flash device and its interface voltage;  $V_{CCQ}$  is for the controller and the MMC interface voltage as shown in Figure 8. The core regulator is optional and only required when internal core logic voltage is regulated from  $V_{CCQ}$ . A  $C_{Reg}$  capacitor must be connected to the  $V_{DDi}$  terminal to stabilize regulator output on the system.



**Figure 6.4 – eMMC Internal Power Diagram**

## 6.2.2 eMMC Power Supply Voltage

The *eMMC* supports one or more combinations of  $V_{CC}$  and  $V_{CCQ}$  as shown in Table 6.2. The  $V_{CCQ}$  must be defined at equal to or less than  $V_{CC}$ .

**Table 6.2 – eMMC Operating Voltage**

| Parameter                | Symbol     | MIN | MAX  | Unit | Remarks |
|--------------------------|------------|-----|------|------|---------|
| Supply voltage (NAND)    | $V_{CC}$   | 2.7 | 3.6  | V    |         |
| Supply voltage (I/O)     | $V_{CCQ}$  | 2.7 | 3.6  | V    |         |
|                          |            | 1.7 | 1.95 | V    |         |
| Supply power-up for 3.3V | $t_{PRUH}$ |     | 35   | ms   |         |
| Supply power-up for 1.8V | $t_{PRUL}$ |     | 25   | ms   |         |

The *eMMC* must support at least one of the valid voltage configurations, and can optionally support all valid voltage configurations.

**Table 6.3 – eMMC Voltage Combinations**

|          |           | $V_{CCQ}$  |                          |
|----------|-----------|------------|--------------------------|
|          |           | 1.7V–1.95V | 2.7V–3.6V <sup>(1)</sup> |
| $V_{CC}$ | 2.7V–3.6V | Valid      | Valid                    |

**Note:**

1.  $V_{CCQ}$  (I/O) 3.3 volt range is not supported in HS200 /HS400 devices. Also  $V_{CCQ}$  (I/O) 3.3 volt range is not supported in automotive A2 Grade device.

### 6.2.3 Bus Signal Line Load

The total capacitance  $C_L$  of each line of the *eMMC* bus is the sum of the bus master capacitance  $C_{HOST}$ , the bus capacitance  $C_{BUS}$  itself and the capacitance  $C_{DEVICE}$  of *eMMC* connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances must be under 20pF.

**Table 6.4 – Signal Line Load**

| Parameter                             | Symbol       | Min     | Max      | Unit | Remark                                                                                                                                                            |
|---------------------------------------|--------------|---------|----------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Pull-up resistance for CMD            | $R_{CMD}$    | 4.7     | 50       | Kohm | to prevent bus floating                                                                                                                                           |
| Pull-up resistance for DAT0–7         | $R_{DAT}$    | 10      | 50       | Kohm | to prevent bus floating                                                                                                                                           |
| Bus signal line capacitance           | $C_L$        |         | 30       | pF   | Single Device                                                                                                                                                     |
| Single Device capacitance             | $C_{DEVICE}$ |         | 6        | pF   |                                                                                                                                                                   |
| Maximum signal line inductance        |              |         | 16       | nH   |                                                                                                                                                                   |
| V <sub>CCQ</sub> decoupling capacitor |              | 2.2+0.1 | 4.7+0.22 | μF   | It should be located as close as possible to the balls defined in order to minimize connection parasitic                                                          |
| V <sub>CC</sub> capacitor value       |              | 1+0.1   | 4.7+0.22 | μF   | It should be located as close as possible to the balls defined in order to minimize connection parasitic                                                          |
| V <sub>DDi</sub> capacitor value      | $C_{REG}$    | 1       | 4.7+0.1  | μF   | To stabilize regulator output to controller core logics. It should be located as close as possible to the balls defined in order to minimize connection parasitic |

### 6.2.4 HS400 reference load

The circuit in Figure 9 shows the reference load used to define the HS400 Device Output Timings and overshoot / undershoot parameters.

The reference load is made up by the transmission line and the  $C_{\text{REFERENCE}}$  capacitance.

The reference load is not intended to be a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester.

System designers should use IBIS or other simulation tools to correlate the reference load to system environment.

Manufacturers should correlate to their production test conditions.

Delay time ( $t_d$ ) of the transmission line has been introduced to make the reference load independent from the PCB technology and trace length.

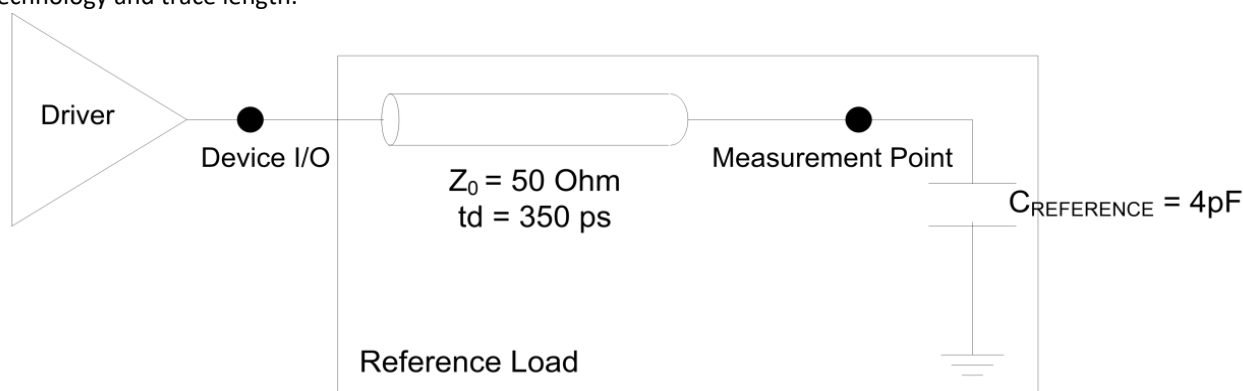


Figure 6.5 – HS400 reference load

## 6.3 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

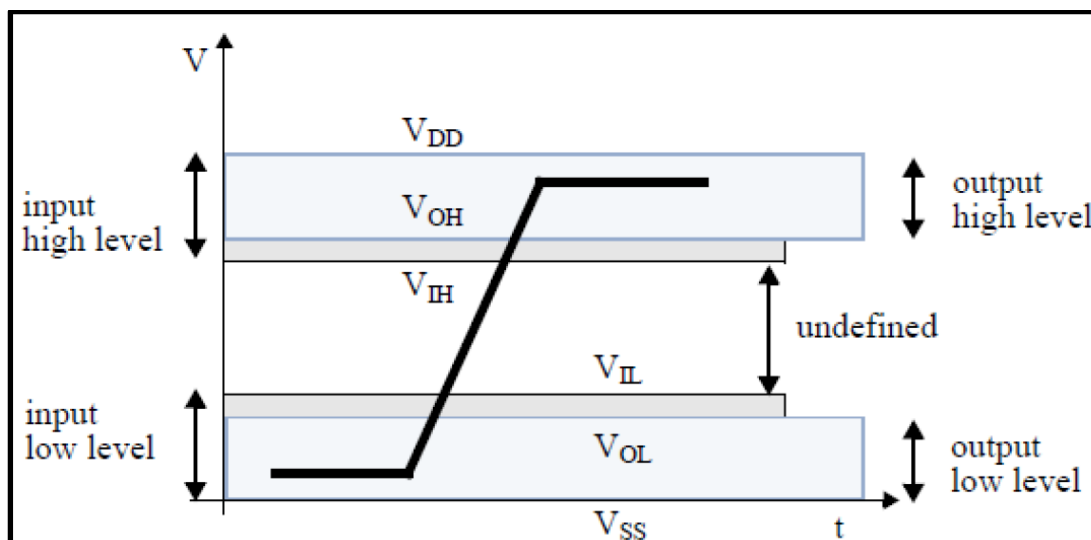


Figure 6.6 – Bus Signal Levels

### 6.3.1 Open-drain Mode Bus Signal Level

Table 6.5– Open-drain Bus Signal Level

| Parameter           | Symbol | Min             | Max. | Unit | Conditions         |
|---------------------|--------|-----------------|------|------|--------------------|
| Output HIGH voltage | VOH    | $V_{CCQ} - 0.2$ |      | V    | IOH = -100 $\mu$ A |
| Output LOW voltage  | VOL    |                 | 0.3  | V    | IOL = 2 mA         |

The input levels are identical with the push-pull mode bus signal levels.

### 6.3.2 Push-pull mode bus signal level— eMMC

The device input and output voltages shall be within the following specified ranges for any  $V_{DD}$  of the allowed voltage range

For 2.7V-3.6V  $V_{CCQ}$  range (compatible with JESD8C.01)

**Table 6.6 – Push-pull Signal Level—High-voltage eMMC**

| Parameter           | Symbol | Min               | Max.              | Unit | Conditions                         |
|---------------------|--------|-------------------|-------------------|------|------------------------------------|
| Output HIGH voltage | VOH    | $0.75 * V_{CCQ}$  |                   | V    | IOH = -100 $\mu$ A @ $V_{CCQ}$ min |
| Output LOW voltage  | VOL    |                   | $0.125 * V_{CCQ}$ | V    | IOL = 100 $\mu$ A @ $V_{CCQ}$ min  |
| Input HIGH voltage  | VIH    | $0.625 * V_{CCQ}$ | $V_{CCQ} + 0.3$   | V    |                                    |
| Input LOW voltage   | VIL    | $V_{SS} - 0.3$    | $0.25 * V_{CCQ}$  | V    |                                    |

For 1.70V – 1.95V  $V_{CCQ}$  range (: Compatible with EIA/JEDEC Standard “EIA/JESD8-7 Normal Range” as defined in the following table.

**Table 6.7 – Push-pull Signal Level—1.70 -1.95  $V_{CCQ}$  Voltage Range**

| Parameter           | Symbol | Min                | Max.               | Unit | Conditions |
|---------------------|--------|--------------------|--------------------|------|------------|
| Output HIGH voltage | VOH    | $V_{CCQ} - 0.45V$  |                    | V    | IOH = -2mA |
| Output LOW voltage  | VOL    |                    | 0.45V              | V    | IOL = 2mA  |
| Input HIGH voltage  | VIH    | $0.65 * V_{CCQ}^1$ | $V_{CCQ} + 0.3$    | V    |            |
| Input LOW voltage   | VIL    | $V_{SS} - 0.3$     | $0.35 * V_{CCQ}^2$ | V    |            |

**Notes:**

1.  $0.7 * V_{DD}$  for MMC™4.3 and older revisions.
2.  $0.3 * V_{DD}$  for MMC™4.3 and older revisions.

### Bus Operating Conditions for HS200 & HS400

The bus operating conditions for HS200 devices is the same as specified in sections 10.5.1 of JESD84-B51 through 10.5.2 of JESD84-B51. The only exception is that  $V_{CCQ}=3.3v$  is not supported.

### 6.3.3 Device Output Driver Requirements for HS200 & HS400

Refer to section 10.5.4 of the JEDEC Standard Specification JESD84-B51.

## 6.4 Bus Timing

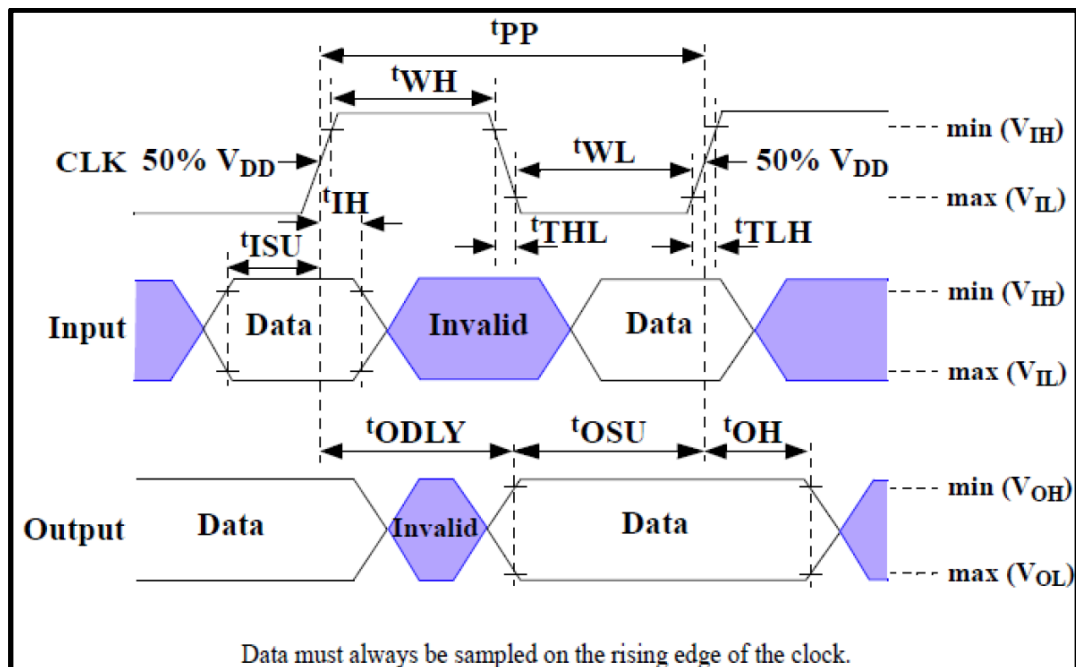


Figure 6.7 – Timing Diagram

## 6.5 Device Interface Timings

**Table 6.8 – High-speed Device Interface Timing**

| Parameter                                              | Symbol | Min | Max.              | Unit | Remark                           |
|--------------------------------------------------------|--------|-----|-------------------|------|----------------------------------|
| Clock CLK <sup>(1)</sup>                               |        |     |                   |      |                                  |
| Clock frequency Data Transfer Mode (PP) <sup>(2)</sup> | fPP    | 0   | 52 <sup>(3)</sup> | MHz  | CL ≤ 30 pF<br>Tolerance: +100KHz |
| Clock frequency Identification Mode (OD)               | fOD    | 0   | 400               | kHz  | Tolerance: +20KHz                |
| Clock high time                                        | tWH    | 6.5 |                   | ns   | CL ≤ 30 pF                       |
| Clock low time                                         | tWL    | 6.5 |                   | ns   | CL ≤ 30 pF                       |
| Clock rise time <sup>(4)</sup>                         | tTLH   |     | 3                 | ns   | CL ≤ 30 pF                       |
| Clock fall time                                        | tTHL   |     | 3                 | ns   | CL ≤ 30 pF                       |
| Inputs CMD, DAT (referenced to CLK)                    |        |     |                   |      |                                  |
| Input set-up time                                      | tISU   | 3   |                   | ns   | CL ≤ 30 pF                       |
| Input hold time                                        | tIH    | 3   |                   | ns   | CL ≤ 30 pF                       |
| Outputs CMD, DAT (referenced to CLK)                   |        |     |                   |      |                                  |
| Output delay time during data transfer                 | tODLY  |     | 13.7              | ns   | CL ≤ 30 pF                       |
| Output hold time                                       | tOH    | 2.5 |                   | ns   | CL ≤ 30 pF                       |
| Signal rise time <sup>(5)</sup>                        | tRISE  |     | 3                 | ns   | CL ≤ 30 pF                       |
| Signal fall time                                       | tFALL  |     | 3                 | ns   | CL ≤ 30 pF                       |

**Notes:**

1. CLK timing is measured at 50% of VDD.
2. eMMC shall support the full frequency range from 0-26MHz or 0-52MHz
3. Device can operate as high-speed Device interface timing at 26 MHz clock frequency.
4. CLK rise and fall times are measured by min (VIH) and max (VIL).
5. Inputs CMD DAT rise and fall times are measured by min (VIH) and max (VIL) and outputs CMD DAT rise and fall times are measured by min (VOH) and max (VOL).

**Table 6.9 – Backward-compatible Device Interface Timing**

| Parameter                                              | Symbol | Min  | Max. | Unit | Remark <sup>(1)</sup> |
|--------------------------------------------------------|--------|------|------|------|-----------------------|
| Clock CLK <sup>(2)</sup>                               |        |      |      |      |                       |
| Clock frequency Data Transfer Mode (PP) <sup>(3)</sup> | fPP    | 0    | 26   | MHz  | CL ≤ 30 pF            |
| Clock frequency Identification Mode (OD)               | fOD    | 0    | 400  | kHz  |                       |
| Clock high time                                        | tWH    | 10   |      |      | CL ≤ 30 pF            |
| Clock low time                                         | tWL    | 10   |      | ns   | CL ≤ 30 pF            |
| Clock rise time <sup>(4)</sup>                         | tTLH   |      | 10   | ns   | CL ≤ 30 pF            |
| Clock fall time                                        | tTHL   |      | 10   | ns   | CL ≤ 30 pF            |
| Inputs CMD, DAT (referenced to CLK)                    |        |      |      |      |                       |
| Input set-up time                                      | tISU   | 3    |      | ns   | CL ≤ 30 pF            |
| Input hold time                                        | tIH    | 3    |      | ns   | CL ≤ 30 pF            |
| Outputs CMD, DAT (referenced to CLK)                   |        |      |      |      |                       |
| Output set-up time <sup>(5)</sup>                      | tOSU   | 11.7 |      | ns   | CL ≤ 30 pF            |
| Output hold time <sup>(5)</sup>                        | tOH    | 8.3  |      | ns   | CL ≤ 30 pF            |

**Notes:**

1. The Device must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.
2. CLK timing is measured at 50% of VDD
3. For compatibility with Devices that support the v4.2 standard or earlier, host should not use > 26 MHz before switching to high-speed interface timing.
4. CLK rise and fall times are measured by min (VIH) and max (VIL).
5. tOSU and tOH are defined as values from clock rising edge. However, there may be Devices or devices which utilize clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to settWL value as long as possible within the range which will not go over tCK-tOH(min) in the system or to use slow clock frequency, so that host could have data set up margin for those devices. In this case, each device which utilizes clock falling edge might show the correlation either between tWL and tOSU or between tCK and tOSU for the device in its own datasheet as a note.

## 6.6 Bus Timing for DAT Signals During Dual Data Rate Operation

These timings apply to the DAT[7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operate synchronously of both the rising and the falling edges of CLK. The CMD signal still operates synchronously of the rising edge of CLK and therefore complies with the bus timing specified in section 10.5, therefore there is no timing change for the CMD signal.

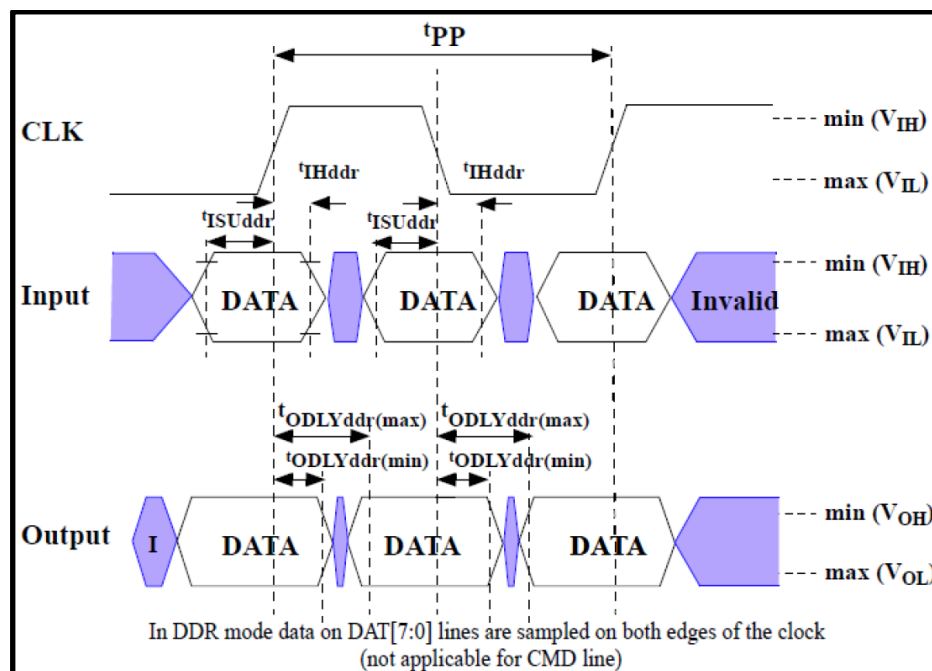


Figure 6.8 – Timing Diagram: Data Input/Output in Dual Data Rate Mode

### 6.6.1 Dual Data Rate Interface Timings

Table 6.10 – High-speed Dual Data Rate Interface Timing

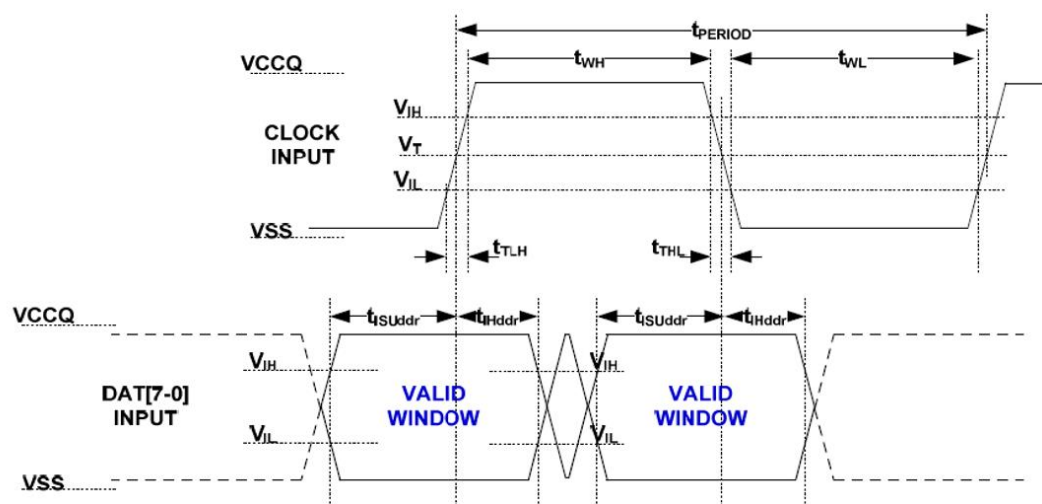
| Parameter                                      | Symbol               | Min | Max. | Unit | Remark                       |
|------------------------------------------------|----------------------|-----|------|------|------------------------------|
| <b>Input CLK<sup>(1)</sup></b>                 |                      |     |      |      |                              |
| Clock duty cycle                               |                      | 45  | 55   | %    | Includes jitter, phase noise |
| <b>Input DAT (referenced to CLK-DDR mode)</b>  |                      |     |      |      |                              |
| Input set-up time                              | t <sub>SUddr</sub>   | 2.5 |      | ns   | CL ≤ 20 pF                   |
| Input hold time                                | t <sub>IHddr</sub>   | 2.5 |      | ns   | CL ≤ 20 pF                   |
| <b>Output DAT (referenced to CLK-DDR mode)</b> |                      |     |      |      |                              |
| Output delay time during data transfer         | t <sub>ODLYddr</sub> | 1.5 | 7    | ns   | CL ≤ 20 pF                   |
| Signal rise time (all signals) <sup>(2)</sup>  | t <sub>RISE</sub>    |     | 2    | ns   | CL ≤ 20 pF                   |
| Signal fall time (all signals)                 | t <sub>FALL</sub>    |     | 2    | ns   | CL ≤ 20 pF                   |

#### Notes:

1. CLK timing is measured at 50% of VDD.
2. Inputs CMD, DAT rise and fall times are measured by min (V<sub>IH</sub>) and max (V<sub>IL</sub>), and outputs CMD, DAT rise and fall times are measured by min (V<sub>OH</sub>) and max (V<sub>OL</sub>).

## 6.6.2 HS400 Device Input Timing

The CMD input timing for HS400 mode is the same as CMD input timing for HS200 mode.



### Notes:

1.  $t_{ISU}$  and  $t_{IH}$  are measured at  $V_{IL}$  (max.) and  $V_{IH}$  (min.).
2.  $V_{IH}$  denotes  $V_{IH}$  (min.) and  $V_{IL}$  denotes  $V_{IL}$  (max.).

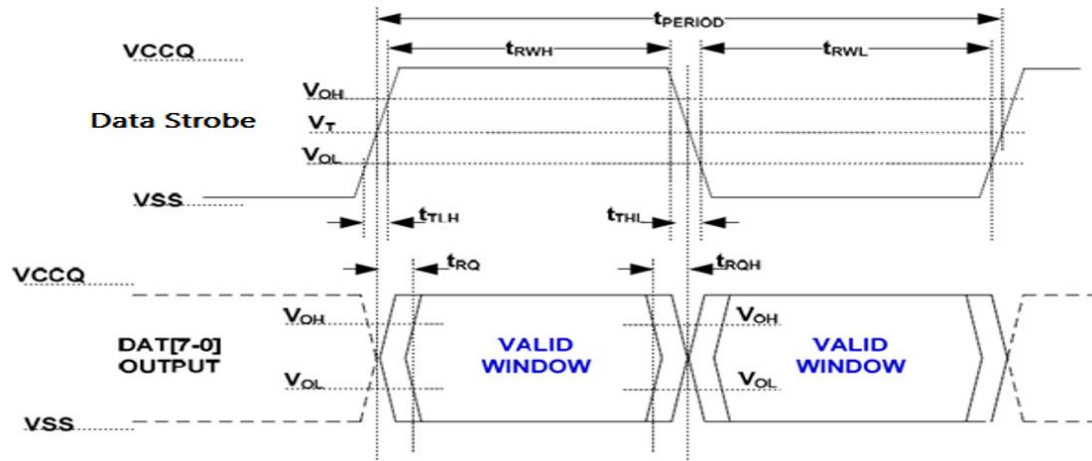
Figure 6.9 – HS400 Device Data input timing

Table 6.11 – HS400 Device input timing

| Parameter                            | Symbol       | Min   | Max | Unit | Remark                                                                                                  |
|--------------------------------------|--------------|-------|-----|------|---------------------------------------------------------------------------------------------------------|
| <b>Input CLK</b>                     |              |       |     |      |                                                                                                         |
| Cycle time data transfer mode        | $t_{PERIOD}$ | 5     |     |      | 200MHz(Max), between rising edges With respect to $V_T$ .                                               |
| Slew rate                            | SR           | 1.125 |     | V/ns | With respect to $V_{IH}/V_{IL}$ .                                                                       |
| Duty cycle distortion                | $t_{CKDCD}$  | 0.0   | 0.3 | ns   | Allowable deviation from an ideal 50% duty cycle. With respect to $V_T$ . Includes jitter, phase noise. |
| Minimum pulse width                  | $t_{CKMPW}$  | 2.2   |     | ns   | With respect to $V_T$ .                                                                                 |
| <b>Input DAT (referenced to CLK)</b> |              |       |     |      |                                                                                                         |
| Input set-up time                    | $t_{ISUDDR}$ | 0.4   |     | ns   | $C_{Device} \leq 6pF$ With respect to $V_{IH}/V_{IL}$ .                                                 |
| Input hold time                      | $t_{IHDDR}$  | 0.4   |     | ns   | $C_{Device} \leq 6pF$ With respect to $V_{IH}/V_{IL}$ .                                                 |
| Slew rate                            | SR           | 1.125 |     | V/ns | With respect to $V_{IH}/V_{IL}$ .                                                                       |

### 6.6.3 HS400 Device Output Timing

The Data Strobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC status response.



**Note:**

1.  $V_{OH}$  denotes  $V_{OH}$  (min.) and  $V_{OL}$  denotes  $V_{OL}$  (max.).

Figure 6.10 – HS400 Device output timing

**Table 6.12 – HS400 Device Output timing**

| Parameter                                     | Symbol  | Min   | Max | Unit    | Remark                                                                                                                   |
|-----------------------------------------------|---------|-------|-----|---------|--------------------------------------------------------------------------------------------------------------------------|
| <b>Data Strobe</b>                            |         |       |     |         |                                                                                                                          |
| Cycle time data transfer mode                 | tPERIOD | 5     |     |         | 200MHz(Max), between rising edges<br>With respect to VT                                                                  |
| Slew rate                                     | SR      | 1.125 |     | V/ns    | With respect to VOH/VOL and HS400 reference load                                                                         |
| Duty cycle distortion                         | tDSDCD  | 0.0   | 0.2 | ns      | Allowable deviation from the input CLK duty cycle distortion (tCKDCD)<br>With respect to VT Includes jitter, phase noise |
| Minimum pulse width                           | tDSMPW  | 2.0   |     | ns      | With respect to VT                                                                                                       |
| Read pre-amble                                | tRPRE   | 0.4   | -   | tPERIOD | Max value is specified by manufacturer. Value up to infinite is valid                                                    |
| Read post-amble                               | tRPST   | 0.4   | -   | tPERIOD | Max value is specified by manufacturer.<br>Value up to infinite is valid                                                 |
| <b>Output DAT (referenced to Data Strobe)</b> |         |       |     |         |                                                                                                                          |
| Output skew                                   | tRQ     |       | 0.4 | ns      | With respect to VOH/VOL and HS400 reference load                                                                         |
| Output hold skew                              | tRQH    |       | 0.4 | ns      | With respect to VOH/VOL and HS400 reference load.                                                                        |
| Slew rate                                     | SR      | 1.125 |     | V/ns    | With respect to VOH/VOL and HS400 reference load                                                                         |

**Note:**

1. Measured with HS400 reference load

**Table 6.13 – HS400 Capacitance**

| Parameter                             | Symbol  | Min | Max                | Unit |
|---------------------------------------|---------|-----|--------------------|------|
| Pull-up resistance for CMD            | RCMD    | 4.7 | 100 <sup>(1)</sup> | Kohm |
| Pull-up resistance for DAT0-7         | RDAT    | 10  | 100 <sup>(1)</sup> | Kohm |
| Pull-down resistance for Data Strobe  | RDS     | 10  | 100 <sup>(1)</sup> | Kohm |
| Internal pull up resistance DAT1-DAT7 | Rint    | 10  | 150                | Kohm |
| Single Device capacitance             | CDevice |     | 6                  | pF   |

**Note:**

1. Recommended maximum value is 30 kΩ for 1.2 V and 50 kΩ for 1.8 V interface supply voltages.

## 7. eMMC Device Overview

The eMMC device transfers data via a configurable number of data bus signals. The communication signals are:

### 7.1 Clock (CLK)

Each cycle of this signal directs a one-bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.

### 7.2 Data Strobe

This signal is generated by the device and used for output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output each cycle of this signal directs two bits transfer(2x) on the data - one bit for positive edge and the other bit for negative edge. For CRC status response output and CMD response output (enabled only HS400 enhanced strobe mode), the CRC status is latched on the positive edge only, and don't care on the negative edge.

### 7.3 Command (CMD)

This signal is a bidirectional command channel used for Device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the eMMC host controller to the eMMC Device and responses are sent from the Device to the host.

### 7.4 Input/Outputs (DAT0-DAT7)

These are bidirectional data channels. The DAT signals operate in push-pull mode. Only the Device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the eMMC host controller. The eMMC Device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the Device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode the Device disconnects the internal pull-ups of lines DAT1-DAT.

**Table 5.1 Communication Interface**

| Name  | Type <sup>1</sup> | Description                    |
|-------|-------------------|--------------------------------|
| CLK   | I                 | Clock                          |
| DAT0  | I/O/PP            | Data                           |
| DAT1  | I/O/PP            | Data                           |
| DAT2  | I/O/PP            | Data                           |
| DAT3  | I/O/PP            | Data                           |
| DAT4  | I/O/PP            | Data                           |
| DAT5  | I/O/PP            | Data                           |
| DAT6  | I/O/PP            | Data                           |
| DAT7  | I/O/PP            | Data                           |
| CMD   | I/O/PP/OD         | Command/Response               |
| RST_n | I                 | Hardware reset                 |
| VCC   | S                 | Supply voltage for Core        |
| VCCQ  | S                 | Supply voltage for I/O         |
| VSS   | S                 | Supply voltage ground for Core |
| VSSQ  | S                 | Supply voltage ground for I/O  |
| DS    | O/PP              | Data strobe                    |

Note:

1. I: input, O: output, PP: push-pull, OD: open-drain, NC: Not connected (or logical high), S: power supply.

## 8. eMMC Functional Description

### 8.1 Pseudo Technology (pSLC)

Each cell in a TLC NAND can be programmed to store 3 bits of data with 8 total voltage states. In Pseudo-SLC mode, the memory cell is used in 1-bit mode, thus resulting in higher endurance, lower error rates and extended temperature range. The firmware optimizes the eMMC device with Pseudo technology to achieve industrial and automotive level reliability. For ISSI eMMC device, Pseudo SLC (pSLC) mode provides one third capacity of TLC mode.

### 8.2 Field Firmware Update (FFU)

Field Firmware Updates (FFU) enables features enhancement in the field. Using this mechanism, the host downloads a new version of the firmware to the eMMC device and, following a successful download, instructs the eMMC device to install the new downloaded firmware into the device.

In order to start the FFU process the host first checks if the eMMC device supports FFU capabilities by reading SUPPORTED\_MODES and FW\_CONFIG fields in the EXT\_CSD. If the eMMC device supports the FFU feature the host may start the FFU process. The FFU process starts by switching to FFU Mode in MODE\_CONFIG field in the EXT\_CSD. In FFU Mode host should use closed-ended or open ended commands for downloading the new firmware and reading vendor proprietary data. In this mode, the host should set the argument of these commands to be as defined in FFU\_ARG field. In case these commands have a different argument the device behavior is not defined and the FFU process may fail. The host should set Block Length to be DATA\_SECTOR\_SIZE. Downloaded firmware bundle must be DATA\_SECTOR\_SIZE size aligned (internal padding of the bundle might be required). Once in FFU Mode the host may send the new firmware bundle to the device using one or more write commands.

The host could regain regular functionality of write and read commands by setting MODE\_CONFIG field in the EXT\_CSD back to Normal state. Switching out of FFU Mode may abort the firmware download operation. When host switched back to FFU Mode, the host should check the FFU Status to get indication about the number of sectors which were downloaded successfully by reading the NUMBER\_OF\_FW\_SECTORS\_CORRECTLY\_PROGRAMMED in the extended CSD. In case the number of sectors which were downloaded successfully is zero the host should re-start downloading the new firmware bundle from its first sector. In case the number of sectors which were downloaded successfully is positive the host should continue the download from the next sector, which would resume the firmware download operation.

In case MODE\_OPERATION\_CODES field is not supported by the device the host sets to NORMAL state and initiates a CMD0/HW\_Reset/Power cycle to install the new firmware. In such case the device doesn't need to use NUMBER\_OF\_FW\_SECTORS\_CORRECTLY\_PROGRAMMED.

In both cases occurrence of a CMD0/HW\_Reset/Power occurred before the host successfully downloaded the new firmware bundle to the device may cause the firmware download process to be aborted

### 8.3 Power Off Notification for Sleep

The host should notify the device before it powers the device off. This allows the device to better prepare itself for being powered off. Power the device off means to turn off all its power supplies. In particular, the host should issue a power off notification (POWER\_OFF\_LONG, POWER\_OFF\_SHORT) if it intends to turn off both VCC and VCCQ power or it may use a power off notification (SLEEP\_NOTIFICATION) if it intends to turn-off VCC after moving the device to Sleep state.

To indicate to the device that power off notification is supported by the host, a supporting host shall first set the POWER\_OFF\_NOTIFICATION byte in EXT\_CSD [34] to POWERED\_ON (0x01). To execute a power off, before powering the device down the host will change the value to either POWER\_OFF\_SHORT (0x02) or POWER\_OFF\_LONG (0x03). Host should wait for the busy line to be de-asserted. Once the setting has changed to either 0x02 or 0x03, host may safely power off the device.

The host may issue SLEEP\_AWAKE (CMD5) to enter or to exit from Sleep state if POWER\_OFF\_NOTIFICATION byte is set to POWERED\_ON. Before moving to Standby state and then to Sleep state, the host sets POWER\_OFF\_NOTIFICATION to SLEEP\_NOTIFICATION and waits for the DAT0 line de-assertion. While in Sleep (slp) state VCC (Memory supply) may be turned off as defined in 4.1.6. Removing power supplies other than VCC while the device is in the Sleep (slp) state may result in undefined device behavior. Before removing all power supplies, the host should transition the device out of Sleep (slp) state back to Transfer state using CMD5 and CMD7 and then execute a power off notification setting POWER\_OFF\_NOTIFICATION byte to either POWER\_OFF\_SHORT or POWER\_OFF\_LONG.

If host continues to send commands to the device after switching to the power off setting (POWER\_OFF\_LONG, POWER\_OFF\_SHORT or SLEEP\_NOTIFICATION) or performs HPI during its busy condition, the device shall restore the POWER\_OFF\_NOTIFICATION byte to POWERED\_ON.

If host tries to change POWER\_OFF\_NOTIFICATION to 0x00 after writing another value there, a SWITCH\_ERROR is generated.

The difference between the two power-off modes is how urgent the host wants to turn power off. The device should respond to POWER\_OFF\_SHORT quickly under the generic CMD6 timeout. If more time is acceptable, POWER\_OFF\_LONG may be used and the device shall respond to it within the POWER\_OFF\_LONG\_TIME timeout.

While POWER\_OFF\_NOTIFICATION is set to POWERED\_ON, the device expects the host to host shall:

- Keep the device power supplies alive (both VCC and VCCQ) and in their active mode
- Not power off the device intentionally before changing POWER\_OFF\_NOTIFICATION to either POWER\_OFF\_LONG or POWER\_OFF\_SHORT
- Not power off VCC intentionally before changing POWER\_OFF\_NOTIFICATION to SLEEP\_NOTIFICATION and before moving the device to Sleep state

Before moving to Sleep state hosts may set the POWER\_OFF\_NOTIFICATION byte to SLEEP\_NOTIFICATION (0x04) if aware that the device is capable of autonomously initiating background operations for possible performance improvements. Host should wait for the busy line to be de-asserted. Busy line may be asserted up the period defined in SLEEP\_NOTIFICATION\_TIME byte in EXT\_CSD [216]. Once the setting has changed to 0x04 host may set the device into Sleep mode (CMD7+CMD5). After getting out from Sleep the POWER\_OFF\_NOTIFICATION byte will restore its value to POWERED\_ON. HPI may interrupt the SLEEP\_NOTIFICATION operation. In that case POWER\_OFF\_NOTIFICATION byte will restore to POWERED\_ON.

#### 8.4 Enhanced User Data Area

ISSI eMMC supports Enhanced User Data Area feature which allows the User Data Area of eMMC to be configured as SLC Mode. Therefore, when host set the Enhanced User Data Area, the area will occupy more size of original set up size. The Max Enhanced User Data Area size is defined as -  $(MAX\_ENH\_SIZE\_MULT \times HC\_WP\_GRP\_SIZE \times HC\_ERASE\_GRP\_SIZE \times 512 \text{ KBytes})$ . The Enhanced use data area size is defined as -  $(ENH\_SIZE\_MULT \times HC\_WP\_GRP\_SIZE \times HC\_ERASE\_GRP\_SIZE \times 512 \text{ KBytes})$ . The host shall follow the flow chart of JEDEC spec for configuring the parameters of General Purpose Area Partitions and Enhanced User Data Area.

#### 8.5 Write Cache

Cache is a temporary storage space in an eMMC device. The cache should in typical case reduce the access time and increase the speed (compared to an access to the main nonvolatile storage). The cache is not directly accessible by the host. This temporary storage space may be utilized also for some implementation specific operations like as an execution memory for the memory controller and/or as storage for an address mapping table etc. However, there is data inconsistency risk when using nonvolatile cache. It's recommend only turning on the cache for the application which requires not too high reliability.

The cache shall be OFF by default after power up, RST\_n assertion or CMD0. All accesses shall be directed to the nonvolatile storage like defined elsewhere in this specification. The cache function can be turned ON and OFF by writing to the CACHE\_CTRL byte (EXT\_CSD byte [33]). Turning the cache ON shall enable behavior model defined in this section. Turning the cache OFF shall trigger flushing of the data to the nonvolatile storages

#### 8.6 Cache Enhancement Barrier

Barrier function provides a way to perform a delayed in-order flushing of a cached data. The main motivation for using barrier commands is to avoid the long delay that is introduced by flush commands. There are cases where the host is not interested in flushing the data right away, however it would like to keep an order between different cached data batches. The barrier command enables the host achieving the in-order goal but without paying the flush delay, since the real flushing can be delayed by the device to some later idle time. The formal definition of the barrier rule is as follows:

Denote a sequence of requests  $R_i$ ,  $i=0, \dots, N$ . Assuming a barrier is set between requests  $R_x$  and  $R_{x+1}$  ( $0 < x < N$ ) then all the requests  $R_0..R_x$  must be flushed to the non-volatile memory before any of the requests  $R_{x+1}..R_N$ .

Between two barriers the device is free to write data into the non-volatile memory in any order. If the host wants to preserve a certain order it shall flush the cache or set another barrier at a point where order is important.

The barrier is set by writing to the BARRIER bit of the FLUSH\_CACHE byte (EXT\_CSD byte [32]). Any error resulted can be read from the status register by CMD13 after the completion of the programming as defined for a normal write request. The error could affect any data written to the cache since the previous flush operation.

The device shall support any number of barrier commands between two flush commands. In case of multiple barrier commands between two flush commands a subset of the cached data may be committed to the non-volatile memory according to the barrier rule. Internally, a device may have an upper limit on the barrier amount it can absorb without flushing the cache. That is, if the host exceeds this barrier amount, the device may issue, internally, a normal flush.

The device shall expose its barrier support capability via the BARRIER\_SUPPORT byte (EXT\_CSD byte [486]). If a device does not support barrier function this register shall be zero. If a device supports barrier function this register shall be one.

Assuming the device supports barrier function, if the BARRIER bit of the FLUSH\_CACHE byte is set, a barrier operation shall be executed.

If the cache gets totally full and/or the cache is not able to receive the data of the next access (per block count indicated in CMD23 or per initiated single / open ended multiple block write in general) then it shall still be the responsibility of the eMMC device to store the data of the next access within the timeouts that are specified elsewhere in this specification. The actual algorithm to handle the new data and possible flush of some older cached data is left for the implementation.

**Note: When issuing a force-programming write request (CMD23 with bit 24 on) or a reliable write request (CMD23 with bit 31 on), the host should be aware that the data will be written to the non-volatile memory, potentially, before any cached data, even if a barrier command was issued. Therefore, if the writing order to the non-volatile memory is important, it is the responsibility of the host to issue a flush command before the force-programming or the reliable-write request.**

In order to use the barrier function, the host shall set bit 0 of BARRIER\_EN (EXT\_CSD byte [31]). The barrier feature is optional for an eMMC device.

### 8.7 Cache Flushing Policy

The host may require the device to flush data from the cache in an in-order manner. From time to time, to guarantee in-order flushing, the host may command the device to flush the device cache or may use a barrier command.

However, if the eMMC device flushing policy is to flush data from the cache in an in-order manner, cache barrier commands or flush commands operations (In case goal is to guarantee the flushing order) are redundant and impose a needless overhead to the device and host.

FIFO bit in CACHE\_FLUSH\_POLICY field (EXT\_CSD byte [240]) is used by the device to indicate to the host that the device cache flushing policy is First-In-First-Out; this means that the device guarantees that the order of the flushing of data would be the in same order which data was written to the cache. When the FIFO bit is set it is recommended for the host not to send cache barrier commands or flush operations which goal is to guarantee the flushing order as they are redundant and impose a burden to the system.

However, if the FIFO bit is set to 1b and the device supports the cache barrier mechanism, the host may still send barrier commands without getting an error. Sending these commands will not change the device behavior as device flushes cache in-order anyway.

The CACHE\_FLUSH\_POLICY field is read-only field and never change its value either by the host or device.

### 8.8 Command Queuing (Disable by default)

To facilitate command queuing in eMMC, the device manages an internal task queue to which the host can queue data transfer tasks.

Initially the task queue is empty. Every task is issued by the host and initially queued as pending. The device controller works to prepare pending tasks for execution. When a task is ready for execution its state changes to “ready for execution”. The exact meaning of “ready for execution” is left for device implementation.

The host tracks the state of all queued tasks and may order the execution of any task, which is marked as “ready for execution” by sending a command indicating its task ID. When the execute command is received (CMD46/CMD47) the device executes the data transfer transaction.

For example, in order to queue a write transaction, the host sends a CMD44 indicating the task’s parameters. The device responds and the host sends a CMD45, indicating the start block address.

The device regards the two commands as a single task in the queue and sends a response indicating success if no error is detected. This exchange may be executed on the CMD line while a data transfer, or busy state, is ongoing on the DAT lines. The host tracks the state of the queue using CMD13.

At a later time, when data transfer is not in progress, the host issues a CMD47, ordering the device to execute a task from the queue, providing the Task ID in its argument. The device responds with an R1 response and the data transfer starts.

Note that if hosts need to access RPMB partition, the host should disable the Command Queue mechanism and access RPMB partition not through the command queue.

General Purpose partitions may be accessed when command queuing is enabled.

The queue must be empty when CMD6 is sent (to switch partitions or to disable command queuing).

Sending CMD6 while the queue is not empty shall be regarded as illegal command (as explained 6.6.42.9 Supported Commands).

Prior to enabling command queuing, the block size shall be set to 512B. Device may respond with an error to CMD46/CMD47 if block size is not 512B.

### **8.9 Production State Awareness (PSA)**

eMMC device could utilize the information of whether it is in production environment and operate differently than it operates in the field.

For example, content that was loaded into the storage device prior to soldering might get corrupted, at higher probability, during device soldering. The eMMC device could use “special” internal operations for loading content prior to device soldering that would reduce production failures and use “regular” operations post-soldering.

PRODUCTION\_STATE\_AWARENESS [133] field in extended CSD is used as a mechanism through which the host should report to the device whether it is pre or post soldering state.

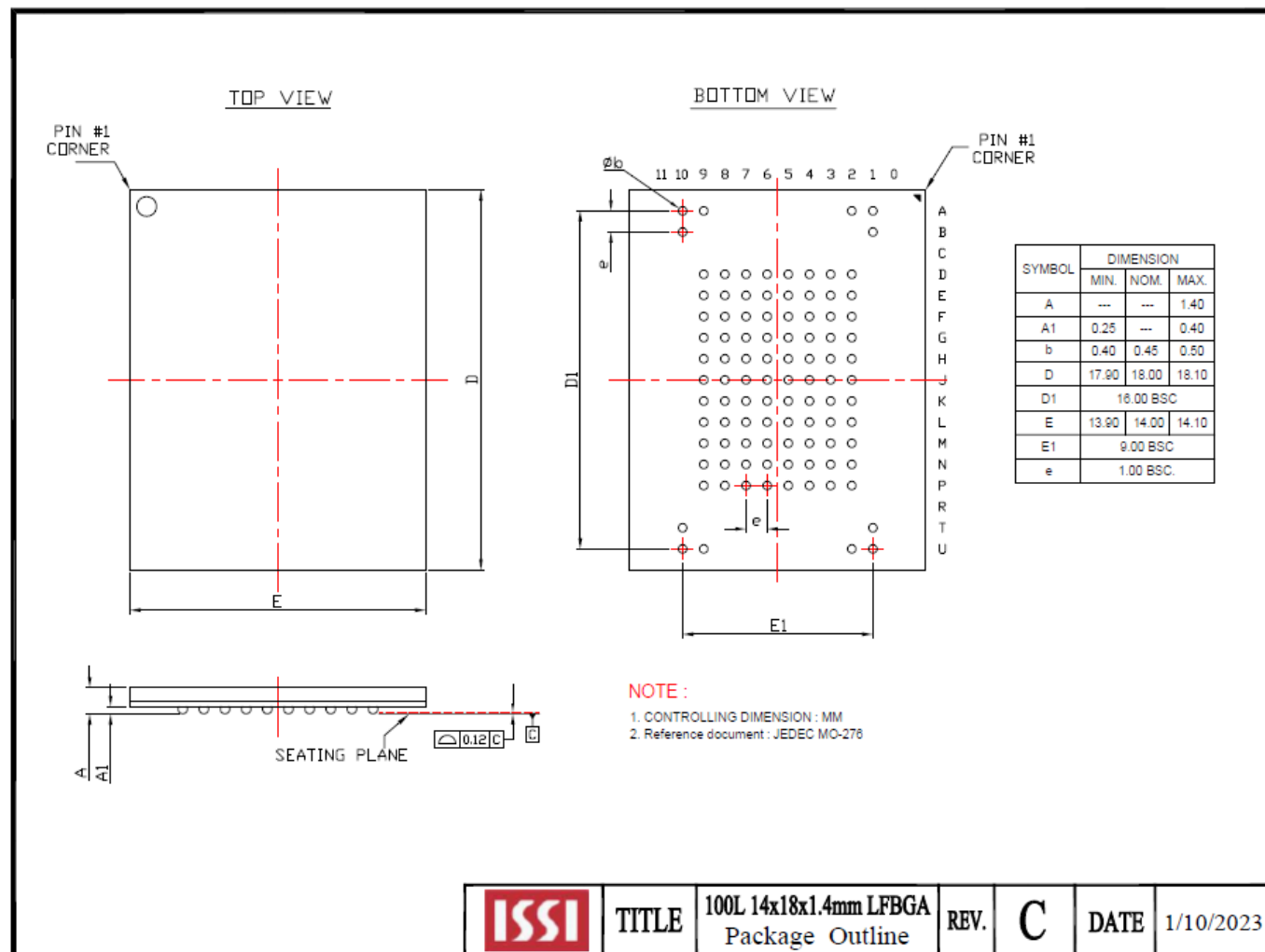
This standard defines two methods, Manual Mode and Auto Mode, to manage the device production state.

The trigger for starting or re-starting the process is setting correctly PRE\_LOADING\_DATA\_SIZE field. Before setting this field the host is expected to make sure that the device is clean and any data that was written before to the device is expected to be erased using CMD35, CMD36 and CMD38.

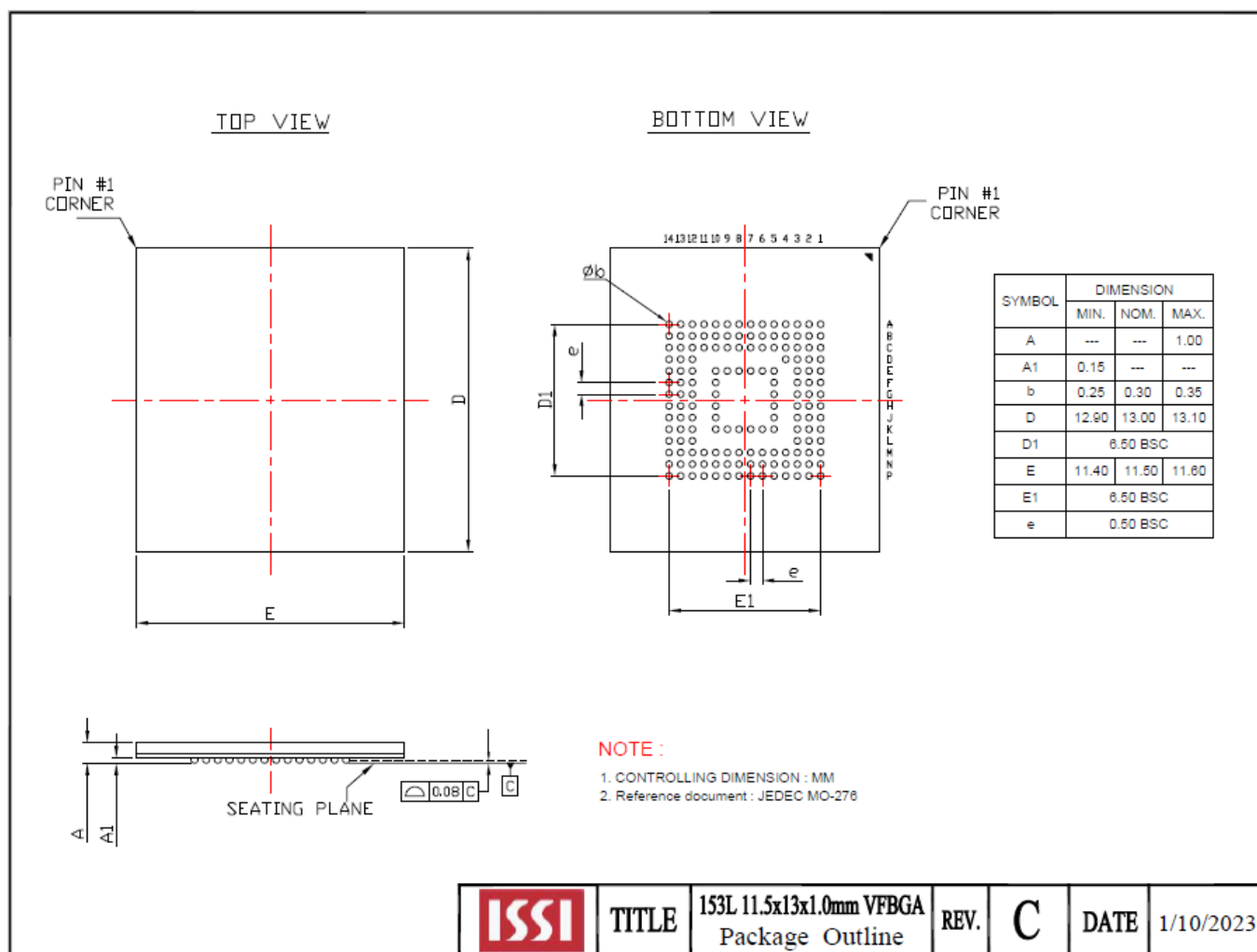
In case the host erased data, overrode existing data or performed re-partition during production state awareness it should restart the production state awareness process by re-setting PRE\_LOADING\_DATA\_SIZE.

## 9. PACKAGE TYPE INFORMATION

### 100-ball FBGA Package (Q)



# 153-BALL FBGA Package (C)



## 10. ORDERING INFORMATION – Valid Part Numbers

IS 22 T F 08G - J C L A2

### TEMPERATURE RANGE

I = Industrial Grade (-40°C to +85°C) (Call Factory)

A1 = Automotive Grade (-40°C to +85°C)

A2 = Automotive Grade (-40°C to +105°C)

### PACKAGING CONTENT

L = Green Package (RoHS Compliant, Halogen-free) and TSCA Compliant

### PACKAGE Type

C = 153-ball FBGA

Q = 100-ball FBGA

### OPTION

J = Standard (Boot Partition Size: 4MB)

B = Boot Partition Size: 16MB

### Generation.

Blank = 1<sup>st</sup> Gen.

### eMMC Density

08G = 8 GB

### INTERFACE

F = eMMC 5.1

### Flash Cell Technology

T = ISSI eMMC with TLC NAND

### Product Family

21 = Managed NAND

22 = Automotive Managed NAND

### BASE PART NUMBER

IS = Integrated Silicon Solution Inc.

| Density    | Interface | Package  | Temp. Grade                   | Order Part Number |
|------------|-----------|----------|-------------------------------|-------------------|
| <b>8GB</b> | eMMC 5.1  | 100 FBGA | Automotive, A1 <sup>(1)</sup> | IS22TF08G-JQLA1   |
|            |           |          |                               | IS22TF08G-BQLA1   |
|            |           |          | Automotive, A2 <sup>(1)</sup> | IS22TF08G-JQLA2   |
|            |           |          |                               | IS22TF08G-BQLA2   |
|            |           | 153 FBGA | Automotive, A1 <sup>(1)</sup> | IS22TF08G-JCLA1   |
|            |           |          |                               | IS22TF08G-BCLA1   |
|            |           |          | Automotive, A2 <sup>(1)</sup> | IS22TF08G-JCLA2   |
|            |           |          |                               | IS22TF08G-BCLA2   |

**Note:**

1. A1, A2: Meets AEC-Q100 requirements with PPAP.