

8Gb (x16 x 2 channel) Mobile LPDDR4/LPDDR4X

PRELIMINARY INFORMATION
JULY 2022

FEATURES

- Configuration:
 - 256Mb x16 x 2 channels
 - 8 internal banks per channel
- Low-voltage Core and I/O Power Supplies
 - VDD1 = 1.70-1.95V
 - VDD2 = 1.06-1.17V
 - VDDQ = 1.06-1.17V (LPDDR4)
 - VDDQ = 0.57-0.65V (LPDDR4X)
- LVSTL(Low Voltage Swing Terminated Logic) I/O Interface
- Internal VREF and VREF Training
- Dynamic ODT :
 - DQ ODT :VSSQ Termination
 - CA ODT :VSS Termination
- Max. Clock Frequency : 2133MHz (4266Mbps)
- 16n Pre-fetch DDR architecture
- Single data rate (multiple cycles) command/address bus
- Bidirectional/differential data strobe per byte of data (DQS/DQS#)
- Programmable and on-the-fly burst lengths (BL=16, 32)
- ZQ Calibration
- Operation Temperature
 - Industrial (T_c = -40°C to 95°C)
 - Automotive, A1 (T_c = -40°C to 95°C)
 - Automotive, A2 (T_c = -40°C to 105°C)
 - Automotive, A3 (T_c = -40°C to 125°C)
- Clock-Stop capability

DESCRIPTION

The IS43/46LQ32256B and IS43/46LQ32256BL are 8Gbit CMOS LPDDR4 SDRAM. The device is organized as 2 channels per device, and individual channel is 8-banks and 16-bits. This product uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 16N prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. This product offers fully synchronous operations referenced to both rising and falling edges of the clock. The data paths are internally pipelined and 16n bits prefetched to achieve very high bandwidth.

- On-chip temperature sensor whose status can be read from MR4
- 200-ball x32 BGA Package (10x14.5 mm)

ADDRESS TABLE

| Parameter | |
|------------------|---------|
| # of Channel | 2 |
| Row Addresses | R0-R14 |
| Column Addresses | C0-C9 |
| Bank Addresses | BA0-BA2 |

Note: Address information is per channel base.

KEY TIMING PARAMETERS

| Speed Grade | Freq. (MHz) | Data Rate (Mb/s) | Write Latency | | Read Latency | |
|-------------|-------------|------------------|---------------|-------|--------------|--------|
| | | | Set A | Set B | DBI OFF | DBI ON |
| -046 | 2133 | 4266 | 18 | 34 | 36 | 40 |
| -053 | 1866 | 3733 | 16 | 30 | 32 | 36 |
| -062 | 1600 | 3200 | 14 | 26 | 28 | 32 |

Note: Other clock frequencies/data rates supported; please refer to AC timing tables.

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- the risk of injury or damage has been minimized;
- the user assume all such risks; and
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1. BALL ASSIGNMENTS AND DESCRIPTIONS

200-ball x32 Discrete Package, 0.80mm x 0.65mm using MO-311

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|----|------|-------------------------|----------|--------|------|--------------|---|--------|--------|----------|---------|------|
| A | DNU | DNU | VSS | VDD2 | ZQ0 | 0.80mm Pitch | | NC | VDD2 | VSS | DNU | DNU |
| B | DNU | DQ0_A | VDDQ | DQ7_A | VDDQ | | | VDDQ | DQ15_A | VDDQ | DQ8_A | DNU |
| C | VSS | DQ1_A | DMI0_A | DQ6_A | VSS | | | VSS | DQ14_A | DMI1_A | DQ9_A | VSS |
| D | VDDQ | VSS | DQS0_T_A | VSS | VDDQ | | | VDDQ | VSS | DQS1_T_A | VSS | VDDQ |
| E | VSS | DQ2_A | DQS0_C_A | DQ5_A | VSS | | | VSS | DQ13_A | DQS1_C_A | DQ10_A | VSS |
| F | VDD1 | DQ3_A | VDDQ | DQ4_A | VDD2 | | | VDD2 | DQ12_A | VDDQ | DQ11_A | VDD1 |
| G | VSS | ODT_CA_A ⁽³⁾ | VSS | VDD1 | VSS | | | VSS | VDD1 | VSS | NC | VSS |
| H | VDD2 | CA0_A | NC | CS0_A | VDD2 | | | VDD2 | CA2_A | CA3_A | CA4_A | VDD2 |
| J | VSS | CA1_A | VSS | CKE0_A | NC | | | CK_t_A | CK_c_A | VSS | CA5_A | VSS |
| K | VDD2 | VSS | VDD2 | VSS | NC | | | NC | VSS | VDD2 | VSS | VDD2 |
| L | | | | | | 0.65mm Pitch | | | | | | |
| M | | | | | | | | | | | | |
| N | VDD2 | VSS | VDD2 | VSS | NC | | | NC | VSS | VDD2 | VSS | VDD2 |
| P | VSS | CA1_B | VSS | CKE0_B | NC | | | CK_T_B | CK_C_B | VSS | CA5_B | VSS |
| R | VDD2 | CA0_B | NC | CS0_B | VDD2 | | | VDD2 | CA2_B | CA3_B | CA4_B | VDD2 |
| T | VSS | ODT_CA_B ⁽³⁾ | VSS | VDD1 | VSS | | | VSS | VDD1 | VSS | RESET_N | VSS |
| U | VDD1 | DQ3_B | VDDQ | DQ4_B | VDD2 | | | VDD2 | DQ12_B | VDDQ | DQ11_B | VDD1 |
| V | VSS | DQ2_B | DQS0_C_B | DQ5_B | VSS | | | VSS | DQ13_B | DQS1_C_B | DQ10_B | VSS |
| W | VDDQ | VSS | DQS0_T_B | VSS | VDDQ | | | VDDQ | VSS | DQS1_T_B | VSS | VDDQ |
| Y | VSS | DQ1_B | DMI0_B | DQ6_B | VSS | | | VSS | DQ14_B | DMI1_B | DQ9_B | VSS |
| AA | DNU | DQ0_B | VDDQ | DQ7_B | VDDQ | | | VDDQ | DQ15_B | VDDQ | DQ8_B | DNU |
| AB | DNU | DNU | VSS | VDD2 | VSS | | | VSS | VDD2 | VSS | DNU | DNU |

NOTE 1 0.8mm pitch (X-axis), 0.65mm pitch (Y-axis), 22 rows.

NOTE 2 Top View, A1 in top left corner.

NOTE 3 The ODT_CA pin is ignored by LPDDR4X devices.

2. INPUT/OUTPUT FUNCTIONAL DESCRIPTION

2.1 PAD DEFINITION AND DESCRIPTION

Table 2.1 — Pad Definition and Description

| Symbol | Type | Description |
|---|-----------|---|
| CK_t_A, CK_c_A, CK_t_B, CK_c_B | Input | Clock: CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. Each channel (A & B) has its own clock pair. |
| CKE_A CKE_B | Input | Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel (A & B) has its own CKE signal. |
| CS_A CS_B | Input | Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal. |
| CA[5:0]_A CA[5:0]_B | Input | Command/Address Inputs: CA signals provide the Command and Address inputs according to the Command Truth Table. Each channel (A&B) has its own CA signals. |
| ODT_CA_A ODT_CA_B | Input | LPDDR4 CA ODT Control: The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins. LPDDR4X CA ODT Control: The ODT_CA pin is ignored by LPDDR4X devices. CA ODT is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to either VDD2 or VSS. |
| DQ[15:0]_A, DQ[15:0]_B | I/O | Data Input/Output: Bi-direction data bus. |
| DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B | I/O | Data Strobe: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair. Each channel (A & B) has its own DQS strobes. |
| DMI[1:0]_A, DMI[1:0]_B | I/O | Data Mask Inversion: DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel (A & B) has its own DMI signals. |
| ZQ | Reference | Calibration Reference: Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to V _{DDQ} through a 240Ω ± 1% resistor. |
| V _{DDQ} , V _{DD1} , V _{DD2} | Supply | Power Supplies: Isolated on the die for improved noise immunity. |
| V _{SS} , V _{SSQ} | GND | Ground Reference: Power supply ground reference |
| RESET_n | Input | RESET: When asserted LOW, the RESET_n signal resets both channels of the die. |

ORDERING INFORMATION – Valid Part Numbers

IS 43 LQ 32256 _ B _ - 062 B L I

TEMPERATURE RANGE

I = Industrial (-40°C to +95°C)

A1 = Automotive, A1 Grade (-40°C to +95°C)

A2 = Automotive, A2 Grade (-40°C to +105°C)

A3 = Automotive, A3 Grade (-40°C to +125°C)

PACKAGING CONTENT

L = RoHS compliant

Package Type

B = 200-ball BGA

Speed Grade

046 = 2133MHz

053 = 1866MHz

062 = 1600MHz

VDDQ

Blank = Regular VDDQ (LPDDR4)

L = Low VDDQ (LPDDR4X)

Die GenerationB = 2nd Generation**ECC support**

Blank = No ECC Support

Density

32256 = 256Mb x 32 (8Gb)

Device Type

LQ = LPDDR4 DRAM

Product Family

43 = DDR DRAM

46 = Automotive DDR DRAM

ISSI Prefix

IS = Integrated Silicon Solution Inc.

ORDERING INFORMATION, 256Mb x 32 LPDDR4

Industrial Range: $T_c = -40^{\circ}\text{C}$ to $+95^{\circ}\text{C}$

| Clock | Speed Grade | Order Part No. | Package |
|----------|-------------|---------------------|--------------------------|
| 1600 MHz | -062 | IS43LQ32256B-062BLI | 200 ball FBGA, lead free |
| 1866 MHz | -053 | IS43LQ32256B-053BLI | 200 ball FBGA, lead free |
| 2133 MHz | -046 | IS43LQ32256B-046BLI | 200 ball FBGA, lead free |

Automotive, A1 Range: $T_c = -40^{\circ}\text{C}$ to $+95^{\circ}\text{C}$

| Clock | Speed Grade | Order Part No. | Package |
|----------|-------------|----------------------|--------------------------|
| 1600 MHz | -062 | IS46LQ32256B-062BLA1 | 200 ball FBGA, lead free |
| 1866 MHz | -053 | IS46LQ32256B-053BLA1 | 200 ball FBGA, lead free |
| 2133 MHz | -046 | IS46LQ32256B-046BLA1 | 200 ball FBGA, lead free |

Automotive, A2 Range: $T_c = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$

| Clock | Speed Grade | Order Part No. | Package |
|----------|-------------|----------------------|--------------------------|
| 1600 MHz | -062 | IS46LQ32256B-062BLA2 | 200 ball FBGA, lead free |
| 1866 MHz | -053 | IS46LQ32256B-053BLA2 | 200 ball FBGA, lead free |
| 2133 MHz | -046 | IS46LQ32256B-046BLA2 | 200 ball FBGA, lead free |

Automotive, A3 Range: $T_c = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$

| Clock | Speed Grade | Order Part No. | Package |
|----------|-------------|----------------------|--------------------------|
| 1600 MHz | -062 | IS46LQ32256B-062BLA3 | 200 ball FBGA, lead free |
| 1866 MHz | -053 | IS46LQ32256B-053BLA3 | 200 ball FBGA, lead free |
| 2133 MHz | -046 | IS46LQ32256B-046BLA3 | 200 ball FBGA, lead free |

ORDERING INFORMATION, 256Mb x 32 LPDDR4XIndustrial Range: T_c = -40°C to +95°C

| Clock | Speed Grade | Order Part No. | Package |
|----------|-------------|----------------------|--------------------------|
| 1600 MHz | -062 | IS43LQ32256BL-062BLI | 200 ball FBGA, lead free |
| 1866 MHz | -053 | IS43LQ32256BL-053BLI | 200 ball FBGA, lead free |
| 2133 MHz | -046 | IS43LQ32256BL-046BLI | 200 ball FBGA, lead free |

Automotive, A1 Range: T_c = -40°C to +95°C

| Clock | Speed Grade | Order Part No. | Package |
|----------|-------------|-----------------------|--------------------------|
| 1600 MHz | -062 | IS46LQ32256BL-062BLA1 | 200 ball FBGA, lead free |
| 1866 MHz | -053 | IS46LQ32256BL-053BLA1 | 200 ball FBGA, lead free |
| 2133 MHz | -046 | IS46LQ32256BL-046BLA1 | 200 ball FBGA, lead free |

Automotive, A2 Range: T_c = -40°C to +105°C

| Clock | Speed Grade | Order Part No. | Package |
|----------|-------------|-----------------------|--------------------------|
| 1600 MHz | -062 | IS46LQ32256BL-062BLA2 | 200 ball FBGA, lead free |
| 1866 MHz | -053 | IS46LQ32256BL-053BLA2 | 200 ball FBGA, lead free |
| 2133 MHz | -046 | IS46LQ32256BL-046BLA2 | 200 ball FBGA, lead free |

Automotive, A3 Range: T_c = -40°C to +125°C

| Clock | Speed Grade | Order Part No. | Package |
|----------|-------------|-----------------------|--------------------------|
| 1600 MHz | -062 | IS46LQ32256BL-062BLA3 | 200 ball FBGA, lead free |
| 1866 MHz | -053 | IS46LQ32256BL-053BLA3 | 200 ball FBGA, lead free |
| 2133 MHz | -046 | IS46LQ32256BL-046BLA3 | 200 ball FBGA, lead free |

PACKAGE INFORMATION: 200-ball FBGA

