IS31FL3743B

18×11 DOTS MATRIX LED DRIVER WITH 12MHZ SPI

Preliminary Information
September 2018

GENERAL DESCRIPTION

The IS31FL3743B is a general purpose 18×n (n=1~11) LED Matrix programmed via 12MHz SPI interface. Each LED can be dimmed individually with 8-bit PWM data and 8-bit DC scaling data which allowing 256 steps of linear PWM dimming and 256 steps of DC current adjustable level.

Additionally each LED open state can be detected, IS31FL3743B store the open information in Open-Registers. The Open Registers allowing MCU to read out via SPI, inform MCU whether there are LEDs open or short LEDs.

The IS31FL3743B operates from 2.7V to 5.5V and features a very low shutdown and operational current.

IS31FL3743B is available in UQFN-40 (5mm×5mm) package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

FEATURES

- Supply voltage range: 2.7V to 5.5V
- 18 current sinks (Maximum)
- Support 18×n (n=1~11) LED matrix configurations
- Individual 256 PWM control steps
- Individual 256 DC current steps
- Global 256 DC current steps
- SDB rising edge reset SPI module
- 24kHz PWM frequency
- 12MHz SPI interface
- State lookup registers
- Individual open and short error detect function
- 180 degree phase delay operation to reduce power noise
- De-Ghost
- Cascade for synchronization of chips
- UQFN-40 (5mm×5mm) package

APPLICATIONS

- Hand-held devices for LED display
- Gaming device (Keyboard, Mouse etc.)
- LED in white goods application

TYPICAL APPLICATION CIRCUIT

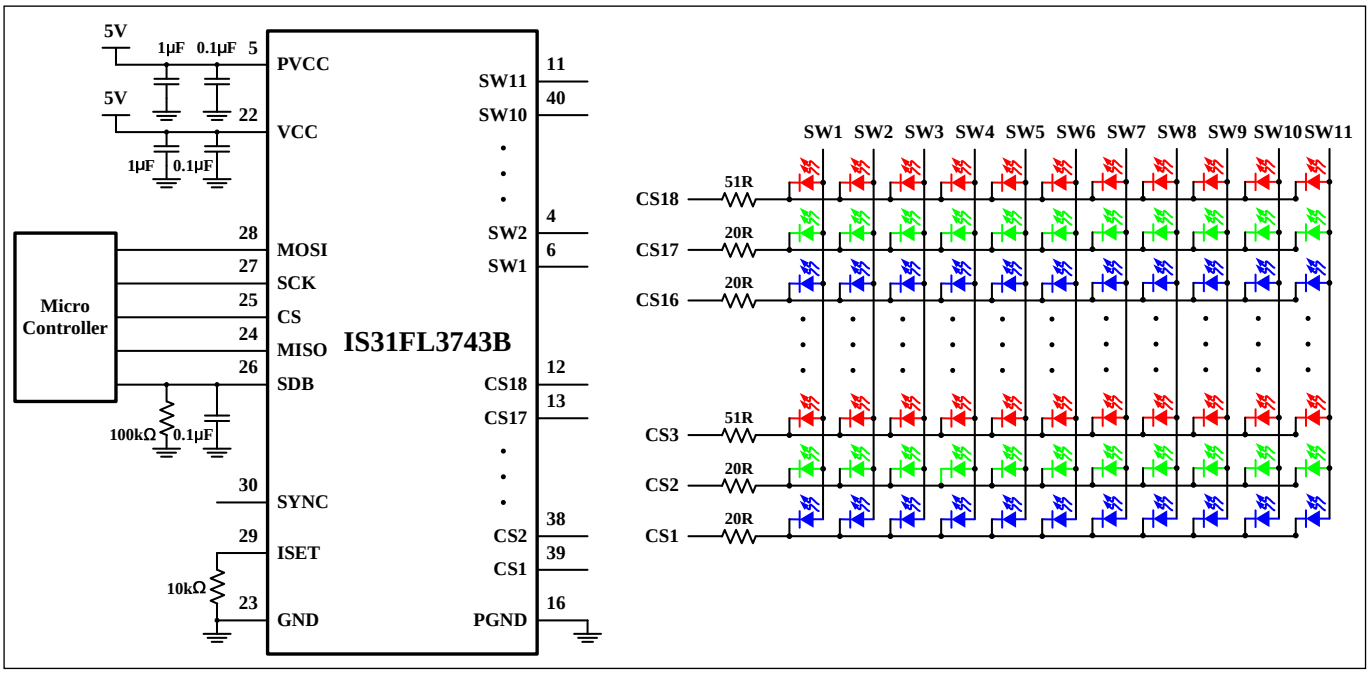


Figure 1 Typical Application Circuit: 66 RGBs

Note 1: For the mobile applications the IC should be placed far away from the mobile antenna in order to prevent the EMI.

Note 2: PVCC and VCC should use same power supply to avoid the additional I_{SD}, it is OK to use PV_{CC}=V_{CC}=5V and V_{IO}=3.3V.

TYPICAL APPLICATION CIRCUIT (CONTINUED)

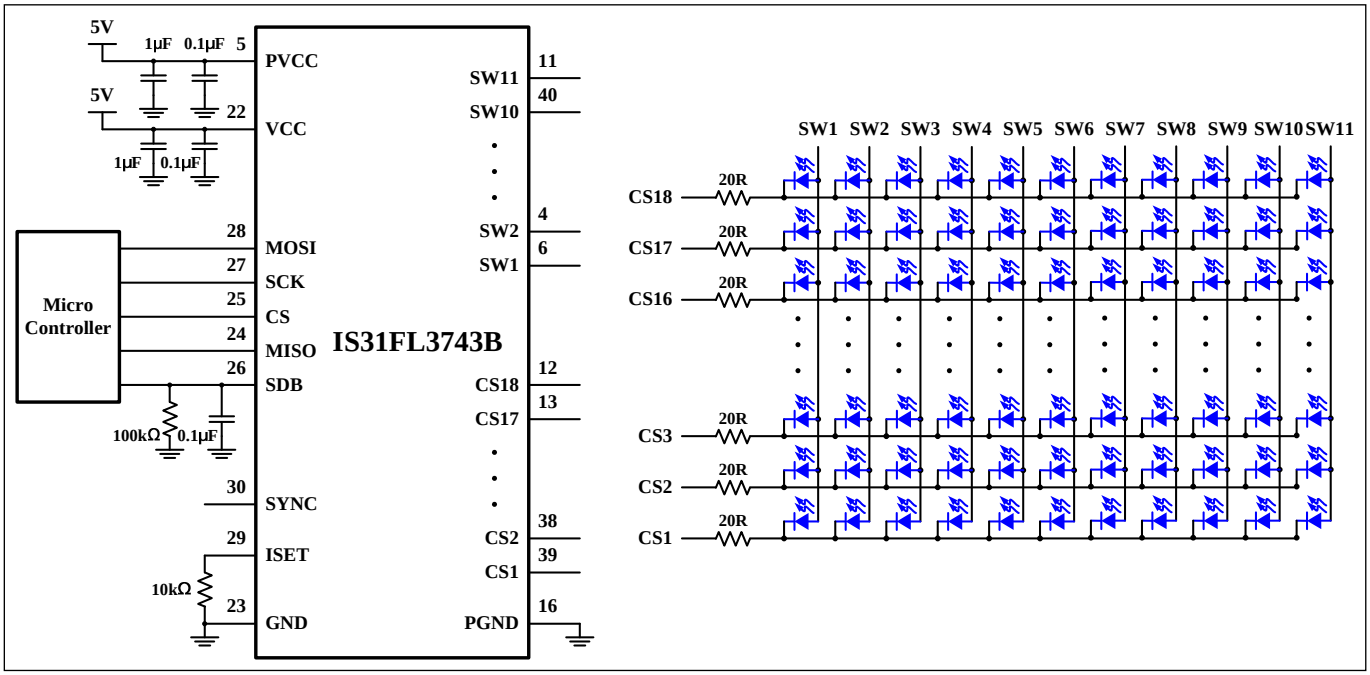


Figure 2 Typical Application Circuit: 198 Mono Color LEDs

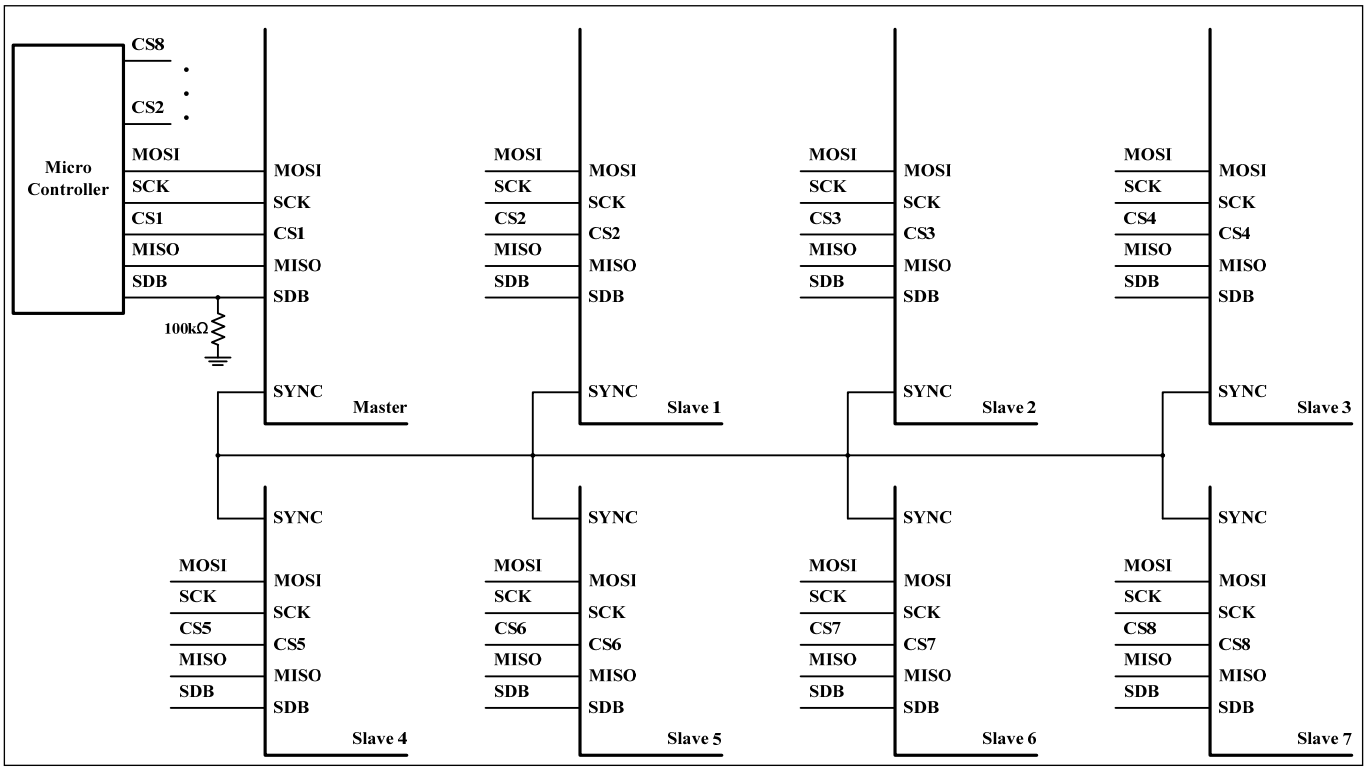
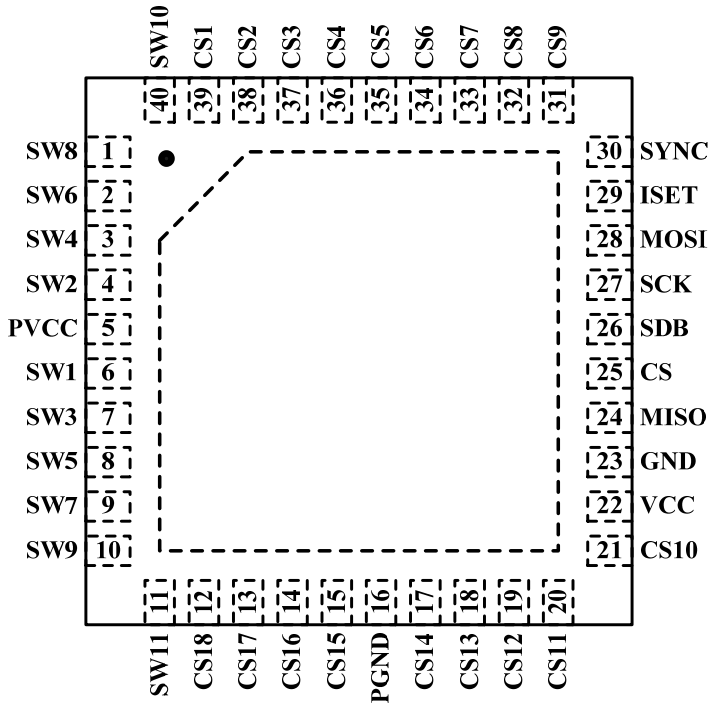


Figure 2 Typical Application Circuit (Eight Parts Synchronization-Work)

Note 3: The 20R between LED and IC is only for thermal reduction, for mono red LED, if PV_{CC}=V_{CC}=3.3V, don't need these resistors.

Note 4: One part is configured as master mode, all the other 7 parts configured as slave mode (slaves should be configured as slave before master set as master). Work as master mode or slave mode specified by Configuration Register (SYNC bits, register 25h, Page 2). Master part output master clock, and all the other parts which work as slave input this master clock.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
UQFN-40	

PIN DESCRIPTION

No.	Pin	Description
1~4	SW8,SW6,SW4,SW2	Power SW.
5	PVCC	Power for current source SW.
6~11	SW1,SW3,SW5, SW7,SW9,SW11	Power SW.
12~15	CS18~CS15	Current sink pin for LED matrix.
16	PGND	Power GND.
17~21	CS14~CS10	Current sink pin for LED matrix.
22	VCC	Analog and digital circuits.
23	GND	Analog GND.
24	MISO	MISO of SPI.
25	CS	CS of SPI.
26	SDB	Shutdown pin.
27	SCK	SPI clock.
28	MOSI	SPI input data.
29	ISET	Set the maximum IOUT current.
30	SYNC	Synchronization.
31~39	CS9~CS1	Current sink pin for LED matrix.
40	SW10	Power SW.
	Thermal Pad	Need to connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3743B-QULS4-TR	UQFN-40, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~+6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4 layer standard test PCB based on JESD 51-2A), θ_{JA}	41.6°C/W
ESD (HBM) ESD (CDM)	±7kV ±1kV

Note 6: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC} = 3.6V, T_A = 25°C, unless otherwise noted.

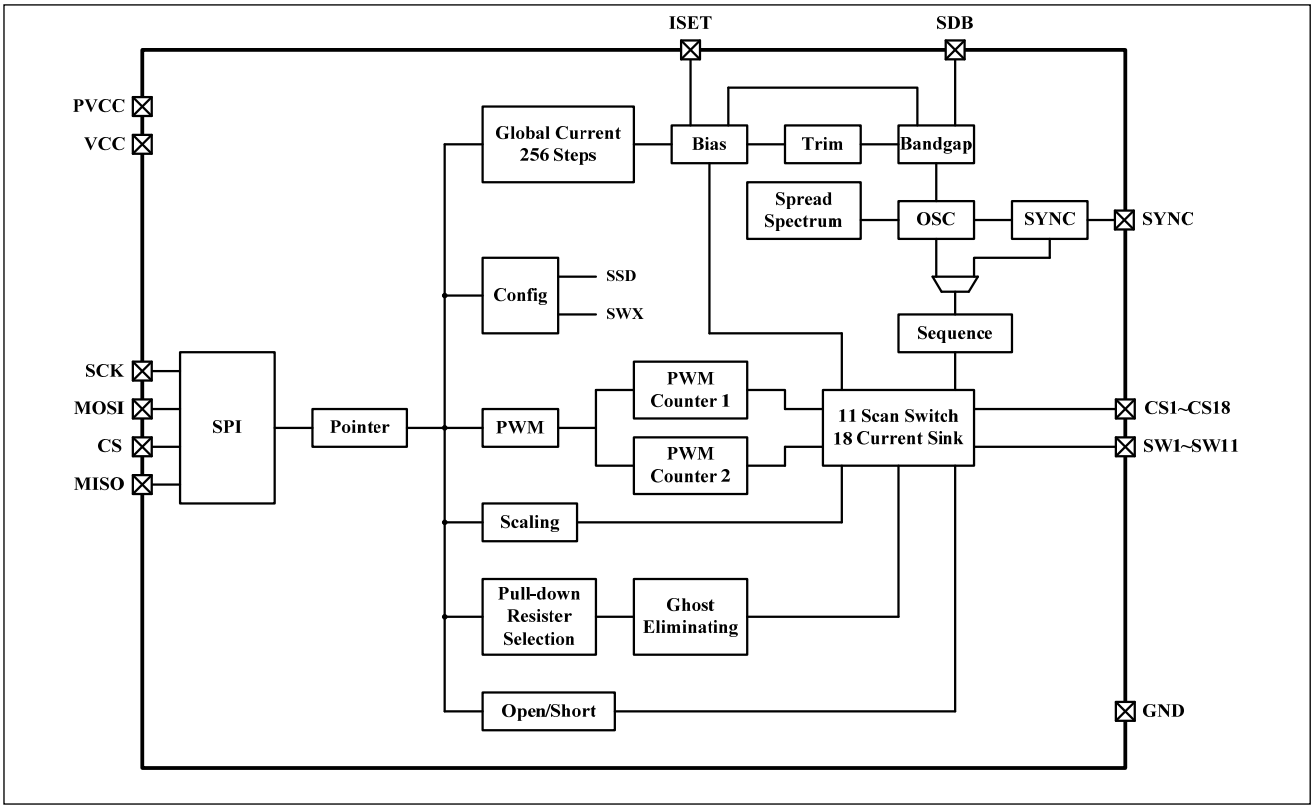
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{SDB}=$V_{CC,}$ all LEDs off		1.8		mA
I_{SD}	Shutdown current	V_{SDB}=0V		1.3		μA
		V_{SDB}= V_{CC}, Configuration Register written "0000 0000		1.3		
I_{OUT}	Maximum constant current of CSx	R_{ISET}=10kΩ, GCC=0xFF, SL=0xFF	32.09	34.5	36.91	mA
I_{LED}	Average current on each LED I_{LED} = $I_{OUT(PEAK)}$/Duty(1/11.377)	R_{ISET}=10kΩ, GCC=0xFF, SL=0xFF		3.03		mA
V_{HR}	Current switch headroom voltage SWx	I_{SWITCH}=612mA R_{ISET}=10kΩ, GCC=0xFF, SL=0xFF		550		mV
	Current sink headroom voltage CSx	I_{SINK}=34mA, R_{ISET}=10kΩ, GCC=0xFF, SL=0xFF		450		
t_{SCAN}	Period of scanning			33		μs
t_{NOL1}	Non-overlap blanking time during scan, the SWx and CSy are all off during this time			0.83		μs
t_{NOL2}	Delay total time for CS1 to CS 18, during this time, the SWx is on but CSx is not all turned on	(Note 7)		0.3		μs
Logic Electrical Characteristics (SCK, MISO, MOSI, CS, SDB, SYNC)						
V_{IL}	Logic "0" input voltage	V_{CC}=2.7V~5.5V			0.6	V
V_{IH}	Logic "1" input voltage	V_{CC}=2.7V~5.5V	2.4			V
V_{OH}	H level MISO pin output voltage	I_{OH}= -8mA	V_{CC}-0.4V		V_{CC}	V
V_{OL}	L level MISO pin output voltage	I_{OL}= 8mA	0		0.4	V
V_{HYS}	Input Schmitt trigger hysteresis	V_{CC}=3.6V		0.2		V
I_{IL}	Logic "0" input current	SDB=L, V_{INPUT} = L (Note 7)		5		nA
I_{IH}	Logic "1" input current	SDB=L, V_{INPUT} = H (Note 7)		5		nA

DIGITAL INPUT SPI SWITCHING CHARACTERISTICS (NOTE 7)

Symbol	Parameter	Min.	Typ.	Max.	Units
f_C	Clock frequency	-		12	MHz
t_{SLCH}	CS active set-up time	34			ns
t_{SHCH}	CS not active set-up time	17			ns
t_{SHSL}	CS detect time	167			ns
t_{CHSH}	CS active hold time	34			ns
t_{CHSL}	CS not active hold time	17			ns
t_{CH}	Clock high time	34			ns
t_{CL}	Clock low time	34			ns
t_{CLCH}	Clock rise time			9	ns
t_{CHCL}	Clock fall time			9	ns
t_{DVCH}	Data in set-up time	7			ns
t_{CHDX}	Data in hold time	9			ns
t_{SHQZ}	Output disable time			34	ns
t_{CLQV}	Clock low to output valid			39	ns
t_{CLQX}	Output hold time	0			ns
t_{QLQH}	Output rise time			17	ns
t_{QLQH}	Output fall time			17	ns

Note 7: Guaranteed by design.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

SPI INTERFACE

IS31FL3743B uses a SPI protocol to control the chip's function with four wires: CS, SCK, MOSI and MISO. SPI transfer starts form CS pin from high to low controlled by Master (Microcontroller), and IS31FL3743B latches data when clock rising.

SPI data format is 8-bit length. The first command byte composite of 1-bit R/W bit, 3-bit chip ID bit and 4-bit page bit. The command byte must be sent first, and is followed by register address byte then the register data. If the R/W bit is "0", it will be write operation and Master (Micro-controller) can write the register data into the register.

The maximum SCK frequency supported in IS31FL3743B is 12MHz.

Table 1 SPI Command Byte

Name	R/W	ID bit	Page No.
Bit	D7	D6:D4	D3:D0
Value	0: Write 1: Read	101	0x00: Point to Page 0 0x01: Point to Page 1 0x02: Point to Page 2

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3743B, load the address of the data register that the first data byte is intended for. During the 8th rising edge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3743B will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3743B (Figure 7).

READING OPERATION

Page 0~Page 2 registers can be read by SPI.

To read the registers of Page 0 thru Page 2, The D7 of the Command Byte need to be set to "1" and select the page number. If read one register, as shown in Figure 8, read the MISO data after sending the command byte and register address. If read more registers, as shown in Figure 9, the register address will auto increase during the 8th rising edge of receiving the last bit of the previous register data.

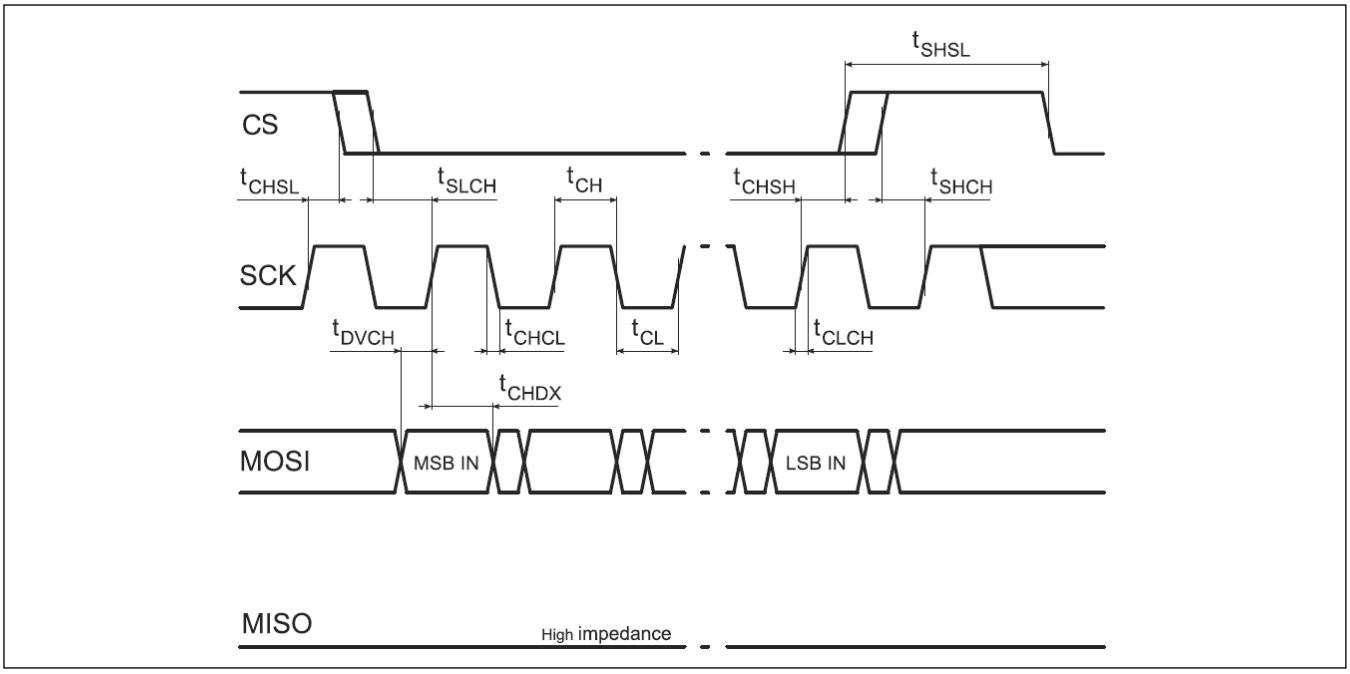


Figure 4 SPI Input Timing

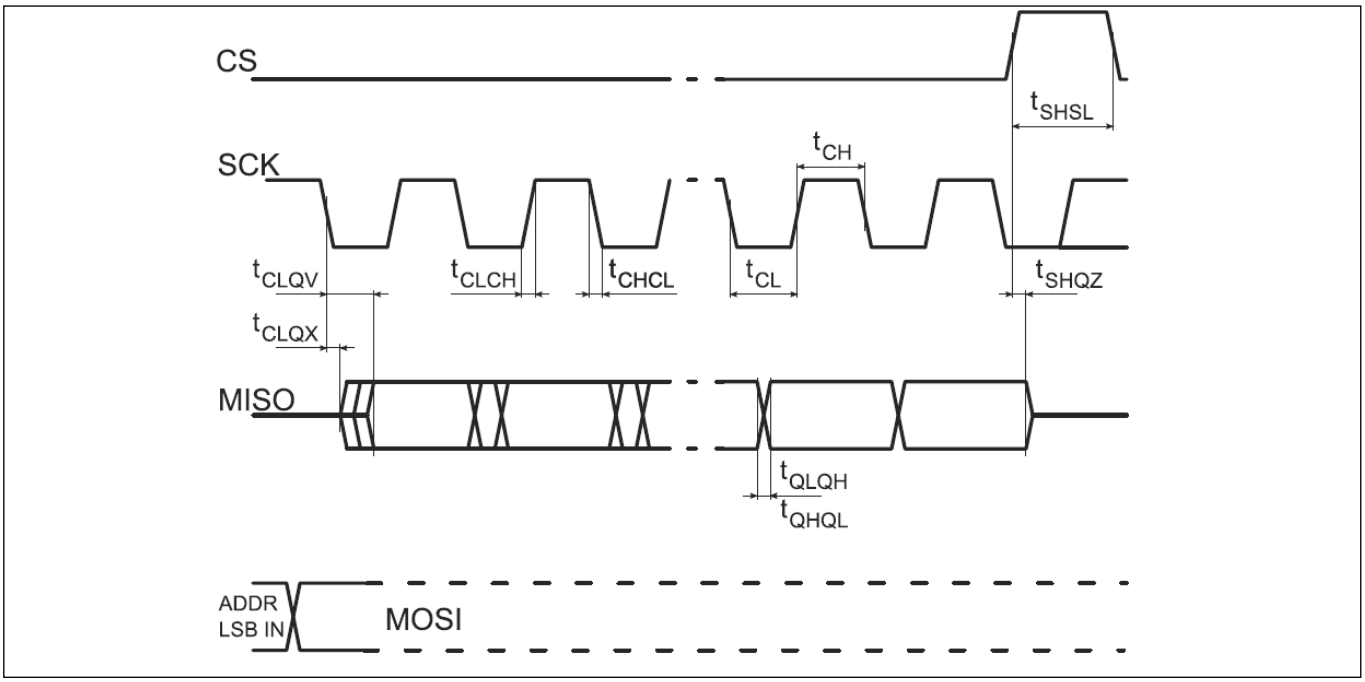


Figure 5 SPI Input Timing

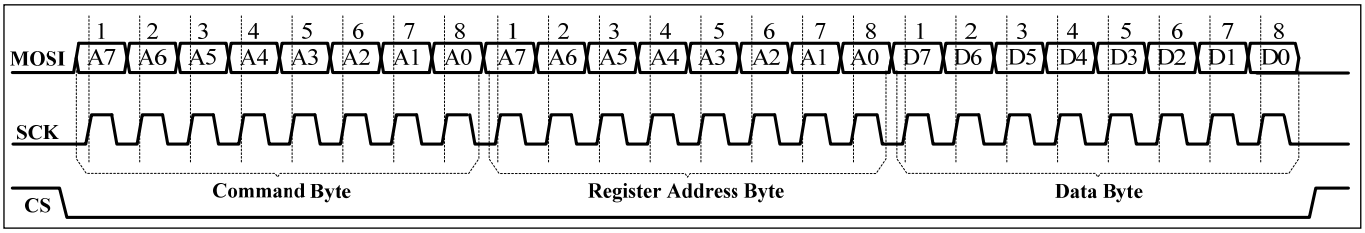


Figure 6 SPI writing to IS31FL3743B (Typical)

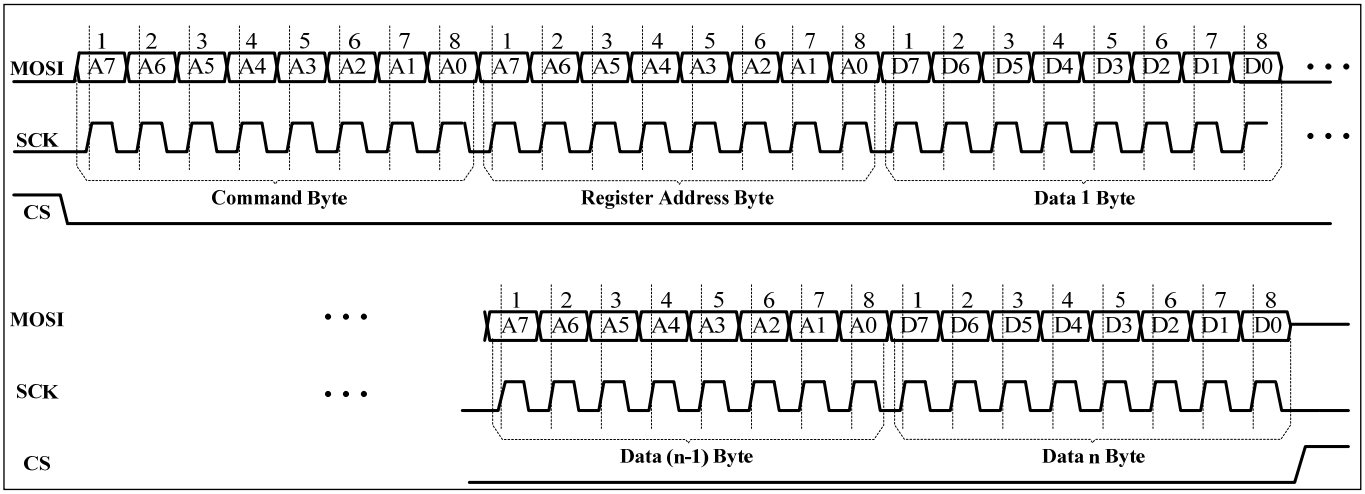


Figure 7 SPI writing to IS31FL3743B (Automatic address increment)

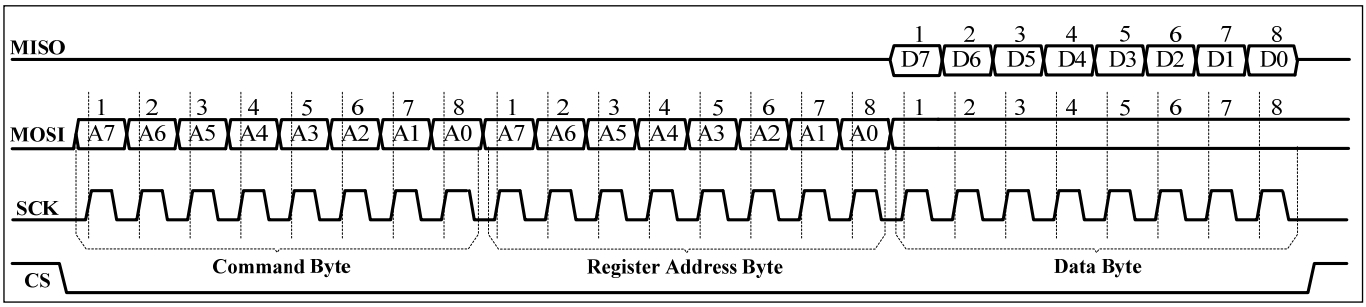


Figure 8 SPI Reading From IS31FL3743B (Typical)

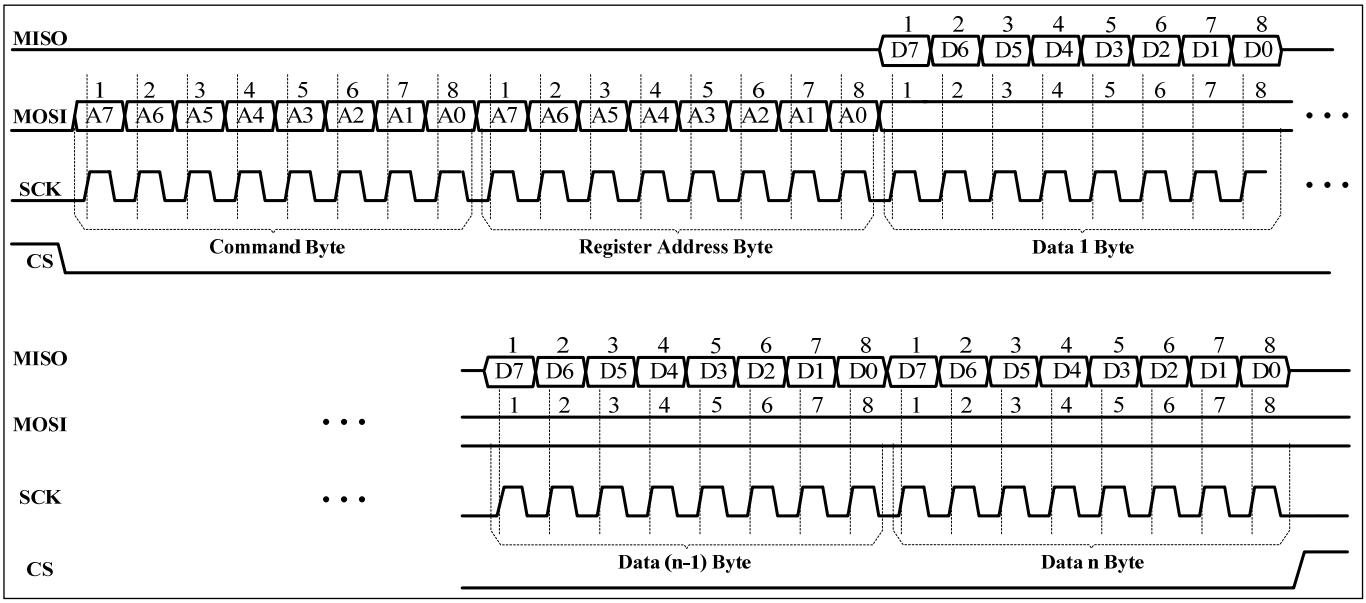


Figure 9 SPI Reading From IS31FL3743B (Automatic Address Increment)

Table 2 Register Definition

Address	Name	Function	Table	R/W	Default
PG0 (0x50): PWM Register					
01h~C6h	PWM Register	Set PWM for each LED	3	W	0000 0000
PG1 (0x51): LED Scaling					
01h~C6h	Scaling Register	Set Scaling for each LED	4	W	0000 0000
PG2 (0x52): Function Register					
00h	Configuration Register	Configure the operation mode	6	W	0000 0000
01h	Global Current Control Register	Set the global current	7	W	0000 0000
02h	Pull Down/Up Resistor Selection Register	Set the pull down resistor for SWx and pull up resistor for CSy	8	W	0011 0011
03h~23h	Open Register	Store the open information	9	R	0000 0000
24h	Temperature Status	Store the temperature point of the IC	10	W	0000 0000
25h	Spread Spectrum Register	Spread spectrum function enable	11	W	0000 0000
2Fh	Reset Register	Reset all register to POR state	-	W	0000 0000

Page 0 (PG0, Page No. = 0x50): PWM Register

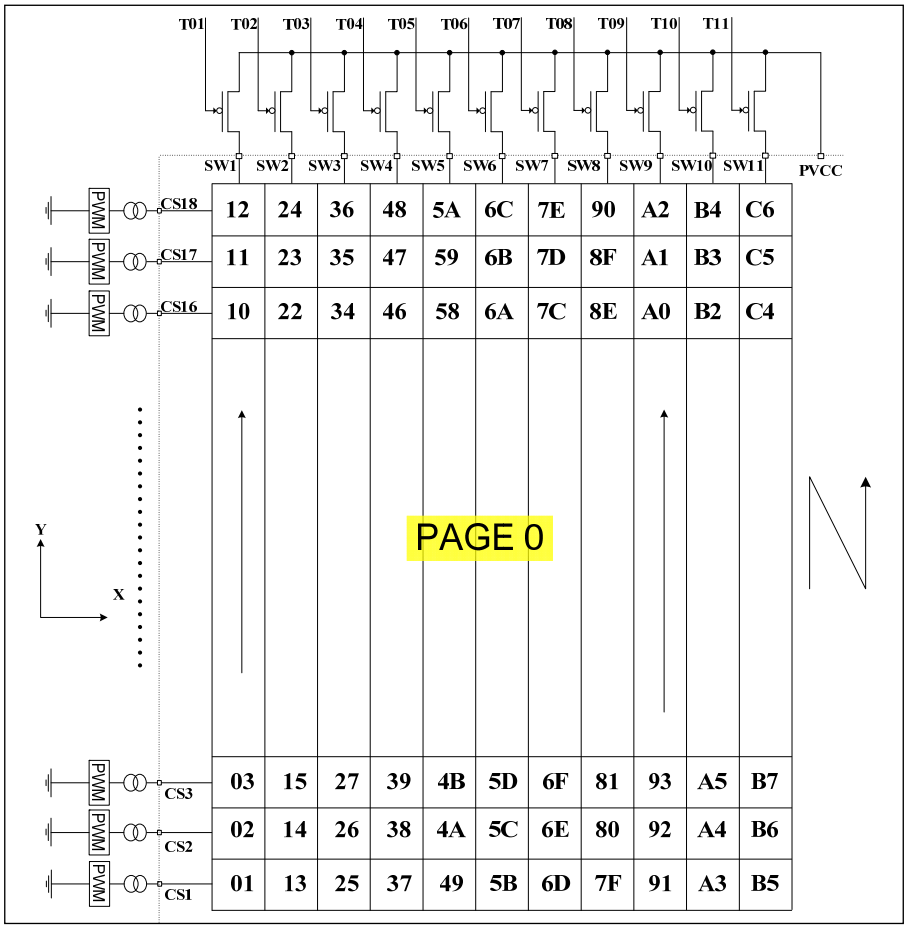


Figure 10 PWM Register

Table 3 PG0: 01h ~ C6h PWM Register

Bit	D7:D0
Name	PWM
Default	0000 0000

Each dot has a byte to modulate the PWM duty in 256 steps.

The value of the PWM Registers decides the average current of each LED noted I_{LED}.

I_{LED} computed by Formula (1):

$$I_{LED} = \frac{PWM}{256} \times I_{OUT\ (PEAK\ )} \times Duty \qquad (1)$$

$$PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where Duty is the duty cycle of SWx, see SCANING TIMING section for more information.

$$Duty = \frac{33\mu s}{(33\mu s + 0.83\mu s + 0.3\mu s)} \times \frac{1}{11} = \frac{1}{11.377} \qquad (2)$$

I_{OUT} is the output current of CSy (y=1~18),

$$I_{OUT(PEAK)} = \frac{343}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \qquad (3)$$

GCC is the Global Current Control register (PG2, 01h) value, SL is the Scaling Register value as Table 9 and R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if D7:D0=1011 0101 (0xB5, 181), GCC=1111 1111, R_{ISET}=10kΩ, SL=1111 1111:

$$I_{LED} = \frac{343}{10\,k\Omega} \times \frac{255}{256} \times \frac{255}{256} \times \frac{1}{11.377} \times \frac{181}{256}$$

Page 1 (PG1, Page No.= 0x51): Scaling Register

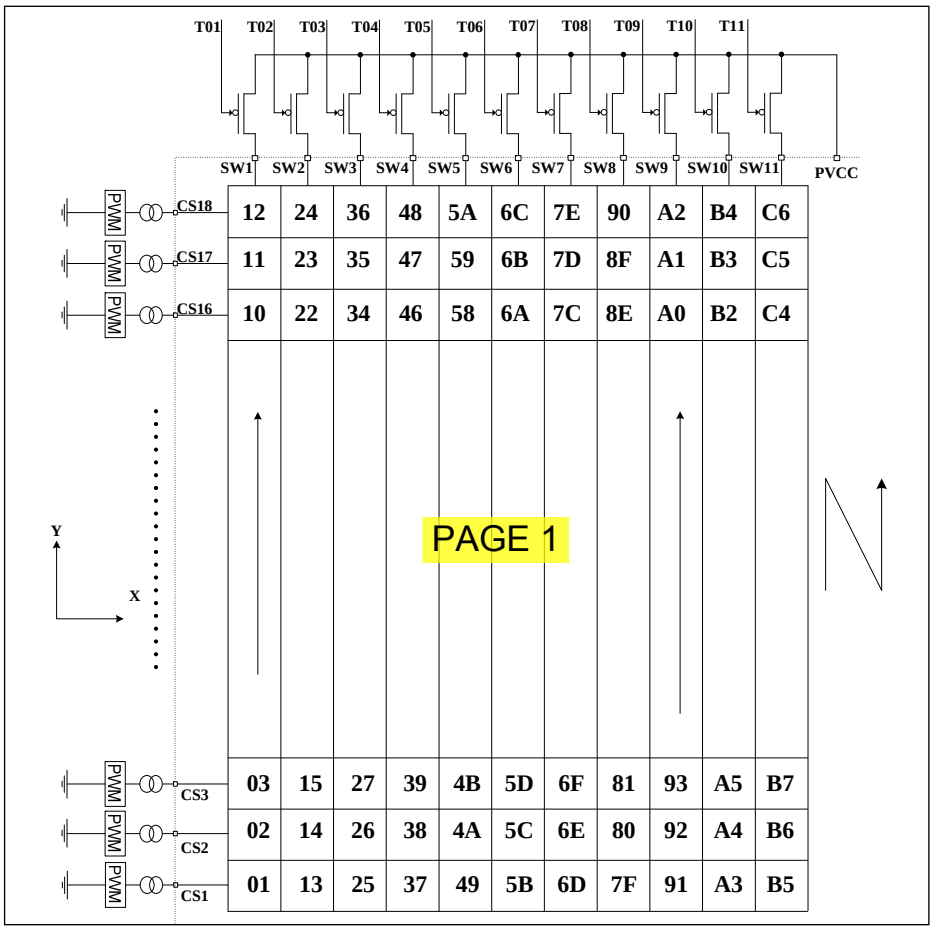


Figure 11 Scaling Register

Table 4 PG1: 01h ~ C6h Scaling Register

Bit	D7:D0
Name	SL
Default	0000 0000

Scaling register control the DC output current of each dot. Each dot has a byte to modulate the scaling in 256 steps.

The value of the Scaling Register decides the peak current of each LED noted $I_{OUT(PEAK)}$.

$I_{OUT(PEAK)}$ computed by Formula (3):

$$I_{OUT(PEAK)} = \frac{343}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \qquad (3)$$

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n$$

I_{OUT} is the output current of CSy (y=1~18), GCC is the Global Current Control Register (PG2, 01h) value and R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if R_{ISET}=10kΩ, GCC=1111 1111, SL=0111 1111:

$$SL = \sum_{n=0}^{7} D[n] \cdot 2^n = 127$$

$$I_{OUT} = \frac{343}{10\,k\Omega} \times \frac{255}{256} \times \frac{127}{256} = 16.8mA$$

$$I_{LED} = 16.8mA \times \frac{1}{11.377} \times \frac{PWM}{256}$$

Table 5 Page 2 (PG2, Page No. = 0x52): Function Register

Register	Name	Function	Table	R/W	Default
00h	Configuration Register	Configure the operation mode	10	W	0000 0000
01h	Global Current Control Register	Set the global current	11	W	0000 0000
02h	Pull Down/Up Resistor Selection Register	Set the pull down resistor for SWx and pull up resistor for CSy	12	W	0011 0011
03h~23h	Open/short Register	Store the open/short information	13	R	0000 0000
24h	Temperature Status	Store the temperature point of the IC	14	W	0000 0000
25h	Spread Spectrum Register	Spread spectrum function enable	15	W	0000 0000
2Fh	Reset Register	Reset all register to POR state	-	W	0000 0000

Table 6 00h Configuration Register

Bit	D7:D4	D3	D2:D1	D0
Name	SWS	-	OSDE	SSD
Default	0000	1	00	0

The Configuration Register sets operating mode of IS31FL3743B.

Note the D3 need to be configured as '1'.

When OSDE set to "01", open detection will be trigger once, the user could trigger open detection again by set OSDE from "00" to "01".

Before set OSDE, the GCC should set to 0x0F, please check OPEN/SHORT DETECT FUNCTION section for more information.

When SSD is "0", IS31FL3743B works in software shutdown mode and to normal operate the SSD bit should set to "1". SWS control the duty cycle of the SW, default mode is 1/11.

SSD Software Shutdown Control
0 Software shutdown
1 Normal operation

OSDE Open Detection Enable
00/11 Disable open/short detection
01 Enable open detection
10 Enable short detection

SWS SWx Setting
0000 SW1~SW11, 1/11
0001 SW1~SW10, 1/10, SW11 no-active
0010 SW1~SW9, 1/9, SW10~SW11 no-active
0011 SW1~SW8, 1/8, SW9~SW11 no-active
0100 SW1~SW7, 1/7, SW8~SW11 no-active
0101 SW1~SW6, 1/6, SW7~SW11 no-active
0110 SW1~SW5, 1/5, SW6~SW11 no-active
0111 SW1~SW4, 1/4, SW5~SW11 no-active
1000 SW1~SW3, 1/3, SW4~SW11 no-active
1001 SW1~SW2, 1/2, SW3~SW11 no-active
1010 All CSx work as current sinks only, no scan
Others Not allowed

Table 7 01h Global Current Control Register

Bit	D7:D0
Name	GCC
Default	0000 0000

The Global Current Control Register modulates all CSy (x=1~18) DC current which is noted as I_{OUT} in 256 steps.

I_{OUT} is computed by the Formula (3):

$$I_{OUT(PEAK)} = \frac{343}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \quad (3)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

Table 8 02h Pull Down/Up Resistor Selection Register

Bit	D7	D6:D4	D3	D2:D0
Name	PHC	SWPDR	-	CSPUR
Default	0	011	0	011

Set pull down resistor for SWx and pull up resistor for CSy.

Please check DE-GHOST FUNCTION section for more information.

PHC Phase choice
0 0 degree phase delay
1 180 degree phase delay

SWPDR SWx Pull down Resistor Selection Bit

000 No pull down resistor
001 0.5kΩ only in SWx off time
010 1.0kΩ only in SWx off time
011 2.0kΩ only in SWx off time
100 1.0kΩ all the time
101 2.0kΩ all the time
110 4.0kΩ all the time
111 8.0kΩ all the time

CSPUR CSy Pull up Resistor Selection Bit

000 No pull up resistor
001 0.5kΩ only in CSx off time
010 1.0kΩ only in CSx off time
011 2.0kΩ only in CSx off time
100 1.0kΩ all the time
101 2.0kΩ all the time
110 4.0kΩ all the time
111 8.0kΩ all the time

Table 9 Open Register (Read Only)

03h~23h Open Information

Bit	D7:D6	D5:D0
Name	-	CS18:CS13, CS12:CS07,CS06:CS01
Default	00	00 0000

When OSDE (PG2, 00h) is set to “01”, open detection will be trigger once, and the open information will be stored at 03h~23h.

When OSDE (PG2, 00h) set to “10”, short detection will be trigger once, and the short information will be stored at 03h~23h.

Before set OSDE, the GCC should set to 0x0F, please check OPEN/SHORT DETECT FUNCTION section for more information.

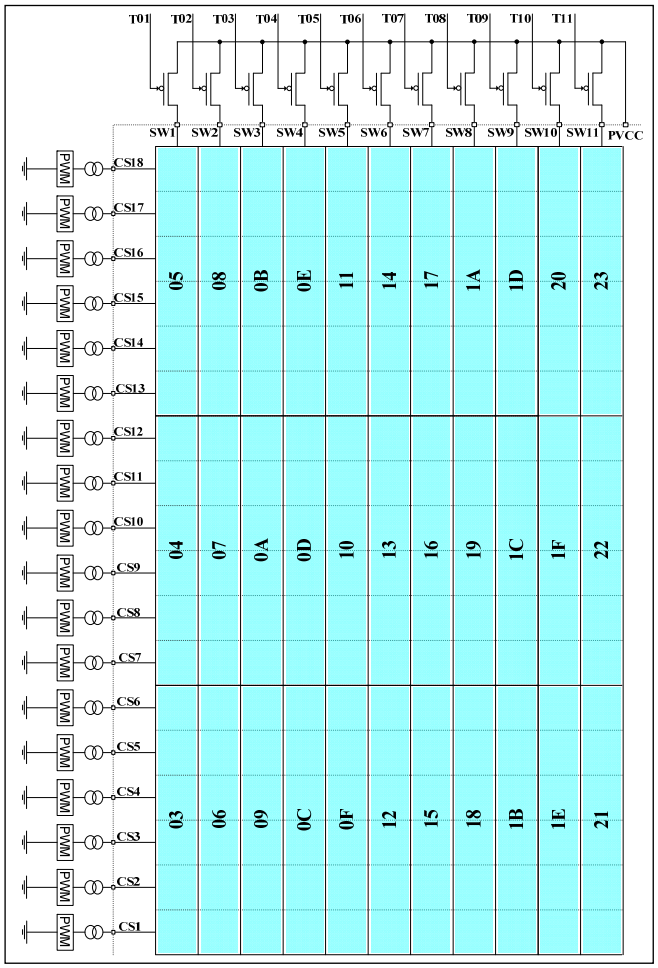


Figure 12 Open Register

Table 10 24h Temperature Status

Bit	D7:D4	D3:D2	D1:D0
Name	-	TS	TROF
Default	0000	00	00

TS store the temperature point of the IC. If the IC temperature reaches the temperature point the IC will trigger the thermal roll off and will decrease the current as TROF set percentage.

TROF percentage of output current

00 100%
01 75%
10 55%
11 30%

TS Temperature Point, Thermal roll off start point

00 140D
01 120D
10 100D
11 90D

Table 11 25h Spread Spectrum Register

Bit	D7:D6	D4	D3:D2	D1:D0
Name	SYNC	SSP	RNG	CLT
Default	00	0	00	00

When SYNC bits are set to “11”, the IS31FL3745 is configured as the master clock source and the SYNC pin will generate a clock signal distributed to the clock slave devices. To be configured as a clock slave device and accept an external clock input the slave device’s SYNC bits must be set to ‘10’.

When SSP enable, the spread spectrum function will be enabled and the RNG & CLT bits will adjust the range and cycle time of spread spectrum function.

SYNC Enable of SYNC function
0x Disable SYNC function, 30kOhm pull-low
10 Slave, clock input
11 Master, clock output

SSP Spread spectrum function enable
0 Disable
1 Enable

RNG Spread spectrum range
00 ±5%
01 ±15%
10 ±24%
11 ±34%

CLT Spread spectrum cycle time
00 1980μs
01 1200μs
10 820μs
11 660μs

2Fh Reset Register

Once user writes the Reset Register with 0xAE, IS31FL3743B will reset all the IS31FL3743B registers to their default value. On initial power-up, the IS31FL3743B registers are reset to their default values for a blank display.

APPLICATION INFORMATION

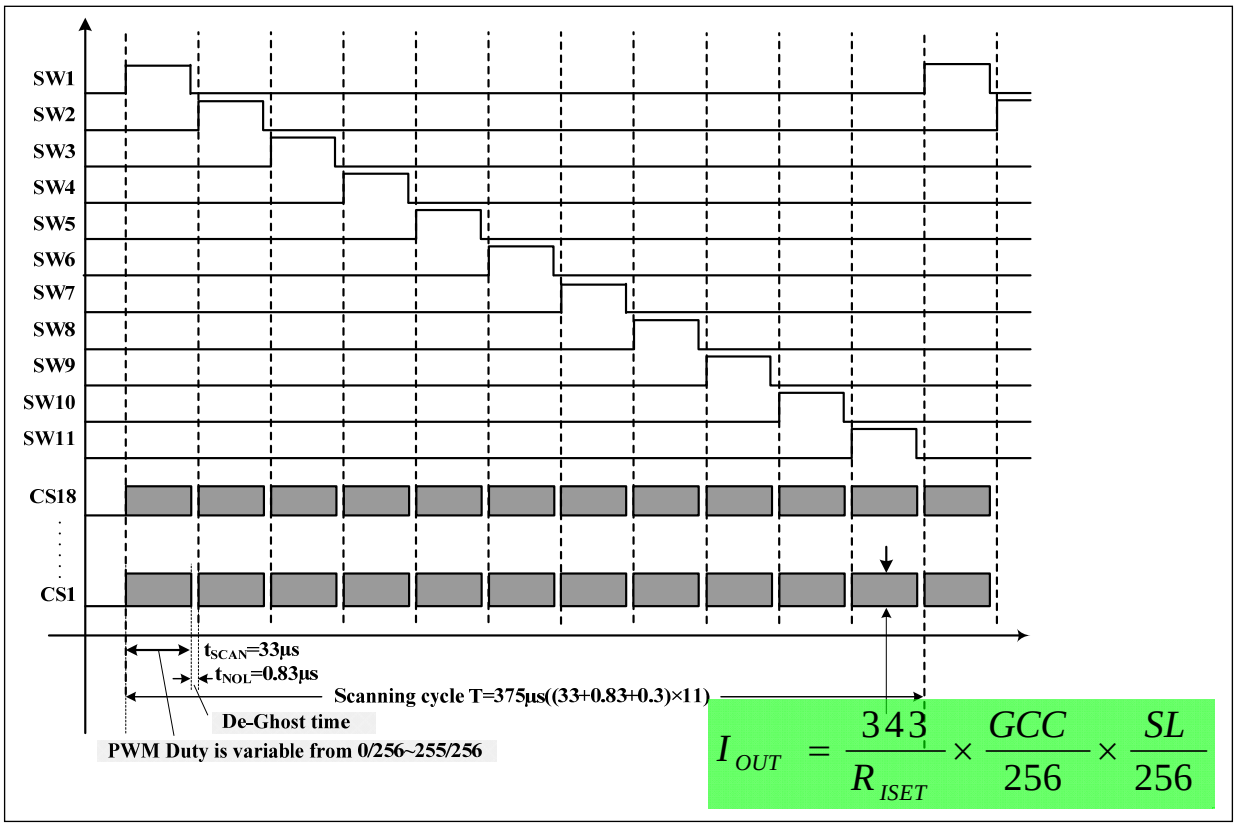


Figure 13 Scanning Timing

SCANING TIMING

As shown in Figure above, the SW1~SW11 is turned on by serial, LED is driven 11 by 11 within the SWx (x=1~11) on time (SWx, x=1~11 is source and it is high when LED on) , including the non-overlap blanking time during scan, the duty cycle of SWx (active high, x=1~11) is:

$$Duty = \frac{33\mu s}{(33\mu s + 0.83\mu s + 0.3\mu s)} \times \frac{1}{11} = \frac{1}{11.377} \quad (2)$$

Where 33μs is t_{SCAN}, the period of scanning and 0.83μs is t_{NOL}, the non-overlap time and 0.3μs is the CSx delay time.

PWM CONTROL

After setting the I_{OUT} and GCC, the brightness of each LEDs (LED average current (I_{LED})) can be modulated with 256 steps by PWM Register, as described in Formula (1).

$$I_{LED} = \frac{PWM}{256} \times I_{OUT\,(PEAK)} \times Duty \quad (1)$$

Where PWM is PWM Registers (PG0, 00h~B3h /PG1, 01h~C6h) data showing in Table 7.

For example, in Figure 1, if R_{ISET}= 10kΩ, PWM= 255, and GCC= 255, Scaling= 255, then

$$I_{OUT\,(PEAK)} = \frac{343}{10\,k\Omega} \times \frac{255}{256} \times \frac{255}{256} = 34\,mA$$

$$I_{LED} = 34\,mA \times \frac{1}{11.377} \times \frac{PWM}{256}$$

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

GAMMA CORRECTION

In order to perform a better visual LED breathing effect we recommend using a gamma corrected PWM value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting, but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3743B can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

Table 12 32 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	4	6	10	13	18
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
22	28	33	39	46	53	61	69
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
78	86	96	106	116	126	138	149
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
161	173	186	199	212	226	240	255

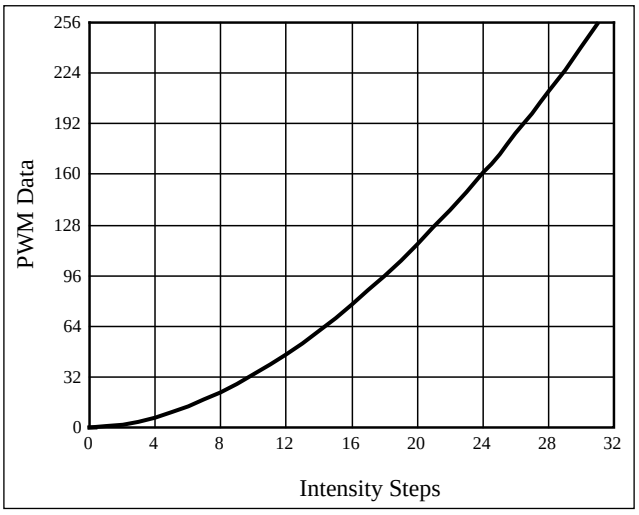


Figure 14 Gamma Correction (32 Steps)

Choosing more gamma steps provides for a more continuous looking breathing effect. This is useful for very long breathing cycles. The recommended configuration is defined by the breath cycle T. When T=1s, choose 32 gamma steps, when T=2s, choose 64 gamma steps. The user must decide the final number of gamma steps not only by the LED itself, but also based on the visual performance of the finished product.

Table 13 64 Gamma Steps with 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	3	4	5	6	7
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
8	10	12	14	16	18	20	22
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
24	26	29	32	35	38	41	44
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
47	50	53	57	61	65	69	73
C(32)	C(33)	C(34)	C(35)	C(36)	C(37)	C(38)	C(39)
77	81	85	89	94	99	104	109
C(40)	C(41)	C(42)	C(43)	C(44)	C(45)	C(46)	C(47)
114	119	124	129	134	140	146	152
C(48)	C(49)	C(50)	C(51)	C(52)	C(53)	C(54)	C(55)
158	164	170	176	182	188	195	202
C(56)	C(57)	C(58)	C(59)	C(60)	C(61)	C(62)	C(63)
209	216	223	230	237	244	251	255

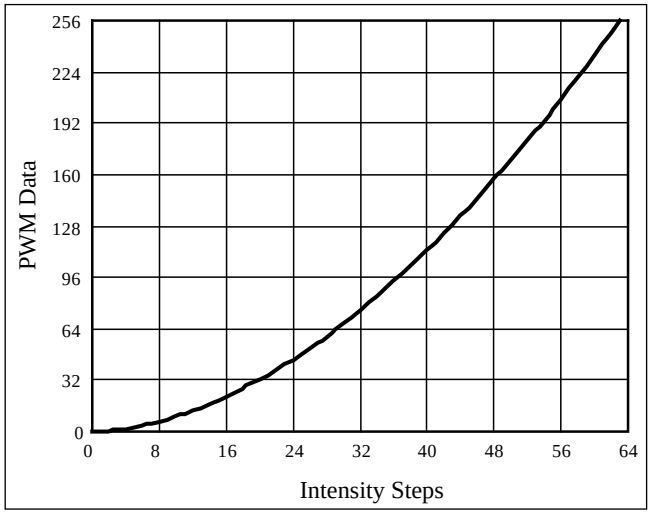


Figure 15 Gamma Correction (64 Steps)

Note: The data of 32 gamma steps is the standard value and the data of 64 gamma steps is the recommended value.

OPERATING MODE

IS31FL3743B can only operate in PWM Mode. The brightness of each LED can be modulated with 256 steps by PWM registers. For example, if the data in PWM Register is “0000 0100”, then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

OPEN/SHORT DETECT FUNCTION

IS31FL3743B has open and short detect bit for each LED.

By setting the OSD bits of the Configuration Register (PG2, 00h) from “00” to “01” or ’10’, the LED Open/short Register will start to store the open/short information and after at least 2 scanning cycles and the MCU can get the open/short information by reading the 03h~23h, for those dots are turned off via LED On/Off Registers (PG0, 00h~17h), the open/short data will not get refreshed when setting the OSD bit of the Configuration Register.

The two configurations need to set before setting the OSD bits:

1 0x0F≤GCC≤0x40, 02h=0x00
2 0x01≤GCC≤0x40, 02h=0x30

Where GCC is the Global Current Control Register (PG2, 01h) and both case 1 or two can get the correct open and short information. 02h is the Pull Down/UP Resistor Selection Register and 0x30 is to enable the SWx pull-up function.

The detect action is one-off event and each time before reading out the open/short information, the OSD bit of the Configuration Register (PG3, 00h) need to be set from “0” to “1” (clear before set operation).

DE-GHOST FUNCTION

The “ghost” term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. A ghosting effect typically can occur when multiplexing LEDs. In matrix architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

To prevent this LED ghost effect, the IS31FL3743B has integrated Pull down resistors for each SWx (x=1~11) and Pull up resistors for each CSy (y=1~18). Select the right SWx Pull down resistor (PG2, 02h) and CSy Pull up resistor (PG2, 02h) which eliminates the ghost LED for a particular matrix layout configuration.

Typically, selecting the 2kΩ will be sufficient to eliminate the LED ghost phenomenon.

The SWx Pull down resistors and CSy Pull up resistors are active only when the CSy/SWx output working the OFF state and therefore no power is lost through these resistors.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Configuration Register (PG2, 00h) to “0”, the IS31FL3743B will operate in software shutdown mode. When the IS31FL3743B is in software shutdown, all current sources are switched off, so that the matrix is blanked. All registers can be operated. Typical current consume is 1.3μA.

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown, typical the current consume is 1.3μA.

The chip releases hardware shutdown when the SDB pin is pulled high. During hardware shutdown state Function Register can be operated.

If V_{CC} has risk drop below 1.75V but above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

LAYOUT

As described in external resistor (R_{ISET}), the chip consumes lots of power. Please consider below factors when layout the PCB.

1. The V_{CC} (PVCC, AVCC) capacitors need to close to the chip and the ground side should well connected to the GND of the chip.

2. R_{ISET} should be close to the chip and the ground side should well connect to the GND of the chip.

3. The thermal pad should connect to ground pins and the PCB should have the thermal pad too, usually this pad should have 16 or 25 via thru the PCB to other side’s ground area to help radiate the heat. About the thermal pad size, please refer to the land pattern of each package.

4. The CSy pins maximum current is 34mA (R_{ISET}=10kΩ), and the SWx pins maximum current is larger, the width of the trace, SWx should have wider trace then CSy.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

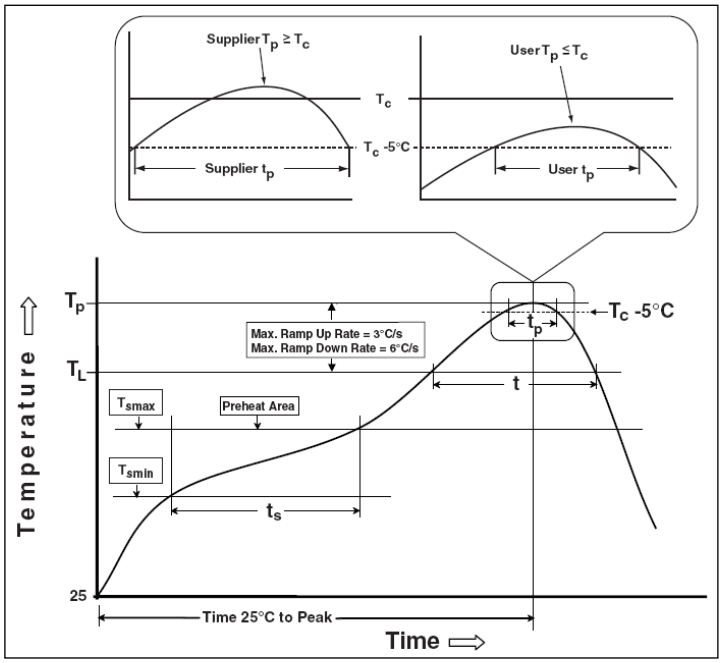
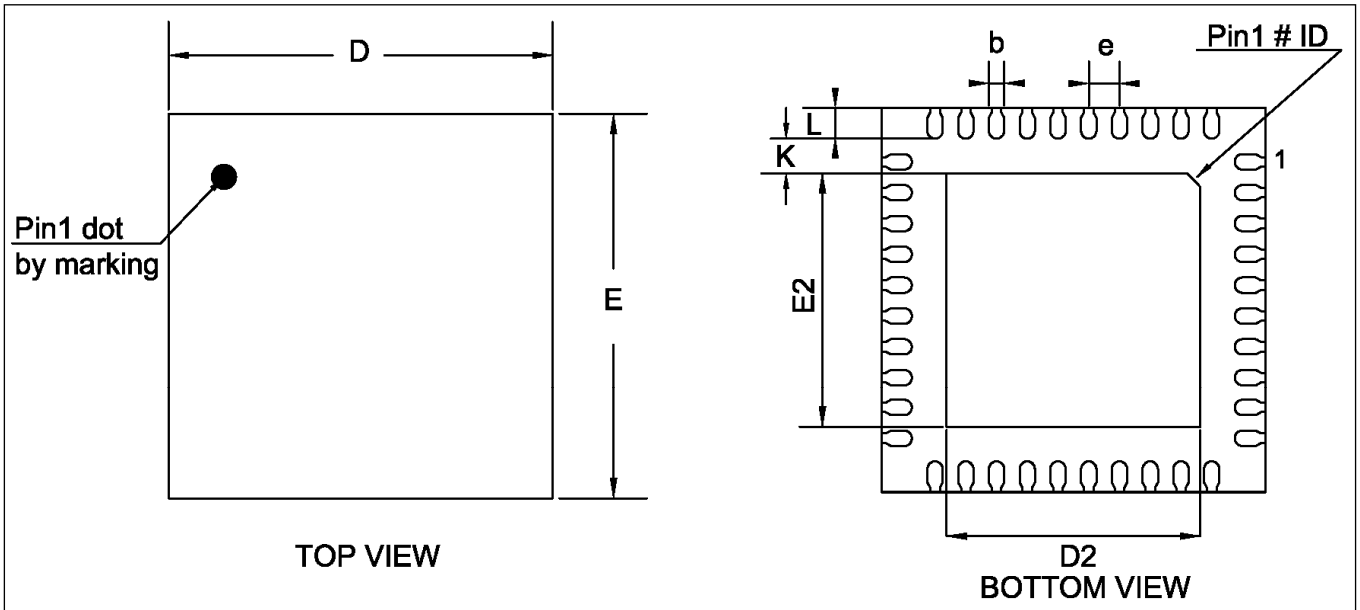
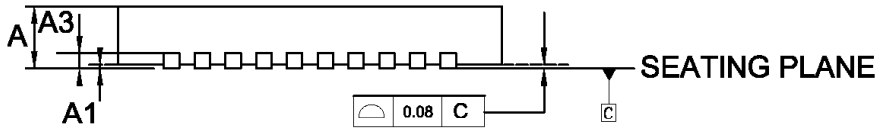


Figure 16 Classification Profile

PACKAGE INFORMATION

UQFN-40





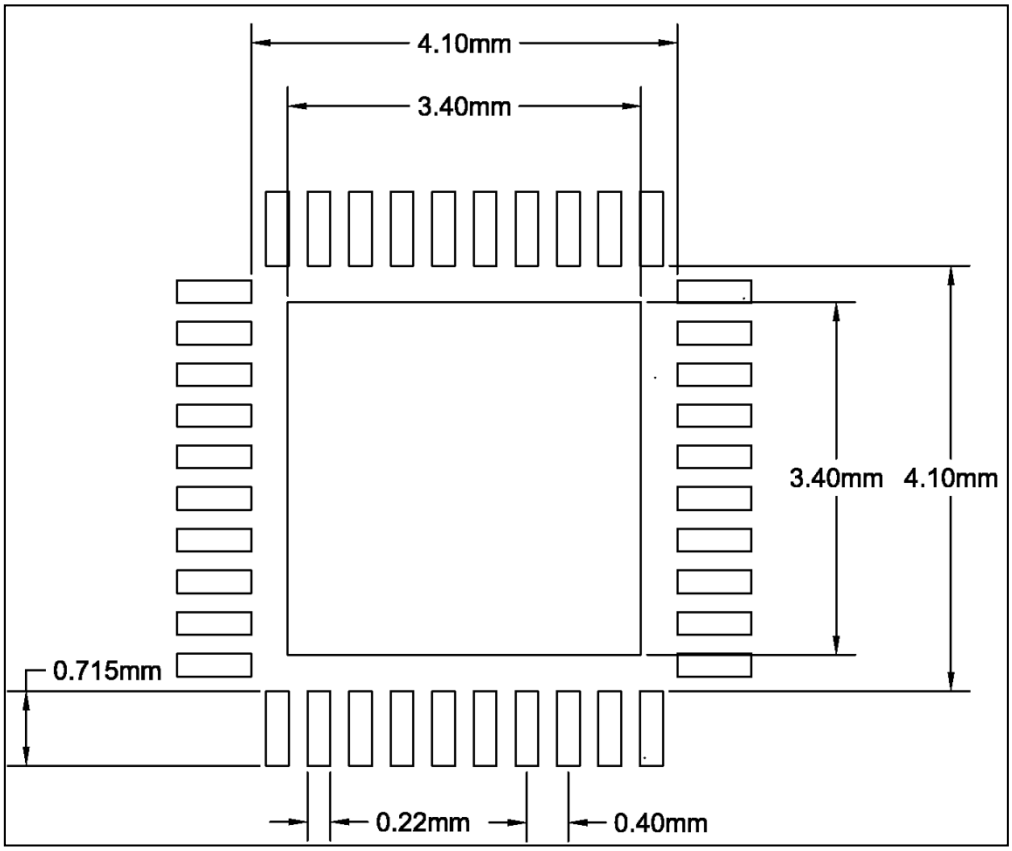
SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3	0.10	0.15	0.20
K	0.20	-	-
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.30	3.40	3.50
E2	3.30	3.40	3.50
L	0.35	0.40	0.45
e	0.40BSC		

NOTE:

1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

RECOMMENDED LAND PATTERN



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2018.04.18
0B	Add V_{OH} and V_{OL} in ELECTRICAL CHARACTERISTICS table	2018.09.20