IS61WV25616MEBLL
IS64WV25616MEBLL

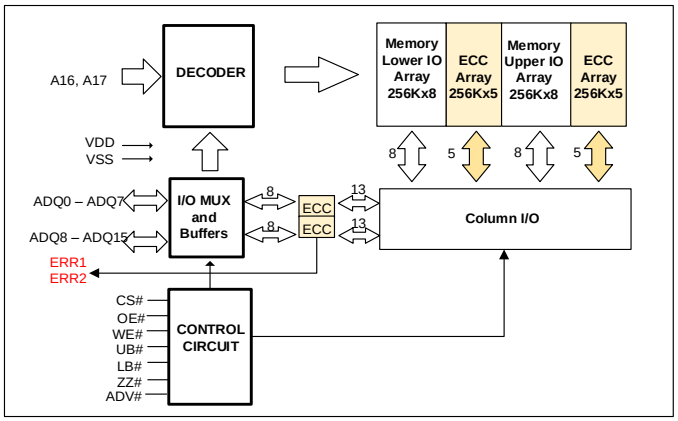
256Kx16 HIGH SPEED ASYNCHRONOUS CMOS STATIC RAM with ADMUX & ECC

PRELIMINARY INFORMATION
MARCH 2017

KEY FEATURES

- High-speed access time: 10ns, 12ns
- Single power supply
  - 2.4V-3.6V VDD
- Ultra Low Standby Current with ZZ# pin
  - IZZ = 30uA (typ.)
- Error Detection and Correction with optional ERR1/ERR2 output pin:
  - ERR1 pin indicates 1-bit error detection and correction.
  - ERR2 pin indicates multi-bit error detection
- ADMUX inputs/outputs : ADQ0~ADQ15
- Three state outputs
- Industrial and Automotive temperature support
- Lead-free available

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The *ISSI* IS61/64WV25616MEBLL are high-speed, low power, 4M bit ADMUX static RAMs organized as 256K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology and implemented ECC function to improve reliability and ADMUX inputs/outputs to minimize pin counts.

This highly reliable process coupled with innovative circuit design techniques including ECC (SEC-DED: Single Error Correcting-Double Error Detecting) yields high-performance and highly reliable devices.

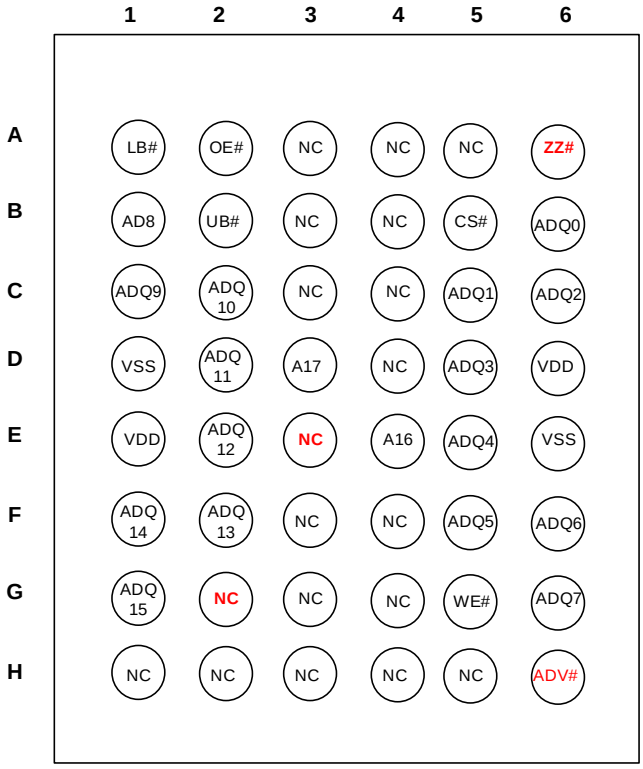
When CS# is High (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels. Especially Ultra Low Standby Power at Snooze mode with ZZ# Low.

The active LOW Write Enable (WE#) controls both writing and reading of the memory. A data byte allows Upper Byte (UB#) and Lower Byte (LB#) access.

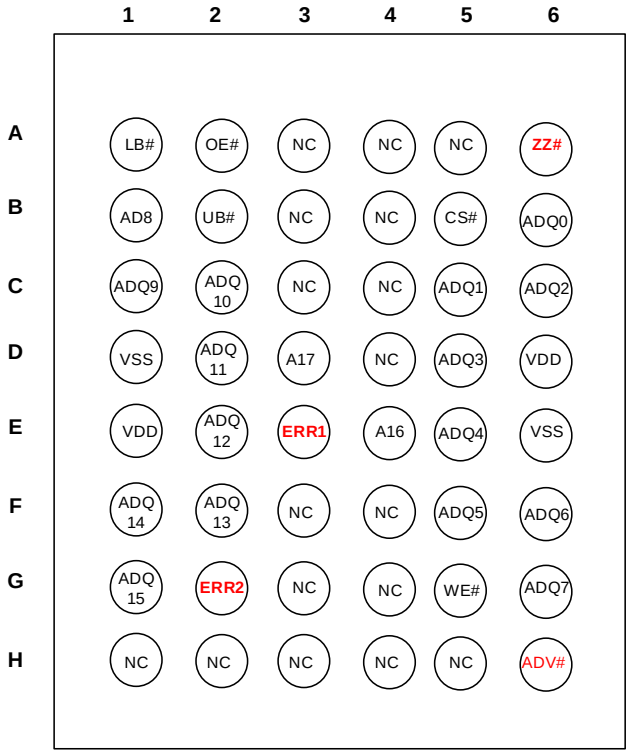
The IS61/64WV25616MEBLL are packaged in the JEDEC standard 48-pin mini BGA (6mm x 8mm), and 44-pin TSOP (TYPE II).

PIN CONFIGURATIONS

48-Pin mini BGA(6mm x 8mm) with ZZ#



48-Pin mini BGA (6mm x 8mm) with ZZ# and ERR1/2



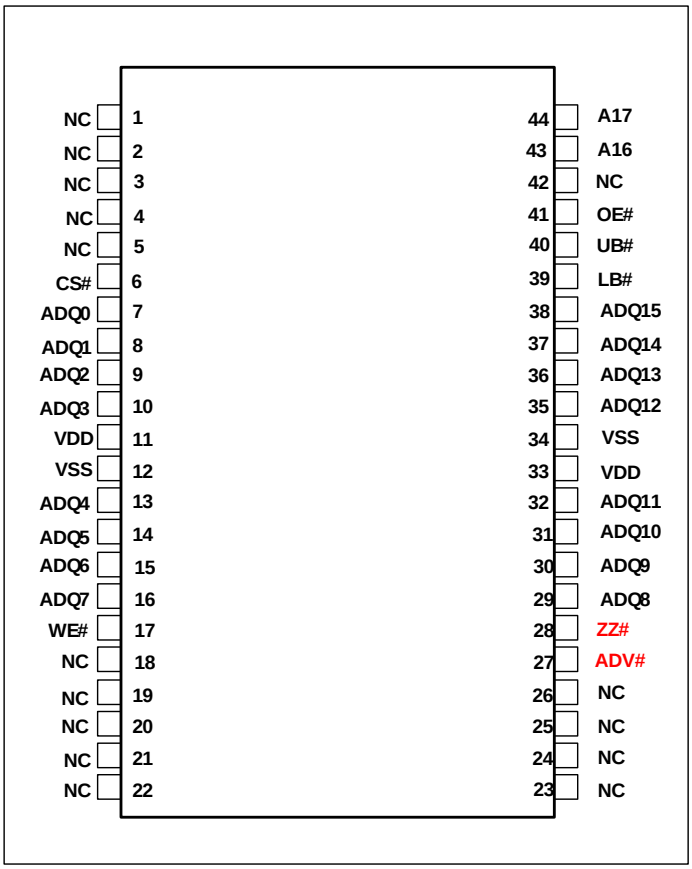
PIN DESCRIPTIONS

ADQ0-ADQ15	Address Inputs (A0~A15) Data Inputs/Outputs (DQ0~DQ15)
A16,A17	Address Input
CS#	Chip Enable Input
OE#	Output Enable Input
WE#	Write Enable Input
LB#	Lower-byte Control (ADQ0-ADQ7)
UB#	Upper-byte Control (ADQ8-ADQ15)
ERR1	1-bit Error Detection and Correction Signal
ERR2	2-bit ERR Detection Signal
ZZ#*	Power Sleep Mode. Ultra Low Standby current when Low.
ADV#	Address Valid signal Signal that a valid address is present on the address bus. Address is latched on the rising edge of ADV# during asynchronous Read/Write operations.
NC	No Connection
VDD	Power
VSS	Ground

Notes:

1. ZZ# pin is internally pulled HIGH.

44-Pin TSOP-II with ZZ#



FUNCTION DESCRIPTION

ADMUX SRAM is the SRAM with Multiplexed Address and I/O pins via ADV# pin to minimize pin-counts.

ADMUX OPERATION

ADMUX (Address DQ Multiplex) operation consists of two paths, based on ADV# state. Address path is the first one and data path follows. During address path operation, ADV# is asserted Low and it indicates device to receive valid address information. Command information will be also applied during ADV# Low. WE# determines operation of read and write. Valid address setup/hold time to ADV# High time must be met to latch the address information, including A16, A17 address.
Data path operation follows with ADV# High. ADQ0~ADQ15 become input/output buffer upon ADV# High.

ADV#	ADQ0~ADQ15	Requirements
LOW	Address Path : Address Buffer	ADQ0~ADQ15 must be HIGH-Z from previous Read operation before asserting ADV# Low in continuous Read Operation to avoid bus contention.
HIGH	Data Path : Input/Output Buffer	Valid Address Setup/Hold time to ADV# High must be met.

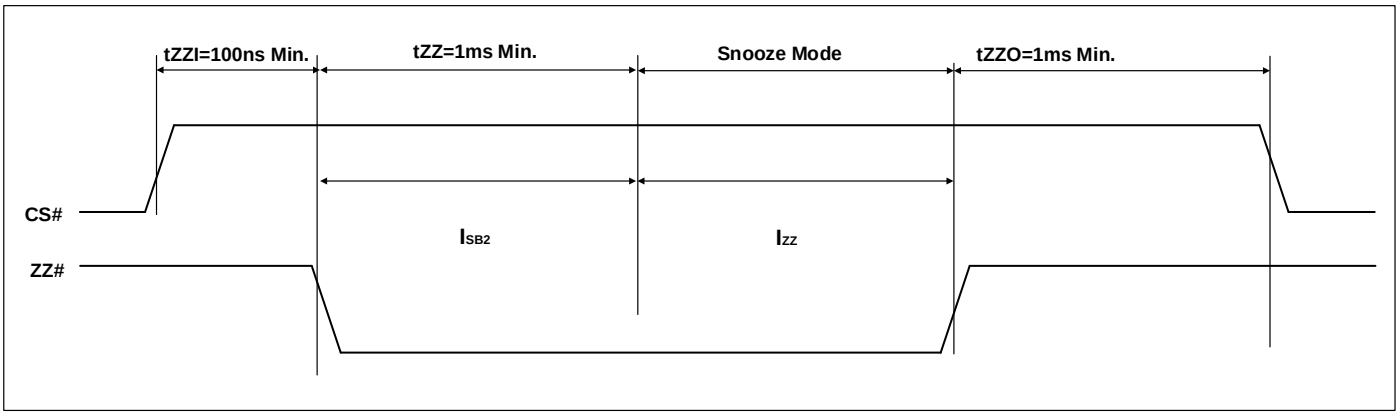
STANDBY MODE

Device enters standby mode when deselected (CS# HIGH). The input and output pins (ADQ0-15) are placed in a high impedance state. The current consumption in this mode will be ISB1, or ISB2.

SNOOZE MODE

Device enters Snooze mode from Standby mode when asserting ZZ# Low, tZZI (100ns Min) after CS# High. Upon assertion of ZZ# Low, the device enters Snooze mode from Standby mode after tZZ (1ms Min.). During Snooze mode, the device must remain standby mode (CS# High), and ZZ# must remain asserted Low. Snooze mode can minimize Standby power consumption.
To exit Snooze mode, ZZ# must be de-asserted (High). The device returns to Standby mode from Snooze mode and CS# can be asserted Low, tZZO (1ms Min.) after de-assertion of ZZ# High.

SNOOZE MODE WAVEFORM



WRITE MODE

Write operation issues with Chip Select (CS#) Low, Write Enable (WE#) Low and ADV# Low. The ADQ pins (ADQ 0-15) act as Address inputs together with A16, A17 when ADV# is Low. UB# and LB# enables a byte write feature. By enabling ADV# High, ADQ pins (ADQ 0-15) become Data Inputs.

READ MODE

Read operation issues with Chip Select (CS#) Low, Write Enable (WE#) High, and ADV# Low. The ADQ pins (ADQ 0-15) act as Address inputs together with A16, A17 when ADV# is Low. UB# and LB# enables a byte Read feature. OE# is an Asynchronous pin to control output time.
By enabling ADV# High, ADQ pins (ADQ 0-15) become Data Outputs. Upon Read operation, ADQ bus must be entered into HIGH-Z state at the end of the READ cycle by disabling OE#, CS#, or UB#/LB# to avoid bus contention with following external address.

ERROR DETECTION AND ERROR CORRECTION

- Independent ECC per each byte
  - detect and correct 1-bit error per byte or detect multi-bit error per byte
- Optional ERR1 output signal indicates 1-bit error detection and correction
- Optional ERR2 output signal indicates multi-bit error detection.
- Controller can use either ERR1 or ERR2 to monitor ECC event. Unused pins (ERR1 or ERR2) can be left floating.
- Better reliability than parity code schemes which can only detect an error but not correct an error
- Backward Compatible: Drop in replacement to current in industry standard devices (without ECC)

ERR1, ERR2 OUTPUT SIGNAL BEHAVIOR

ERR1	ERR2	DQ pin	Status	Remark
0	0	Valid Q	No Error	
1	0	Valid Q	1-Bit Error only	1-bit error per byte detected and corrected
0	1	In-Valid Q	Multi-Bit Error only	No 1-bit error. Multi-bit error per byte detected (out of 2 bytes)
1	1	In-Valid Q	1-bit & Multi-bit error	1-bit error detected and corrected at one byte, and multi-bit error detected at another byte.
High-Z	High-Z	Valid D	Non-Read	Write operation or Output Disabled

TRUTH TABLE

Mode	CS#	ZZ# (1)	WE#	OE#	LB#	UB#	ADQ0-ADQ7	ADQ8-ADQ15	VDD Current
Not Selected	H	H	X	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
	H	L	X	X	X	X	High-Z	High-Z	I_{ZZ}
Output Disabled	L	H	H	H	L	X	High-Z	High-Z	ICC,ICC1
	L	H	X	X	H	H	High-Z	High-Z	
Read	L	H	H	L	L	H	DOUT	High-Z	ICC,ICC1
	L	H	H	L	H	L	High-Z	DOUT	
	L	H	H	L	L	L	DOUT	DOUT	
Write	L	H	L	X	L	H	DIN	High-Z	ICC,ICC1
	L	H	L	X	H	L	High-Z	DIN	
	L	H	L	X	L	L	DIN	DIN	

Notes:

1. ZZ# pin can be left floating because it is internally pulled HIGH.

ABSOLUTE MAXIMUM RATINGS AND Operating Range

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
Vterm	Terminal Voltage with Respect to VSS	–0.5 to V_{DD} + 0.5V	V
V_{DD}	V_{DD} Related to VSS	–0.3 to 4.0	V
tStg	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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PIN CAPACITANCE (1)

Parameter	Symbol	Test Condition	Max	Units
Input capacitance	C_{IN}	T_A = 25°C, f = 1 MHz, V_{DD} = V_{DD}(typ)	6	pF
DQ capacitance (IO0–IO15)	$C_{I/O}$		8	pF

Note:
1. These parameters are guaranteed by design and tested by a sample basis only.

OPERATING RANGE(1)

Range	Ambient Temperature	PART NUMBER	SPEED (MAX)	VDD
Commercial	0°C to +70°C	IS61WV25616MEBLL	10 ns	2.4V – 3.6V
Industrial	-40°C to +85°C		10 ns	2.4V – 3.6V
Automotive (A1)	-40°C to +85°C	IS64WV25616MEBLL	10 ns	2.4V – 3.6V
Automotive (A3)	-40°C to +125°C	IS64WV25616MEBLL	12 ns	2.4V – 3.6V

Note:
1. Full device AC operation assumes a 100 µs ramp time from 0 to V_{DD}(min) and 200 µs wait time after V_{DD} stabilization.

THERMAL CHARACTERISTICS (1)

Parameter	Symbol	Rating	Units
Thermal resistance from junction to ambient (airflow = 1m/s)	$R_{\theta JA}$	TBD	°C/W
Thermal resistance from junction to pins	$R_{\theta JB}$	TBD	°C/W
Thermal resistance from junction to case	$R_{\theta JC}$	TBD	°C/W

Note:
1. These parameters are guaranteed by design and tested by a sample basis only.

AC TEST CONDITIONS (OVER THE OPERATING RANGE)

Parameter	Unit (2.4V~3.6V)
Input Pulse Level	0.4V to V_{DD} -0.3V
Input Rise and Fall Time	1.0ns
Input and Output Timing and Reference Level (V_{REF})	$V_{DD}/2$
Output Load Conditions	Refer to Figure 1 and 2

OUTPUT LOAD CONDITIONS FIGURES

Figure1

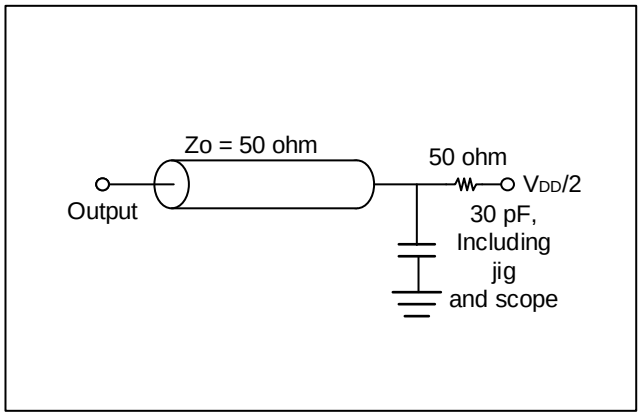
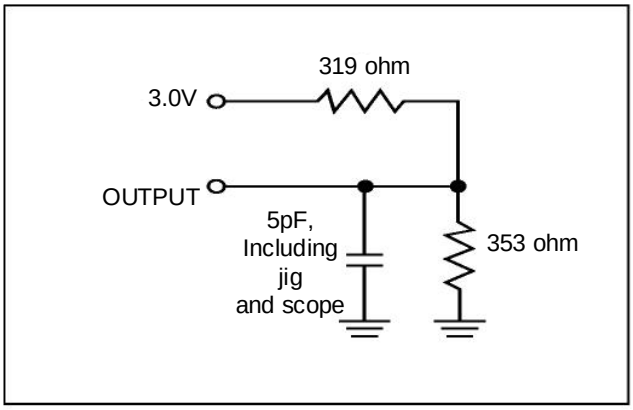


Figure2



DC ELECTRICAL CHARACTERISTICS

IS61(64)WV25616MEBLL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

VDD = 2.4V ~ 3.6V

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = -1.0 mA	1.8	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 1.0 mA	—	0.4	V
V_{IH}(1)	Input HIGH Voltage		2.0	V_{DD} + 0.3	V
V_{IL}(1)	Input LOW Voltage		–0.3	0.8	V
I_{LI}(2)	Input Leakage	VSS < V_{IN} < V_{DD}	–1	1	µA
I_{LO}	Output Leakage	VSS < V_{IN} < V_{DD}, Output Disabled	–1	1	µA

Notes:
1. VIL(min) = -0.3V DC ; VIL(min) = -2.0V AC (pulse width 2.0ns). Not 100% tested.
   VIH (max) = VDD + 0.3V DC ; VIH(max) = VDD + 2.0V AC (pulse width 2.0ns). Not 100% tested..
2. Input Leakage for ZZ# pin is +/-10uA because it is internally pulled HIGH.

POWER SUPPLY CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

Symbol	Parameter	Test Conditions	Grade	-10 Max.	-12 Max.	Unit
ICC	V_{DD} Dynamic Operating Supply Current	V_{DD} = MAX, I_{OUT} = 0 mA, f = tRC_{MIN}	Com.	60	55	mA
			Ind.	70	65	
			Auto.	80	75	
			Typ. (2)	40		
ICC1	Operating Supply Current	V_{DD} = MAX, I_{OUT} = 0 mA, f = 0	Com.	15	15	mA
			Ind.	20	20	
			Auto.	30	30	
ISB1	TTL Standby Current (TTL Inputs)	V_{DD} = MAX, V_{IN} = V_{IH} or V_{IL}, CS# ≥ V_{IH}, f = 0	Com.	25	25	mA
			Ind.	30	30	
			Auto.	40	40	
ISB2	CMOS Standby Current (CMOS Inputs)	V_{DD} = MAX, CS# ≥ V_{DD} - 0.2V, V_{IN} ≥ V_{DD} - 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com.	15	15	mA
			Ind.	20	20	
			Auto.	30	30	
			Typ. (2)	10		
IZZ	Snooze Mode Current (CMOS Inputs)	V_{DD} = MAX, CS# ≥ V_{DD} - 0.2V, ZZ# ≤ 0.2V, V_{IN} ≥ V_{DD} - 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com.	60	60	uA
			Ind.	80	80	
			Auto.	110	110	
			Typ. (2)	30		

Notes:
1. At f = fMAX, address and data inputs are cycling at the maximum frequency, f = 0 means no input line change.
2. Typical values are measured at V_{DD} = 3.0V, T_A = 25 °C and not 100% tested.

AC CHARACTERISTICS (OVER OPERATING RANGE)

READ CYCLE AC CHARACTERISTICS

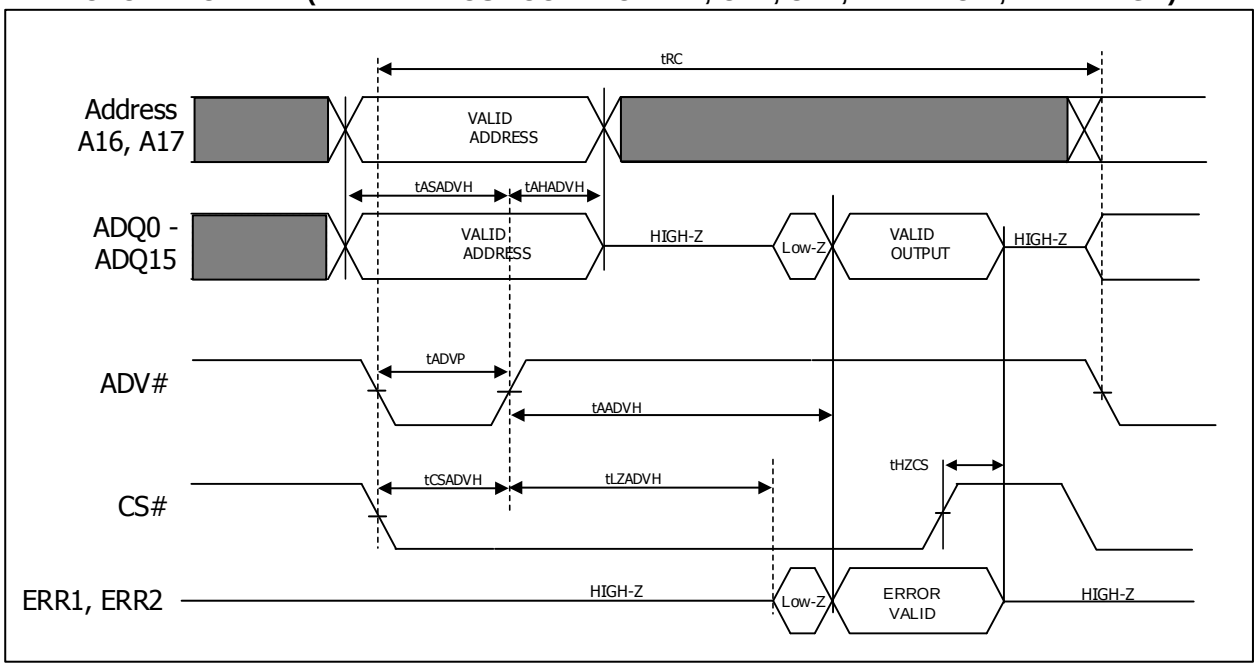
Parameter	Symbol	-10(1)		-12(1)		unit	notes
		Min	Max	Min	Max		
Read Cycle Time	tRC	18	-	20	-	ns	3
ADV# High Access Time	tAADVH	-	10	-	12	ns	
ADV# High to Low-Z Output	tLZADVH	3	-	3	-	ns	
OE# Access Time	tDOE	-	5	-	6	ns	
OE# to High-Z Output	tHZOE	-	5	-	5	ns	2
OE# to Low-Z Output	tLZOE	0	-	0	-	ns	2
CS# to High-Z Output	tHZCS	-	5	-	5	ns	2
UB#, LB# Access Time	tBA	-	5	-	6	ns	
UB#, LB# to High-Z Output	tHZB	-	5	-	5	ns	2
UB#, LB# to Low-Z Output	tLZB	0	-	0	-	ns	2
CS# Setup to ADV# High	tCSADVH	3	-	3	-	ns	4
Address Setup to ADV# High	tASADVH	3	-	3	-	ns	
Address Hold from ADV# High	tAHADVH	2	-	2	-	ns	
ADV# Low Pulse Width	tADVP	3	-	3	-	ns	

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of VDD/2, and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. ADQ bus must be entered into HIGH-Z state at the end of the READ, which requires tRC greater than tAA/tACS.
4. CS# must stay Low during valid Read Operation.

Timing Diagram

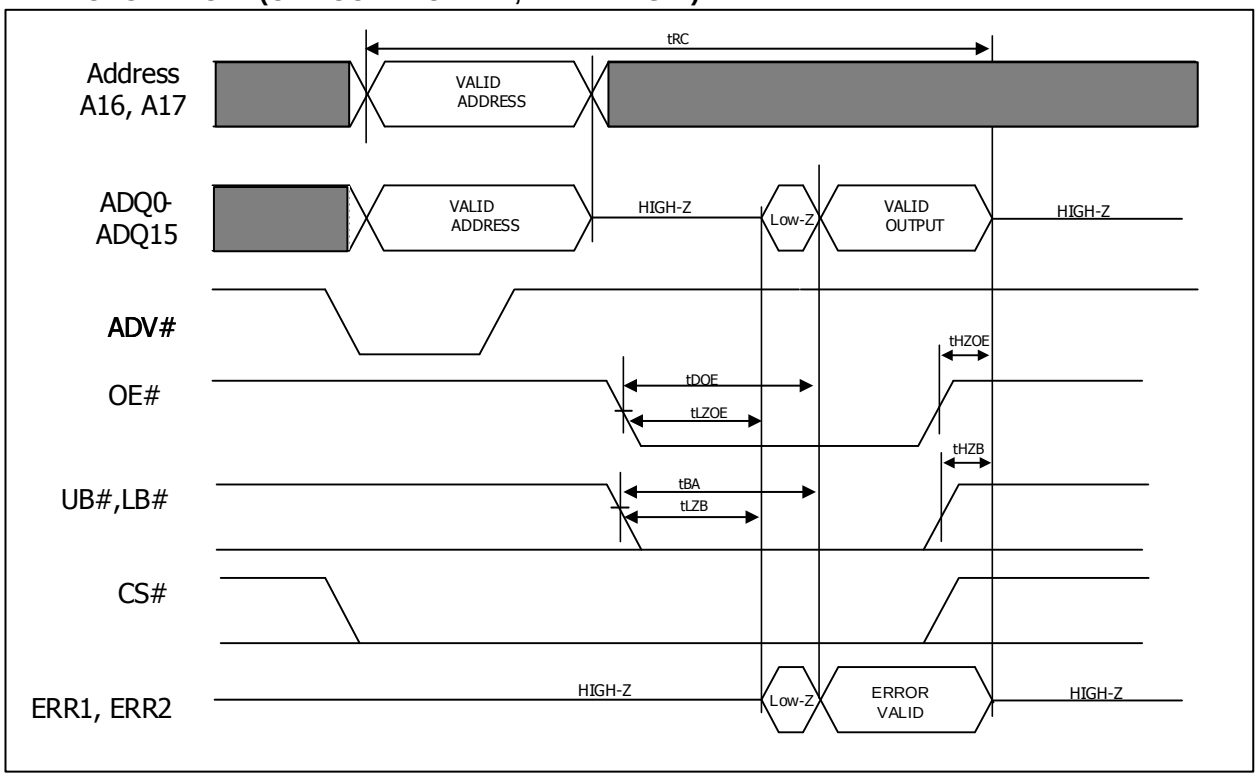
READ CYCLE NO. 1[1,2,3] (ADV# AND CS# CONTROLLED, OE#, UB#, LB# = LOW, WE# = HIGH)



Notes:

1. ERR1, ERR2 signals act like a Read Data Q during Read Operation.
2. ADQ bus must be entered into HIGH-Z state at the end of the READ cycle by disabling OE#, CS#, or UB#/LB# to avoid bus contention with following external address.
3. If tAHADVH applies longer than tLZADVH, OE# needs to be controlled to avoid BUS contention

READ CYCLE NO. 2 (OE# CONTROLLED, WE# = HIGH)



WRITE CYCLE AC CHARACTERISTICS

Parameter	Symbol	-10(1)		-12(1)		unit	notes
		Min	Max	Min	Max		
Write Cycle Time	tWC	18	-	20	-	ns	
UB#,LB# to Write End	tPWB	7	-	8	-	ns	2
WE# Pulse Width	tPWE	7	-	8	-	ns	2,3
Data Setup to Write End	tSD	5	-	6	-	ns	
Data Hold from Write End	tHD	0	-	0	-	ns	
Address Setup to ADV# High	tASADVH	3.0	-	3.0	-	ns	
CS# Setup to ADV# High	tCSADVH	3.0	-	3.0	-	ns	2
Address Hold from ADV# High	tAHADVH	2	-	2	-	ns	
ADV# Low Pulse Width	tADVP	3.0	-	3.0	-	ns	
ADV# High to Write End	tADVHWH	10	-	12	-	ns	
WE# LOW to High-Z Output	tHZWE	-	5	-	5	ns	3
WE# HIGH to Low-Z Output	tLZWE	3	-	3	-	ns	3

Notes:

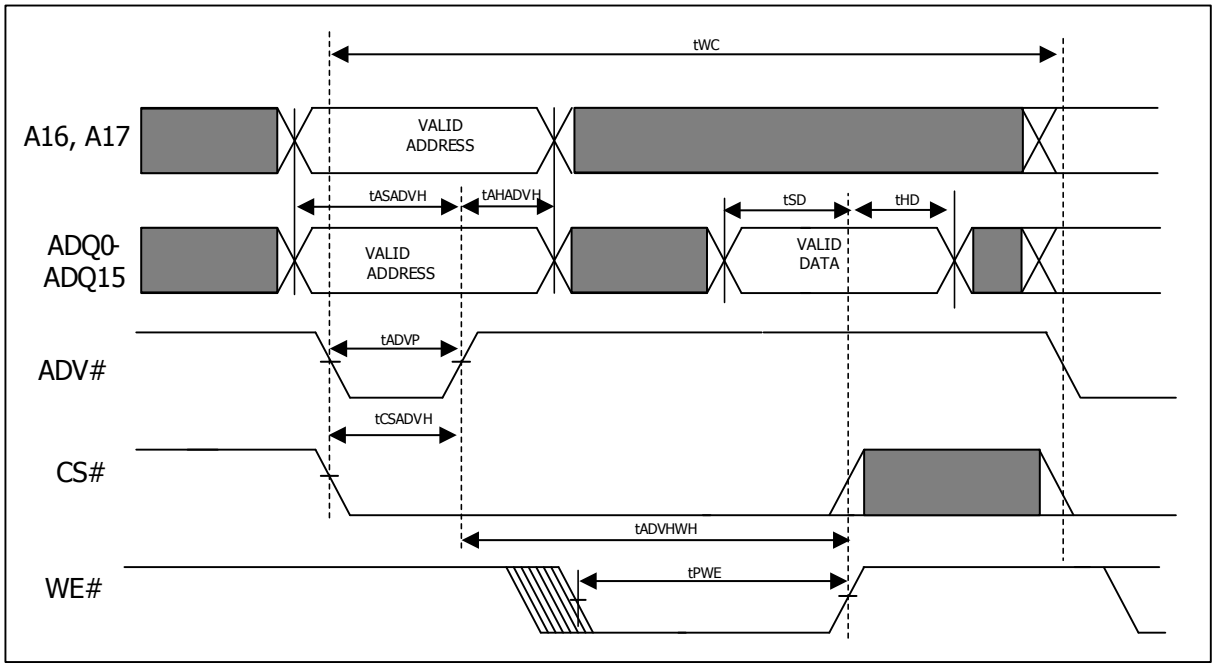
1 Test conditions assume signal transition times of 3 ns or less, timing reference levels of VDD/2, and output loading specified in Figure 1.

2 The internal write time is defined by the overlap of CS#=LOW, UB# or LB# = LOW , and WE#=LOW. All signals must be in valid states to initiate a Write, but anyone can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

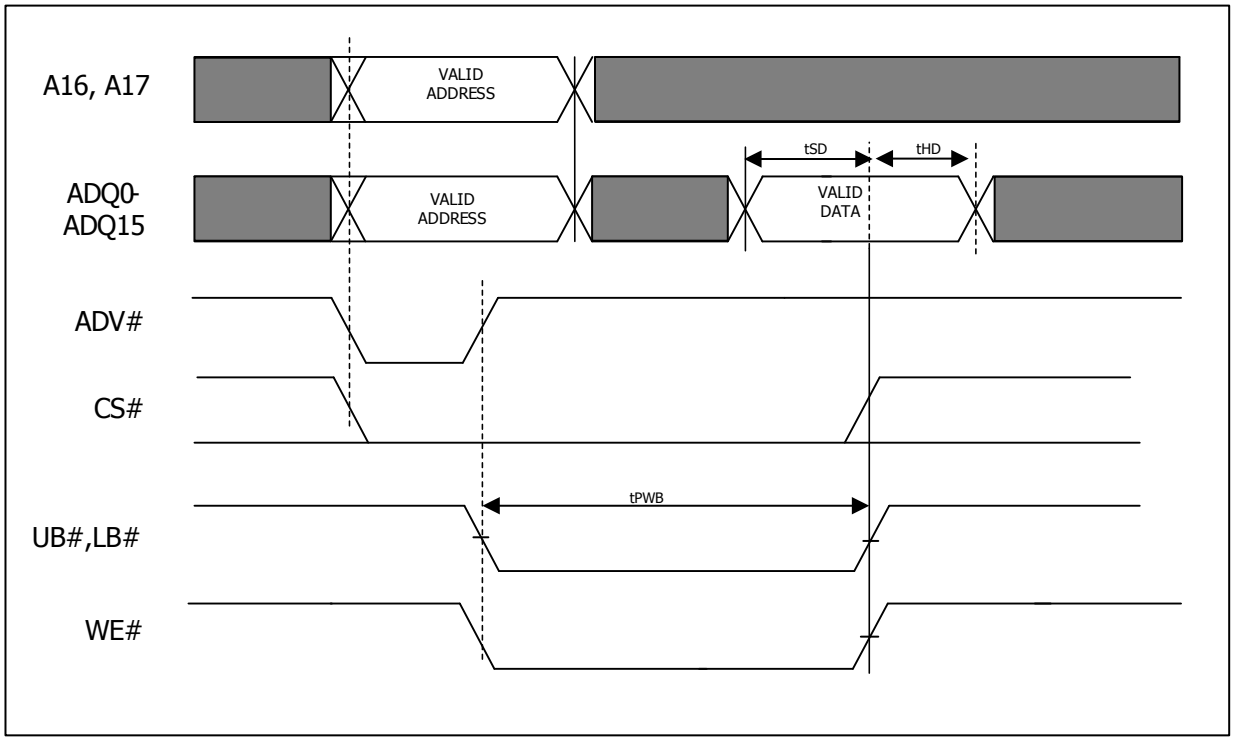
3 If OE# is LOW during write cycle, (WE# controlled, CS# = UB# = LB# = LOW), the minimum write pulse width is the sum of tHZWE and tSD.

Timing Diagram

WRITE CYCLE NO. 1 (WE# CONTROLLED, UB#, LB# = LOW, OE# = HIGH)



WRITE CYCLE NO. 2 (UB# AND LB# CONTROLLED, OE# = HIGH)

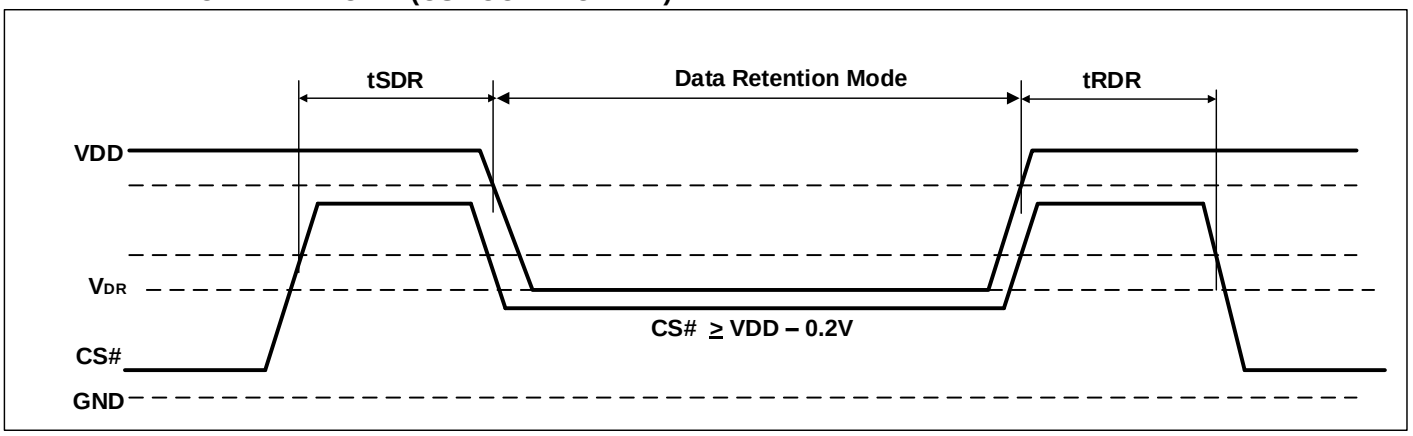


DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Test Condition	OPTION	Min.	Typ.(2)	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.0	-	3.6	V
I_{DR}	Data Retention Current	V_{DD}= MAX, CS# ≥ V_{DD} – 0.2V	Com.	-	10	15	mA
			Ind.	-	-	20	
			Auto	-	-	30	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0	-	-	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		tRC	-	-	ns

Notes:
1. If CS# >VDD–0.2V, all other inputs including UB# and LB# must meet this condition.
2. Typical values are measured at VDD=3.0V, TA = 25℃ and not 100% tested.

DATA RETENTION WAVEFORM (CS# CONTROLLED)



ORDERING INFORMATION

Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
10	IS61WV25616MEBLL-10BI	mini BGA (6mm x 8mm)
10	IS61WV25616MEBLL-10BLI	mini BGA (6mm x 8mm), Lead-free
10	IS61WV25616MEBLL-10B2I	mini BGA (6mm x 8mm), ERR1/ERR2 Pins
10	IS61WV25616MEBLL-10B2LI	mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free
10	IS61WV25616MEBLL-10TI	TSOP (Type II)
10	IS61WV25616MEBLL-10TLI	TSOP (Type II), Lead-free
12	IS61WV25616MEBLL-12BI	mini BGA (6mm x 8mm)
12	IS61WV25616MEBLL-12BLI	mini BGA (6mm x 8mm), Lead-free
12	IS61WV25616MEBLL-12B2I	mini BGA (6mm x 8mm), ERR1/ERR2 Pins
12	IS61WV25616MEBLL-12B2LI	mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free
12	IS61WV25616MEBLL-12TI	TSOP (Type II)
12	IS61WV25616MEBLL-12TLI	TSOP (Type II), Lead-free

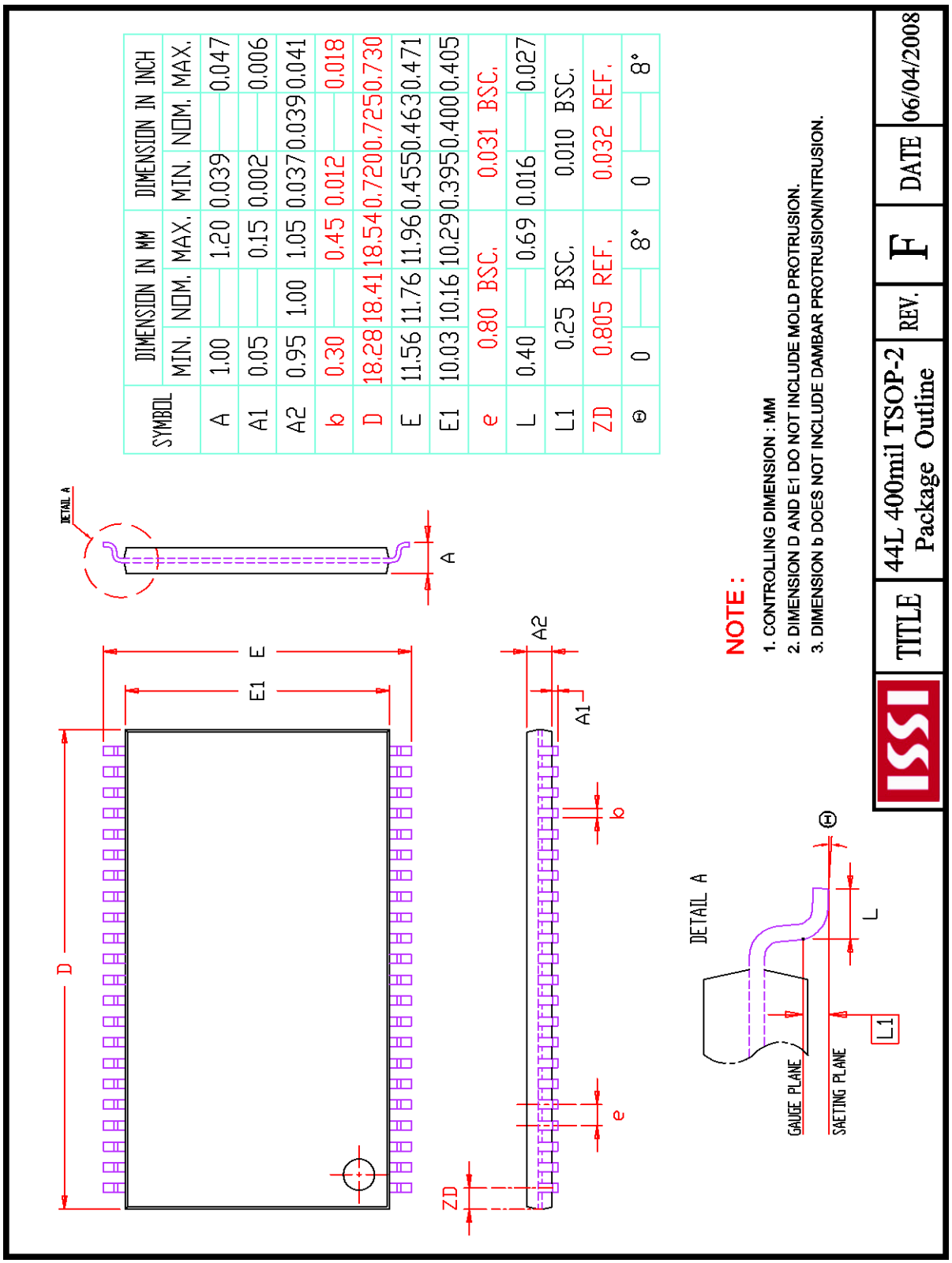
AUTOMOTIVE RANGE (A1): –40°C TO +85°C

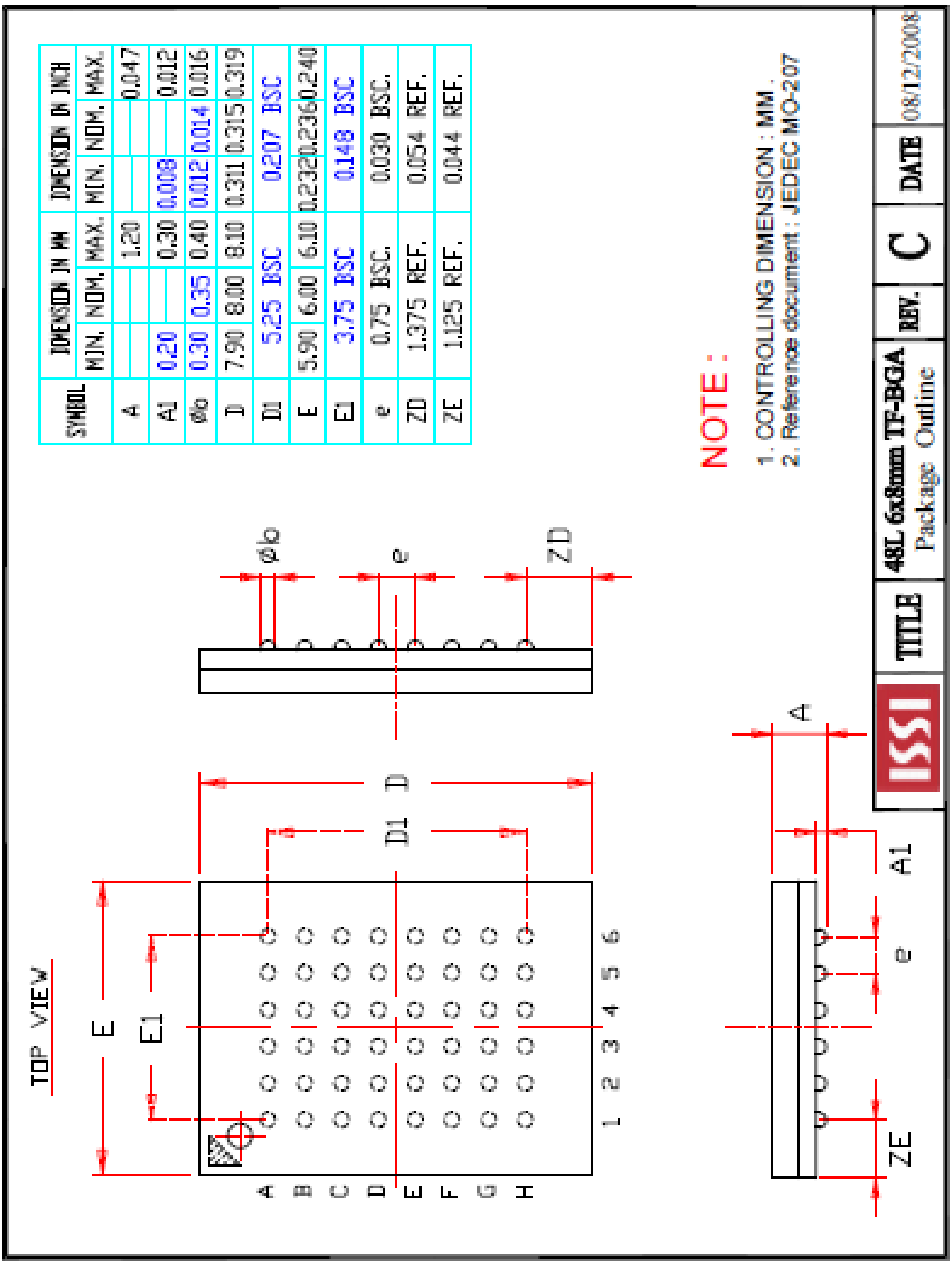
Speed (ns)	Order Part No.	Package
10	IS64WV25616MEELL-10BA1	mini BGA (6mm x 8mm)
10	IS64WV25616MEELL-10BLA1	mini BGA (6mm x 8mm), Lead-free
10	IS64WV25616MEBLL-10B2A1	mini BGA (6mm x 8mm), ERR1/ERR2 Pins
10	IS64WV25616MEBLL-10B2LA1	mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free
10	IS64WV25616MEBLL-10CTA1	TSOP (Type II), Copper Leadframe
10	IS64WV25616MEBLL-10CTLA1	TSOP (Type II), Copper Leadframe , Lead-free

AUTOMOTIVE RANGE (A3): –40°C TO +125°C

Speed (ns)	Order Part No.	Package
12	IS64WV25616MEELL-12BA3	mini BGA (6mm x 8mm)
12	IS64WV25616MEELL-12BLA3	mini BGA (6mm x 8mm), Lead-free
12	IS64WV25616MEBLL-12B2A3	mini BGA (6mm x 8mm), ERR1/ERR2 Pins
12	IS64WV25616MEBLL-12B2LA3	mini BGA (6mm x 8mm), ERR1/ERR2 Pins, Lead-free
12	IS64WV25616MEBLL-12CTA3	TSOP (Type II), Copper Leadframe
12	IS64WV25616MEBLL-12CTLA3	TSOP (Type II), Copper Leadframe , Lead-free

PACKAGE INFORMATION




SYMBOL
DIMENSION IN MM
MIN. NOM. MAX.
DIMENSION IN INCH
MIN. NOM. MAX.
A — — 1.20 — — 0.047
A1 0.20 — 0.30 0.008 — 0.012
ϕb 0.30 0.35 0.40 0.012 0.014 0.016
D 7.90 8.00 8.10 0.311 0.315 0.319
D1 5.25 BSC 0.207 BSC
E 5.90 6.00 6.10 0.232 0.236 0.240
E1 3.75 BSC 0.148 BSC
e 0.75 BSC. 0.030 BSC.
ZD 1.375 REF. 0.054 REF.
ZE 1.125 REF. 0.044 REF.
NOTE :
1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207
ISSI
TITLE
48L 6x8mm TF-BGA Package Outline
REV. C
DATE 08/12/2008
TOP VIEW
A B C D E F G H
1 2 3 4 5 6
D
D1
E
E1
ϕb
e
ZD
A
A1
e
ZE