IS25DLP512M
IS25DWP512M

512Mb (2 x 256Mb)
3.3V/1.8V SERIAL FLASH MEMORY WITH 80MHZ DUAL-CHANNEL MULTI I/O SPI & QUAD I/O QPI DTR INTERFACE

ADVANCED DATA SHEET

512Mb (2 x 256Mb)

3.3V/1.8V SERIAL FLASH MEMORY WITH 80MHZ DUAL-CHANNEL MULTI I/O SPI & QUAD I/O QPI DTR INTERFACE

ADVANCED INFORMATION

FEATURES

- **Industry Standard Serial Interface**
  - IS25DLP/DWP512M: 512Mbit/64Mbyte
  - Dual Die Stack of two IS25LP/WP256D
  - 256 bytes per Programmable Page
  - Supports standard SPI and QPI protocols
  - Double Transfer Rate (DTR) : SPI DTR, Dual I/O SPI DTR , and Quad I/O SPI DTR
  - Supports Serial Flash Discoverable Parameters (SFDP)
  - Support Hardware RESET# Feature

- **High Performance Serial Flash (SPI)**
  - 80MHz Normal and 166Mhz Fast Read
  - DTR (Dual Transfer Rate) up to 80MHz
  - Equivalent Max. DTR Performance of 160 MB/s
  - Selectable dummy cycles
  - Configurable drive strength
  - Supports SPI Modes 0 and 3
  - More than 100,000 erase/program cycles
  - More than 20-year data retention

- **Flexible & Efficient Memory Architecture**
  - Chip Erase with Uniform: Sector/Block Erase (4/32/64 Kbyte)
  - Program 1 to 256 bytes per page
  - Program/Erase Suspend & Resume

- **Efficient Read and Program modes**
  - Low Instruction Overhead Operations
  - QPI for reduced instruction overhead
  - Continuous Read 8/16/32/64-Byte Burst Wrap
  - Selectable burst length

- **Low Power with Wide Temp. Ranges**
  - Single Voltage Supply
    IS25DLP: 2.30V to 3.60V
    IS25DWP: 1.65V to 1.95V
  - 10 mA Active Read Current per die
  - 8 µA Standby Current per die
  - 1 µA Deep Power Down per die
  - Temp Grades:
    Extended: -40°C to +105°C
    Extended+: -40°C to +125°C
    Auto Grade: up to +125°C

- **Advanced Security Protection**
  - Software and Hardware Write Protection
  - Power Supply lock protect
  - 4x256-Byte dedicated security area with user-lockable bits, (OTP) One Time Programmable Memory
  - 128 bit Unique ID for each device

- **Industry Standard Pin-out & Packages**
  - M = 16-pin SOIC 300mil
  - H = 24-ball TFBGA 6x8mm 5x5

GENERAL DESCRIPTION

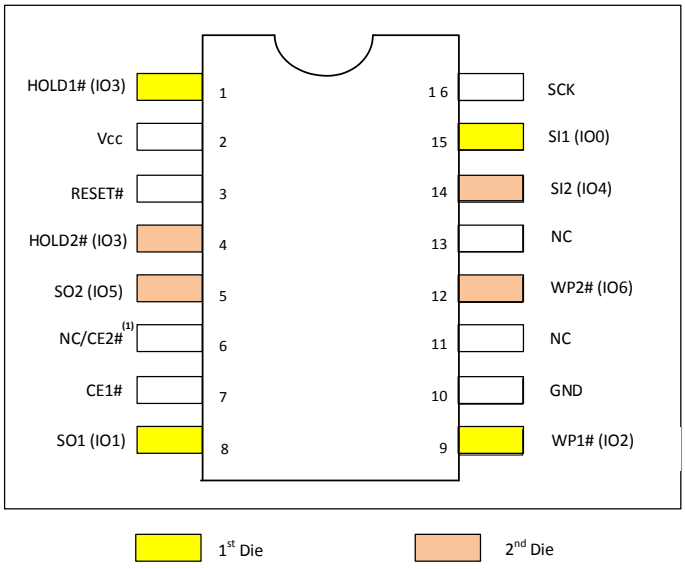
This document contains for the IS25DLP/DWP512M device. The device is a dual die stack of two IS25LP/WP256D dies.
For detailed specifications, please refer to the discrete die datasheet linked below.

Document	Datasheet
IS25LP256D Datasheet	Call Factory
IS25WP256D Datasheet	Call Factory

1. **All specification noted are per IS25LP/WP256D device**

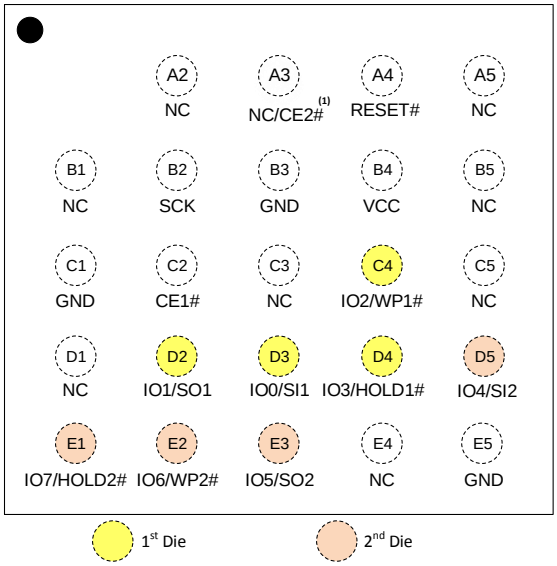
TABLE OF CONTENTS

1. PIN CONFIGURATION



16-pin SOIC 300mil

Top View, Balls Facing Down



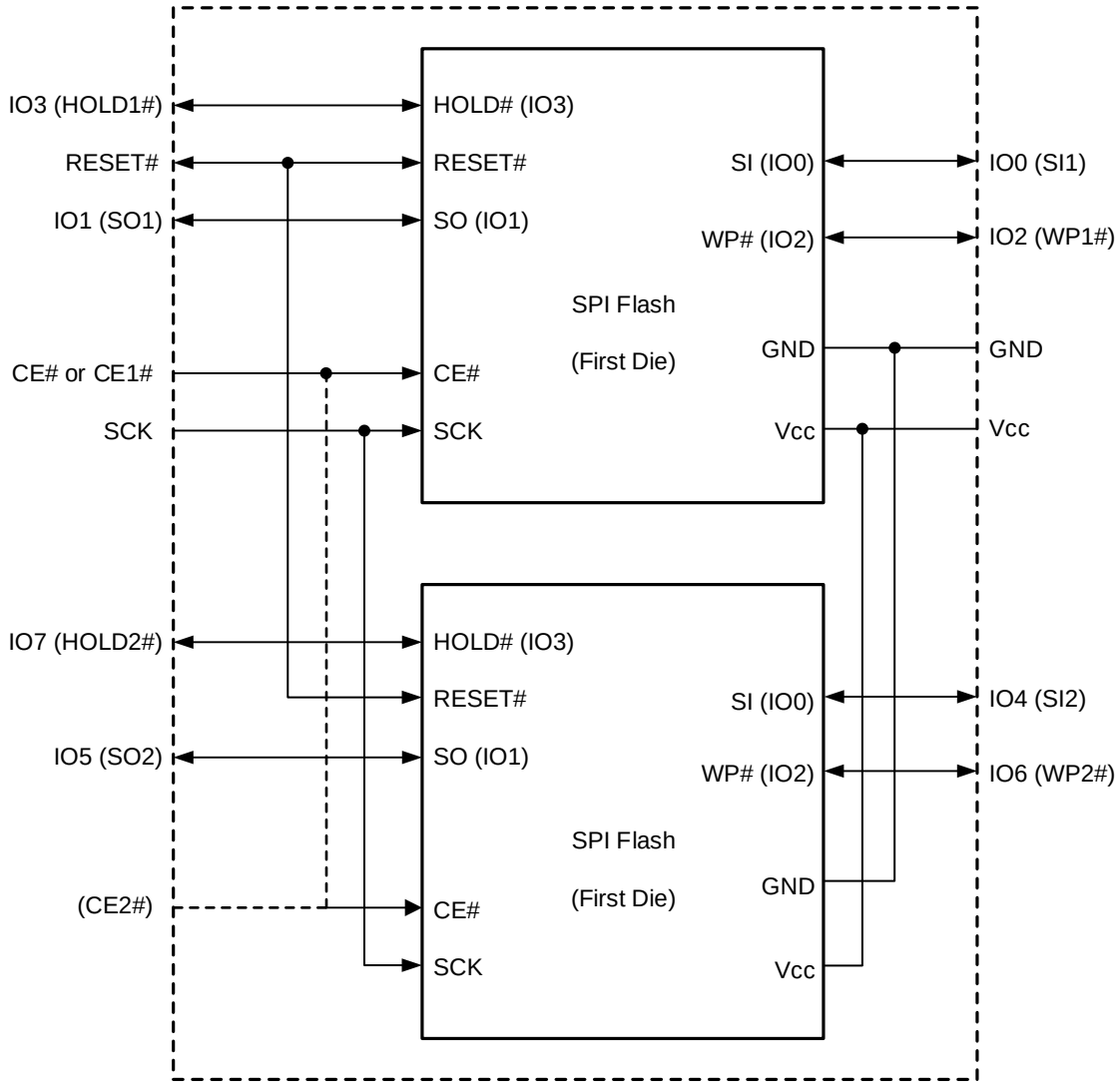
24-ball TFBGA

Note:
1. **See the Ordering Information for the CE2# pin (or ball) option.**

PIN DESCRIPTIONS

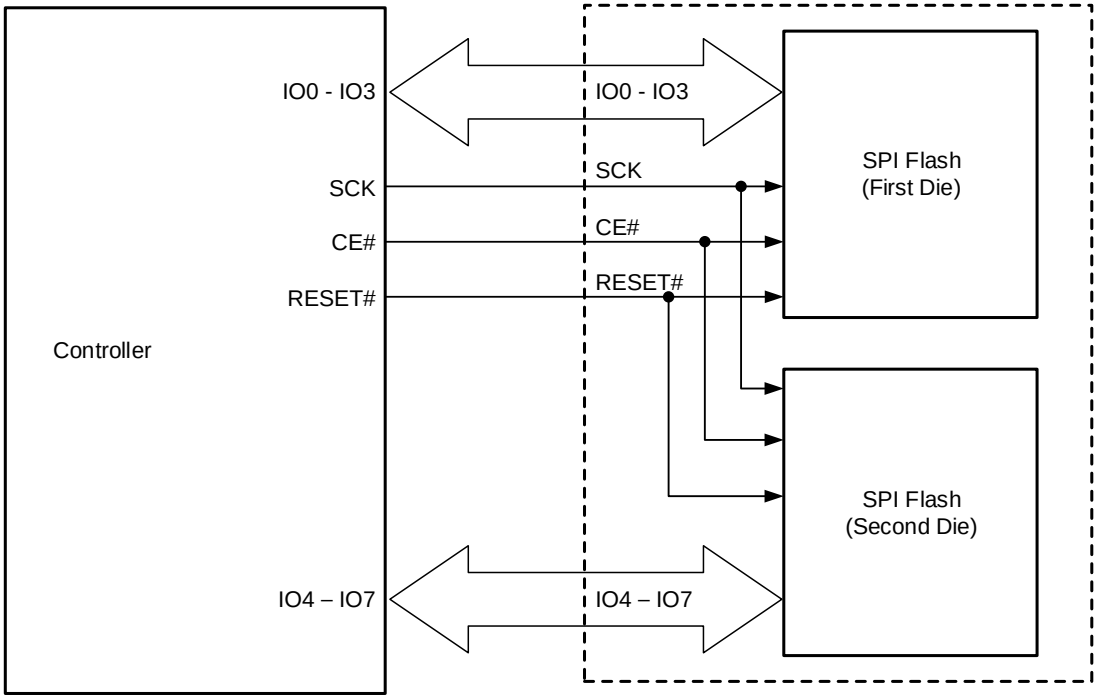
SYMBOL	TYPE	DESCRIPTION
CE# (1 CE#)	INPUT	**Chip Enable:** The Chip Enable pin (CE#) enables or disables the device operation. Since CE# is connected to both stack dies, CE# enables or disables the operation of both dies simultaneously. When CE# is high the device is deselected and output pins are in a high impedance state. When deselected the device non-critical internal circuitry power down to allow minimal levels of power consumption while in a standby state. When CE# is pulled low the device will be selected and brought out of standby mode. The device is considered active and instructions can be written to, data read, and written to the device. After power-up, CE# must transition from high to low before a new instruction will be accepted. Keeping CE# in a high state deselects the device and switches it into its low power state. Data will not be accepted when CE# is high.
CE1# CE2# (2 CE#)	INPUT	**Chip Enable:** The Chip Enable pins (CE1#, CE2#) enable or disable the device operation. CE1# is connected to the first die and CE2# is connected to the second die, CE1# enables or disables the first die and CE2# does the second die. When CE1# or CE2# is high the corresponding die is deselected and output pins of the die are in a high impedance state. When deselected the die non-critical internal circuitry power down to allow minimal levels of power consumption while in a standby state. When CE1# or CE2# is pulled low the corresponding die will be selected and brought out of standby mode. The die is considered active and instructions can be written to, data read, and written to the device. After power-up, CE1# or CE#2 must transition from high to low before a new instruction will be accepted. Keeping CE1# or CE2# in a high state deselects the corresponding die and switches it into its low power state. Data will not be accepted on the corresponding die when CE1# or CE2# is high.
IO0 (SI1), IO1 (SO1) IO4 (SI2), IO5 (SO2)	INPUT/OUTPUT	**Serial Data Input/Serial Data IO, Serial Output/Serial Data IO:** Same as 16-pin SOIC 300mil
IO2 (WP1#) IO6 (WP2#)	INPUT/OUTPUT	**Write Protect/Serial Data IO:** Same as 16-pin SOIC 300mil
IO3 (HOLD1#) IO7 (HOLD2#)	INPUT/OUTPUT	**Hold/Serial Data IO:** Same as 16-pin SOIC 300mil
RESET#	INPUT	**RESET#:** The RESET# pin is a hardware RESET signal. When RESET# is driven HIGH, the memory is in the normal operating mode. When RESET# is driven LOW, the memory enters reset mode and output is High-Z. If RESET# is driven LOW while an internal WRITE, PROGRAM, or ERASE operation is in progress, data may be lost.
SCK	INPUT	**Serial Data Clock:** Synchronized Clocks for input and output timing operations.
Vcc	POWER	**Power:** Device Core Power Supply
VIO	POWER	**Power:** Device IO Power Supply, Same Power Supply as Vcc, Connect to VCC
GND	GROUND	**Ground:** Connect to ground when referenced to Vcc
NC	Unused	**NC:** Pins labeled “NC” stand for “No Connect” and should be left unconnected.

2. BLOCK DIAGRAM

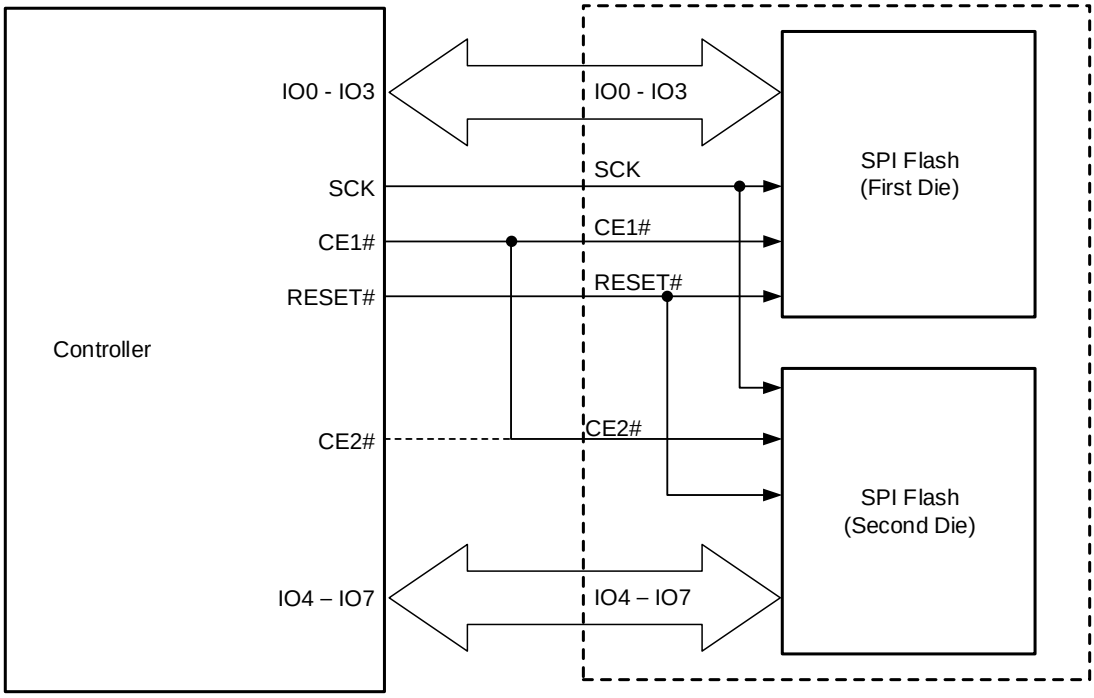


3. PROPOSED CONNECTION

(1 CE# Device)



(2 CE# Device)



4. DEVICE OPERATION

5.1 PROGRAMMING

In the device with 1 CE# pin, both dies will be controlled at the same time. Each die can be programmed independently by command set due to separate IO pins. The first die is controlled by IO0 - IO3 and the second die is controlled by IO4 – IO7.

In the device with 2 CE# pins (CE1# for the first die and CE2# for the second die), it is recommended that CE1# and CE2# should be connected on the board to control both dies at the same time for software to be compatible with 1 CE# device.

5.2 SIMULTANEOUS DIE OPERATION

The user may only access one Flash die of the dual die stack at a time via its respective IO pins.

5.3 SEQUENTIAL READS

Sequential reads are not supported across the end of the first die to the beginning of the second. If the user desires to sequentially read across the two die, data must be read out of the first die via IO0 – IO3 and then read out of the second die via IO4 – IO7.

5.4 SECTOR/CHIP ERASE

A sector erase command must be issued for sectors in each die separately. Full device Bulk Erase via a single command can be supported. In order to execute full device chip erase, a Chip Erase command must be issued for each die by sending the same command via IO0 – IO3 and IO4 – IO7.

If the FRDIO instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not affect the current cycle.

5.5 STATUS REGISTER

Each die of the dual die stack is managed by its own Status Register. Reads and updates to the Status Registers must be managed separately. It is recommended that Status Register control bit settings of each die are kept identical to maintain consistency when switching between die.

5.6 FUNCTION AND READ REGISTER

Each die of the dual die stack is managed by its own Function and Read Register. Updates to the control bits must be managed separately. It is recommended that Register bit settings of each die are kept identical to maintain consistency when switching between die.

5.7 BLOCK PROTECTION

Each die of the dual die stack will maintain its own Block Protection. Updates to the Block Protection Table and respective bits must be managed separately. It is recommended that the Block Protection settings of each die are kept identical to maintain consistency when switching between die.

5. PRODUCT IDENTIFICATION/SFDP/SECURITY INFORMATION ROW

6.1 PRODUCT ID READ COMMANDS (ABh, 90h, 9Fh)

Each die of the dual die stack will have identical identification data as the IS25WP256A die. User can read product ID from either die to identify the device.

6.2 SFDP (5Ah)

Each die of the dual die stack will have identical SFDP table. User can read SFDP table from either die to identify the device.

6.3 SECURITY INFORMATION ROW (64h, 62h, 68h)

Each die of the dual die stack will have identical information row. Since each die has 4 x 256 bytes security information row, user can utilize it up to 8 x 256 bytes by erasing or programming information row independently.

6. ELECTRICAL CHARACTERISTICS

7.1 ABSOLUTE MAXIMUM RATINGS (1)

Storage Temperature		-65°C to +150°C
Surface Mount Lead Soldering Temperature	Standard Package	240°C 3 Seconds
	Lead-free Package	260°C 3 Seconds
Input Voltage with Respect to Ground on All Pins		-0.5V to V_{CC} + 0.5V
All Output Voltage with Respect to Ground		-0.5V to V_{CC} + 0.5V
V_{CC}	IS25LP	-0.5V to +6.0V
	IS25WP	-0.5V to +2.5V
Electrostatic Discharge Voltage (Human Body Model)(2)		-2000V to +2000V

Notes:

1. **Applied conditions greater than those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**
2. **ANSI/ESDA/JEDEC JS-001**

7.2 OPERATING RANGE

Operating Temperature (Extended Grade)		-40°C to 125°C
V_{CC} Power Supply	IS25DLP	2.30V (VMIN) –3.60V (VMAX); 3.0V (Typ)
	IS25DWP	1.65V (VMIN) –1.95V (VMAX); 1.8V (Typ)

7.3 DC CHARACTERISTICS - THIS SECTION SUMMARIZES THE DC CHARACTERISTICS OF THE DEVICE PER DIE

(Under operating range)

Symbol	Parameter		Condition		Min	Typ[2]	Max	Units
I_{CC1}	V_{CC} Active Read current[3]		NORD at 80MHz			4	9	mA
			FRD Single at 166MHz			7	9	
			FRD Dual at 166MHz			9	11	
			FRD Quad at 166MHz			11	14	
			FRD Single at 133MHz			6	8	
			FRD Dual at 133MHz			8	10	
			FRD Quad at 133MHz			10	13	
			FRD Quad at 83MHz			8	10	
			FRD Quad at 104MHz			9	11	
			FRD Single DTR at 80MHz			6	8	
			FRD Dual DTR at 80MHz			8	10	
			FRD Quad DTR at 80MHz			10	13	
I_{CC2}	V_{CC} Program Current		CE# = V_{CC}	85°C		25	TBD[6]	mA
				105°C			TBD[6]	
				125°C			30	
I_{CC3}	V_{CC} WRSR Current		CE# = V_{CC}	85°C		25	TBD[6]	
				105°C			TBD[6]	
				125°C			30	
I_{CC4}	V_{CC} Erase Current (SER/4SER/BER32/4BER32/ BER64/4BER64)		CE# = V_{CC}	85°C		25	TBD[6]	
				105°C			TBD[6]	
				125°C			30	
I_{CC5}	V_{CC} Erase Current (CE)		CE# = V_{CC}	85°C		25	TBD[6]	
				105°C			TBD[6]	
				125°C			30	
I_{SB1}	V_{CC} Standby Current CMOS		CE# = V_{CC}, CE#, RESET#[4] = V_{CC}	85°C		10	TBD[6]	µA
				105°C			TBD[6]	
				125°C			100	
I_{SB2}	Deep power down current	IS25LP	CE# = V_{CC}, CE#, RESET#[4] = V_{CC}	85°C		5	TBD[6]	µA
				105°C			TBD[6]	
				125°C			40	
		IS25WP	CE# = V_{CC}, CE#, RESET#[4] = V_{CC}	85°C		1	TBD[6]	
				105°C			TBD[6]	
				125°C			TBD	
I_{LI}	Input Leakage Current		V_{IN} = 0V to V_{CC}				±1[5]	µA
I_{LO}	Output Leakage Current		V_{IN} = 0V to V_{CC}				±1[5]	µA
V_{IL}[1]	Input Low Voltage				-0.5		0.3V_{CC}	V
V_{IH}[1]	Input High Voltage				0.7V_{CC}		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage		I_{OL} = 100 µA				0.2	V
V_{OH}	Output High Voltage		I_{OH} = -100 µA		V_{CC} - 0.2			V

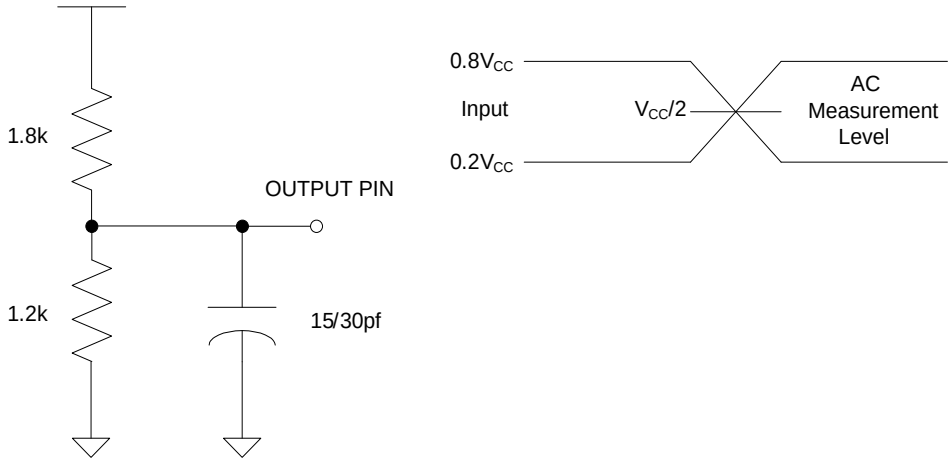
Notes:

1. **Maximum DC voltage on input or I/O pins is VCC + 0.5V. During voltage transitions, input or I/O pins may overshoot VCC by +2.0V for a period of time not to exceed 20ns. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, input or I/O pins may undershoot GND by -2.0V for a period of time not to exceed 20ns.**
2. **Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC}$ (Typ), TA=25°C.**
3. **Outputs are unconnected during reading data so that output switching current is not included.**
4. **Only for the dedicated RESET# pin (or ball).**
5. **The Max of I_{LI} and I_{LO} for the dedicated RESET# pin (or ball) is ±2 µA.**
6. **These parameters are characterized and are not 100% tested.**

7.4 AC MEASUREMENT CONDITIONS

Symbol	Parameter	Min	Max	Units
CL	Load Capacitance up to 104MHz (52MHz DTR)		30	pF
	Load Capacitance up to 166MHz (80MHz DTR)		15	pF
TR,TF	Input Rise and Fall Times		5	ns
VIN	Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
VREFI	Input Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V
VREFO	Output Timing Reference Voltages	$0.5V_{CC}$		V

Figure7.1 Output test load & AC measurement I/O Waveform



7.5 AC CHARACTERISTICS

(Under operating range, refer to section 9.4 for AC measurement conditions)

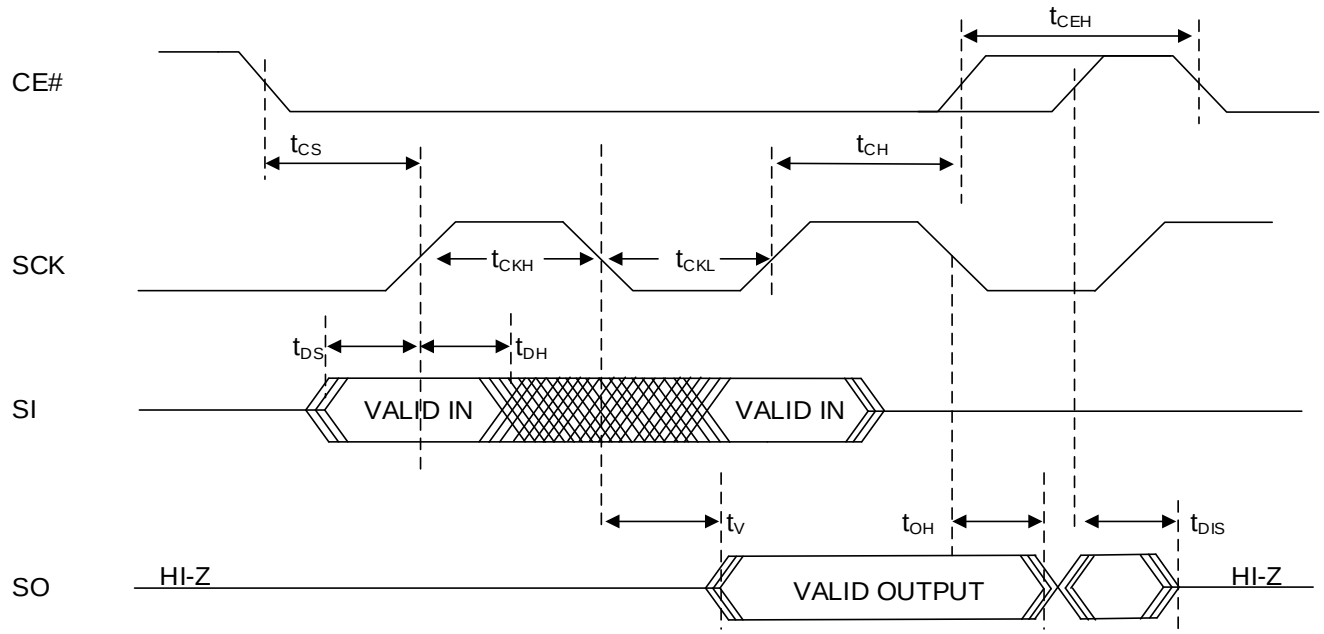
Symbol	Parameter		Min	Typ[3]	Max	Units
f_{CT}	Clock Frequency for fast read mode: SPI, Dual, Dual I/O, Quad I/O, and QPI.		0		166	MHz
f_{C2}, f_{T2}, f_{Q2}	Clock Frequency for fast read DTR: SPI DTR, Dual DTR, Dual I/O DTR, Quad I/O DTR, and QPI DTR.		0		80	MHz
f_C	Clock Frequency for read mode SPI		0		80	MHz
t_{CLCH}[1]	SCK Rise Time (peak to peak)		0.1			V/ns
t_{CHCL}[1]	SCK Fall Time (peak to peak)		0.1			V/ns
t_{CKH}	SCK High Time	For read mode	45% f_C			ns
		For others	45% $f_{CT/C2/T2/Q2}$			
t_{CKL}	SCK Low Time	For read mode	45% f_C			ns
		For others	45% $f_{CT/C2/T2/Q2}$			
t_{CEH}	CE# High Time		7			ns
t_{CS}	CE# Setup Time		3			ns
t_{CH}	CE# Hold Time		3			ns
t_{DS}	Data In Setup Time	Normal Mode	2			ns
		DTR Mode	1.5			
t_{DH}	Data in Hold Time	Normal Mode	2			ns
		DTR Mode	1.5			
t_V	Output Valid	@ 166MHz (CL = 15pF)			7	ns
		@ 133MHz (CL = 15pF)			7	
		@ 104MHz (CL = 30pF)			8	
t_{OH}	Output Hold Time		2			ns
t_{DIS}[1]	Output Disable Time				8	ns
t_{HLCH}	HOLD Active Setup Time relative to SCK		2			ns
t_{CHHH}	HOLD Active Hold Time relative to SCK		2			ns
t_{HHCH}	HOLD Not Active Setup Time relative to SCK		2			ns
t_{CHHL}	HOLD Not Active Hold Time relative to SCK		2			ns
t_{LZ}[1]	HOLD to Output Low Z				8	ns
t_{HZ}[1]	HOLD to Output High Z				8	ns
t_{EC}	Sector Erase Time (4Kbyte)			50	300	ms
	Block Erase Time (32Kbyte)			0.1	0.5	s
	Block Erase time (64Kbyte)			0.15	1.0	s
	Chip Erase Time	256Mb		50	180	s
		128Mb		25	90	
t_{PP}	Page Program Time			0.2	0.8	ms

Symbol	Parameter		Min	Typ(3)	Max	Units
t_{RES1}(1)	Release deep power down	IS25LP			3	µs
		IS25WP			5	
t_{DP}(1)	Deep power down				3	µs
t_W	Write Status Register time			2	15	ms
t_{SUS}(1)	Suspend to read ready				100	µs
t_{SRST}(1)	Software Reset recovery time				100	µs
t_{RESET}(1),(4)	RESET# pin low pulse width		1(2)			µs
t_{HWRST}(1),(4)	Hardware Reset recovery time				100	µs

Notes:
1. **These parameters are characterized and not 100% tested.**
2. **If the RESET# pulse is driven for a period shorter than 1µs (t_{RESET} minimum), it may still reset the device, however the 1µs minimum period is recommended to ensure reliable operation.**
3. **Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} (Typ), TA=25°C**
4. **Only applicable to the parts that have the RESET# pin option**

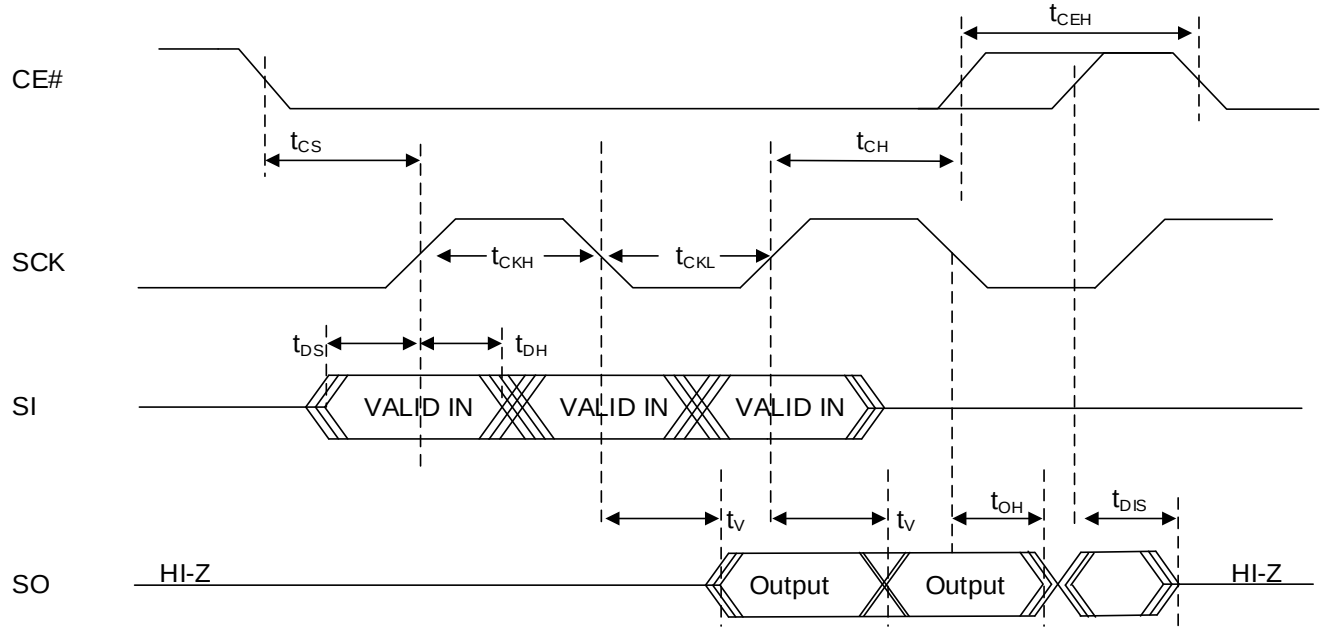
7.6 SERIAL INPUT/OUTPUT TIMING

Figure 7.2 SERIAL INPUT/OUTPUT TIMING (Normal Mode) (1)



Note1. For SPI Mode 0 (0,0)

Figure 7.3 SERIAL INPUT/OUTPUT TIMING (DTR Mode) (1)

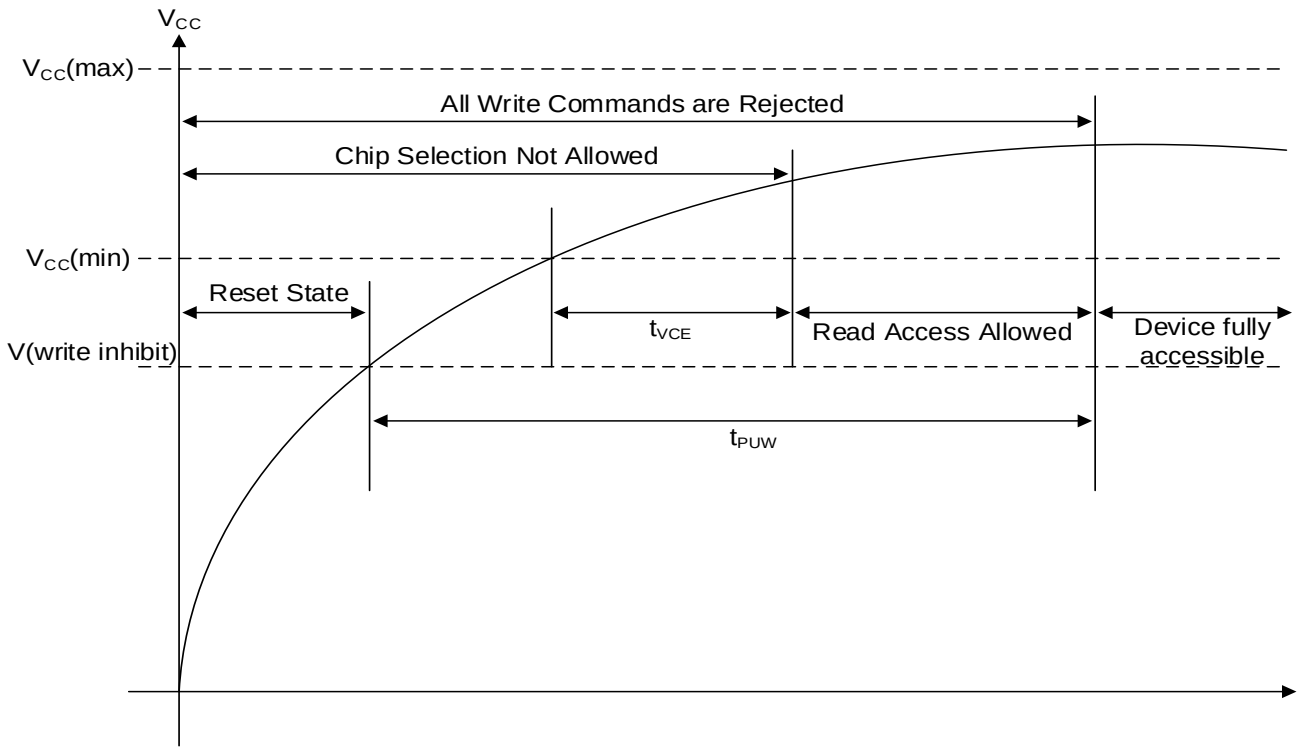


Note1. For SPI Mode 0 (0,0)

7.7 POWER-UP AND POWER-DOWN

At Power-up and Power-down, the device must be NOT SELECTED until Vcc reaches at the right level. (Adding a simple pull-up resistor on CE# is recommended.)

Power up timing



Symbol	Parameter		Min.	Max	Unit
tVCE(1)	Vcc(min) to CE# Low		1		ms
tPUW(1)	Power-up time delay to write instruction		1	10	ms
V_{WI}(1)	Write Inhibit Voltage	IS25LP		2.1	V
		IS25WP		1.4	

Note: These parameters are characterized and not 100% tested.

7.8 PROGRAM/ERASE PERFORMANCE

Parameter		Typ	Max	Unit
Sector Erase Time (4Kbyte)		50	300	ms
Block Erase Time (32Kbyte)		0.1	0.5	s
Block Erase Time (64Kbyte)		0.15	1.0	s
Chip Erase Time	256Mb	50	180	s
Page Programming Time		0.2	0.8	ms
Byte Program		8	40	µs

Note: These parameters are characterized and not 100% tested.

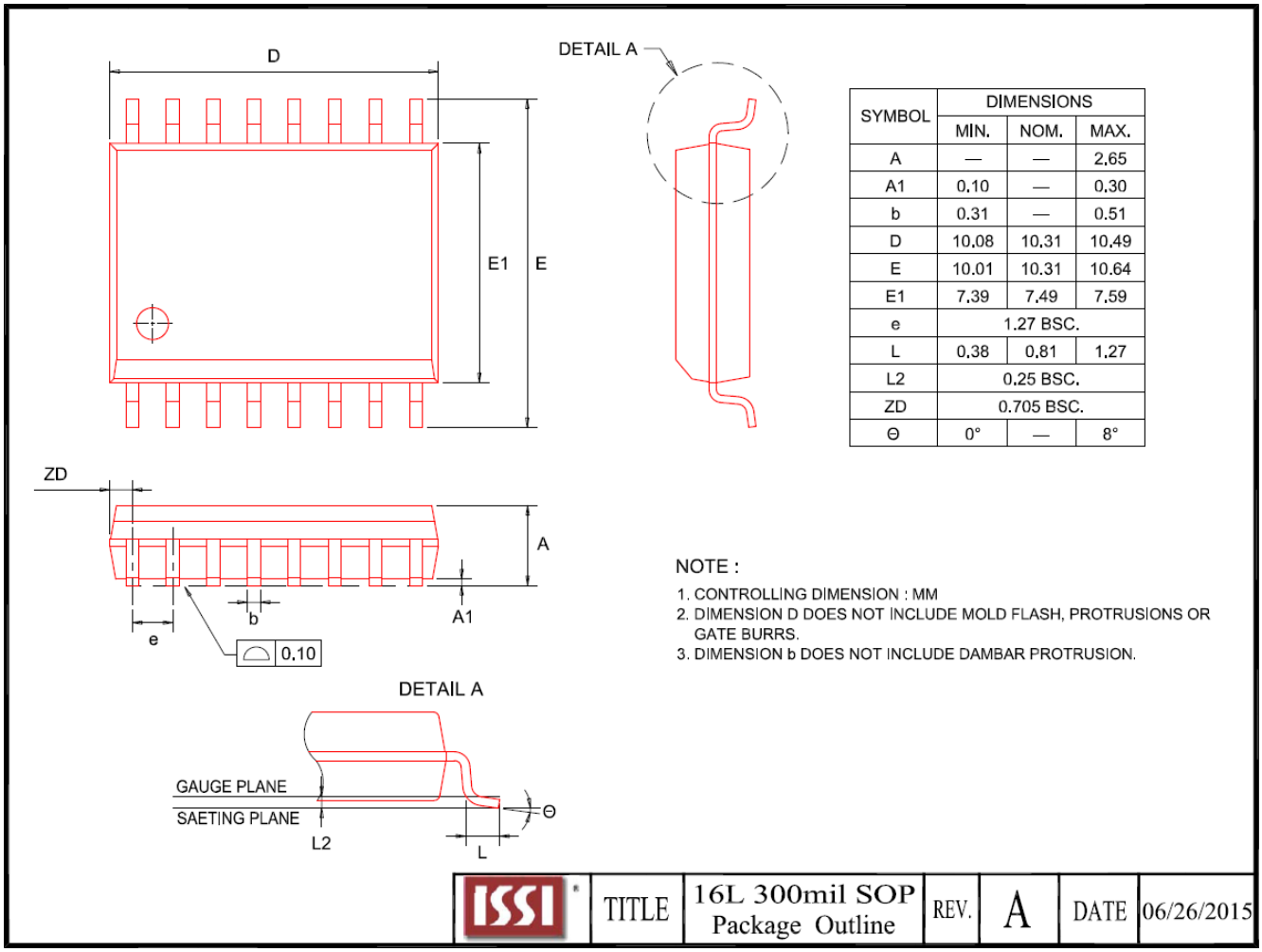
7.9 RELIABILITY CHARACTERISTICS

Parameter	Min	Max	Unit	Test Method
Endurance	100,000	-	Cycles	JEDEC Standard A117
Data Retention	20	-	Years	JEDEC Standard A117
Latch-Up	-100	+100	mA	JEDEC Standard 78

Note: These parameters are characterized and not 100% tested.

7. PACKAGE TYPE INFORMATION

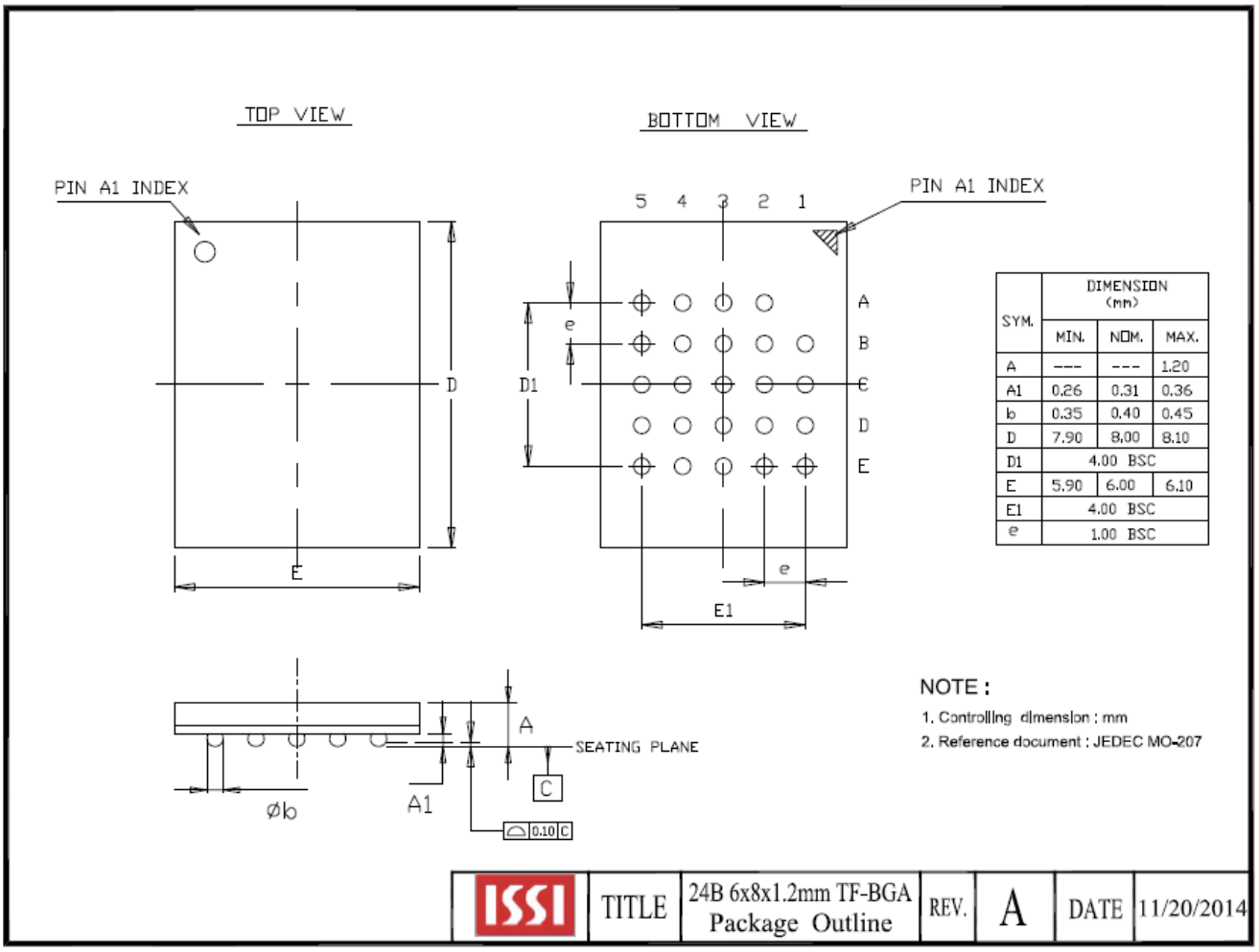
8.1 16-LEAD PLASTIC SMALL OUTLINE PACKAGE (300 MILS BODY WIDTH) (M)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	2.65
A1	0.10	—	0.30
b	0.31	—	0.51
D	10.08	10.31	10.49
E	10.01	10.31	10.64
E1	7.39	7.49	7.59
e	1.27 BSC.		
L	0.38	0.81	1.27
L2	0.25 BSC.		
ZD	0.705 BSC.		
Θ	0°	—	8°

Note: Lead co-planarity is 0.08mm.

8.2 24-BALL THIN PROFILE FINE PITCH BGA 6X8MM 5X5 (H)



SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.26	0.31	0.36
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1	4.00 BSC		
E	5.90	6.00	6.10
E1	4.00 BSC		
e	1.00 BSC		

Note: Lead co-planarity is 0.08mm.

8. ORDERING INFORMATION- Valid Part Numbers

IS25DWP 512M _ - J M L E

TEMPERATURE RANGE
E = Extended (-40°C to +105°C)
E1 = Extended+ (-40°C to +125°C)
A2 = Automotive Grade (-40°C to +105°C)
A3 = Automotive Grade (-40°C to +125°C)

PACKAGING CONTENT
L = **RoHS compliant**

PACKAGE Type
M = 16-pin SOIC 300mil
H = 24-ball TFBGA (6x8mm) 5x5

Option
J = Standard, 1 CE#
C = 2 CE#

Die Revision
Blank = First Gen.

Density
512M = 512 Megabit

BASE PART NUMBER
IS = Integrated Silicon Solution Inc.
25LP = FLASH, 2.30V ~ 3.60V, QPI
25WP = FLASH, 1.65V ~ 1.95V, QPI

Density	Voltage	Order Part Number		Package
512Mb	3.0V	IS25DLP512M-JMLE	IS25DLP512M-JMLE1	16-pin SOIC 300mil
		IS25DLP512M-JMLA1	IS25DLP512M-JMLA2	16-pin SOIC 300mil
		IS25DLP512M-CMLE	IS25DLP512M-CMLE1	16-pin SOIC 300mil
		IS25DLP512M-CMLA1	IS25DLP512M-CMLA2	16-pin SOIC 300mil
		IS25DLP512M-JHLE	IS25DLP512M-JHLE1	24-ball TFBGA 6x8mm 5x5
		IS25DLP512M-JHLA1	IS25DLP512M-JHLA2	24-ball TFBGA 6x8mm 5x5
		IS25DLP512M-CHLE	IS25DLP512M-CHLE1	24-ball TFBGA 6x8mm 5x5
		IS25DLP512M-CHLA1	IS25DLP512M-CHLA2	24-ball TFBGA 6x8mm 5x5
	1.8V	IS25DWP512M-JMLE	IS25DWP512M-JMLE1	16-pin SOIC 300mil
		IS25DWP512M-JMLA1	IS25DWP512M-JMLA2	16-pin SOIC 300mil
		IS25DWP512M-CMLE	IS25DWP512M-CMLE1	16-pin SOIC 300mil
		IS25DWP512M-CMLA1	IS25DWP512M-CMLA2	16-pin SOIC 300mil
		IS25DWP512M-JHLE	IS25DWP512M-JHLE1	24-ball TFBGA 6x8mm 5x5
		IS25DWP512M-JHLA1	IS25DWP512M-JHLA2	24-ball TFBGA 6x8mm 5x5
		IS25DWP512M-CHLE	IS25DWP512M-CHLE1	24-ball TFBGA 6x8mm 5x5
		IS25DWP512M-CHLA1	IS25DWP512M-CHLA2	24-ball TFBGA 6x8mm 5x5