The documentation and process conversion measures necessary to comply with this revision shall be completed by 21 August 2010.

INCH-POUND

MIL-PRF-19500/702C
21 May 2010
SUPERSEDING
MIL-PRF-19500/702B
30 May 2007

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, FIELD EFFECT RADIATION HARDENED
(TOTAL DOSE AND SINGLE EVENT EFFECTS)
TRANSISTOR, N-CHANNEL, SILICON, TYPES 2N7482T3, 2N7483T3, AND 2N7484T3,
JANTXVR, F, G, AND H AND JANSR, F, G, AND H

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for an N-Channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event effects (SEE)), power transistor. Two levels of product assurance are provided for each device type as specified in MIL-PRF-19500, with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}). See 6.5 for JANHC and JANKC die versions.

1.2 Physical dimensions. See figure 1, (TO-257AA, T3).

1.3 Maximum ratings. T_A = +25°C, unless otherwise specified.

Type	P_T (1) T_C = +25°C	P_T T_A = +25°C	$R_{\theta JC}$ (2)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (3) (4) T_C = +25°C	I_{D2} (3) (4) T_C = +100°C	I_S	I_{DM} (5)	T_J and T_{STG}
	W	W	°C/W	V dc	V dc	V dc	A dc	A dc	A dc	A (pk)	°C
2N7482T3	75	1.56	1.67	30	30	±20	18	18	18	72	-55 to +150
2N7483T3	75	1.56	1.67	60	60	±20	18	18	18	72	
2N7484T3	75	1.56	1.67	100	100	±20	18	14	18	72	

(1) Derate linearly 0.6 W/°C for T_C > +25°C.
(2) See figure 2, thermal impedance curves.
(3) The following formula derives the maximum theoretical I_D specs. I_D is limited to 18A by package and device construction.

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS}(on) \text{ at } T_{JM})}}$$

(4) See figure 3, maximum drain current graph.
(5) I_{DM} = 4 X I_{D1}, as defined in note (3).

* Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.daps.dla.mil/.

1.4 Primary electrical characteristics at T_C = +25°C.

Type	Min $V_{(BR)DSS}$ V_{GS} = 0 I_D = 1.0mA dc	$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ I_D = 1.0 mA dc		Max I_{DSS1} V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS}	Max $r_{DS(on)}$ (1) V_{GS} = 12V, I_D = I_{D2}		E_{AS}
					T_J = +25°C	T_J = +150°C	
	V dc	V dc		μA dc	Ω	Ω	mJ
		Min	Max				
2N7482T3	30	2.0	4.0	10	0.030	0.060	177
2N7483T3	60	2.0	4.0	10	0.040	0.080	110
2N7484T3	100	2.0	4.0	10	0.070	0.160	87

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

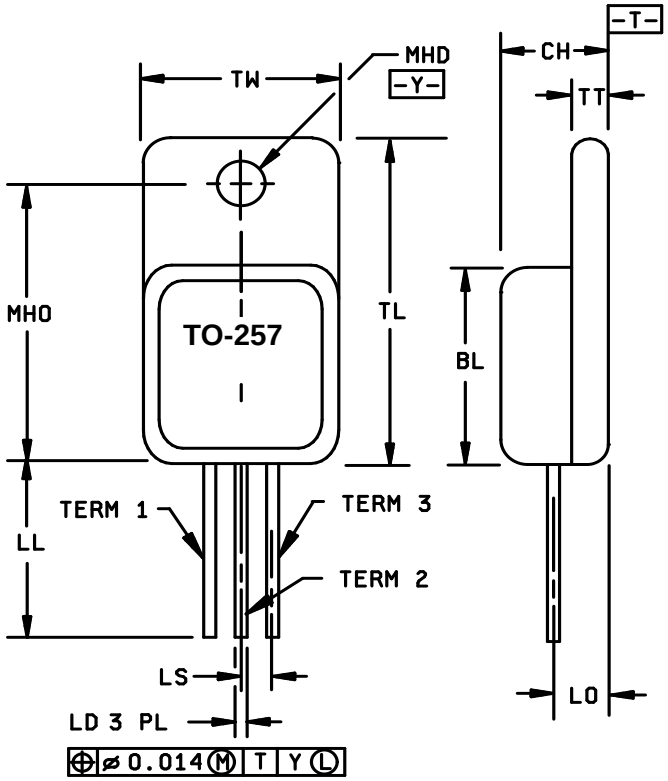
DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or https://assist.daps.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.410	.430	10.41	10.92
CH	.190	.200	4.83	5.08
LD	.025	.035	0.64	0.89
LL	.500	.625	12.70	15.88
LO	.120		3.05	
LS	.100 BSC		2.54	
MHD	.140	.150	3.56	3.81
* MHO	.527	.537	13.39	13.64
TL	.645	.665	16.38	16.89
TT	.035	.045	.889	1.14
TW	.410	.420	10.41	10.67
TERM 1	Drain			
TERM 2	Source			
TERM 3	Gate			



NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. All terminals are isolated from case.
4. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
5. Protrusion thickness of ceramic eyelets included in dimension LL.

* FIGURE 1. Dimensions and configuration (TO-257AA, T3).

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figure 1 (TO-257AA, T3) herein.

3.4.1 Lead finish. Unless otherwise specified, lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Internal construction. Multiple chip construction shall not be permitted.

3.5 Electrostatic discharge protection. The devices covered by this specification require electrostatic discharge protection.

3.5.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.5).

a. Devices should be handled on benches with conductive handling devices.

b. Ground test equipment, tools, and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.

h. Gate must be terminated to source, $R \leq 100\ k\Omega$, whenever bias voltage is to be applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4, table I and II).

* 4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.1.1 SEE. Design capability shall be tested on the initial qualification and thereafter whenever a major die design or process change is introduced. See design safe operation area figures herein. End-point measurements shall be in accordance with table III.

4.3 Screening (JANS and JANTXV). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS	JANTXV
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E_{AS} test (see 4.3.2)	Method 3470 of MIL-STD-750, E_{AS} test (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)
9	Subgroup 2 of table I herein I_{DSS1}, I_{GSSF1}, and I_{GSSR1} as a minimum	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(ON)1}$, $V_{GS(TH)1}$, subgroup 2 of table I herein. ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater.	I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $r_{DS(ON)1}$, $V_{GS(TH)1}$, subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein, ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1}$ = ±20 percent of initial value. $\Delta V_{GS(TH)1}$ = ±20 percent of initial value.	Subgroups 2 and 3 of table I herein, ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1}$ = ±20 percent of initial value. $\Delta V_{GS(TH)1}$ = ±20 percent of initial value.

(1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, and $V_{GS(th)1}$ shall be invoked.
(3) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply V_{GS} = 24 V, minimum for t = 250 μS, minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

a. Peak current ..... $I_{AS} = I_{D1}$.

b. Inductance ..... $L = \left[\frac{2E_{AS}}{(I_{D1})^2}\right]\left[\frac{V_{BR} - V_{DD}}{V_{BR}}\right]$ mH minimum.

c. Gate to source resistor R_{GS}: ..... $25\ \Omega \leq R_{GS} \leq 200\ \Omega$.

d. Supply voltage ..... V_{DD} = 25 V dc, except V_{DD} = 50 V dc for 2N7484T3.

e. Initial case temperature ..... T_C = +25° C, -5° C, +10° C.

f. Gate voltage, ... V_{GS} = 12 V dc.

g. Number of pulses to be applied: ..... 1 pulse minimum.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μs max. See table III, group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of MIL-PRF-19500, and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.4.2.1 Group B inspection, table E-VIA (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
B3	1051	Test condition G, 100 cycles.
B3	2077	SEM (scanning electron microscope).
B4	1042	Intermittent operation life, condition D, 2,000 cycles. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.
B5	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated; T_A = +175°C, t = 24 hours minimum; or T_A = +150°C, t = 48 hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, V_{DS} = rated; T_A = +175°C, t = 120 hours minimum; or T_A = +150°C, t = 240 hours minimum.
B5	2037	Bond strength, test condition A.

4.4.2.2 Group B inspection, table E-VIB (JANTXV) of MIL-PRF-19500.

Subgroup	Method	Condition
B2	1051	Test condition G, 25 cycles.
B3	1042	Intermittent operation life, condition D, 2,000 cycles. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.

4.4.2.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

Subgroup	Method	Condition
C2	2036	Test condition A; weight = 10 pounds; t = 10 s.
C5	3161	Thermal resistance, see 4.3.3, $R_{\theta JC(max)}$ = 1.67°C/W.
C6	1042	Intermittent operation life, condition D, 6,000 cycles. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.

4.4.3 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and table II herein.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2						
Thermal impedance 2/	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage drain to source	3407	V_{GS} = 0, I_D = 1 mA dc, bias condition C	$V_{(BR)DSS}$			
2N7482T3				30		V dc
2N7483T3				60		V dc
2N7484T3				100		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)1}$	2.0	4.0	V dc
Gate current	3411	V_{GS} = +20 V dc, bias condition C, V_{DS} = 0	I_{GSSF1}		+100	nA dc
Gate current	3411	V_{GS} = -20 V dc, bias condition C, V_{DS} = 0	I_{GSSR1}		-100	nA dc
Drain current	3413	V_{GS} = 0, bias condition C, V_{DS} = 80 percent of rated V_{DS},	I_{DSS1}		10	µA dc
Static drain to source on state resistance	3421	V_{GS} = 12 V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)1}$			
2N7482T3					0.030	Ω
2N7483T3					0.040	Ω
2N7484T3					0.070	Ω
Forward voltage	4011	V_{GS} = 0, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	V_{SD}			
2N7482T3					1.2	V dc
2N7483T3					1.2	V dc
2N7484T3					1.2	V dc

See footnotes at end of table.

TABLE I. Group A inspection – Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 3						
High temperature operation		$T_C = T_J = +125°C$				
Gate current	3411	V_{GS} = ±20V dc, bias condition C, V_{DS} = 0	I_{GSS2}		±200	nA dc
Drain current	3413	V_{GS} = 0, bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS2}		25	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)3}$			
2N7482T3					0.050	Ω
2N7483T3					0.070	Ω
2N7484T3					0.140	Ω
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)2}$	1.0		V dc
Low temperature operation		$T_C = T_J = -55°C$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS(TH)3}$, I_D = 1 mA dc	$V_{GS(TH)3}$		5.0	V dc
Subgroup 4						
Forward transconductance	3475	$I_D = I_{D2}$, V_{DD} = 15 V dc (see 4.5.1)	g_{FS}			
2N7482T3				16		S
2N7483T3				16		S
2N7484T3				13		S
Switching time test	3472	$I_D = I_{D1}$, V_{GS} = 12 V dc, R_G = 7.5 Ω, V_{DD} = 50 percent of rated V_{DS}				
Turn-on delay time			$t_{D(on)}$		25	ns
Rise time			t_r		100	ns
Turn-off delay time			$t_{D(off)}$		35	ns
Fall time			t_f		30	ns

See footnotes at end of table.

TABLE I. Group A inspection – Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 5						
Safe operating area test (high voltage)	3474	See figure 4, t_p = 10 ms min. V_{DS} = 80 percent of max. rated V_{DS}				
Electrical measurements		See table I, subgroup 2				
Subgroup 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Condition B, $I_D = I_{D1}$, V_{GS} = 12 V dc, V_{DD} = 50 percent of rated V_{DS}				
On-state gate charge			$Q_{G(ON)}$			
2N7482T3					65	nC
2N7483T3					45	nC
2N7484T3					50	nC
Gate to source charge			Q_{GS}			
2N7482T3					20	nC
2N7483T3					10	nC
2N7484T3					7.4	nC
Gate to drain charge			Q_{GD}			
2N7482T3					10	nC
2N7483T3					15	nC
2N7484T3					20	nC
Reverse recovery time	3473	di/dt = -100 A/µs, $V_{DD} \leq$ 50 V $I_D = I_{D1}$	t_{rr}			
2N7482T3					102	ns
2N7483T3					99	ns
2N7484T3					250	ns

1/ For sampling plan, see MIL-PRF-19500.
2/ This test required for the following end-point measurements only:
Group B, subgroups 2 and 3 (JANTXV).
Group B, subgroups 3 and 4 (JANS).
Group C, subgroups 2 and 6.
Group E, subgroup 1.

TABLE II Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits				Unit
				R, F, G and H		R, F and G		H 4/		
	Method	Conditions		Min	Max	Min	Max	Min	Max	
Subgroup 1 Not applicable										
Subgroup 2 Steady-state total dose irradiation (V_{GS} bias) 5/	1019	T_C = + 25°C V_{GS} = 12 V; V_{DS} = 0 V								
Steady-state total dose irradiation (V_{DS} bias) 5/	1019	V_{GS} = 0; V_{DS} = 80 percent of rated V_{DS}(preirradiation)								
End-point electricals:										
Breakdown voltage, drain to source	3407	V_{GS} = 0; I_D = 1 mA; bias condition C	$V_{(BR)DSS}$							
2N7482T3				30		30		30		V dc
2N7483T3				60		60		60		V dc
2N7484T3				100		100		100		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$; I_D = 1 mA	$V_{GS(th)1}$	2.0	4.0	2.0	4.0	1.5	4.0	V dc
Gate current	3411	V_{GS} = +20 V; V_{DS} = 0, bias condition C	I_{GSSF1}		100		100		100	nA dc
Gate current	3411	V_{GS} = -20 V; V_{DS} = 0, bias condition C	I_{GSSR1}		-100		-100		-100	nA dc
Drain current	3413	V_{GS} = 0; V_{DS} = 80 percent of rated V_{DS} (preirradiation), bias condition C	I_{DSS}		10		10		25	μA dc
Static drain to source on-state voltage	3405	V_{GS} = 12 V; I_D = I_{D2}; condition A, pulsed (see 4.5.1)	$V_{DS(on)}$							
2N7482T3					0.540		0.540		0.630	V dc
2N7483T3					0.720		0.720		0.864	V dc
2N7484T3					0.980		0.980		1.190	V dc
Forward voltage source drain diode	4011	V_{GS} = 0; I_D = I_{D1}, bias condition C	V_{SD}		1.2		1.2		1.2	V dc

1/ For sampling plan see MIL-PRF-19500.
2/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheet utilizing the same die design.
3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.
4/ The H designation represents devices which pass end-points at all R, F, and G designated total-ionizing-dose (TID) levels.
5/ Separate samples shall be pulled for each bias.

* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling	1051	Test condition G, 500 cycles.	
Hermetic seal Fine leak Gross leak	1071	As applicable.	
Electrical measurements		Table I, subgroup 2 herein.	
Subgroup 2 1/			45 devices c = 0
Steady-state gate bias	1042	Condition B, 1,000 hours.	
Electrical measurements		Table I, subgroup 2 herein.	
Steady-state reverse bias	1042	Condition A, 1,000 hours.	
Electrical measurements		Table I, subgroup 2 herein.	
Subgroup 4			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 10			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer.	

See footnotes at end of table.

* TABLE III. Group E inspection (all quality levels) - for qualification or re-qualification only - Continued.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
Subgroup 11			3 devices
SEE 2/ 3/ 4/	1080	See figure 5.	
Electrical measurements 5/		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2.	
SEE irradiation		Fluence = 3E5 ±20 percent ions/cm^2, flux = 2E3 to 2E4 ions/cm^2/sec, temperature = 25 ±5°C.	
		Surface LET = 38 MeV-cm^2/mg ±5%, range = 38 µm ±7.5%, energy = 300 MeV ±7.5%.	
2N7482T3		In situ bias conditions: V_{DS} = 30 V and V_{GS} = -10 V, V_{DS} = 25 V and V_{GS} = -15 V, V_{DS} = 15 V and V_{GS} = -20 V, (nominal 3.86 MeV/Nucleon at Brookhaven National Lab Accelerator).	
2N7483T3		In situ bias conditions: V_{DS} = 60 V and V_{GS} = -15 V, V_{DS} = 30 V and V_{GS} = -20 V, (nominal 3.86 MeV/Nucleon at Brookhaven National Lab Accelerator.	
2N7484T3		In situ bias conditions: V_{DS} = 100 V and V_{GS} = -20 V, (nominal 3.86 MeV/Nucleon at Brookhaven National Lab Accelerator).	
		Surface LET = 61 MeV-cm^2/mg ±5%, range = 31 µm ±10%, energy = 330 MeV ±7.5%,	
2N7482T3		In situ bias conditions: V_{DS} = 30 V and V_{GS} = -10 V, V_{DS} = 22.5 V and V_{GS} = -15 V, V_{DS} = 15 V and V_{GS} = -20 V, (nominal 2.92 MeV/Nucleon at Brookhaven National Lab Accelerator).	
2N7483T3		In situ bias conditions: V_{DS} = 46 V and V_{GS} = -5 V, V_{DS} = 30 V and V_{GS} = -10 V, V_{DS} = 25 V and V_{GS} = -15 V, V_{DS} = 15 V and V_{GS} = -20 V, (nominal 2.92 MeV/Nucleon at Brookhaven National Lab Accelerator).	

See footnotes at end of table.

* TABLE III. Group E inspection (all quality levels) - for qualification or re-qualification only - Continued.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
Subgroup 11- continued			3 devices
2N7484T3		In situ bias conditions: V_{DS} = 100 V and V_{GS} = -10 V, V_{DS} = 35 V and V_{GS} = -15 V, V_{DS} = 25 V and V_{GS} = -20 V, (nominal 2.92 MeV/Nucleon at Brookhaven National Lab Accelerator). Surface LET = 84 MeV-cm^2/mg ±5%, range = 28 µm ±7.5%, energy = 350 MeV ±7.5%.	
2N7482T3		In situ bias conditions: V_{DS} = 25 V and V_{GS} = -5 V, V_{DS} = 20 V and V_{GS} = -10 V, (nominal 1.98 MeV/Nucleon at Brookhaven National Lab Accelerator).	
2N7483T3		In situ bias conditions: V_{DS} = 35 V and V_{GS} = -5 V, V_{DS} = 25 V and V_{GS} = -10 V, V_{DS} = 15 V and V_{GS} = -15 V, V_{DS} = 10 V and V_{GS} = -20 V, (nominal 1.98 MeV/Nucleon at Brookhaven National Lab Accelerator).	
2N7484T3		In situ bias conditions: V_{DS} = 100 V and V_{GS} = -5 V, V_{DS} = 80 V and V_{GS} = -10 V, V_{DS} = 25 V and V_{GS} = -15 V, (nominal 1.98 MeV/Nucleon at Brookhaven National Lab Accelerator).	
Electrical measurements 5/		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2.	

1/ A separate sample for each test shall be pulled.
2/ Group E qualification of SEE testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.
3/ Device qualification to a higher level LET is sufficient to qualify all lower level LETs.
4/ The sampling plan applies to each bias condition.
5/ Examine I_{GSSF1}, I_{GSSR1}, and I_{DSS1} before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option.

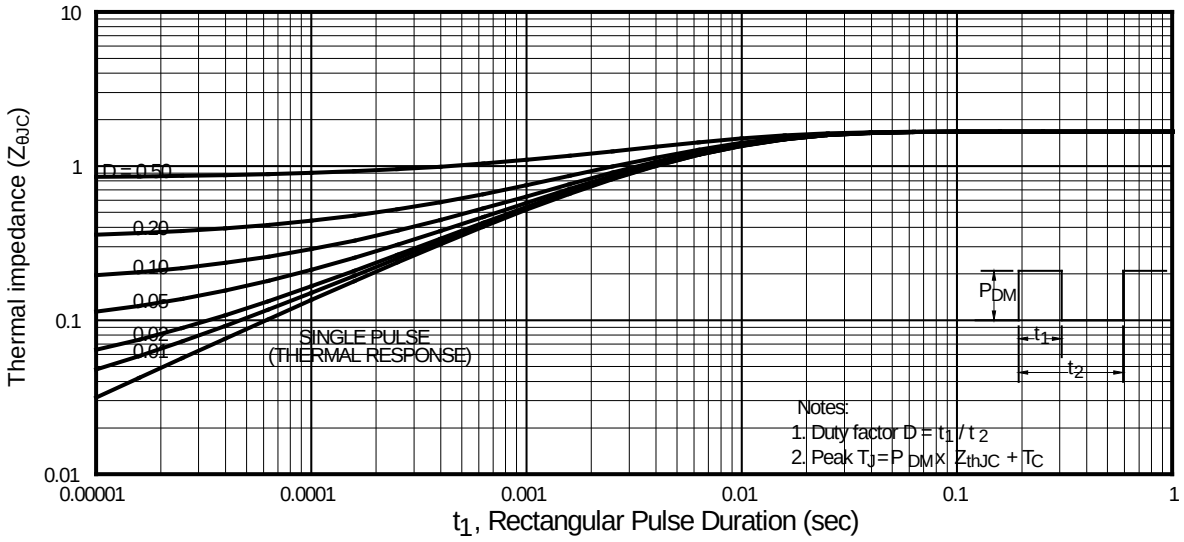
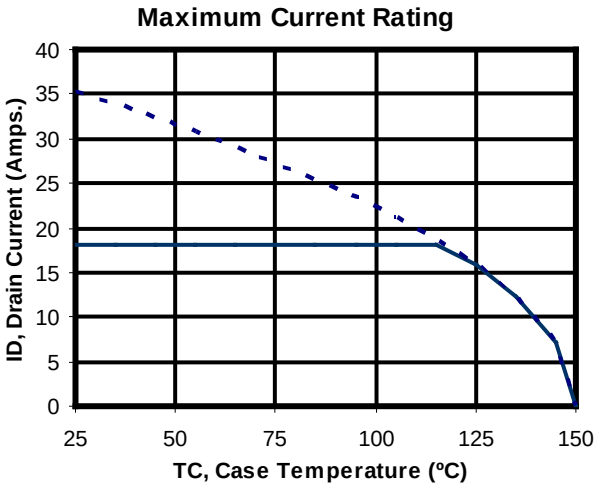
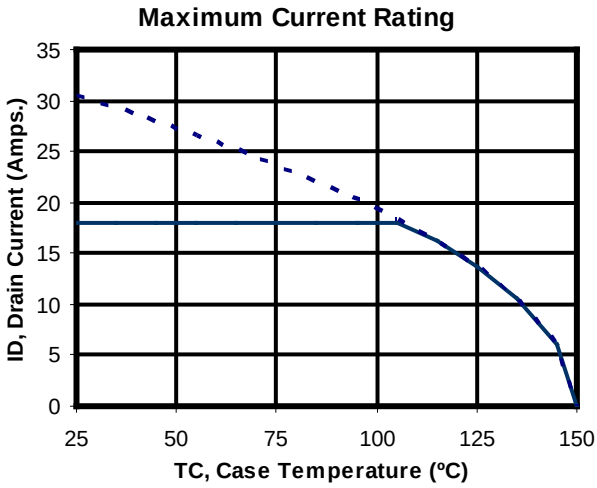


FIGURE 2. Thermal impedance curve.

2N7482T3



2N7483T3



2N7484T3

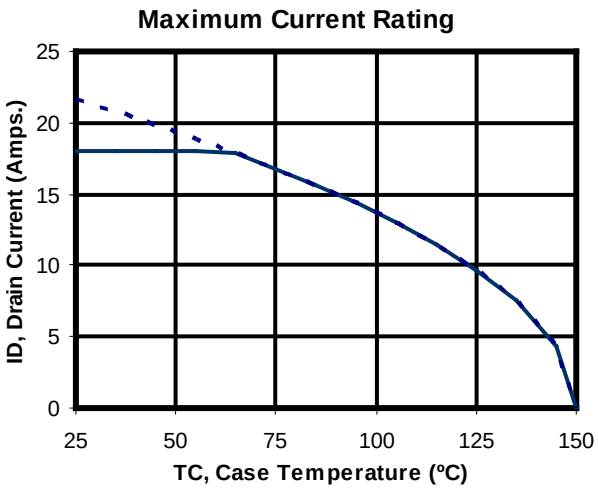


FIGURE 3. Maximum drain current versus case temperature graphs.

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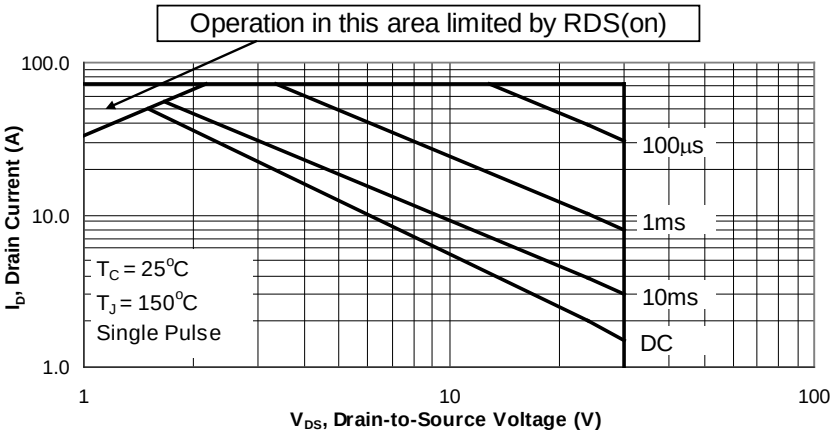

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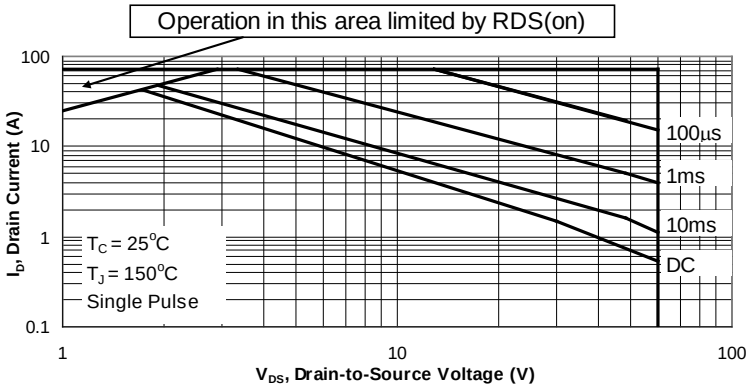

FIGURE 4. Safe operating area graph.

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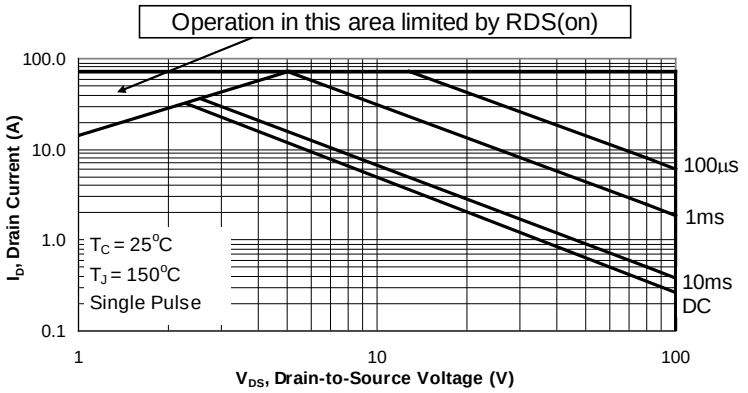
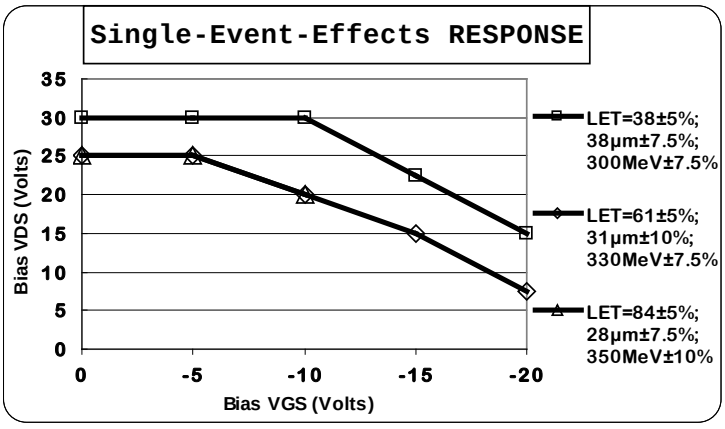
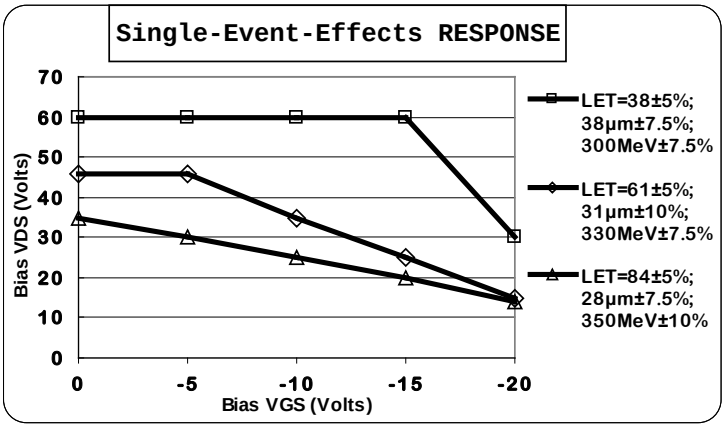


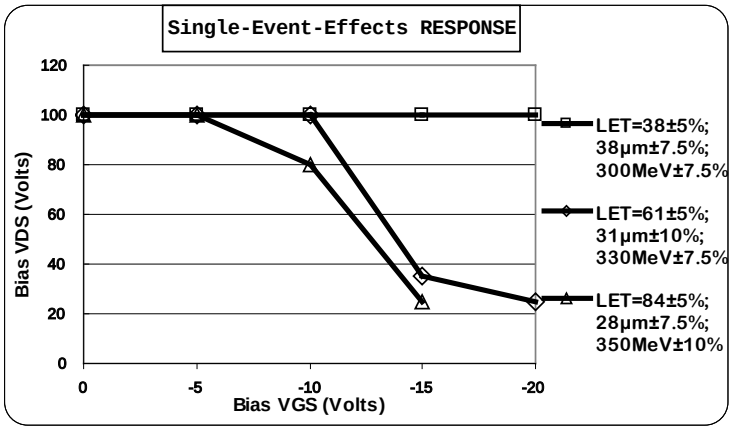
FIGURE 4. Safe operating area graph - Continued.



2N7482T3



2N7483T3



2N7484T3

* FIGURE 5. Typical SEE safe operating area graph.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. Product assurance level and type designator.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.daps.dla.mil .

6.4 Cross-reference list. The following information shows the generic P/N and its associated military P/N (without JAN and RHA prefix).

Generic P/N	Military P/N
IRHY57Z30CM	2N7482T3
IRHY57034CM	2N7483T3
IRHY57130CM	2N7484T3

6.5 JANC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet MIL-PRF-19500/657.

* 6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Review activity:
Air Force - 99

Preparing activity:
DLA - CC

(Project 5961-2010-042)

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.daps.dla.mil/ .