Intel® Pentium® M Processor

Datasheet

April 2004

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Revision History

Document Number	Revision	Description	Date
2 2612	001	Initial release o datasheet	March 2003
2 2612	002	pdates include dded speci ications or Intel Pentium M Processor 1.7 GHz, Lo Volta e Pentium M processor 1.2 GHz, and Itra Lo Volta e Pentium M processor 1 GHz in a le and a le 23	une 2003
2 2612	003	pdates include dded speci ications or Intel Pentium M Processor Lo Volta e 1.30 GHz, and Intel Pentium M Processor Itra Lo Volta e 1.10 GHz in a le and a le 23 pdated I V 3 0 and BPM 3 pin direction	March 2004

1 Introduction

This document provides electrical, mechanical, and thermal specifications for the Intel® Pentium® M processor.

The Intel Pentium M processor is offered at the following core frequencies:

- 1.30 GHz
- 1.40 GHz
- 1.50 GHz
- 1.60 GHz
- 1.70 GHz

The Low Voltage Intel Pentium M processor is offerred at the following core frequencies:

- 1.10 GHz
- 1.20 GHz
- 1.30 GHz

The Ultra Low Voltage Intel Pentium M processor is offered at the following core frequencies:

- 900 MHz
- 1.00 GHz
- 1.10 GHz

Key features of the Intel Pentium M processor incldue:

- Supports Intel® Architecture with Dynamic Execution
- High performance, low-power core
- On-die, primary 32-kB instruction cache and 32-kB write-back data cache
- On-die, 1-MB second level cache with Advanced Transfer Cache Architecture
- Advanced Branch Prediction and Data Prefetch Logic
- Streaming SIMD Extensions 2 (SSE2) enable break-through levels of performance in multimedia applications including 3D graphics, video decoding/encoding, and speech recognition.
- 400-MHz, Source-Synchronous processor system bus to improve performance by transferring data four times per bus clock (4X data transfer rate, as in AGP 4X).
- Advanced Power Management features including Enhanced Intel SpeedStep® technology
- Micro-FCPGA and Micro-FCBGA packaging technologies
- Manufactured on Intel's advanced 0.13 micron process technology with copper interconnect.
- Support for MMX™ technology
- Internet Streaming SIMD instructions and full compatibility with IA-32 software.

- Micro-op Fusion and Advanced Stack Management that reduce the number of micro-ops handled by the processor.
- Advanced branch prediction architecture that significantly reduces the number of mispredicted branches.
- Double-precision floating-point instructions enhance performance for applications that require greater range and precision, including scientific and engineering applications and advanced 3D geometry techniques, such as ray tracing.

Note: The term AGTL+ has been used for Assisted Gunning Transceiver Logic technology on other Intel products.

The Intel Pentium M processor is offered in two packages: a socketable Micro Flip-Chip Pin Grid Array (Micro-FCPGA) and a surface mount Micro Flip-Chip Ball Grid Array (Micro-FCBGA) package technology. The Micro-FCPGA package plugs into a 479-hole, surface-mount, zero insertion force (ZIF) socket, which is referred to as the mPGA479M socket.

1.1 Terminology

A "#" symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the "#" symbol implies that the signal is inverted. For example, D[3:0] = "HLHL" refers to a hex 'A', and D[3:0]# = "LHLH" also refers to a hex "A" (H= High logic level, L= Low logic level).

"System Bus" refers to the interface between the processor and system core logic (also known as the chipset components).

1.2 References

Material and concepts available in the following documents may be beneficial when reading this document. Also, please note that “platform design guides,” when used throughout this document, refers to the following documents: *Intel® 855PM MHz Chipset Platform Design Guide* and *Intel® 855GM Chipset Platform Design Guide.*

Table 1. References

Document	Order Number
Intel® 855PM Chipset Platform Design Guide	http //de eloper.intel.com
Intel® 855PM Chipset Datasheet	http //de eloper.intel.com
Intel® 855PM Chipset Specification Update	http //de eloper.intel.com
Intel® 855GM Chipset Platform Design Guide	http //de eloper.intel.com
Intel® 855GM Chipset Datasheet	http //de eloper.intel.com
Intel® 855GM Chipset Specification Update	http //de eloper.intel.com
Intel® Pentium® M Processor Specification Update	http //de eloper.intel.com
Intel® Architecture Software Developer's Manual	http //de eloper.intel.com
Volume I: Basic Architecture	
Volume II: Instruction Set Reference	
Volume III: System Programming Guide	
ITP700 Debug Port Design Guide	http //de eloper.intel.com

NOTE: Contact our Intel representati e or the latest re ision and order num er o this document.

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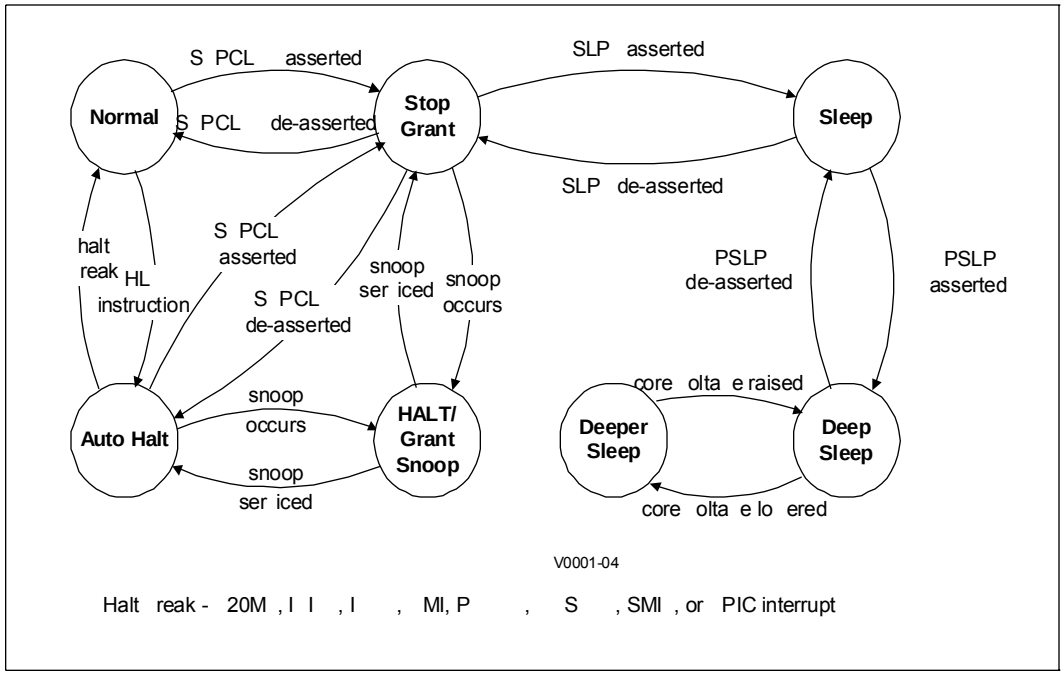
2 Low Power Features

2.1 Clock Control and Low Power States

The Intel Pentium M processor supports the AutoHALT, Stop-Grant, Sleep, Deep Sleep, and Deeper Sleep states for optimal power management. See Figure 1 for a visual representation of the processor low-power states.

Figure 1. Clock Control States



2.1.1 Normal State

This is the normal operating state for the processor.

2.1.2 AutoHALT Powerdown State

AutoHALT is a low-power state entered when the processor executes the HALT instruction. The processor transitions to the Normal state upon the occurrence of SMI#, INIT#, LINT[1:0] (NMI, INTR), or PSB interrupt message. RESET# will cause the processor to immediately initialize itself.

A System Management Interrupt (SMI) handler will return execution to either Normal state or the AutoHALT Powerdown state. See the *Intel Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information.

The system can generate a STPCLK# while the processor is in the AutoHALT Powerdown state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

While in AutoHALT Powerdown state, the processor will process bus snoops. Stop-Grant State

When the STPCLK# pin is asserted, the Stop-Grant state of the processor is entered 20 bus clocks after the response phase of the processor-issued Stop-Grant Acknowledge special bus cycle.

Since the AGTL+ signal pins receive power from the system bus, these pins should not be driven (allowing the level to return to V_{CCP}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the system bus should be driven to the inactive state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the deassertion of the STPCLK# signal. When re-entering the Stop-Grant state from the Sleep state, STPCLK# should be deasserted ten or more bus clocks after the de-assertion of SLP#.

A transition to the HALT/Grant Snoop state will occur when the processor detects a snoop on the system bus (see Section 2.1.3). A transition to the Sleep state (see Section 2.1.4) will occur with the assertion of the SLP# signal.

While in the Stop-Grant state, SMI#, INIT# and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal state. Only one occurrence of each event will be recognized upon return to the Normal state.

While in Stop-Grant state, the processor will process snoops on the system bus and it will latch interrupts delivered on the system bus.

The PBE# signal can be driven when the processor is in Stop-Grant state. PBE# will be asserted if there is any pending interrupt latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear will still cause assertion of PBE#. Assertion of PBE# indicates to system logic that it should return the processor to the Normal state

2.1.3 HALT/Grant Snoop State

The processor will respond to snoop or interrupt transactions on the system bus while in Stop-Grant state or in AutoHALT Power Down state. During a snoop or interrupt transaction, the processor enters the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the system bus has been serviced (whether by the processor or another agent on the system bus) or the interrupt has been latched. After the snoop is serviced or the interrupt is latched, the processor will return to the Stop-Grant state or AutoHALT Power Down state, as appropriate.

2.1.4 Sleep State

The Sleep state is a low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and has stopped all internal clocks. The Sleep state can only be entered from Stop-Grant state. Once in the Stop-Grant state, the processor will enter the Sleep state upon the assertion of the SLP# signal. The SLP# pin should only be asserted when the processor is in the Stop-Grant state. SLP# assertions while the processor is not in the Stop-Grant state are out of specification and may result in unapproved operation.

Snoop events that occur while in Sleep state or during a transition into or out of Sleep state will cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP#, DPSLP# or RESET#) are allowed on the system bus while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant state. If RESET# is driven active while the processor is in the Sleep state, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering an even lower power state, the Deep Sleep state by asserting the DPSLP# pin. (See Section 2.1.5.) While the processor is in the Sleep state, the SLP# pin must be deasserted if another asynchronous system bus event needs to occur.

2.1.5 Deep Sleep State

Deep Sleep state is a very low power state the processor can enter while maintaining context. Deep Sleep state is entered by asserting the DPSLP# pin while in the Sleep state. BCLK may be stopped during the Deep Sleep state for additional platform level power savings. BCLK stop/restart timings on Intel 855PM and Intel 855GM chipset-based platforms are as follows:

- Deep Sleep entry - DPSLP# and CPU_STP# are asserted simultaneously. The platform clock chip will stop/tristate BCLK within 2 BCLKs +/- a few nanoseconds.
- Deep Sleep exit - DPSLP# and CPU_STP# are deasserted simultaneously. The platform clock chip will drive BCLK to differential DC levels within 2-3 ns and starts toggling BCLK 2-6 BCLK periods later.

To re-enter the Sleep state, the DPSLP# pin must be deasserted. BCLK can be re-started after DPSLP# deassertion as described above. A period of 30 microseconds (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep state. Once in the Sleep state, the SLP# pin must be deasserted to re-enter the Stop-Grant state.

While in Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions of signals are allowed on the system bus while the processor is in Deep Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

2.1.6 Deeper Sleep State

The Deeper Sleep state is the lowest power state the processor can enter. This state is functionally identical to the Deep Sleep state but at a lower core voltage. The control signals to the voltage regulator to initiate a transition to the Deeper Sleep state are provided on the platform. Please refer to the platform design guides for details.

2.2 Enhanced Intel SpeedStep® Technology

The Intel Pentium M processor features Enhanced Intel SpeedStep® technology. Unlike previous implementations of Intel SpeedStep technology, this technology enables the processor to switch between multiple frequency and voltage points instead of two. This will enable superior performance with optimal power savings. Switching between states is software controlled unlike previous implementations where the GHI# pin is used to toggle between two states. The following are the key features of Enhanced Intel SpeedStep technology:

- Multiple voltage/frequency operating points provide optimal performance at the lowest power.
- Voltage/Frequency selection is software controlled by writing to processor MSR's (Model Specific Registers) thus eliminating chipset dependency.

  - If the target frequency is higher than the current frequency, Vcc is ramped up by placing a new value on the VID pins and the PLL then locks to the new frequency.
  - If the target frequency is lower than the current frequency, the PLL locks to the new frequency and the Vcc is changed through the VID pin mechanism.
  - Software transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until its completion.
- The processor controls voltage ramp rates internally to ensure glitch free transitions.
- Low transition latency and large number of transitions possible per second.
  - Processor core (including L2 cache) is unavailable for up to 10 µs during the frequency transition
  - The bus protocol (BNR# mechanism) is used to block snooping
- No bus master arbiter disable required prior to transition and no processor cache flush necessary.
- Improved Intel Thermal Monitor mode.
  - When the on-die thermal sensor indicates that the die temperature is too high, the processor can automatically perform a transition to a lower frequency/voltage specified in a software programmable MSR.
  - The processor waits for a fixed time period. If the die temperature is down to acceptable levels, an up transition to the previous frequency/voltage point occurs.
  - An interrupt is generated for the up and down Intel Thermal Monitor transitions enabling better system level thermal management.

2.3 Processor System Bus Low Power Enhancements

The Intel Pentium M processor incorporates the following processor system bus low power enhancements:

- Dynamic FSB power down
- BPRI# control for address and control input buffers
- Dynamic on-die termination disabling
- Low VCCP (I/O termination voltage)

The Intel Pentium M processor incorporates the DPWR# signal that controls the Data Bus input buffers on the processor. The DPWR# signal disables the buffers when not used and activates them only when data bus activity occurs, resulting in significant power savings with no performance impact. BPRI# control also allows the processor address and control input buffers to be turned off when the BPRI# signal is inactive. The On Die Termination on the processor PSB buffers is disabled when the signals are driven low, resulting in additional power savings. The low I/O termination voltage is on a dedicated voltage plane independent of the core voltage, enabling low I/O switching power at all times.

2.4 Processor Power Status Indicator (PSI#) Signal

The Intel Pentium M processor incorporates the PSI# signal that is asserted when the processor is in a low power (Deep Sleep or Deeper Sleep) state. This signal is asserted upon Deep Sleep entry and deasserted upon exit. PSI# can be used to improve the light load efficiency of the voltage regulator, resulting in platform power savings and extended battery life. PSI# can also be used to simplify voltage regulator designs since it removes the need for integrated 100 µs timers required to mask the PWRGOOD signal during Deeper Sleep transitions. It also reduces PWRGOOD monitoring requirements in the Deeper Sleep state.

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3 Electrical Specifications

3.1 System Bus and GTLREF

The Intel Pentium M processor system bus signals use Advanced Gunning Transceiver Logic (AGTL+) signalling technology, a variant of GTL+ signalling technology with low power enhancements. This signalling technology provides improved noise margins and reduced ringing through low-voltage swings and controlled edge rates. The termination voltage level for the Intel Pentium M processor AGTL+ signals is VCCP = 1.05 V (nominal). Due to speed improvements to data and address bus, signal integrity and platform design methods have become more critical than with previous processor families. Design guidelines for the Intel Pentium M processor system bus are detailed in the platform design guides.

The AGTL+ inputs require a reference voltage (GTLREF) that is used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF must be generated on the system board. Termination resistors are provided on the processor silicon and are terminated to its I/O voltage (VCCP). The Intel 855PM and Intel 855GM chipsets also provide on-die termination, thus eliminating the need to terminate the bus on the system board for most AGTL+ signals.

Refer to the platform design guides for board level termination resistor requirements.

The AGTL+ bus depends on incident wave switching. Therefore, timing calculations for AGTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the system bus, including trace lengths, is highly recommended when designing a system.

3.2 Power and Ground Pins

For clean on-chip power distribution, the Intel Pentium M processor has a large number of V_{CC} (power) and V_{SS} (ground) inputs. All power pins must be connected to V_{CC} power planes while all V_{SS} pins must be connected to system ground planes. Use of multiple power and ground planes is recommended to reduce I*R drop. Please refer to the platform design guides for more details. The processor V_{CC} pins must be supplied the voltage determined by the VID (Voltage ID) pins.

3.3 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in Table 5. Failure to do so can result in timing violations or reduced lifetime of the component. For further information and design guidelines, refer to the platform design guides.

3.3.1 V_{CC} Decoupling

Regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR) and keep a low interconnect resistance from the regulator to the socket. Bulk decoupling for the large current swings when the part is powering on, or entering/exiting low-power states, must be provided by the voltage regulator solution. For more details on decoupling recommendations, please refer to the platform design guides. It is **strongly recommended** that the layout and decoupling recommendations in the design guides be followed.

3.3.2 System Bus AGTL+ Decoupling

Intel Pentium M processors integrate signal termination on the die as well as incorporate high frequency decoupling capacitance on the processor package. Decoupling must also be provided by the system motherboard for proper AGTL+ bus operation. For more information, refer to the platform design guides.

3.3.3 System Bus Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the system bus interface speed as well as the core frequency of the processor. As in previous generation processors, the Intel Pentium M processor core frequency is a multiple of the BCLK[1:0] frequency. In regards to processor clocking, the Intel Pentium M processor uses a differential clocking implementation.

3.4 Voltage Identification

The Intel Pentium M processor uses six voltage identification pins, VID[5:0], to support automatic selection of power supply voltages. The VID pins for the Intel Pentium M processor are CMOS outputs driven by the processor VID circuitry. Table 2 specifies the voltage level corresponding to the state of VID[5:0]. A “1” in this refers to a high-voltage level and a “0” refers to low-voltage level.

Table 2. Voltage Identification Definition

VID						V_{CC} V	VID						V_{CC} V
5	4	3	2	1	0		5	4	3	2	1	0	
0	0	0	0	0	0	1.708	1	0	0	0	0	0	1.1 6
0	0	0	0	1	0	1.676	1	0	0	0	1	0	1.164
0	0	0	0	1	1	1.660	1	0	0	0	1	1	1.148
0	0	0	1	0	0	1.644	1	0	0	1	0	0	1.132
0	0	0	1	0	1	1.628	1	0	0	1	0	1	1.116
0	0	0	1	1	0	1.612	1	0	0	1	1	0	1.100
0	0	0	1	1	1	1. 6	1	0	0	1	1	1	1.084
0	0	1	0	0	0	1. 80	1	0	1	0	0	0	1.068
0	0	1	0	0	1	1. 64	1	0	1	0	0	1	1.0 2
0	0	1	0	1	0	1. 48	1	0	1	0	1	0	1.036
0	0	1	0	1	1	1. 32	1	0	1	0	1	1	1.020
0	0	1	1	0	0	1. 16	1	0	1	1	0	0	1.004
0	0	1	1	0	1	1. 00	1	0	1	1	0	1	0. 88
0	0	1	1	1	0	1.484	1	0	1	1	1	0	0. 72
0	0	1	1	1	1	1.468	1	0	1	1	1	1	0. 6
0	1	0	0	0	0	1.4 2	1	1	0	0	0	0	0. 40
0	1	0	0	0	1	1.436	1	1	0	0	0	1	0. 24
0	1	0	0	1	0	1.420	1	1	0	0	1	0	0. 08
0	1	0	0	1	1	1.404	1	1	0	0	1	1	0.8 2
0	1	0	1	0	0	1.388	1	1	0	1	0	0	0.876
0	1	0	1	0	1	1.372	1	1	0	1	0	1	0.860
0	1	0	1	1	0	1.3 6	1	1	0	1	1	0	0.844
0	1	0	1	1	1	1.340	1	1	0	1	1	1	0.828
0	1	1	0	0	0	1.324	1	1	1	0	0	0	0.812
0	1	1	0	0	1	1.308	1	1	1	0	0	1	0.7 6
0	1	1	0	1	0	1.2 2	1	1	1	0	1	0	0.780
0	1	1	0	1	1	1.276	1	1	1	0	1	1	0.764
0	1	1	1	0	0	1.260	1	1	1	1	0	0	0.748
0	1	1	1	0	1	1.244	1	1	1	1	0	1	0.732
0	1	1	1	1	0	1.228	1	1	1	1	1	0	0.716
0	1	1	1	1	1	1.212	1	1	1	1	1	1	0.700

3.5 Catastrophic Thermal Protection

The Intel Pentium M processor supports the THERMTRIP# signal for catastrophic thermal protection. An external thermal sensor should also be used to protect the processor and the system against excessive temperatures. Even with the activation of THERMTRIP#, that halts all processor internal clocks and activity, leakage current can be high enough such that the processor cannot be protected in all conditions without the removal of power to the processor. If the external thermal sensor detects a catastrophic processor temperature of 125 °C (maximum), or if the THERMTRIP# signal is asserted, the VCC supply to the processor must be turned off within 500 ms to prevent permanent silicon damage due to thermal runaway.

3.6 Signal Terminations and Unused Pins

All RSVD (RESERVED) pins must remain unconnected. Connection of these pins to V_{CC}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future Intel Pentium M processors. See Section 4.2 for a pin listing of the processor and the location of all RSVD pins.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused active low AGTL+ inputs may be left as no connects if AGTL+ termination is provided on the processor silicon. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs can be left unconnected.

For details on signal terminations, please refer to the platform design guides. TAP signal termination requirements are also discussed in *ITP700 Debug Port Design Guide*.

The TEST1, TEST2, and TEST3 pins must be left unconnected but should have a stuffing option connection to V_{SS} separately using 1-kΩ, pull-down resistors.

3.7 System Bus Signal Groups

To simplify the following discussion, the system bus signals have been combined into groups by buffer type. AGTL+ input signals have differential input buffers, which use GTLREF as a reference level. In this document, the term "AGTL+ Input" refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, "AGTL+ Output" refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

Table 3 identifies which signals are common clock, source synchronous, and asynchronous. Common clock signals which are dependent upon the crossing of the rising edge of BCLK0 and the falling edge of BCLK1. Source synchronous signals are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asychronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle.

Table 3. System Bus Pin Groups

Signal Group	Type	Signals
G L Common Clock Input	S nchronous to BCL 1 0	BP I , F , P , P , S , S 2 0 ,
G L Common Clock I/	S nchronous to BCL 1 0	S , B , BPM 3 0 [1], B 0 , BS , , HI , HI M , L C , P [1]
G L Source S nchronous I/	S nchronous to associated stro e	4 0 , 16 3 → S B 0 31 17 → S B 1 1 0 , I V0 → S BP0 , S B 0 31 16 , I V1 → S BP1 , S B 1 47 32 , I V2 → S BP2 , S B 2 63 48 , I V3 → S BP3 , S B 3
G L Stro es	S nchronous to BCL 1 0	S B 1 0 , S BP 3 0 , S B 3 0
CM S Input	s nchronous	20M , PSLP , IG , I I , LI 0/I , LI 1/ MI, P G , SMI , SLP , S PCL
pen rain utput	s nchronous	F , I , P CH , H M IP
CM S utput	s nchronous	PSI , VI 0
CM S Input	S nchronous to C	C , I, MS, S
pen rain utput	S nchronous to C	
S stem Bus Clock	Clock	BCL 1 0 , I P_CL 1 0
Po er/ ther		C MP 3 0 , B [2], G L F, SV , S 3, S 2, S 1, H M , H M C, V_{CC}, V_{CC} 3 0 , V_{CCP}, V_{CC} 1 0 , V_{CC_S} s , V_{SS}, V_{SS_S} s

S

1. BPM 2 0 and P are G L output onl si nals.
2. In processor s stems here there is no de u port implemented on the s stem oard, these si nals are used to support a de u port interposer. In s stems ith the de u port implemented on the s stem oard, these si nals are no connects

3.8 CMOS Signals

CMOS input signals are shown in Table 3. Legacy output FERR#, IERR# and other non-AGTL+ signals (THERMTRIP# and PROCHOT#) utilize Open Drain output buffers. All of the CMOS signals are required to be asserted for at least three BCLKs in order for the chipset to recognize them. See Section 3.10 for the DC specifications of the CMOS signal groups.

3.9 Maximum Ratings

Table 4 lists the processor's maximum environmental stress ratings. The processor should not receive a clock while subjected to these conditions. Functional operating parameters are listed in the DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor includes protective circuitry to resist damage from Electro Static Discharge (ESD), system designers must always take precautions to avoid high static voltages or electric fields.

Table 4. Processor DC Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
S G	Processor stora e temperature	40	8	C	2
V_{CC}	n processor suppl olta e ith respect to V_{SS}	-0.3	1.7	V	1
V_{in} G L	G L u er C input olta e ith respect to V_{SS}	-0.1	1.7	V	1, 2
V_{in} s nch_CM S	CM S u er C input olta e ith respect to V_{SS}	-0.1	1.7	V	1, 2

NOTES:
1. his ratin applies to an processor pin.
2. Contact Intel or stora e re uirements in e cess o one ear.

3.10 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core (pads) unless noted otherwise. See Table 15 for the pin signal definitions and signal pin assignments. Most of the signals on the processor system bus are in the AGTL+ signal group and the DC specifications for these signals are also listed. DC specifications for the CMOS group are listed in Table 16.

Table 5 through Table 16 list the DC specifications for the Intel Pentium M processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. The Highest Frequency (HFM) and Lowest Frequency Modes (LFM) refer to the highest and lowest core operating frequencies supported on the processor. Active Mode load line specifications apply in all states except in the Deep Sleep and Deeper Sleep states. $V_{CC,BOOT}$ is the default voltage driven by the voltage regulator at power up in order to set the VID values. Unless specified otherwise, all specifications for the Intel Pentium M processor are at Tjunction = 100°C. Care should be taken to read all notes associated with each parameter.

Table 5. Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{CC17}	Intel Pentium M processor 1.70 GHz Core V_{CC} or nhanced Intel SpeedStep technolo operatin points 1.70 GHz 1.40 GHz 1.20 GHz 1.00 GHz 800 MHz 600 MHz		 1.484 1.308 1.228 1.116 1.004 0. 6		V	1, 2
V_{CC16}	Intel Pentium M processor 1.60 GHz Core V_{CC} or nhanced Intel SpeedStep technolo operatin points 1.60 GHz 1.40 GHz 1.20 GHz 1.00 GHz 800 MHz 600 MHz		 1.484 1.420 1.276 1.164 1.036 0. 6		V	1, 2
V_{CC1}	Intel Pentium M processor 1. 0 GHz Core V_{CC} or nhanced Intel SpeedStep technolo operatin points 1. 0 GHz 1.40 GHz 1.20 GHz 1.00 GHz 800 MHz 600 MHz		 1.484 1.4 2 1.3 6 1.228 1.116 0. 6		V	1, 2
V_{CC14}	Intel Pentium M processor 1.40 GHz Core V_{CC} or nhanced Intel SpeedStep technolo operatin points 1.40 GHz 1.20 GHz 1.00 GHz 800 MHz 600 MHz		 1.484 1.436 1.308 1.180 0. 6		V	1, 2
V_{CC13}	Intel Pentium M processor 1.30 GHz Core V_{CC} or nhanced Intel SpeedStep technolo operatin points 1.30 GHz 1.20 GHz 1.00 GHz 800 MHz 600 MHz		 1.388 1.3 6 1.2 2 1.260 0. 6		V	1, 2

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{CCLV13}	Lo Volta e Intel Pentium M processor 1.30 GHz Core V_{CC} or nhanced Intel SpeedStep technolo operatin points 1.30 GHz 1.20 GHz 1.10 GHz 1.00 GHz 00 MHz 800 MHz 600 MHz		1.180 1.164 1.100 1.020 1.004 0. 88 0. 6		V	1,2
V_{CCLV12}	Lo Volta e Intel Pentium M processor 1.20 GHz Core V_{CC} or nhanced Intel SpeedStep technolo operatin points 1.20 GHz 1.10 GHz 1.00 GHz 00 MHz 800 MHz 600 MHz		1.180 1.164 1.100 1.020 1.004 0. 6		V	1,2
V_{CCLV11}	Lo Volta e Intel Pentium M processor 1.10 GHz Core V_{CC} or nhanced Intel SpeedStep technolo operatin points 1.10 GHz 1.00 GHz 00 MHz 800 MHz 600 MHz		1.180 1.164 1.100 1.020 0. 6		V	1, 2
$V_{CC\ LV11}$	Itra Lo Volta e Intel Pentium M processor 1.10 GHz Core V_{CC} or nhanced Intel SpeedStep technolo operatin points 1.10 GHz 1.00 GHz 00 MHz 800 MHz 600 MHz		1.004 0. 88 0. 72 0. 6 0.844			
$V_{CC\ LV10}$	Itra Lo Volta e Intel Pentium M processor 1.00 GHz Core V_{CC} or nhanced Intel SpeedStep technolo operatin points 1.00 GHz 00 MHz 800 MHz 600 MHz		1.004 0. 88 0. 72 0.844		V	1, 2

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$V_{CC\ LV}$	Ultra Low Voltage Intel Pentium M processor 900 MHz Core V_{CC} for Enhanced Intel SpeedStep technology operating points 900 MHz 800 MHz 600 MHz		 1.004 0.988 0.844		V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for initial power up	1.14	1.20	1.26	V	2
V_{CCP}	GTL Termination Voltage	0.997	1.0	1.102	V	2
V_{CC}	PLL Supply Voltage	1.71	1.8	1.89	V	2
$V_{CC\_DEEP\_SLP,TR}$	Transient Deeper Sleep Voltage	0.6	0.748	0.7	V	2
$V_{CC\_DEEP\_SLP,STATIC}$	Static Deeper Sleep Voltage	0.70	0.748	0.78	V	2
I_{CC_TDC}	I_{CC} for Intel Pentium M processors Recommended Design Target			26		
I_{CC}	I_{CC} for Intel Pentium M processors Frequency/Voltage 600 MHz 0.844 V 600 MHz 0.988 V 900 MHz 1.004 V 1.00 GHz 1.004 V 1.10 GHz 1.004 V 1.10 GHz 1.180 V 1.20 GHz 1.180 V 1.30 GHz 1.180 V 1.30 GHz 1.388 V 1.40 GHz 1.484 V 1.50 GHz 1.484 V 1.60 GHz 1.484 V 1.70 GHz 1.484 V			 26.8 12 12 12.1 18 21 21 21		3
$I_{AH,}$ I_{SGAH}	I_{CC} Auto-Halt Stop-Grant at 0.844 V (LV Pentium M) 0.988 V 1.004 V (LV Pentium M) 1.180 V 1.388 V (Pentium M 1.30 GHz) 1.484 V			 11.8 13.3 12.7 14.7 15.4 18.6		4
I_{SLP}	I_{CC} Sleep at 0.844 V (LV Pentium M) 0.988 V 1.004 V (LV Pentium M) 1.180 V 1.388 V (Pentium M 1.30 GHz) 1.484 V			 11.7 13.3 12.6 14.6 15.2 18.4		4
I_{DSLP}	I_{CC} Deep Sleep at 0.844 V (LV Pentium M) 0.988 V 1.004 V (LV Pentium M) 1.180 V 1.388 V (Pentium M 1.30 GHz) 1.484 V			 11.6 13.1 12.3 14.2 15.8 17.8		4
I_{DPSLP}	I_{CC} Deeper Sleep			11.8		4

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I P SLP LV	I_{CC} eeper Sleep (LV Intel Pentium M onl)			1.2		4
$dI_{CC/}$	V_{CC} po er suppl current sle rate			0.	/ns	6, 7
I_{CC}	I_{CC} or V_{CC} suppl			120	m	
I_{CCP}	I_{CC} or V_{CCP} suppl			2.		

NOTES:
1. he t pical alues sho n are the VI encoded olta es. Static and ipple tolerances (or minimum and ma imum olta es) are de ined in the load line ta les i.e. a le 6 throu h a le 13.
2. he olta e speci ications are assumed to e measured at a ia on the mother oard s opposite side o the processor s socket (or BG) all ith a 100-MHz and idth oscilloscope, 1. -pF ma imum pro e capacitance, and 1-Mohm minimum impedance. he ma imum len th o round ire on the pro e should e less than mm. nsure e ternal noise rom the s stem is not coupled in the scope pro e.
3. Speci ied at $V_{CC,S}$ IC (nominal) under ma imum si nal loadin conditions.
4. Speci ied at the VI olta e.
. he I_{CC} S(ma) speci ication comprehends uture processor HFM re uencies. Plat orms should e desi ned to this speci ication.
6. Based on simulations and a era ed o er the duration o an chan e in current. Speci ied desi n/ characterization at nominal V_{CC}. ot 100 tested.
7. Measured at the ulk capacitors on the mother oard.

Table 6. Voltage Tolerances for Intel Pentium M Processors with HFM VID = 1.484 V (Active State)

Mode	Highest Frequency Mode: VID = 1.484 V, Offset = 0%						Lowest Frequency Mode: VID = 0.956 V, Offset = 0%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
ACTIVE	0	1.484	1.462	1. 06	1.4 2	1. 16	0.0	0. 6	0. 42	0. 70	0. 32	0. 80
	0.	1.481	1.4	1. 03	1.44	1. 13	0.4	0.	0. 41	0. 6	0. 31	0. 7
	1.	1.478	1.4 6	1. 01	1.446	1. 11	0.7	0. 4	0. 40	0. 68	0. 30	0. 78
	2.8	1.476	1.4 3	1.4 8	1.443	1. 08	1.1	0. 3	0. 38	0. 67	0. 28	0. 77
	3.7	1.473	1.4 1	1.4	1.441	1. 0	1.4	0. 2	0. 37	0. 66	0. 27	0. 76
	4.6	1.470	1.448	1.4 2	1.438	1. 02	1.8	0. 1	0. 36	0. 6	0. 26	0. 7
	.6	1.467	1.44	1.4 0	1.43	1. 00	2.1	0. 0	0. 3	0. 64	0. 2	0. 74
	6.	1.46	1.442	1.487	1.432	1.4 7	2.	0. 48	0. 34	0. 63	0. 24	0. 73
	7.4	1.462	1.440	1.484	1.430	1.4 4	2.	0. 47	0. 33	0. 62	0. 23	0. 72
	8.3	1.4	1.437	1.481	1.427	1.4 1	3.2	0. 46	0. 32	0. 61	0. 22	0. 71
	.3	1.4 6	1.434	1.478	1.424	1.488	3.6	0. 4	0. 31	0. 60	0. 21	0. 70
	10.2	1.4 3	1.431	1.476	1.421	1.486	3.	0. 44	0. 30	0.	0. 20	0. 6
	11.1	1.4 1	1.428	1.473	1.418	1.483	4.3	0. 43	0. 2	0. 7	0. 1	0. 67
	12.0	1.448	1.426	1.470	1.416	1.480	4.7	0. 42	0. 28	0. 6	0. 18	0. 66
	13.0	1.44	1.423	1.467	1.413	1.477	.0	0. 41	0. 27	0.	0. 17	0. 6
	13.	1.442	1.420	1.46	1.410	1.47	.4	0. 40	0. 26	0. 4	0. 16	0. 64
	14.8	1.440	1.417	1.462	1.407	1.472	.7	0. 3	0. 24	0. 3	0. 14	0. 63
	1 .7	1.437	1.41	1.4	1.40	1.46	6.1	0. 38	0. 23	0. 2	0. 13	0. 62
	16.7	1.434	1.412	1.4 6	1.402	1.466	6.4	0. 37	0. 22	0. 1	0. 12	0. 61
	17.6	1.431	1.40	1.4 3	1.3	1.463	6.8	0. 36	0. 21	0. 0	0. 11	0. 60
	18.	1.428	1.406	1.4 1	1.3 6	1.461						
	1 .4	1.426	1.403	1.448	1.3 3	1.4 8						
	20.4	1.423	1.401	1.44	1.3 1	1.4						
	21.3	1.420	1.3 8	1.442	1.388	1.4 2						
	22.2	1.417	1.3	1.440	1.38	1.4 0						
	23.1	1.41	1.3 2	1.437	1.382	1.447						
	24.1	1.412	1.3 0	1.434	1.380	1.444						
	2 .0	1.40	1.387	1.431	1.377	1.441						

Figure 2. Illustration of Active State V_{CC} Static and Ripple Tolerances (Highest Frequency Mode)

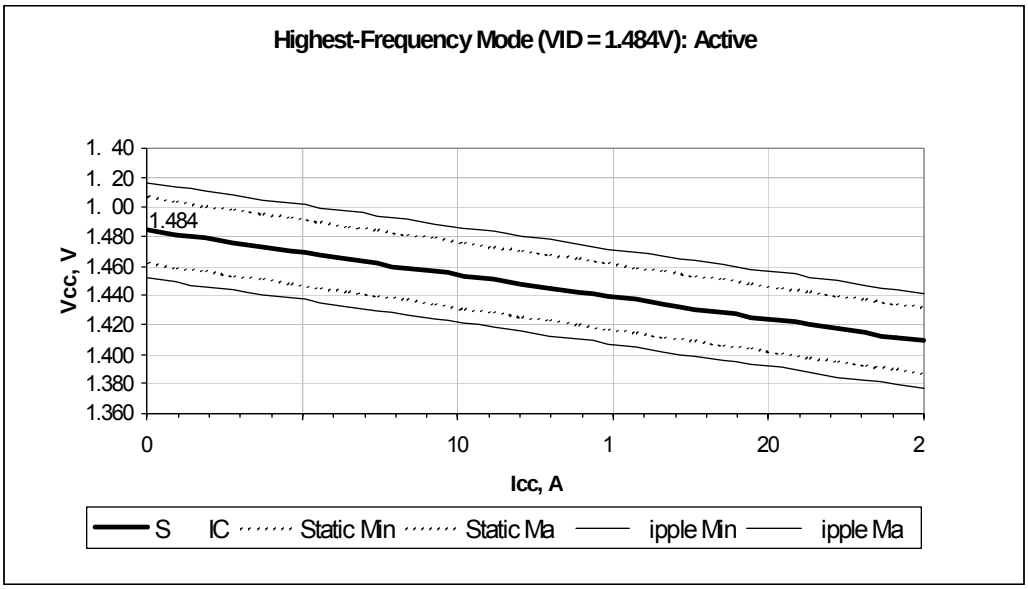


Table 7. Voltage Tolerances for Intel Pentium M Processors with HFM VID = 1.484 V (Deep Sleep State)

Mode	Highest Frequency Mode: VID = 1.484 V, Offset = 1.2%						Lowest Frequency Mode: VID = 0.956 V, Offset = 1.2%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
Deep Sleep	0.0	1.466	1.444	1.488	1.434	1.4 8	0.0	0. 4	0. 30	0.	0. 20	0. 6
	0.	1.46	1.442	1.487	1.432	1.4 7	0.2	0. 44	0. 30	0. 8	0. 20	0. 68
	1.0	1.463	1.441	1.48	1.431	1.4	0.4	0. 43	0. 2	0. 8	0. 1	0. 68
	1.6	1.462	1.43	1.484	1.42	1.4 4	0.6	0. 43	0. 28	0. 7	0. 18	0. 67
	2.1	1.460	1.438	1.482	1.428	1.4 2	0.8	0. 42	0. 28	0. 6	0. 18	0. 66
	2.6	1.4 8	1.436	1.481	1.426	1.4 1	1.0	0. 41	0. 27	0. 6	0. 17	0. 66
	3.1	1.4 7	1.43	1.47	1.42	1.48	1.2	0. 41	0. 26	0.	0. 16	0. 6
	3.6	1.4	1.433	1.478	1.423	1.488	1.4	0. 40	0. 26	0.	0. 16	0. 6
	4.2	1.4 4	1.431	1.476	1.421	1.486	1.7	0. 40	0. 2	0. 4	0. 1	0. 64
	4.7	1.4 2	1.430	1.474	1.420	1.484	1.	0. 3	0. 2	0. 3	0. 1	0. 63
	.2	1.4 1	1.428	1.473	1.418	1.483	2.1	0. 38	0. 24	0. 3	0. 14	0. 63
	.7	1.44	1.427	1.471	1.417	1.481	2.3	0. 38	0. 23	0. 2	0. 13	0. 62
	6.2	1.447	1.42	1.470	1.41	1.480	2.	0. 37	0. 23	0. 1	0. 13	0. 61
	6.8	1.446	1.424	1.468	1.414	1.478	2.7	0. 36	0. 22	0. 1	0. 12	0. 61
	7.3	1.444	1.422	1.467	1.412	1.477	2.	0. 36	0. 22	0. 0	0. 12	0. 60
	7.8	1.443	1.421	1.46	1.411	1.47	3.1	0. 36	0. 21	0. 0	0. 11	0. 60

Figure 3. Illustration of Deep Sleep State Voltage Tolerances (Lowest Frequency Mode)

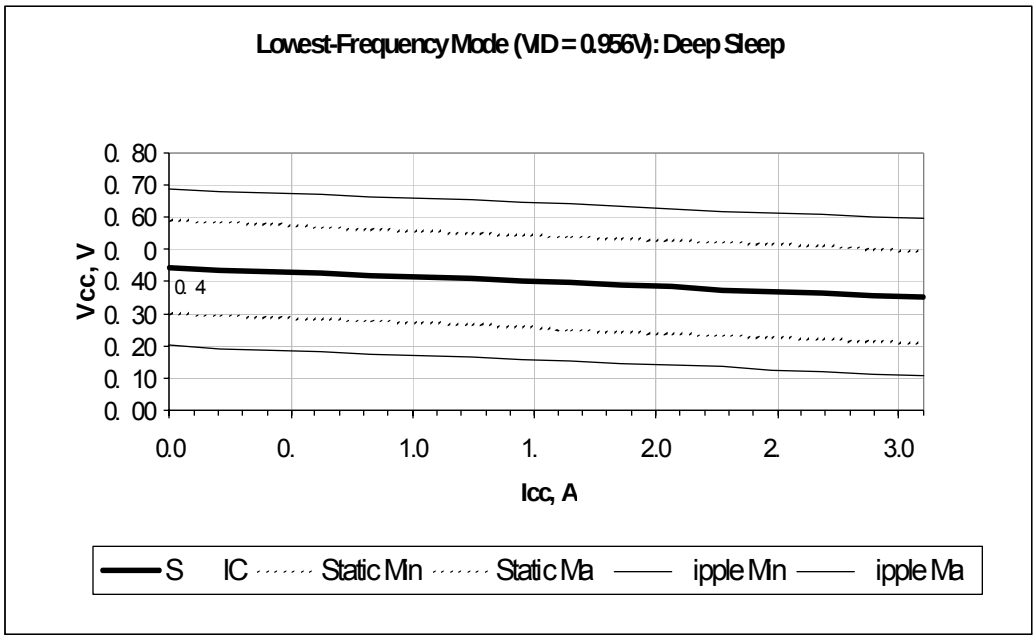


Table 8. Voltage Tolerances for Intel Pentium M Processors with HFM VID = 1.388 V (Active State)

Mode	Highest Frequency Mode: VID = 1.388 V, Offset = 0%						Lowest Frequency Mode: VID = 0.956 V, Offset = 0%					
	V_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
ACTIVE	0	1.388	1.367	1.40	1.3 7	1.41	0.0	0. 6	0. 42	0. 70	0. 32	0. 80
	0.	1.38	1.364	1.406	1.3 4	1.416	0.4	0.	0. 41	0. 6	0. 31	0. 7
	1.	1.382	1.362	1.403	1.3 2	1.413	0.7	0. 4	0. 40	0. 68	0. 30	0. 78
	2.8	1.380	1.3	1.400	1.34	1.410	1.1	0. 3	0. 38	0. 67	0. 28	0. 77
	3.7	1.377	1.3 6	1.3 8	1.346	1.408	1.4	0. 2	0. 37	0. 66	0. 27	0. 76
	4.6	1.374	1.3 3	1.3	1.343	1.40	1.8	0. 1	0. 36	0. 6	0. 26	0. 7
	.6	1.371	1.3 1	1.3 2	1.341	1.402	2.1	0. 0	0. 3	0. 64	0. 2	0. 74
	6.	1.36	1.348	1.38	1.338	1.3	2.	0. 48	0. 34	0. 63	0. 24	0. 73
	7.4	1.366	1.34	1.387	1.33	1.3 7	2.	0. 47	0. 33	0. 62	0. 23	0. 72
	8.3	1.363	1.342	1.384	1.332	1.3 4	3.2	0. 46	0. 32	0. 61	0. 22	0. 71
	.3	1.360	1.33	1.381	1.32	1.3 1	3.6	0. 4	0. 31	0. 60	0. 21	0. 70
	10.2	1.3 7	1.337	1.378	1.327	1.388	3.	0. 44	0. 30	0.	0. 20	0. 6
	11.1	1.3	1.334	1.37	1.324	1.38	4.3	0. 43	0. 2	0. 7	0. 1	0. 67
	12.0	1.3 2	1.331	1.373	1.321	1.383	4.7	0. 42	0. 28	0. 6	0. 18	0. 66
	13.0	1.34	1.328	1.370	1.318	1.380	.0	0. 41	0. 27	0.	0. 17	0. 6
	13.	1.346	1.326	1.367	1.316	1.377	.4	0. 40	0. 26	0. 4	0. 16	0. 64
	14.8	1.344	1.323	1.364	1.313	1.374	.7	0. 3	0. 24	0. 3	0. 14	0. 63
	1 .7	1.341	1.320	1.362	1.310	1.372	6.1	0. 38	0. 23	0. 2	0. 13	0. 62
	16.7	1.338	1.317	1.3	1.307	1.36	6.4	0. 37	0. 22	0. 1	0. 12	0. 61
	17.6	1.33	1.314	1.3 6	1.304	1.366	6.8	0. 36	0. 21	0. 0	0. 11	0. 60
	18.	1.332	1.312	1.3 3	1.302	1.363						
	1 .4	1.330	1.30	1.3 0	1.2	1.360						
	20.4	1.327	1.306	1.348	1.2 6	1.3 8						
	21.3	1.324	1.303	1.34	1.2 3	1.3						
	22.2	1.321	1.301	1.342	1.2 1	1.3 2						
	23.1	1.31	1.2 8	1.33	1.288	1.34						
	24.1	1.316	1.2	1.337	1.28	1.347						
	2 .0	1.313	1.2 2	1.334	1.282	1.344						

Table 9. Voltage Tolerances for Intel Pentium M Processors with HFM VID = 1.388 V (Deep Sleep State)

Mode	Highest Frequency Mode: VID =1.388 V, Offset = 1.2%						Lowest Frequency Mode: VID = 0.956 V, Offset = 1.2%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
Deep Sleep	0.0	1.371	1.3 1	1.3 2	1.341	1.402	0.0	0. 4	0. 30	0.	0. 20	0. 6
	0.6	1.370	1.34	1.3 0	1.33	1.400	0.2	0. 44	0. 30	0. 8	0. 20	0. 68
	1.2	1.368	1.347	1.38	1.337	1.3	0.4	0. 43	0. 2	0. 8	0. 1	0. 68
	1.8	1.366	1.34	1.387	1.33	1.3 7	0.6	0. 43	0. 28	0. 7	0. 18	0. 67
	2.3	1.364	1.343	1.38	1.333	1.3	0.8	0. 42	0. 28	0. 6	0. 18	0. 66
	2.	1.363	1.342	1.383	1.332	1.3 3	1.0	0. 41	0. 27	0. 6	0. 17	0. 66
	3.	1.361	1.340	1.382	1.330	1.3 2	1.2	0. 41	0. 26	0.	0. 16	0. 6
	4.1	1.3	1.338	1.380	1.328	1.3 0	1.4	0. 40	0. 26	0.	0. 16	0. 6
	4.7	1.3 7	1.336	1.378	1.326	1.388	1.7	0. 40	0. 2	0. 4	0. 1	0. 64
	.3	1.3 6	1.33	1.376	1.32	1.386	1.	0. 3	0. 2	0. 3	0. 1	0. 63
	.	1.3 4	1.333	1.37	1.323	1.38	2.1	0. 38	0. 24	0. 3	0. 14	0. 63
	6.	1.3 2	1.331	1.373	1.321	1.383	2.3	0. 38	0. 23	0. 2	0. 13	0. 62
	7.0	1.3 0	1.32	1.371	1.31	1.381	2.	0. 37	0. 23	0. 1	0. 13	0. 61
	7.6	1.348	1.328	1.36	1.318	1.37	2.7	0. 36	0. 22	0. 1	0. 12	0. 61
	8.2	1.347	1.326	1.368	1.316	1.378	2.	0. 36	0. 22	0. 0	0. 12	0. 60
	8.8	1.34	1.324	1.366	1.314	1.376	3.1	0. 36	0. 21	0. 0	0. 11	0. 60

Table 10. Voltage Tolerances for Low Voltage Intel Pentium M Processors (Active State)

Mode	Highest Frequency Mode: VID = 1.180 V, Offset = 0%						Lowest Frequency Mode: VID = 0.956 V, Offset = 0%					
	V_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
ACTIVE	0	1.180	1.162	1.1 8	1.1 2	1.208	0.0	0. 6	0. 42	0. 70	0. 32	0. 80
	0.4	1.17	1.161	1.1 6	1.1 1	1.206	0.4	0.	0. 41	0. 6	0. 31	0. 7
	0.	1.177	1.160	1.1	1.1 0	1.20	0.7	0. 4	0. 40	0. 68	0. 30	0. 78
	1.3	1.176	1.1 8	1.1 4	1.148	1.204	1.1	0. 3	0. 38	0. 67	0. 28	0. 77
	1.8	1.17	1.1 7	1.1 2	1.147	1.202	1.4	0. 2	0. 37	0. 66	0. 27	0. 76
	2.2	1.173	1.1 6	1.1 1	1.146	1.201	1.8	0. 1	0. 36	0. 6	0. 26	0. 7
	2.7	1.172	1.1 4	1.1 0	1.144	1.200	2.1	0. 0	0. 3	0. 64	0. 2	0. 74
	3.1	1.171	1.1 3	1.188	1.143	1.1 8	2.	0. 48	0. 34	0. 63	0. 24	0. 73
	3.6	1.16	1.1 2	1.187	1.142	1.1 7	2.	0. 47	0. 33	0. 62	0. 23	0. 72
	4.0	1.168	1.1 0	1.186	1.140	1.1 6	3.2	0. 46	0. 32	0. 61	0. 22	0. 71
	4.4	1.167	1.14	1.184	1.13	1.1 4	3.6	0. 4	0. 31	0. 60	0. 21	0. 70
	4.	1.16	1.148	1.183	1.138	1.1 3	3.	0. 44	0. 30	0.	0. 20	0. 6
	.3	1.164	1.146	1.182	1.136	1.1 2	4.3	0. 43	0. 2	0. 7	0. 1	0. 67
	.8	1.163	1.14	1.180	1.13	1.1 0	4.7	0. 42	0. 28	0. 6	0. 18	0. 66
	6.2	1.161	1.144	1.17	1.134	1.18	.0	0. 41	0. 27	0.	0. 17	0. 6
	6.7	1.160	1.142	1.178	1.132	1.188	.4	0. 40	0. 26	0. 4	0. 16	0. 64
	7.1	1.1	1.141	1.176	1.131	1.186	.7	0. 3	0. 24	0. 3	0. 14	0. 63
	7.6	1.1 7	1.140	1.17	1.130	1.18	6.1	0. 38	0. 23	0. 2	0. 13	0. 62
	8.0	1.1 6	1.138	1.174	1.128	1.184	6.4	0. 37	0. 22	0. 1	0. 12	0. 61
	8.4	1.1	1.137	1.172	1.127	1.182	6.8	0. 36	0. 21	0. 0	0. 11	0. 60
	8.	1.1 3	1.136	1.171	1.126	1.181						
	.3	1.1 2	1.134	1.170	1.124	1.180						
	.8	1.1 1	1.133	1.168	1.123	1.178						
	10.2	1.14	1.132	1.167	1.122	1.177						
	10.7	1.148	1.130	1.166	1.120	1.176						
	11.1	1.147	1.12	1.164	1.11	1.174						
	11.6	1.14	1.128	1.163	1.118	1.173						
	12.0	1.144	1.126	1.162	1.116	1.172						

Table 11. Voltage Tolerances for Low Voltage Intel Pentium M Processors (Deep Sleep State)

Mode	Highest Frequency Mode: VID = 1.180 V, Offset = 1.2%						Lowest Frequency Mode: VID = 0.956 V, Offset = 1.2%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
Deep Sleep	0.0	1.166	1.148	1.184	1.138	1.1 4	0.0	0. 4	0. 30	0.	0. 20	0. 6
	0.3	1.16	1.147	1.183	1.137	1.1 3	0.2	0. 44	0. 30	0. 8	0. 20	0. 68
	0.6	1.164	1.146	1.182	1.136	1.1 2	0.4	0. 43	0. 2	0. 8	0. 1	0. 68
	0.8	1.163	1.146	1.181	1.136	1.1 1	0.6	0. 43	0. 28	0. 7	0. 18	0. 67
	1.1	1.162	1.14	1.180	1.13	1.1 0	0.8	0. 42	0. 28	0. 6	0. 18	0. 66
	1.4	1.162	1.144	1.17	1.134	1.18	1.0	0. 41	0. 27	0. 6	0. 17	0. 66
	1.7	1.161	1.143	1.17	1.133	1.18	1.2	0. 41	0. 26	0.	0. 16	0. 6
	2.0	1.160	1.142	1.178	1.132	1.188	1.4	0. 40	0. 26	0.	0. 16	0. 6
	2.2	1.1	1.141	1.177	1.131	1.187	1.7	0. 40	0. 2	0. 4	0. 1	0. 64
	2.	1.1 8	1.141	1.176	1.131	1.186	1.	0. 3	0. 2	0. 3	0. 1	0. 63
	2.8	1.1 7	1.140	1.17	1.130	1.18	2.1	0. 38	0. 24	0. 3	0. 14	0. 63
	3.1	1.1 7	1.13	1.174	1.12	1.184	2.3	0. 38	0. 23	0. 2	0. 13	0. 62
	3.4	1.1 6	1.138	1.173	1.128	1.183	2.	0. 37	0. 23	0. 1	0. 13	0. 61
	3.6	1.1	1.137	1.173	1.127	1.183	2.7	0. 36	0. 22	0. 1	0. 12	0. 61
	3.	1.1 4	1.136	1.172	1.126	1.182	2.	0. 36	0. 22	0. 0	0. 12	0. 60
	4.2	1.1 3	1.136	1.171	1.126	1.181	3.1	0. 36	0. 21	0. 0	0. 11	0. 60

Table 12. Voltage Tolerances for Ultra Low Voltage Intel Pentium M Processors (Active State)

Mode	Highest Frequency Mode: VID = 1.004 V, Offset = 0%						Lowest Frequency Mode: VID = 0.844 V, Offset = 0%					
	V_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
ACTIVE	0	1.004	0. 8	1.01	0. 7	1.02	0.0	0.844	0.831	0.8 7	0.821	0.867
	0.3	1.003	0. 88	1.018	0. 78	1.028	0.3	0.843	0.831	0.8 6	0.821	0.866
	0.7	1.002	0. 87	1.017	0. 77	1.027	0.	0.842	0.830	0.8	0.820	0.86
	1.0	1.001	0. 86	1.016	0. 76	1.026	0.8	0.842	0.82	0.8 4	0.81	0.864
	1.3	1.000	0. 8	1.01	0. 7	1.02	1.1	0.841	0.828	0.8 4	0.818	0.864
	1.7	0.	0. 84	1.014	0. 74	1.024	1.3	0.840	0.827	0.8 3	0.817	0.863
	2.0	0. 8	0. 83	1.013	0. 73	1.023	1.6	0.83	0.827	0.8 2	0.817	0.862
	2.3	0. 7	0. 82	1.012	0. 72	1.022	1.8	0.838	0.826	0.8 1	0.816	0.861
	2.7	0. 6	0. 81	1.011	0. 71	1.021	2.1	0.838	0.82	0.8 0	0.81	0.860
	3.0	0.	0. 80	1.010	0. 70	1.020	2.4	0.837	0.824	0.8 0	0.814	0.860
	3.3	0. 4	0. 7	1.00	0. 6	1.01	2.6	0.836	0.823	0.84	0.813	0.8
	3.7	0. 3	0. 78	1.008	0. 68	1.018	2.	0.83	0.823	0.848	0.813	0.8 8
	4.0	0. 2	0. 77	1.007	0. 67	1.017	3.2	0.83	0.822	0.847	0.812	0.8 7
	4.3	0. 1	0. 76	1.006	0. 66	1.016	3.4	0.834	0.821	0.846	0.811	0.8 6
	4.7	0. 0	0. 7	1.00	0. 6	1.01	3.7	0.833	0.820	0.846	0.810	0.8 6
	.0	0. 8	0. 74	1.004	0. 64	1.014	3.	0.832	0.820	0.84	0.810	0.8
	.3	0. 88	0. 73	1.003	0. 63	1.013	4.2	0.831	0.81	0.844	0.80	0.8 4
	.7	0. 87	0. 72	1.002	0. 62	1.012	4.	0.831	0.818	0.843	0.808	0.8 3
	6.0	0. 86	0. 71	1.001	0. 61	1.011	4.7	0.830	0.817	0.842	0.807	0.8 2
	6.3	0. 8	0. 70	1.000	0. 60	1.010	.0	0.82	0.816	0.842	0.806	0.8 2
	6.7	0. 84	0. 6	0.	0.	1.00						
	7.0	0. 83	0. 68	0. 8	0. 8	1.008						
	7.3	0. 82	0. 67	0. 7	0. 7	1.007						
	7.7	0. 81	0. 66	0. 6	0. 6	1.006						
	8.0	0. 80	0. 6	0.	0.	1.00						
	8.3	0. 7	0. 64	0. 4	0. 4	1.004						
	8.7	0. 78	0. 63	0. 3	0. 3	1.003						
	.0	0. 77	0. 62	0. 2	0. 2	1.002						

Table 13. Voltage Tolerances for Ultra Low Voltage Intel Pentium M Processors (Deep Sleep State)

Mode	Highest Frequency Mode: VID = 1.004 V, Offset = 1.2%						Lowest Frequency Mode: VID = 0.844 V, Offset = 1.2%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
Deep Sleep	0.0	0. 2	0. 77	1.007	0. 67	1.017	0.0	0.834	0.821	0.847	0.811	0.8 7
	0.2	0. 2	0. 76	1.007	0. 66	1.017	0.1	0.834	0.821	0.846	0.811	0.8 6
	0.3	0. 1	0. 76	1.006	0. 66	1.016	0.2	0.833	0.821	0.846	0.811	0.8 6
	0.	0. 1	0. 76	1.006	0. 66	1.016	0.3	0.833	0.820	0.846	0.810	0.8 6
	0.6	0. 0	0. 7	1.00	0. 6	1.01	0.4	0.833	0.820	0.84	0.810	0.8
	0.8	0. 0	0. 7	1.00	0. 6	1.01	0.	0.832	0.820	0.84	0.810	0.8
	0.	0. 8	0. 74	1.004	0. 64	1.014	0.6	0.832	0.81	0.84	0.80	0.8
	1.1	0. 8	0. 74	1.004	0. 64	1.014	0.7	0.832	0.81	0.844	0.80	0.8 4
	1.2	0. 88	0. 73	1.003	0. 63	1.013	0.	0.831	0.81	0.844	0.80	0.8 4
	1.4	0. 88	0. 73	1.003	0. 63	1.013	1.0	0.831	0.818	0.844	0.808	0.8 4
	1.	0. 87	0. 72	1.002	0. 62	1.012	1.1	0.831	0.818	0.843	0.808	0.8 3
	1.7	0. 87	0. 72	1.002	0. 62	1.012	1.2	0.830	0.818	0.843	0.808	0.8 3
	1.8	0. 86	0. 71	1.002	0. 61	1.012	1.3	0.830	0.817	0.843	0.807	0.8 3
	2.0	0. 86	0. 71	1.001	0. 61	1.011	1.4	0.830	0.817	0.842	0.807	0.8 2
	2.1	0. 86	0. 70	1.001	0. 60	1.011	1.	0.82	0.817	0.842	0.807	0.8 2
	2.3	0. 8	0. 70	1.000	0. 60	1.010	1.6	0.82	0.816	0.842	0.806	0.8 2

Table 14. System Bus Differential BCLK Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_L	Input Lo Volta e		0		V	
V_H	Input Hi h Volta e	0.660	0.710	0.8 0	V	
$V_{C SS}$	Crossin Volta e	0.2	0.3	0.	V	2
$\Delta V_{C SS}$	an e o Crossin Points	/	/	0.140	V	6
V_{H}	hreshold e ion	$V_{C SS}$ -0.100		$V_{C SS}$ 0.100	V	3
I_{LI}	Input Leaka e Current			100		4
Cpad	Pad Capacitance	1.8	2.3	2.7	pF	

NOTES:
1. nless other ise noted, all speci ications in this ta le appl to all processor re uencies.
2. Crossin Volta e is de ined as a solute olta e here risin ed e o BCL 0 is e ual to the allin ed e o BCL 1.
3. hreshold e ion is de ined as a re ion entered a out the crossin olta e in hich the di erential recei er s itches. It includes input threshold h steresis.
4. For Vin et een 0 V and V_H.
. Cpad includes die capacitance onl . o packa e parasitics are included.
6. $\Delta V_{C SS}$ is de ined as the total ariation o all crossin olta es as de ined in note 2.

Table 15. AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
VCCP	I/ Volta e	0. 7	1.0	1.102	V	
G L F	e erence Volta e	2/3 VCCP - 2	2/3 VCCP	2/3 VCCP 2	V	
V_{IH}	Input Hi h Volta e	G L F 0.1		VCCP 0.1	V	3,
V_{IL}	Input Lo Volta e	-0.1		G L F-0.1	V	2
V_{H}	utput Hi h Volta e		VCCP			
	ermination esistance	47		63	Ω	6
	Bu er n esistance	17.7	24.7	32.		4
I_{LI}	Input Leaka e Current			100		7
Cpad	Pad Capacitance	1.8	2.3	2.7	pF	8

NOTES:
1. nless other ise noted, all speci ications in this ta le appl to all processor re uencies.
2. V_{IL} is de ined as the ma imum olta e le el at a recei in a ent that ill e interpreted as a lo ical lo alue.
3. V_{IH} is de ined as the minimum olta e le el at a recei in a ent that ill e interpreted as a lo ical hi h alue.
4. his is the pull do n dri er resistance. Measured at 0.31 VCCP. (min) 0.38 , (t p) 0.4 , (ma) 0. 2 .
. G L F should e enerated rom VCCP ith a 1 tolerance resistor di ider. he VCCP re erred to in these speci ications is the instantaneous VCCP.
6. is the on-die termination resistance measured at V_{L} o the G L output dri er. Measured at 0.31 VCCP. is connected to VCCP on die.
7. Speci ied ith on die and are turned o .
8. Cpad includes die capacitance onl . o packa e parasitics are included.

.

Table 16. CMOS Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
VCCP	I/ Volta e	0. 7	1.0	1.102	V	
VIL	Input Lo Volta e CM S	-0.1		0.3 VCCP	V	2
VIH	Input Hi h Volta e	0.7 VCCP		VCCP 0.1	V	2
V L	utput Lo Volta e	-0.1	0	0.1 VCCP	V	2
V H	utput Hi h Volta e	0. VCCP	VCCP	VCCP 0.1	V	2
I L	utput Lo Current	1.4		4.08	m	3
I H	utput Hi h Current	1.4		4.08	m	4
I_{LI}	Leaka e Current			100		
Cpad	Pad Capacitance	1.0	2.3	3.0	pF	6

NOTES:
1. nless other ise noted, all speci ications in this ta le appl to all processor re uencies.
2. he VCCP re erred to in these speci ications re ers to instantaneous VCCP.
3. Measured at 0.1 VCCP.
4. Measured at 0. VCCP.
. For Vin et een 0V and VCCP. Measured hen the dri er is tristated.
6. Cpad includes die capacitance onl . o packa e parasitics are included.

Table 17. Open Drain Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V H	utput Hi h Volta e		VCCP		V	3
V L	utput Lo Volta e	0		0.20	V	
I L	utput Lo Current	16		0	m	2
I_L	Leaka e Current			200		4
Cpad	Pad Capacitance	1.7	2.3	3.0	pF	

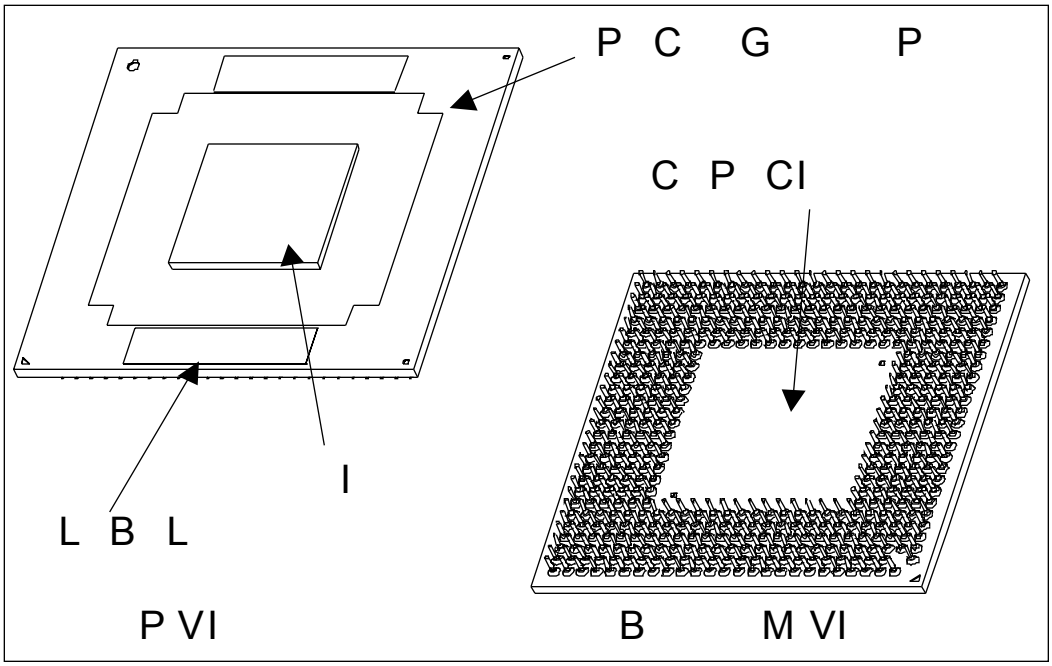
NOTES:
1. nless other ise noted, all speci ications in this ta le appl to all processor re uencies.
2. Measured at 0.2 V
3. V H is determined alue o the e ternal pullup resistor to VCCP. Please re er to the desi n uide or details.
4. For Vin et een 0 V and V H.
. Cpad includes die capacitance onl . o packa e parasitics are included.

4 Package Mechanical Specifications and Pin Information

The Intel Pentium M processor is available in 478-pin, Micro-FCPGA and 479-ball, Micro-FCBGA packages. The Low Voltage and Ultra Low Voltage Intel Pentium M processors are available only in the Micro-FCBGA package. Different views of the Micro-FCPGA package are shown in Figure 4 through Figure 6. Package dimensions are shown in Table 18. Different views of the Micro-FCBGA package are shown in Figure 8 through Figure 10. Package dimensions are shown in Table 19. The Intel Pentium M Processor Die Offset is illustrated in Figure 7.

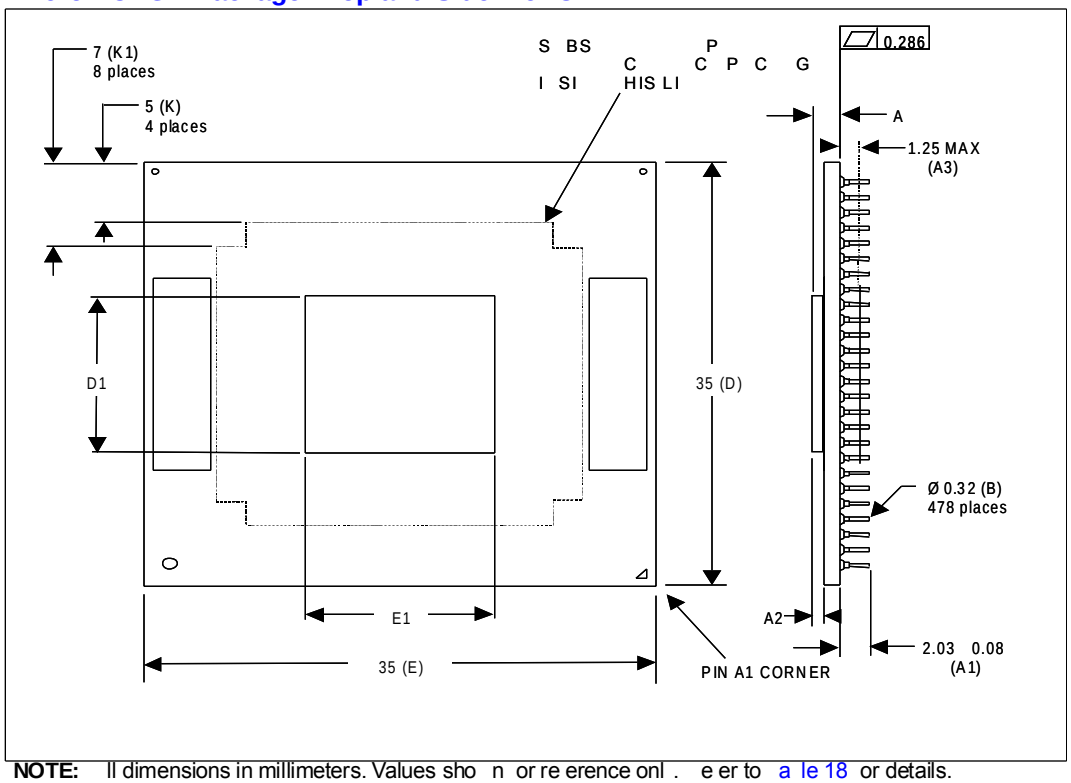
The Micro-FCBGA may have capacitors placed in the area surrounding the die. Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors, and possibly damage the device or render it inactive. The use of an insulating material between the capacitors and any thermal solution is recommended to prevent capacitor shorting.

Figure 4. Micro-FCPGA Package Top and Bottom Isometric Views



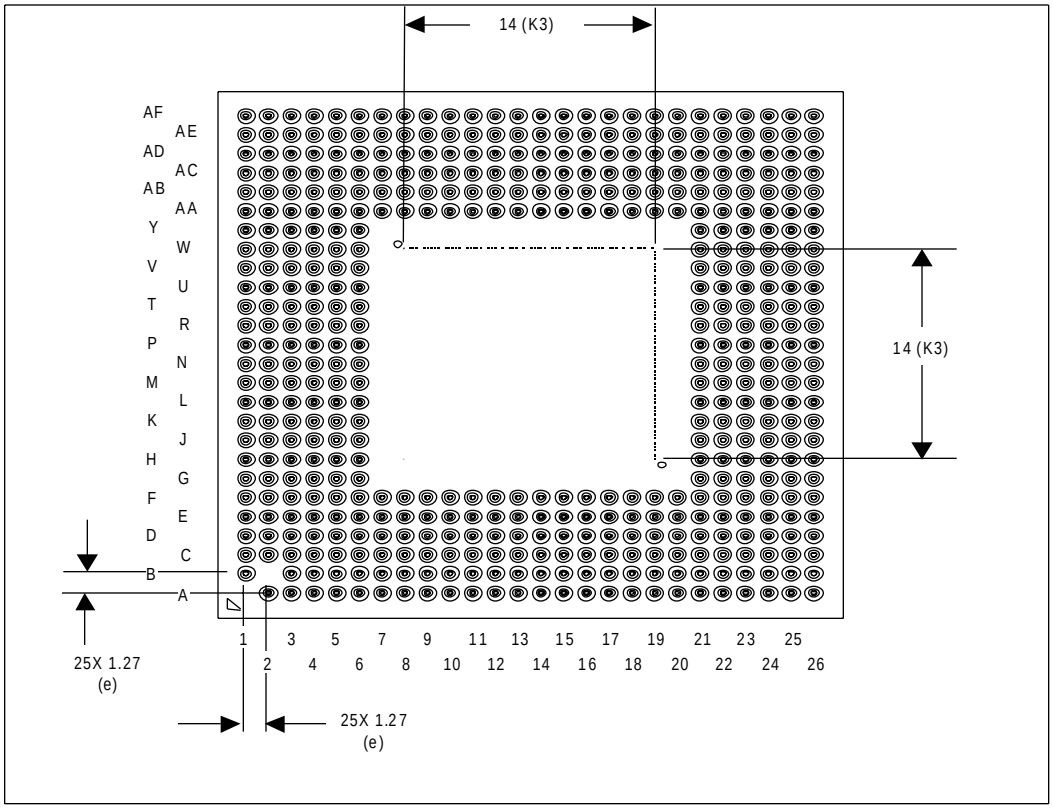
NOTE: ll dimensions in millimeters. Values sho n or re erence onl . e er to a le 18 or details.

Figure 5. Micro-FCPGA Package - Top and Side Views



NOTE: ll dimensions in millimeters. Values sho n or re erence onl . e er to a le 18 or details.

Figure 6. Micro-FCPGA Package - Bottom View



NOTE: ll dimensions in millimeters. Values sho n or re erence onl . e er to a le 18 or details.

Figure 7. Intel Pentium M Processor Die Offset

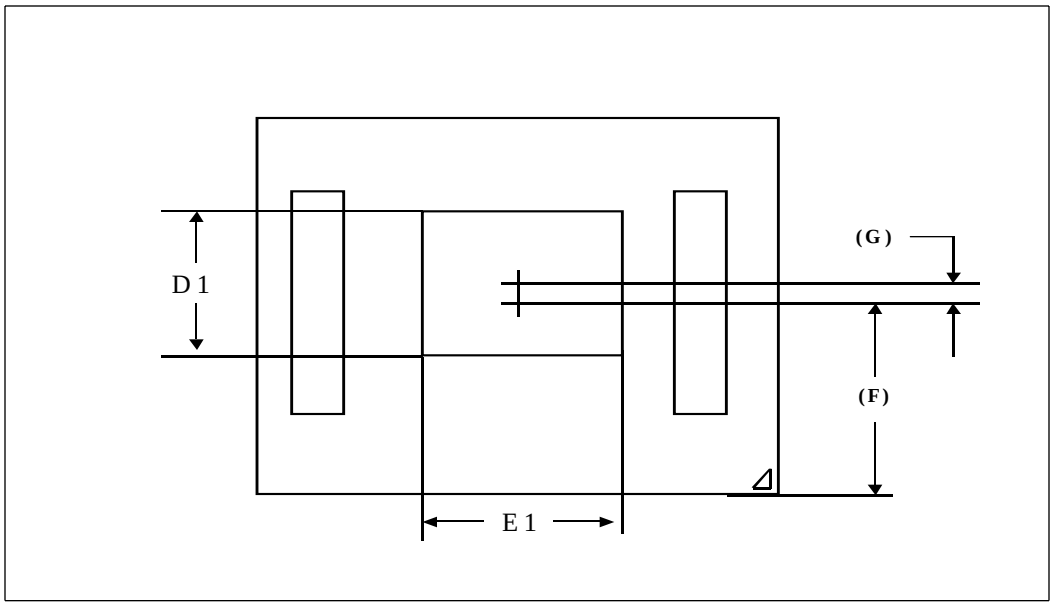


Table 18. Micro-FCPGA Package Dimensions

Symbol	Parameter	Min	Max	Unit
	erall hei ht, top o die to packa e seatin plane	1.88	2.02	mm
-	erall hei ht, top o die to PCB sur ace, includin socket (e er to ote 1)	4.74	.16	mm
1	Pin len th	1.	2.11	mm
2	ie hei ht	0.82		mm
3	Pin-side capacitor hei ht	-	1.2	mm
B	Pin diameter	0.28	0.36	mm
	Packa e su strate len th	34.	3 .1	mm
	Packa e su strate idth	34.	3 .1	mm
1	ie len th	10. 6		mm
1	ie idth	7.84		mm
F	o Packa e Su strate Center	17.		mm
G	ie set rom Packa e Center	1.133		mm
e	Pin pitch	1.27		mm
	Packa e ed e keep-out			mm
1	Packa e corner keep-out	7		mm
3	Pin-side capacitor oundar	14		mm
-	Pin tip radial true position	0.2 4		mm
	Pin count	478		each
Pdie	llo a le pressure on the die or thermal solution	-	68	kPa
	Packa e ei ht	4.		
	Packa e Sur ace Flatness	0.286		mm

NOTE: erall hei ht ith socket is ased on desi n dimensions o the Micro-FCPG packa e ith no thermal solution attached. Values are ased on desi n speci ications and tolerances. his dimension is su ect to chan e ased on socket desi n, M mother oard desi n or M SM process.

Figure 8. Micro-FCBGA Package Top and Bottom Isometric Views

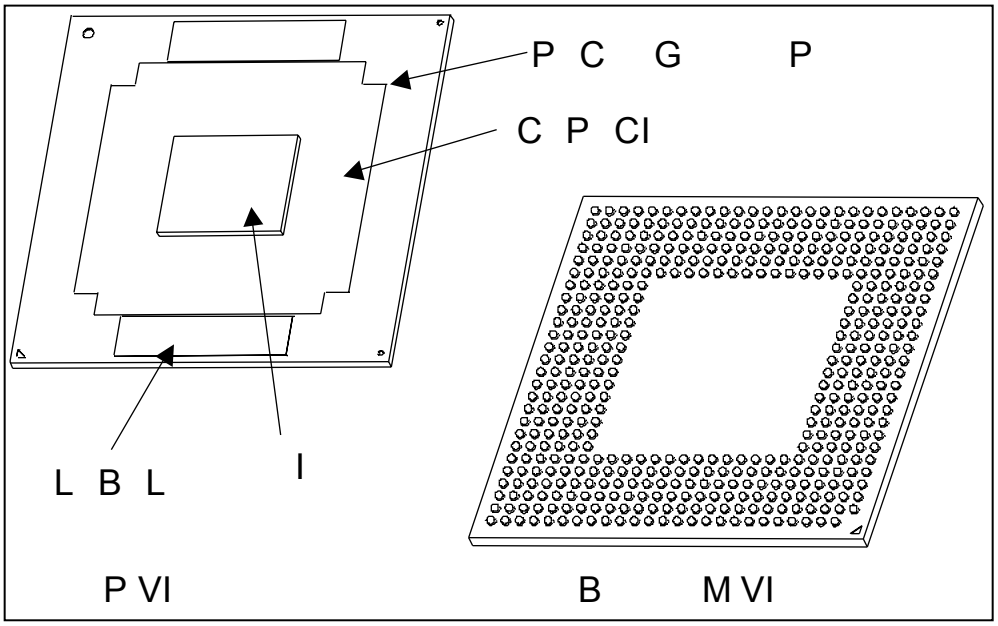
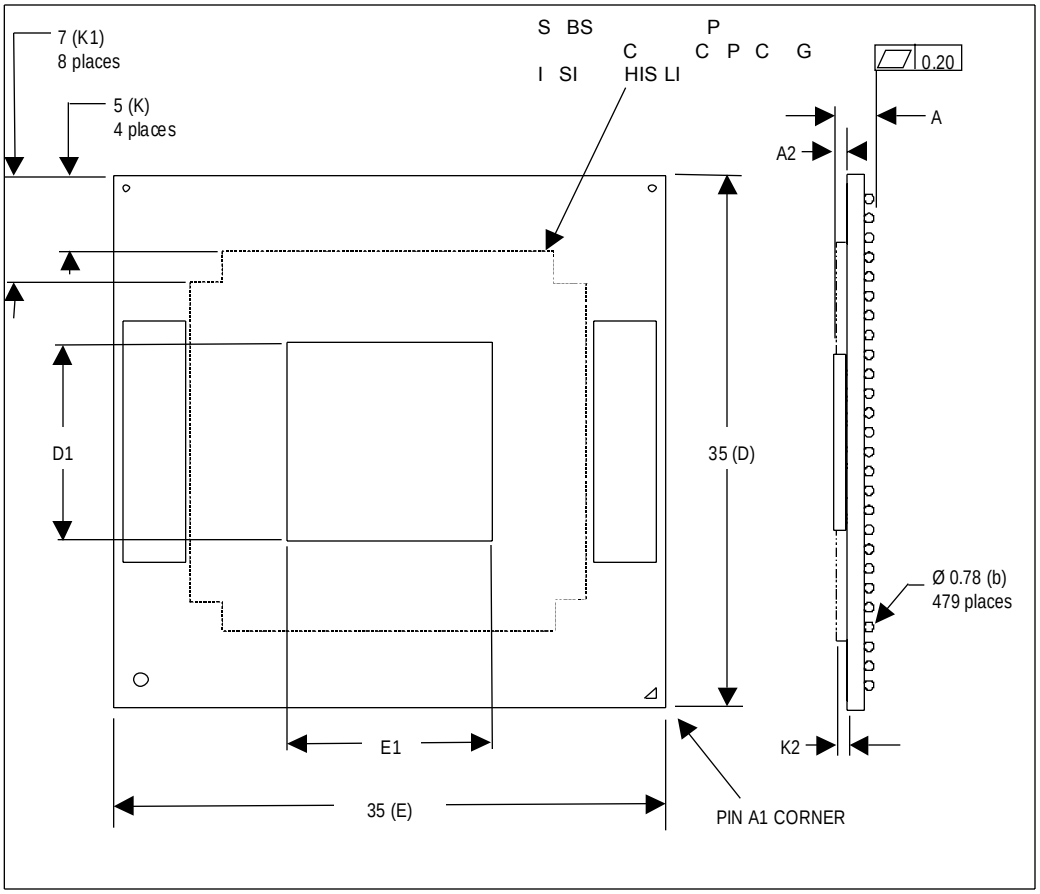


Figure 9. Micro-FCBGA Package Top and Side Views



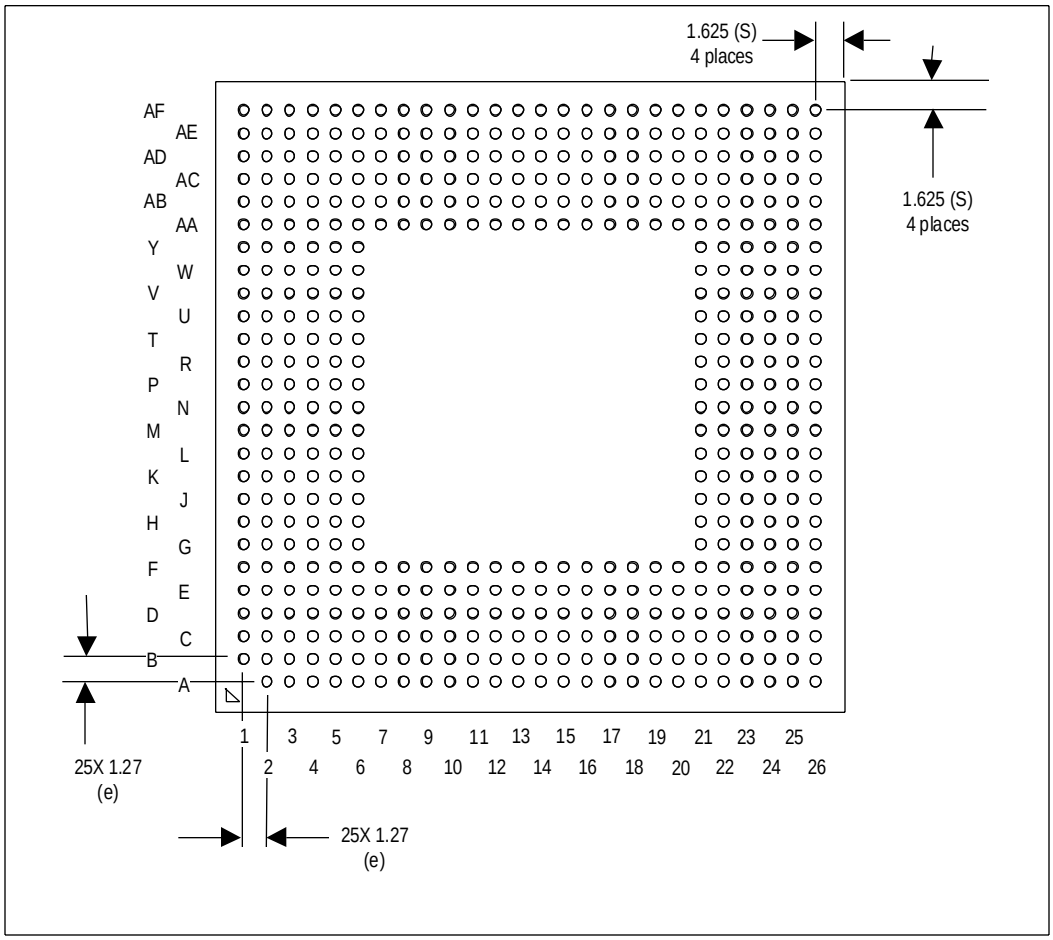
NOTE: ll dimensions in millimeters. Values sho n or re erence onl . e er to a le 1 or details.

Table 19. Micro-FCBGA Package Dimensions

Symbol	Parameter	Min	Max	Unit
	erall hei ht, as deli ered (e er to ote 1)	2.60	2.8	mm
2	ie hei ht	0.82		mm
	Ball diameter	0.78		mm
	Packa e su strate len th	34.	3 .1	mm
	Packa e su strate idth	34.	3 .1	mm
1	ie len th	10. 6		mm
1	ie idth	7.84		mm
F	o Packa e Su strate Center	17.		mm
G	ie set rom Packa e Center	1.133		mm
e	Ball pitch	1.27		mm
	Packa e ed e keep-out			mm
1	Packa e corner keep-out	7		mm
2	ie-side capacitor hei ht	-	0.7	mm
S	Packa e ed e to irst all center	1.62		mm
	Ball count	47		each
-	Solder all coplanarit	0.2		mm
Pdie	llo a le pressure on the die or thermal solution	-	68	kPa
	Packa e ei ht	4.		

NOTE: erall hei ht as deli ered. Values are ased on desi n speci ications and tolerances. his dimension is su ect to chan e ased on M mother oard desi n or M SM process.

Figure 10. Micro-FCBGA Package Bottom View



NOTE: ll dimensions in millimeters. Values sho n or re erence onl . e er to a le 1 or details.

4.1 Processor Pin-Out and Pin List

Figure 11 on the next page shows the top view pinout of the Intel Pentium M processor. The pin list arranged in two different formats is shown in Table 19 and Table 20.

Figure 11. The Coordinates of the Processor Pins as Viewed From the Top of the Package

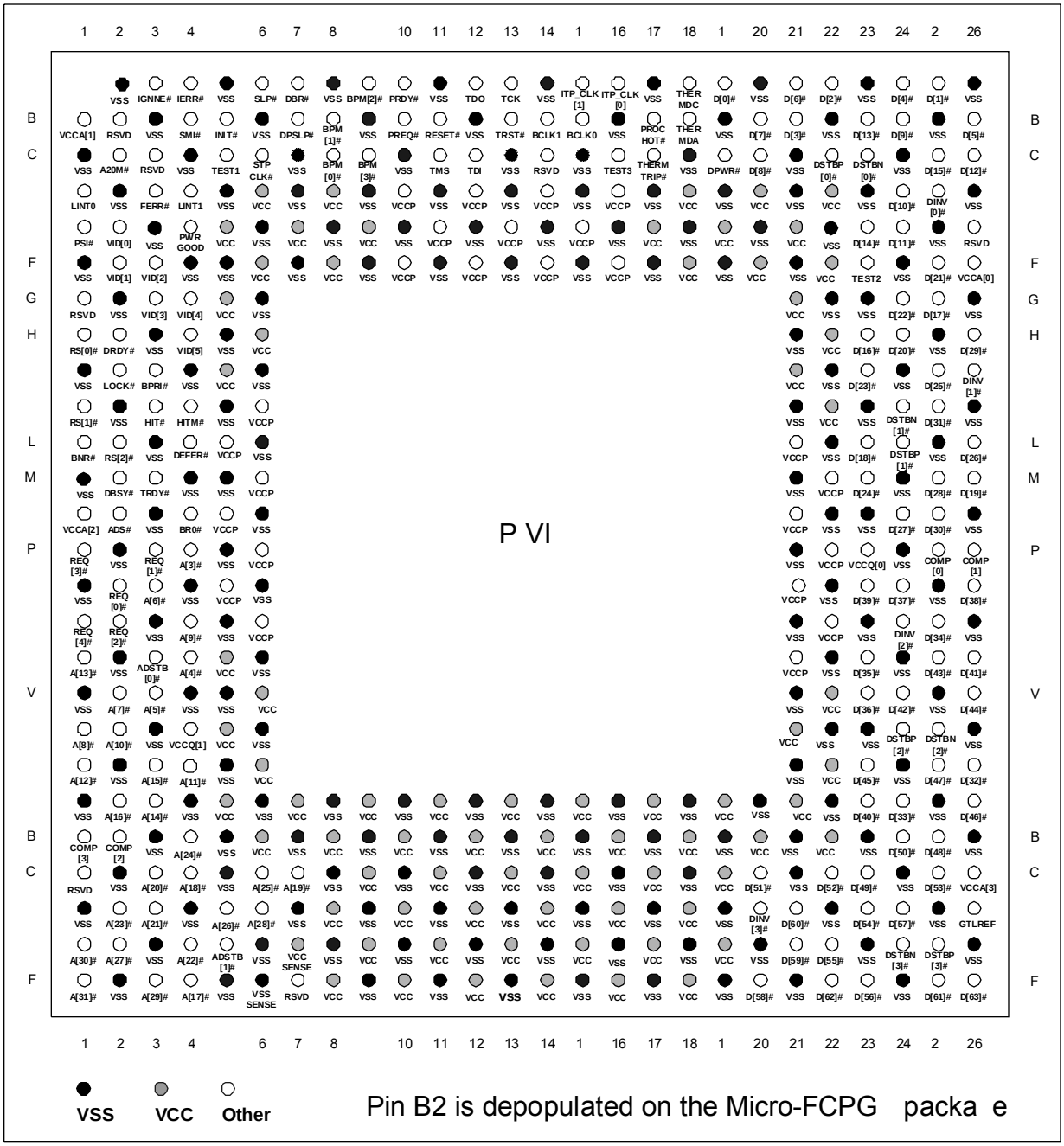


Table 20. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
3	P4	Source S nch	Input/ utput
4	4	Source S nch	Input/ utput
	V3	Source S nch	Input/ utput
6	3	Source S nch	Input/ utput
7	V2	Source S nch	Input/ utput
8	1	Source S nch	Input/ utput
	4	Source S nch	Input/ utput
10	2	Source S nch	Input/ utput
11	4	Source S nch	Input/ utput
12	1	Source S nch	Input/ utput
13	1	Source S nch	Input/ utput
14	3	Source S nch	Input/ utput
1	3	Source S nch	Input/ utput
16	2	Source S nch	Input/ utput
17	F4	Source S nch	Input/ utput
18	C4	Source S nch	Input/ utput
1	C7	Source S nch	Input/ utput
20	C3	Source S nch	Input/ utput
21	3	Source S nch	Input/ utput
22	4	Source S nch	Input/ utput
23	2	Source S nch	Input/ utput
24	B4	Source S nch	Input/ utput
2	C6	Source S nch	Input/ utput
26		Source S nch	Input/ utput
27	2	Source S nch	Input/ utput
28	6	Source S nch	Input/ utput
2	F3	Source S nch	Input/ utput
30	1	Source S nch	Input/ utput
31	F1	Source S nch	Input/ utput
20M	C2	CM S	Input
S	2	Common Clock	Input/ utput
S B 0	3	Source S nch	Input/ utput
S B 1		Source S nch	Input/ utput
BCL 0	B1	Bus Clock	Input
BCL 1	B14	Bus Clock	Input
B	L1	Common Clock	Input/ utput

Table 20. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
BPM 0	C8	Common Clock	utput
BPM 1	B8	Common Clock	utput
BPM 2		Common Clock	utput
BPM 3	C	Common Clock	Input/ utput
BP I	3	Common Clock	Input
B 0	4	Common Clock	Input/ utput
C MP 0	P2	Po er/ ther	Input/ utput
C MP 1	P26	Po er/ ther	Input/ utput
C MP 2	B2	Po er/ ther	Input/ utput
C MP 3	B1	Po er/ ther	Input/ utput
0	1	Source S nch	Input/ utput
1	2	Source S nch	Input/ utput
2	22	Source S nch	Input/ utput
3	B21	Source S nch	Input/ utput
4	24	Source S nch	Input/ utput
	B26	Source S nch	Input/ utput
6	21	Source S nch	Input/ utput
7	B20	Source S nch	Input/ utput
8	C20	Source S nch	Input/ utput
	B24	Source S nch	Input/ utput
10	24	Source S nch	Input/ utput
11	24	Source S nch	Input/ utput
12	C26	Source S nch	Input/ utput
13	B23	Source S nch	Input/ utput
14	23	Source S nch	Input/ utput
1	C2	Source S nch	Input/ utput
16	H23	Source S nch	Input/ utput
17	G2	Source S nch	Input/ utput
18	L23	Source S nch	Input/ utput
1	M26	Source S nch	Input/ utput
20	H24	Source S nch	Input/ utput
21	F2	Source S nch	Input/ utput
22	G24	Source S nch	Input/ utput
23	23	Source S nch	Input/ utput
24	M23	Source S nch	Input/ utput
2	2	Source S nch	Input/ utput
26	L26	Source S nch	Input/ utput
27	24	Source S nch	Input/ utput
28	M2	Source S nch	Input/ utput

Table 20. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
2	H26	Source S nch	Input/ utput
30	2	Source S nch	Input/ utput
31	2	Source S nch	Input/ utput
32	26	Source S nch	Input/ utput
33	24	Source S nch	Input/ utput
34	2	Source S nch	Input/ utput
3	23	Source S nch	Input/ utput
36	V23	Source S nch	Input/ utput
37	24	Source S nch	Input/ utput
38	26	Source S nch	Input/ utput
3	23	Source S nch	Input/ utput
40	23	Source S nch	Input/ utput
41	26	Source S nch	Input/ utput
42	V24	Source S nch	Input/ utput
43	2	Source S nch	Input/ utput
44	V26	Source S nch	Input/ utput
4	23	Source S nch	Input/ utput
46	26	Source S nch	Input/ utput
47	2	Source S nch	Input/ utput
48	B2	Source S nch	Input/ utput
4	C23	Source S nch	Input/ utput
0	B24	Source S nch	Input/ utput
1	C20	Source S nch	Input/ utput
2	C22	Source S nch	Input/ utput
3	C2	Source S nch	Input/ utput
4	23	Source S nch	Input/ utput
	22	Source S nch	Input/ utput
6	F23	Source S nch	Input/ utput
7	24	Source S nch	Input/ utput
8	F20	Source S nch	Input/ utput
	21	Source S nch	Input/ utput
60	21	Source S nch	Input/ utput
61	F2	Source S nch	Input/ utput
62	F22	Source S nch	Input/ utput
63	F26	Source S nch	Input/ utput
B	7	CM S	utput
BS	M2	Common Clock	Input/ utput
F	L4	Common Clock	Input
I V 0	2	Source S nch	Input/ utput

Table 20. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
I V 1	26	Source S nch	Input/ utput
I V 2	24	Source S nch	Input/ utput
I V 3	20	Source S nch	Input/ utput
PSLP	B7	CM S	Input
P	C1	Common Clock	Input
	H2	Common Clock	Input/ utput
S B 0	C23	Source S nch	Input/ utput
S B 1	24	Source S nch	Input/ utput
S B 2	2	Source S nch	Input/ utput
S B 3	24	Source S nch	Input/ utput
S BP 0	C22	Source S nch	Input/ utput
S BP 1	L24	Source S nch	Input/ utput
S BP 2	24	Source S nch	Input/ utput
S BP 3	2	Source S nch	Input/ utput
F	3	pen rain	utput
G L F	26	Po er/ ther	Input
HI	3	Common Clock	Input/ utput
HI M	4	Common Clock	Input/ utput
I	4	pen rain	utput
IG	3	CM S	Input
I I	B	CM S	Input
I P_CL 0	16	CM S	input
I P_CL 1	1	CM S	input
LI 0	1	CM S	Input
LI 1	4	CM S	Input
L C	2	Common Clock	Input/ utput
P	10	Common Clock	utput
P	B10	Common Clock	Input
P CH	B17	pen rain	utput
PSI	1	CM S	utput
P G	4	CM S	Input
0	2	Source S nch	Input/ utput
1	P3	Source S nch	Input/ utput
2	2	Source S nch	Input/ utput
3	P1	Source S nch	Input/ utput
4	1	Source S nch	Input/ utput
S	B11	Common Clock	Input
S 0	H1	Common Clock	Input
S 1	1	Common Clock	Input

Table 20. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
S 2	L2	Common Clock	Input
SV	F7	eser ed	
SV	B2	eser ed	
SV	C14	eser ed	
SV	C3	eser ed	
SV	26	eser ed	
SV	G1	eser ed	
SV	C1	eser ed	
SLP	6	CM S	Input
SMI	B4	CM S	Input
S PCL	C6	CM S	Input
C	13	CM S	Input
I	C12	CM S	Input
	12	pen rain	utput
S 1	C	est	
S 2	F23	est	
S 3	C16	est	
H M	B18	Po er/ ther	
H M C	18	Po er/ ther	
H M IP	C17	pen rain	utput
MS	C11	CM S	Input
	M3	Common Clock	Input
S	B13	CM S	Input
VCC	6	Po er/ ther	
VCC	8	Po er/ ther	
VCC	18	Po er/ ther	
VCC	20	Po er/ ther	
VCC	22	Po er/ ther	
VCC		Po er/ ther	
VCC	7	Po er/ ther	
VCC		Po er/ ther	
VCC	17	Po er/ ther	
VCC	1	Po er/ ther	
VCC	21	Po er/ ther	
VCC	F6	Po er/ ther	
VCC	F8	Po er/ ther	
VCC	F18	Po er/ ther	
VCC	F20	Po er/ ther	
VCC	F22	Po er/ ther	

Table 20. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	G	Po er/ ther	
VCC	G21	Po er/ ther	
VCC	H6	Po er/ ther	
VCC	H22	Po er/ ther	
VCC		Po er/ ther	
VCC	21	Po er/ ther	
VCC	22	Po er/ ther	
VCC		Po er/ ther	
VCC	V6	Po er/ ther	
VCC	V22	Po er/ ther	
VCC		Po er/ ther	
VCC	21	Po er/ ther	
VCC	6	Po er/ ther	
VCC	22	Po er/ ther	
VCC		Po er/ ther	
VCC	7	Po er/ ther	
VCC		Po er/ ther	
VCC	11	Po er/ ther	
VCC	13	Po er/ ther	
VCC	1	Po er/ ther	
VCC	17	Po er/ ther	
VCC	1	Po er/ ther	
VCC	21	Po er/ ther	
VCC	B6	Po er/ ther	
VCC	B8	Po er/ ther	
VCC	B10	Po er/ ther	
VCC	B12	Po er/ ther	
VCC	B14	Po er/ ther	
VCC	B16	Po er/ ther	
VCC	B18	Po er/ ther	
VCC	B20	Po er/ ther	
VCC	B22	Po er/ ther	
VCC	C	Po er/ ther	
VCC	C11	Po er/ ther	
VCC	C13	Po er/ ther	
VCC	C1	Po er/ ther	
VCC	C17	Po er/ ther	
VCC	C1	Po er/ ther	
VCC	8	Po er/ ther	

Table 20. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	10	Po er/ ther	
VCC	12	Po er/ ther	
VCC	14	Po er/ ther	
VCC	16	Po er/ ther	
VCC	18	Po er/ ther	
VCC		Po er/ ther	
VCC	11	Po er/ ther	
VCC	13	Po er/ ther	
VCC	1	Po er/ ther	
VCC	17	Po er/ ther	
VCC	1	Po er/ ther	
VCC	F8	Po er/ ther	
VCC	F10	Po er/ ther	
VCC	F12	Po er/ ther	
VCC	F14	Po er/ ther	
VCC	F16	Po er/ ther	
VCC	F18	Po er/ ther	
VCC 0	F26	Po er/ ther	
VCC 1	B1	Po er/ ther	
VCC 2	1	Po er/ ther	
VCC 3	C26	Po er/ ther	
VCCP	10	Po er/ ther	
VCCP	12	Po er/ ther	
VCCP	14	Po er/ ther	
VCCP	16	Po er/ ther	
VCCP	11	Po er/ ther	
VCCP	13	Po er/ ther	
VCCP	1	Po er/ ther	
VCCP	F10	Po er/ ther	
VCCP	F12	Po er/ ther	
VCCP	F14	Po er/ ther	
VCCP	F16	Po er/ ther	
VCCP	6	Po er/ ther	
VCCP	L	Po er/ ther	
VCCP	L21	Po er/ ther	
VCCP	M6	Po er/ ther	
VCCP	M22	Po er/ ther	
VCCP		Po er/ ther	
VCCP	21	Po er/ ther	

Table 20. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VCCP	P6	Po er/ ther	
VCCP	P22	Po er/ ther	
VCCP		Po er/ ther	
VCCP	21	Po er/ ther	
VCCP	6	Po er/ ther	
VCCP	22	Po er/ ther	
VCCP	21	Po er/ ther	
VCC 0	P23	Po er/ ther	
VCC 1	4	Po er/ ther	
VCCS S	7	Po er/ ther	utput
VI 0	2	CM S	utput
VI 1	F2	CM S	utput
VI 2	F3	CM S	utput
VI 3	G3	CM S	utput
VI 4	G4	CM S	utput
VI	H4	CM S	utput
VSS	2	Po er/ ther	
VSS		Po er/ ther	
VSS	8	Po er/ ther	
VSS	11	Po er/ ther	
VSS	14	Po er/ ther	
VSS	17	Po er/ ther	
VSS	20	Po er/ ther	
VSS	23	Po er/ ther	
VSS	26	Po er/ ther	
VSS	B3	Po er/ ther	
VSS	B6	Po er/ ther	
VSS	B	Po er/ ther	
VSS	B12	Po er/ ther	
VSS	B16	Po er/ ther	
VSS	B1	Po er/ ther	
VSS	B22	Po er/ ther	
VSS	B2	Po er/ ther	
VSS	C1	Po er/ ther	
VSS	C4	Po er/ ther	
VSS	C7	Po er/ ther	
VSS	C10	Po er/ ther	
VSS	C13	Po er/ ther	
VSS	C1	Po er/ ther	

Table 20. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	C18	Po er/ ther	
VSS	C21	Po er/ ther	
VSS	C24	Po er/ ther	
VSS	2	Po er/ ther	
VSS		Po er/ ther	
VSS	7	Po er/ ther	
VSS		Po er/ ther	
VSS	11	Po er/ ther	
VSS	13	Po er/ ther	
VSS	1	Po er/ ther	
VSS	17	Po er/ ther	
VSS	1	Po er/ ther	
VSS	21	Po er/ ther	
VSS	23	Po er/ ther	
VSS	26	Po er/ ther	
VSS	3	Po er/ ther	
VSS	6	Po er/ ther	
VSS	8	Po er/ ther	
VSS	10	Po er/ ther	
VSS	12	Po er/ ther	
VSS	14	Po er/ ther	
VSS	16	Po er/ ther	
VSS	18	Po er/ ther	
VSS	20	Po er/ ther	
VSS	22	Po er/ ther	
VSS	2	Po er/ ther	
VSS	F1	Po er/ ther	
VSS	F4	Po er/ ther	
VSS	F	Po er/ ther	
VSS	F7	Po er/ ther	
VSS	F	Po er/ ther	
VSS	F11	Po er/ ther	
VSS	F13	Po er/ ther	
VSS	F1	Po er/ ther	
VSS	F17	Po er/ ther	
VSS	F1	Po er/ ther	
VSS	F21	Po er/ ther	
VSS	F24	Po er/ ther	
VSS	G2	Po er/ ther	

Table 20. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	G6	Po er/ ther	
VSS	G22	Po er/ ther	
VSS	G23	Po er/ ther	
VSS	G26	Po er/ ther	
VSS	H3	Po er/ ther	
VSS	H	Po er/ ther	
VSS	H21	Po er/ ther	
VSS	H2	Po er/ ther	
VSS	1	Po er/ ther	
VSS	4	Po er/ ther	
VSS	6	Po er/ ther	
VSS	22	Po er/ ther	
VSS	24	Po er/ ther	
VSS	2	Po er/ ther	
VSS		Po er/ ther	
VSS	21	Po er/ ther	
VSS	23	Po er/ ther	
VSS	26	Po er/ ther	
VSS	L3	Po er/ ther	
VSS	L6	Po er/ ther	
VSS	L22	Po er/ ther	
VSS	L2	Po er/ ther	
VSS	M1	Po er/ ther	
VSS	M4	Po er/ ther	
VSS	M	Po er/ ther	
VSS	M21	Po er/ ther	
VSS	M24	Po er/ ther	
VSS	3	Po er/ ther	
VSS	6	Po er/ ther	
VSS	22	Po er/ ther	
VSS	23	Po er/ ther	
VSS	26	Po er/ ther	
VSS	P2	Po er/ ther	
VSS	P	Po er/ ther	
VSS	P21	Po er/ ther	
VSS	P24	Po er/ ther	
VSS	1	Po er/ ther	
VSS	4	Po er/ ther	
VSS	6	Po er/ ther	

Table 20. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	22	Po er/ ther	
VSS	2	Po er/ ther	
VSS	3	Po er/ ther	
VSS		Po er/ ther	
VSS	21	Po er/ ther	
VSS	23	Po er/ ther	
VSS	26	Po er/ ther	
VSS	2	Po er/ ther	
VSS	6	Po er/ ther	
VSS	22	Po er/ ther	
VSS	24	Po er/ ther	
VSS	V1	Po er/ ther	
VSS	V4	Po er/ ther	
VSS	V	Po er/ ther	
VSS	V21	Po er/ ther	
VSS	V2	Po er/ ther	
VSS	3	Po er/ ther	
VSS	6	Po er/ ther	
VSS	22	Po er/ ther	
VSS	23	Po er/ ther	
VSS	26	Po er/ ther	
VSS	2	Po er/ ther	
VSS		Po er/ ther	
VSS	21	Po er/ ther	
VSS	24	Po er/ ther	
VSS	1	Po er/ ther	
VSS	4	Po er/ ther	
VSS	6	Po er/ ther	
VSS	8	Po er/ ther	
VSS	10	Po er/ ther	
VSS	12	Po er/ ther	
VSS	14	Po er/ ther	
VSS	16	Po er/ ther	
VSS	18	Po er/ ther	
VSS	20	Po er/ ther	
VSS	22	Po er/ ther	
VSS	2	Po er/ ther	
VSS	B3	Po er/ ther	
VSS	B	Po er/ ther	

Table 20. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	B7	Po er/ ther	
VSS	B	Po er/ ther	
VSS	B11	Po er/ ther	
VSS	B13	Po er/ ther	
VSS	B1	Po er/ ther	
VSS	B17	Po er/ ther	
VSS	B1	Po er/ ther	
VSS	B21	Po er/ ther	
VSS	B23	Po er/ ther	
VSS	B26	Po er/ ther	
VSS	C2	Po er/ ther	
VSS	C	Po er/ ther	
VSS	C8	Po er/ ther	
VSS	C10	Po er/ ther	
VSS	C12	Po er/ ther	
VSS	C14	Po er/ ther	
VSS	C16	Po er/ ther	
VSS	C18	Po er/ ther	
VSS	C21	Po er/ ther	
VSS	C24	Po er/ ther	
VSS	1	Po er/ ther	
VSS	4	Po er/ ther	
VSS	7	Po er/ ther	
VSS		Po er/ ther	
VSS	11	Po er/ ther	
VSS	13	Po er/ ther	
VSS	1	Po er/ ther	
VSS	17	Po er/ ther	
VSS	1	Po er/ ther	
VSS	22	Po er/ ther	
VSS	2	Po er/ ther	
VSS	3	Po er/ ther	
VSS	6	Po er/ ther	
VSS	8	Po er/ ther	
VSS	10	Po er/ ther	
VSS	12	Po er/ ther	
VSS	14	Po er/ ther	
VSS	16	Po er/ ther	
VSS	18	Po er/ ther	

Table 20. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	20	Po er/ ther	
VSS	23	Po er/ ther	
VSS	26	Po er/ ther	
VSS	F2	Po er/ ther	
VSS	F	Po er/ ther	
VSS	F	Po er/ ther	
VSS	F11	Po er/ ther	
VSS	F13	Po er/ ther	
VSS	F1	Po er/ ther	
VSS	F17	Po er/ ther	
VSS	F1	Po er/ ther	
VSS	F21	Po er/ ther	
VSS	F24	Po er/ ther	
VSSS S	F6	Po er/ ther	utput

Table 21. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
2	VSS	Po er/ ther	
3	IG	CM S	Input
4	I	pen rain	utput
	VSS	Po er/ ther	
6	SLP	CM S	Input
7	B	CM S	utput
8	VSS	Po er/ ther	
	BPM 2	Common Clock	utput
10	P	Common Clock	utput
11	VSS	Po er/ ther	
12		pen rain	utput
13	C	CM S	Input
14	VSS	Po er/ ther	
1	I P_CL 1	CM S	input
16	I P_CL 0	CM S	input
17	VSS	Po er/ ther	
18	H M C	Po er/ ther	
1	0	Source S nch	Input/ utput
20	VSS	Po er/ ther	
21	6	Source S nch	Input/ utput
22	2	Source S nch	Input/ utput

Table 21. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
23	VSS	Po er/ ther	
24	4	Source S nch	Input/ utput
2	1	Source S nch	Input/ utput
26	VSS	Po er/ ther	
1	VSS	Po er/ ther	
2	16	Source S nch	Input/ utput
3	14	Source S nch	Input/ utput
4	VSS	Po er/ ther	
	VCC	Po er/ ther	
6	VSS	Po er/ ther	
7	VCC	Po er/ ther	
8	VSS	Po er/ ther	
	VCC	Po er/ ther	
10	VSS	Po er/ ther	
11	VCC	Po er/ ther	
12	VSS	Po er/ ther	
13	VCC	Po er/ ther	
14	VSS	Po er/ ther	
1	VCC	Po er/ ther	
16	VSS	Po er/ ther	
17	VCC	Po er/ ther	
18	VSS	Po er/ ther	
1	VCC	Po er/ ther	
20	VSS	Po er/ ther	
21	VCC	Po er/ ther	
22	VSS	Po er/ ther	
23	40	Source S nch	Input/ utput
24	33	Source S nch	Input/ utput
2	VSS	Po er/ ther	
26	46	Source S nch	Input/ utput
B1	C MP 3	Po er/ ther	Input/ utput
B2	C MP 2	Po er/ ther	Input/ utput
B3	VSS	Po er/ ther	
B4	24	Source S nch	Input/ utput
B	VSS	Po er/ ther	
B6	VCC	Po er/ ther	
B7	VSS	Po er/ ther	
B8	VCC	Po er/ ther	
B	VSS	Po er/ ther	

Table 21. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
B10	VCC	Po er/ ther	
B11	VSS	Po er/ ther	
B12	VCC	Po er/ ther	
B13	VSS	Po er/ ther	
B14	VCC	Po er/ ther	
B1	VSS	Po er/ ther	
B16	VCC	Po er/ ther	
B17	VSS	Po er/ ther	
B18	VCC	Po er/ ther	
B1	VSS	Po er/ ther	
B20	VCC	Po er/ ther	
B21	VSS	Po er/ ther	
B22	VCC	Po er/ ther	
B23	VSS	Po er/ ther	
B24	0	Source S nch	Input/ utput
B2	48	Source S nch	Input/ utput
B26	VSS	Po er/ ther	
C1	SV	eser ed	
C2	VSS	Po er/ ther	
C3	20	Source S nch	Input/ utput
C4	18	Source S nch	Input/ utput
C	VSS	Po er/ ther	
C6	2	Source S nch	Input/ utput
C7	1	Source S nch	Input/ utput
C8	VSS	Po er/ ther	
C	VCC	Po er/ ther	
C10	VSS	Po er/ ther	
C11	VCC	Po er/ ther	
C12	VSS	Po er/ ther	
C13	VCC	Po er/ ther	
C14	VSS	Po er/ ther	
C1	VCC	Po er/ ther	
C16	VSS	Po er/ ther	
C17	VCC	Po er/ ther	
C18	VSS	Po er/ ther	
C1	VCC	Po er/ ther	
C20	1	Source S nch	Input/ utput
C21	VSS	Po er/ ther	
C22	2	Source S nch	Input/ utput

Table 21. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
C23	4	Source S nch	Input/ utput
C24	VSS	Po er/ ther	
C2	3	Source S nch	Input/ utput
C26	VCC 3	Po er/ ther	
1	VSS	Po er/ ther	
2	23	Source S nch	Input/ utput
3	21	Source S nch	Input/ utput
4	VSS	Po er/ ther	
	26	Source S nch	Input/ utput
6	28	Source S nch	Input/ utput
7	VSS	Po er/ ther	
8	VCC	Po er/ ther	
	VSS	Po er/ ther	
10	VCC	Po er/ ther	
11	VSS	Po er/ ther	
12	VCC	Po er/ ther	
13	VSS	Po er/ ther	
14	VCC	Po er/ ther	
1	VSS	Po er/ ther	
16	VCC	Po er/ ther	
17	VSS	Po er/ ther	
18	VCC	Po er/ ther	
1	VSS	Po er/ ther	
20	I V 3	Source S nch	Input/ utput
21	60	Source S nch	Input/ utput
22	VSS	Po er/ ther	
23	4	Source S nch	Input/ utput
24	7	Source S nch	Input/ utput
2	VSS	Po er/ ther	
26	G L F	Po er/ ther	
1	30	Source S nch	Input/ utput
2	27	Source S nch	Input/ utput
3	VSS	Po er/ ther	
4	22	Source S nch	Input/ utput
	S B 1	Source S nch	Input/ utput
6	VSS	Po er/ ther	
7	VCCS S	Po er/ ther	utput
8	VSS	Po er/ ther	
	VCC	Po er/ ther	

Table 21. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
10	VSS	Po er/ ther	
11	VCC	Po er/ ther	
12	VSS	Po er/ ther	
13	VCC	Po er/ ther	
14	VSS	Po er/ ther	
1	VCC	Po er/ ther	
16	VSS	Po er/ ther	
17	VCC	Po er/ ther	
18	VSS	Po er/ ther	
1	VCC	Po er/ ther	
20	VSS	Po er/ ther	
21		Source S nch	Input/ utput
22		Source S nch	Input/ utput
23	VSS	Po er/ ther	
24	S B 3	Source S nch	Input/ utput
2	S BP 3	Source S nch	Input/ utput
26	VSS	Po er/ ther	
F1	31	Source S nch	Input/ utput
F2	VSS	Po er/ ther	
F3	2	Source S nch	Input/ utput
F4	17	Source S nch	Input/ utput
F	VSS	Po er/ ther	
F6	VSSS S	Po er/ ther	utput
F7	SV	eser ed	
F8	VCC	Po er/ ther	
F	VSS	Po er/ ther	
F10	VCC	Po er/ ther	
F11	VSS	Po er/ ther	
F12	VCC	Po er/ ther	
F13	VSS	Po er/ ther	
F14	VCC	Po er/ ther	
F1	VSS	Po er/ ther	
F16	VCC	Po er/ ther	
F17	VSS	Po er/ ther	
F18	VCC	Po er/ ther	
F1	VSS	Po er/ ther	
F20	8	Source S nch	Input/ utput
F21	VSS	Po er/ ther	
F22	62	Source S nch	Input/ utput

Table 21. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
F23	6	Source S nch	Input/ utput
F24	VSS	Po er/ ther	
F2	61	Source S nch	Input/ utput
F26	63	Source S nch	Input/ utput
B1	VCC 1	Po er/ ther	
B2	SV	eser ed	
B3	VSS	Po er/ ther	
B4	SMI	CM S	Input
B	I I	CM S	Input
B6	VSS	Po er/ ther	
B7	PSLP	CM S	Input
B8	BPM 1	Common Clock	utput
B	VSS	Po er/ ther	
B10	P	Common Clock	Input
B11	S	Common Clock	Input
B12	VSS	Po er/ ther	
B13	S	CM S	Input
B14	BCL 1	Bus Clock	Input
B1	BCL 0	Bus Clock	Input
B16	VSS	Po er/ ther	
B17	P CH	pen rain	utput
B18	H M	Po er/ ther	
B1	VSS	Po er/ ther	
B20	7	Source S nch	Input/ utput
B21	3	Source S nch	Input/ utput
B22	VSS	Po er/ ther	
B23	13	Source S nch	Input/ utput
B24		Source S nch	Input/ utput
B2	VSS	Po er/ ther	
B26		Source S nch	Input/ utput
C1	VSS	Po er/ ther	
C2	20M	CM S	Input
C3	SV	eser ed	
C4	VSS	Po er/ ther	
C	S 1	est	
C6	S PCL	CM S	Input
C7	VSS	Po er/ ther	
C8	BPM 0	Common Clock	utput
C	BPM 3	Common Clock	Input/ utput

Table 21. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
C10	VSS	Po er/ ther	
C11	MS	CM S	Input
C12	I	CM S	Input
C13	VSS	Po er/ ther	
C14	SV	eser ed	
C1	VSS	Po er/ ther	
C16	S 3	est	
C17	H M IP	pen rain	utput
C18	VSS	Po er/ ther	
C1	P	Common Clock	Input
C20	8	Source S nch	Input/ utput
C21	VSS	Po er/ ther	
C22	S BP 0	Source S nch	Input/ utput
C23	S B 0	Source S nch	Input/ utput
C24	VSS	Po er/ ther	
C2	1	Source S nch	Input/ utput
C26	12	Source S nch	Input/ utput
1	LI 0	CM S	Input
2	VSS	Po er/ ther	
3	F	pen rain	utput
4	LI 1	CM S	Input
	VSS	Po er/ ther	
6	VCC	Po er/ ther	
7	VSS	Po er/ ther	
8	VCC	Po er/ ther	
	VSS	Po er/ ther	
10	VCCP	Po er/ ther	
11	VSS	Po er/ ther	
12	VCCP	Po er/ ther	
13	VSS	Po er/ ther	
14	VCCP	Po er/ ther	
1	VSS	Po er/ ther	
16	VCCP	Po er/ ther	
17	VSS	Po er/ ther	
18	VCC	Po er/ ther	
1	VSS	Po er/ ther	
20	VCC	Po er/ ther	
21	VSS	Po er/ ther	
22	VCC	Po er/ ther	

Table 21. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
23	VSS	Po er/ ther	
24	10	Source S nch	Input/ utput
2	I V 0	Source S nch	Input/ utput
26	VSS	Po er/ ther	
1	PSI	CM S	utput
2	VI 0	CM S	utput
3	VSS	Po er/ ther	
4	P G	CM S	Input
	VCC	Po er/ ther	
6	VSS	Po er/ ther	
7	VCC	Po er/ ther	
8	VSS	Po er/ ther	
	VCC	Po er/ ther	
10	VSS	Po er/ ther	
11	VCCP	Po er/ ther	
12	VSS	Po er/ ther	
13	VCCP	Po er/ ther	
14	VSS	Po er/ ther	
1	VCCP	Po er/ ther	
16	VSS	Po er/ ther	
17	VCC	Po er/ ther	
18	VSS	Po er/ ther	
1	VCC	Po er/ ther	
20	VSS	Po er/ ther	
21	VCC	Po er/ ther	
22	VSS	Po er/ ther	
23	14	Source S nch	Input/ utput
24	11	Source S nch	Input/ utput
2	VSS	Po er/ ther	
26	SV	eser ed	
F1	VSS	Po er/ ther	
F2	VI 1	CM S	utput
F3	VI 2	CM S	utput
F4	VSS	Po er/ ther	
F	VSS	Po er/ ther	
F6	VCC	Po er/ ther	
F7	VSS	Po er/ ther	
F8	VCC	Po er/ ther	
F	VSS	Po er/ ther	

Table 21. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
F10	VCCP	Po er/ ther	
F11	VSS	Po er/ ther	
F12	VCCP	Po er/ ther	
F13	VSS	Po er/ ther	
F14	VCCP	Po er/ ther	
F1	VSS	Po er/ ther	
F16	VCCP	Po er/ ther	
F17	VSS	Po er/ ther	
F18	VCC	Po er/ ther	
F1	VSS	Po er/ ther	
F20	VCC	Po er/ ther	
F21	VSS	Po er/ ther	
F22	VCC	Po er/ ther	
F23	S 2	est	
F24	VSS	Po er/ ther	
F2	21	Source S nch	Input/ utput
F26	VCC 0	Po er/ ther	
G1	SV	eser ed	
G2	VSS	Po er/ ther	
G3	VI 3	CM S	utput
G4	VI 4	CM S	utput
G	VCC	Po er/ ther	
G6	VSS	Po er/ ther	
G21	VCC	Po er/ ther	
G22	VSS	Po er/ ther	
G23	VSS	Po er/ ther	
G24	22	Source S nch	Input/ utput
G2	17	Source S nch	Input/ utput
G26	VSS	Po er/ ther	
H1	S 0	Common Clock	Input
H2		Common Clock	Input/ utput
H3	VSS	Po er/ ther	
H4	VI	CM S	utput
H	VSS	Po er/ ther	
H6	VCC	Po er/ ther	
H21	VSS	Po er/ ther	
H22	VCC	Po er/ ther	
H23	16	Source S nch	Input/ utput
H24	20	Source S nch	Input/ utput

Table 21. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
H2	VSS	Po er/ ther	
H26	2	Source S nch	Input/ utput
1	VSS	Po er/ ther	
2	L C	Common Clock	Input/ utput
3	BP I	Common Clock	Input
4	VSS	Po er/ ther	
	VCC	Po er/ ther	
6	VSS	Po er/ ther	
21	VCC	Po er/ ther	
22	VSS	Po er/ ther	
23	23	Source S nch	Input/ utput
24	VSS	Po er/ ther	
2	2	Source S nch	Input/ utput
26	I V 1	Source S nch	Input/ utput
1	S 1	Common Clock	Input
2	VSS	Po er/ ther	
3	HI	Common Clock	Input/ utput
4	HI M	Common Clock	Input/ utput
	VSS	Po er/ ther	
6	VCCP	Po er/ ther	
21	VSS	Po er/ ther	
22	VCC	Po er/ ther	
23	VSS	Po er/ ther	
24	S B 1	Source S nch	Input/ utput
2	31	Source S nch	Input/ utput
26	VSS	Po er/ ther	
L1	B	Common Clock	Input/ utput
L2	S 2	Common Clock	Input
L3	VSS	Po er/ ther	
L4	F	Common Clock	Input
L	VCCP	Po er/ ther	
L6	VSS	Po er/ ther	
L21	VCCP	Po er/ ther	
L22	VSS	Po er/ ther	
L23	18	Source S nch	Input/ utput
L24	S BP 1	Source S nch	Input/ utput
L2	VSS	Po er/ ther	
L26	26	Source S nch	Input/ utput
M1	VSS	Po er/ ther	

Table 21. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
M2	BS	Common Clock	Input/ utput
M3		Common Clock	Input
M4	VSS	Po er/ ther	
M	VSS	Po er/ ther	
M6	VCCP	Po er/ ther	
M21	VSS	Po er/ ther	
M22	VCCP	Po er/ ther	
M23	24	Source S nch	Input/ utput
M24	VSS	Po er/ ther	
M2	28	Source S nch	Input/ utput
M26	1	Source S nch	Input/ utput
1	VCC 2	Po er/ ther	
2	S	Common Clock	Input/ utput
3	VSS	Po er/ ther	
4	B 0	Common Clock	Input/ utput
	VCCP	Po er/ ther	
6	VSS	Po er/ ther	
21	VCCP	Po er/ ther	
22	VSS	Po er/ ther	
23	VSS	Po er/ ther	
24	27	Source S nch	Input/ utput
2	30	Source S nch	Input/ utput
26	VSS	Po er/ ther	
P1	3	Source S nch	Input/ utput
P2	VSS	Po er/ ther	
P3	1	Source S nch	Input/ utput
P4	3	Source S nch	Input/ utput
P	VSS	Po er/ ther	
P6	VCCP	Po er/ ther	
P21	VSS	Po er/ ther	
P22	VCCP	Po er/ ther	
P23	VCC 0	Po er/ ther	
P24	VSS	Po er/ ther	
P2	C MP 0	Po er/ ther	Input/ utput
P26	C MP 1	Po er/ ther	Input/ utput
1	VSS	Po er/ ther	
2	0	Source S nch	Input/ utput
3	6	Source S nch	Input/ utput
4	VSS	Po er/ ther	

Table 21. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
	VCCP	Po er/ ther	
6	VSS	Po er/ ther	
21	VCCP	Po er/ ther	
22	VSS	Po er/ ther	
23	3	Source S nch	Input/ utput
24	37	Source S nch	Input/ utput
2	VSS	Po er/ ther	
26	38	Source S nch	Input/ utput
1	4	Source S nch	Input/ utput
2	2	Source S nch	Input/ utput
3	VSS	Po er/ ther	
4		Source S nch	Input/ utput
	VSS	Po er/ ther	
6	VCCP	Po er/ ther	
21	VSS	Po er/ ther	
22	VCCP	Po er/ ther	
23	VSS	Po er/ ther	
24	I V 2	CM S	Input/ utput
2	34	Source S nch	Input/ utput
26	VSS	Po er/ ther	
1	13	Source S nch	Input/ utput
2	VSS	Po er/ ther	
3	S B 0	Source S nch	Input/ utput
4	4	Source S nch	Input/ utput
	VCC	Po er/ ther	
6	VSS	Po er/ ther	
21	VCCP	Po er/ ther	
22	VSS	Po er/ ther	
23	3	Source S nch	Input/ utput
24	VSS	Po er/ ther	
2	43	Source S nch	Input/ utput
26	41	Source S nch	Input/ utput
V1	VSS	Po er/ ther	
V2	7	Source S nch	Input/ utput
V3		Source S nch	Input/ utput
V4	VSS	Po er/ ther	
V	VSS	Po er/ ther	
V6	VCC	Po er/ ther	
V21	VSS	Po er/ ther	

Table 21. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
V22	VCC	Po er/ ther	
V23	36	Source S nch	Input/ utput
V24	42	Source S nch	Input/ utput
V2	VSS	Po er/ ther	
V26	44	Source S nch	Input/ utput
1	8	Source S nch	Input/ utput
2	10	Source S nch	Input/ utput
3	VSS	Po er/ ther	
4	VCC 1	Po er/ ther	
	VCC	Po er/ ther	
6	VSS	Po er/ ther	
21	VCC	Po er/ ther	
22	VSS	Po er/ ther	
23	VSS	Po er/ ther	
24	S BP 2	Source S nch	Input/ utput
2	S B 2	Source S nch	Input/ utput
26	VSS	Po er/ ther	
1	12	Source S nch	Input/ utput
2	VSS	Po er/ ther	
3	1	Source S nch	Input/ utput
4	11	Source S nch	Input/ utput
	VSS	Po er/ ther	
6	VCC	Po er/ ther	
21	VSS	Po er/ ther	
22	VCC	Po er/ ther	
23	4	Source S nch	Input/ utput
24	VSS	Po er/ ther	
2	47	Source S nch	Input/ utput
26	32	Source S nch	Input/ utput

4.2 Alphabetical Signals Reference

Table 22. Signal Description (Sheet 1 of 7)

Name	Type	Description
31 3	Input/ utput	31 3 (ddress) de ine a 2^{32}- te ph sical memor address space. In su - phase 1 o the address phase, these pins transmit the address o a transaction. In su -phase 2, these pins transmit transaction t pe in ormation. hese si nals must connect the appropriate pins o oth a ents on the Intel Pentium M processor s stem us. 31 3 are source s nchronous si nals and are latched into the recei in u ers S B1 0 . ddress si nals are used as straps hich are sampled e ore S is deasserted.
20M	Input	I 20M (ddress-20 Mask) is asserted, the processor masks ph sical address it 20 (20) e ore lookin up a line in an internal cache and e ore dri in a read/ rite transaction on the us. ssertin 20M emulates the 8086 processor s address rap-around at the 1-M te oundar . ssertion o 20M is onl supported in real mode. 20M is an as nchronous si nal. Ho e er, to ensure reco nition o this si nal ollo in an Input/ utput rite instruction, it must e alid alon ith the assertion o the correspondin Input/ utput rite us transaction.
S	Input/ utput	S (ddress Stro e) is asserted to indicate the alidit o the transaction address on the 31 3 and 4 0 pins. ll us a ents o ser e the S acti ation to e in parit checkin , protocol checkin , address decode, internal snoop, or de erred repl l match operations associated ith the ne transaction.
S B1 0	Input/ utput	ddress stro es are used to latch 31 3 and 4 0 on their risin and allin ed es. Stro es are associated ith si nals as sho n elo . **Signals** / **Associated Strobe** 4 0 , 16 3 / S B0 31 17 / S B1
BCL 1 0	Input	he di erential pair BCL (Bus Clock) determines the s stem us re uenc . ll processor s stem us a ents must recei e these si nals to dri e their outputs and latch their inputs.
B	Input/ utput	B (Block e t e uest) is used to assert a us stall an us a ent that is una le to accept ne us transactions. urin a us stall, the current us o ner cannot issue an ne transactions.
BPM 2 0 BPM 3	utput Input/ utput	BPM 3 0 (Breakpoint Monitor) are reakpoint and per ormance monitor si nals. he are outputs rom the processor that indicate the status o reakpoints and pro ramma le counters used or monitorin processor per ormance. BPM 3 0 should connect the appropriate pins o all Intel Pentium M processor s stem us a ents. his includes de u or per ormance monitorin tools. Please re er to the plat orm desi n uides and *ITP700 Debug Port Design Guide* or more detailed in ormation.
BP I	Input	BP I (Bus Priorit e uest) is used to ar itrate or o nership o the processor s stem us. It must connect the appropriate pins o oth processor s stem us a ents. ser in BP I acti e (as asserted the priorit a ent) causes the other a ent to stop issuin ne re uests, unless such re uests are part o an on oin locked operation. he priorit a ent keeps BP I asserted until all o its re uests are completed, then releases the us deassertin BP I .
B 0	Input/ utput	B 0 is used the processor to re uest the us. he ar itration is done et een the Intel Pentium M processor (S mmetric ent) and the MCH-M (Hi h Priorit ent) o the Intel 8 PM or Intel 8 GM chipset.

Table 22. Signal Description (Sheet 2 of 7)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>C MP 3 0</td><td>nalo</td><td>C MP 3 0 must e terminated on the s stem oard usin precision (1 tolerance) resistors. e er to the plat orm desi n uides or more implementation details.</td></tr>
<tr><td>63 0</td><td>Input/
utput</td><td>63 0 (ata) are the data si nals. hese si nals pro ide a 64- it data path et een the processor s stem us a ents, and must connect the appropriate pins on oth a ents. he data dri er asserts to indicate a alid data trans er.
63 0 are uad-pumped si nals and ill thus e dri en our times in a common clock period. 63 0 are latched o the allin ed e o oth S BP 3 0 and S B 3 0 . ach roup o 16 data si nals correspond to a pair o one S BP and one S B . he ollo in ta le sho s the roupin o data si nals to data stro es and I V .
Quad-Pumped Signal Groups
<table>
<tr><th>Data Group</th><th>DSTBN#/
DSTBP#</th><th>DINV#</th></tr>
<tr><td>1 0</td><td>0</td><td>0</td></tr>
<tr><td>31 16</td><td>1</td><td>1</td></tr>
<tr><td>47 32</td><td>2</td><td>2</td></tr>
<tr><td>63 48</td><td>3</td><td>3</td></tr>
</table>
Furthermore, the I V pins determine the polarit o the data si nals. ach roup o 16 data si nals corresponds to one I V si nal. hen the I V si nal is acti e, the correspondin data roup is in erted and there ore sampled acti e hi h.</td></tr>
<tr><td>B</td><td>utput</td><td>B (ata Bus eset) is used onl in processor s stems here no de u port is implemented on the s stem oard. B is used a de u port interposer so that an in-tar et pro e can dri e s stem reset. I a de u port is implemented in the s stem, B is a no connect. B is not a processor si nal.</td></tr>
<tr><td>BS</td><td>Input/
utput</td><td>BS (ata Bus Bus) is asserted the a ent responsi le or dri in data on the processor s stem us to indicate that the data us is in use. he data us is released a ter BS is deasserted. his si nal must connect the appropriate pins on oth processor s stem us a ents.</td></tr>
<tr><td>F</td><td>Input</td><td>F is asserted an a ent to indicate that a transaction cannot e uaranteed in-order completion. ssertion o F is normall the responsi ilit o the addressed memor or Input/ utput a ent. his si nal must connect the appropriate pins o oth processor s stem us a ents.</td></tr>
<tr><td>I V 3 0</td><td>Input/
utput</td><td>I V 3 0 (ata Bus In ersion) are source s nchronous and indicate the polarit o the 63 0 si nals. he I V 3 0 si nals are acti ated hen the data on the data us is in erted. he us a ent ill in ert the data us si nals i more than hal the its, ithin the co ered roup, ould chan e le el in the ne t c cle.
DINV[3:0]# Assignment To Data Bus
<table>
<tr><th>Bus Signal</th><th>Data Bus Signals</th></tr>
<tr><td>I V 3</td><td>63 48</td></tr>
<tr><td>I V 2</td><td>47 32</td></tr>
<tr><td>I V 1</td><td>31 16</td></tr>
<tr><td>I V 0</td><td>1 0</td></tr>
</table></td></tr>
</table>

Table 22. Signal Description (Sheet 3 of 7)

Name	Type	Description
PSLP	Input	PSLP hen asserted on the plat orm causes the processor to transition rom the Sleep state to the eep Sleep state. In order to return to the Sleep state, PSLP must e deasserted. PSLP is dri en the ICH4-M component and also connects to the MCH-M component o the Intel 8 PM or Intel 8 GM chipset.
P	Input	P is a control si nal rom the Intel 8 PM and Intel 8 GM chipsets used to reduce po er on the Intel Pentium M data us input u ers.
	Input/ utput	(ata ead) is asserted the data dri er on each data trans er, indicatin alid data on the data us. In a multi-common clock data trans er, ma e deasserted to insert idle clocks. his si nal must connect the appropriate pins o oth processor s stem us a ents.
S B 3 0	Input/ utput	ata stro e used to latch in 63 0 . **Signals** / **Associated Strobe** 1 0 , I V 0 — S B 0 31 16 , I V 1 — S B 1 47 32 , I V 2 — S B 2 63 48 , I V 3 — S B 3
S BP 3 0	Input/ utput	ata stro e used to latch in 63 0 . **Signals** / **Associated Strobe** 1 0 , I V 0 — S BP 0 31 16 , I V 1 — S BP 1 47 32 , I V 2 — S BP 2 63 48 , I V 3 — S BP 3
F /PB	utput	F (Floatin -point rror)/PB (Pendin Break ent) is a multiple ed si nal and its meanin is uali ied S PCL . hen S PCL is not asserted, F /PB indicates a loatin point hen the processor detects an unmasked loatin -point error. F is similar to the si nal on the Intel 80387 coprocessor, and is included or compati ilit ith s stems usin MS- S t pe loatin -point error reportin . hen S PCL is asserted, an assertion o F /PB indicates that the processor has a pendin reak e ent aitin or ser ice. he assertion o F /PB indicates that the processor should e returned to the ormal state. hen F /PB is asserted, indicatin a reak e ent, it ill remain asserted until S PCL is deasserted. ssertion o P hen S PCL is acti e ill also cause an F reak e ent. For additional in ormation on the pendin reak e ent unctionalit , includin identi ication o support or the eature and ena le/disa le in ormation, re er to Volume 3 o the *Intel® Architecture Software Developer's Manual* and the *Intel® Processor Identification and CPUID Instruction* application note. For termination re uirements please re er to the plat orm desi n uides.
G L F	Input	G L F determines the si nal re erence le el or G L input pins. G L F should e set at 2/3 V_{CCP}. G L F is used the G L recei ers to determine i a si nal is a lo ical 0 or lo ical 1. Please re er to the plat orm desi n uides or details on G L F implementation.

Table 22. Signal Description (Sheet 4 of 7)

Name	Type	Description
HI HI M	Input/ utput Input/ utput	HI (Snoop Hit) and HI M (Hit Modi ied) con e transaction snoop operation results. ither s stem us a ent ma assert oth HI and HI M to ether to indicate that it re uires a snoop stall, hich can e continued reassertin HI and HI M to ether.
I	utput	I (Internal rror) is asserted a processor as the result o an internal error. ssertion o I is usuall accompanied a SH transaction on the processor s stem us. his transaction ma optionall e con erted to an e ternal error si nal (e. ., MI) s stem core lo ic. he processor ill keep I asserted until the assertion o S , BI I , or I I . For termination re uirements please re er to the plat orm desi n uides.
IG	Input	IG (I nore umeric rror) is asserted to orce the processor to i nore a numeric error and continue to e ecute noncontrol loatin -point instructions. I IG is deasserted, the processor enerates an e ception on a noncontrol loatin -point instruction i a pre ious loatin -point instruction caused an error. IG has no e ect hen the it in control re ister 0 (C 0) is set. IG is an as nchronous si nal. Ho e er, to ensure reco nition o this si nal ollo in an Input/ utput rite instruction, it must e alid alon ith the assertion o the correspondin Input/ utput rite us transaction.
I I	Input	I I (Initialization), hen asserted, resets inte er re isters inside the processor ithout a ection its internal caches or loatin -point re isters. he processor then e ins e ecution at the po er on eset ector con i ured durin po er on con i uration. he processor continues to handle snoop re uests durin I I assertion. I I is an as nchronous si nal. Ho e er, to ensure reco nition o this si nal ollo in an Input/ utput rite instruction, it must e alid alon ith the assertion o the correspondin Input/ utput rite us transaction. I I must connect the appropriate pins o oth processor s stem us a ents. I I I is sampled acti e on the acti e to inacti e transition o S , then the processor e ecutes its Built-in Sel - est (BIS) For termination re uirements please re er to the plat orm desi n uides.
I P_CL 1 0	Input	I P_CL 1 0 are copies o BCL that are used onl in processor s stems here no de u port is implemented on the s stem oard. I P_CL 1 0 are used as BCL 1 0 re erences or a de u port implemented on an interposer. I a de u port is implemented in the s stem, I P_CL 1 0 are no connects. hese are not processor si nals.
LI 1 0	Input	LI 1 0 (Local PIC Interrupt) must connect the appropriate pins o all PIC Bus a ents. hen the PIC is disa led, the LI 0 si nal ecomes I , a maska le interrupt re uest si nal, and LI 1 ecomes MI, a nonmaska le interrupt. I and MI are ack ard compati le ith the si nals o those names on the Pentium processor. Both si nals are as nchronous. Both o these si nals must e so t are con i ured usin BI S pro rammin o the PIC re ister space and used either as MI/I or LI 1 0 . Because the PIC is ena led de ault a ter eset, operation o these pins as LI 1 0 is the de ault con i uration.
L C	Input/ utput	L C indicates to the s stem that a transaction must occur atomicall . his si nal must connect the appropriate pins o oth processor s stem us a ents. For a locked se uence o transactions, L C is asserted rom the e innin o the irst transaction to the end o the last transaction. hen the priorit a ent asserts BP I to ar itrate or o nership o the processor s stem us, it ill ait until it o ser es L C deasserted. his ena les s mmetric a ents to retain o nership o the processor s stem us throu hout the us locked operation and ensure the atomicit o lock.

Table 22. Signal Description (Sheet 5 of 7)

Name	Type	Description
P	utput	Pro e ead si nal used de u tools to determine processor de u readiness. Please re er to the *ITP700 Debug Port Design Guide* and the plat orm desi n uides or more implementation details.
P	Input	Pro e e uest si nal used de u tools to re uest de u operation o the processor. Please re er to the *ITP700 Debug Port Design Guide* and the plat orm desi n uides or more implementation details.
P CH	utput	P CH (Processor Hot) ill o acti e hen the processor temperature monitorin sensor detects that the processor has reached its ma imum sa e operatin temperature. his indicates that the processor hermal Control Circuit has een acti ated, i ena led. See Chapter or more details. For termination re uirements please re er to the plat orm desi n uides. his si nal ma re uire olta e translation on the mother oard. Please re er to the plat orm desi n uides or more details.
PSI	utput	Processor Po er Status Indicator si nal. his si nal is asserted hen the processor is in a lo er state (eep Sleep and eeper Sleep). See Section 2.1.3 or more details.
P G	Input	P G (Po er Good) is a processor input. he processor re uires this si nal as a clean indication that the clocks and po er supplies are sta le and ithin their speci ications. Clean implies that the si nal ill remain lo (capa le o sinkin leaka e current), ithout litches, rom the time that the po er supplies are turned on until the come ithin speci ication. he si nal must then transition monotonicall to a hi h state. P G can e dri en inacti e at an time, ut clocks and po er must a ain e sta le e ore a su se uent risin ed e o P G . he P G si nal must e supplied to the processor it is used to protect internal circuits a ainst olta e se uencin issues. It should e dri en hi h throu hout the oundar scan operation. For termination re uirements please re er to the plat orm desi n uides.
4 0	Input/ utput	4 0 (e uest Command) must connect the appropriate pins o oth processor s stem us a ents. he are asserted the current us o ner to de ine the currentl acti e transaction t pe. hese si nals are source s nchronous to S B 0 .
S	Input	ssertin the S si nal resets the processor to a kno n state and in alidates its internal caches ithout ritin ack an o their contents. For a po er-on eset, S must sta acti e or at least t o milliseconds a ter VCC and BCL ha e reached their proper speci ications. n o ser in acti e S , oth s stem us a ents ill deassert their outputs ithin t o clocks. ll processor straps must e alid ithin the speci ied setup time e ore S is deasserted. Please re er to the *ITP700 Debug Port Design Guide* and the plat orm desi n uides or termination re uirements and implementation details. here is a ohm (nominal) on die pullup resistor on this si nal.
S 2 0	Input	S 2 0 (esponse Status) are dri en the response a ent (the a ent responsi le or completion o the current transaction), and must connect the appropriate pins o oth processor s stem us a ents.
SV	eser ed/ o Connect	hese pins are S V and must e le t unconnected on the oard. Ho e er, it is recommended that routin channels to these pins on the oard e kept open or possi le uture use. Please re er to the plat orm desi n uides or more details.

Table 22. Signal Description (Sheet 6 of 7)

Name	Type	Description
SLP	Input	SLP (Sleep), hen asserted in Stop-Grant state, causes the processor to enter the Sleep state. urin Sleep state, the processor stops pro idin internal clock si nals to all units, lea in onl the Phase-Locked Loop (PLL) still operatin . Processors in this state ill not reco nize snoops or interrupts. he processor ill reco nize onl assertion o the S si nal, deassertion o SLP , and remo al o the BCL input hile in Sleep state. I SLP is deasserted, the processor e its Sleep state and returns to Stop-Grant state, restartin its internal clock si nals to the us and processor core units. I PSLP is asserted hile in the Sleep state, the processor ill e it the Sleep state and transition to the eep Sleep state.
SMI	Input	SMI (S stem Mana ement Interrupt) is asserted as nchronousl s stem lo ic. n acceptin a S stem Mana ement Interrupt, the processor sa es the current state and enter S stem Mana ement Mode (SMM). n SMI ckno led e transaction is issued, and the processor e ins pro ram e ecution rom the SMM handler. I SMI is asserted durin the deassertion o S the processor ill tristate its outputs.
S PCL	Input	S PCL (Stop Clock), hen asserted, causes the processor to enter a lo po er Stop-Grant state. he processor issues a Stop-Grant ckno led e transaction, and stops pro idin internal clock si nals to all processor core units e cept the s stem us and PIC units. he processor continues to snoop us transactions and ser ice interrupts hile in Stop-Grant state. hen S PCL is deasserted, the processor restarts its internal clock to all units and resumes e ecution. he assertion o S PCL has no e ect on the us clock S PCL is an as nchronous input.
C	Input	C (est Clock) pro ides the clock input or the processor est Bus (also kno n as the est ccess Port). Please re er to the *ITP700 Debug Port Design Guide* and the plat orm desi n uides or termination re uirements and implementation details.
I	Input	I (est ata In) trans ers serial test data into the processor. I pro ides the serial input needed or G speci ication support. Please re er to the *ITP700 Debug Port Design Guide* and the plat orm desi n uides or termination re uirements and implementation details.
	utput	(est ata ut) trans ers serial test data out o the processor. pro ides the serial output needed or G speci ication support. Please re er to the *ITP700 Debug Port Design Guide* and the plat orm desi n uides or termination re uirements and implementation details.
S 1, S 2, S 3	Input	S 1, S 2, and S 3 must e le t unconnected ut should ha e a stu in option connection to V_{SS} separatel usin 1-k, pull-do n resistors. Please re er to the plat orm desi n uides or more details.
H M	ther	hermal iode node.
H M C	ther	hermal iode Cathode.
H M IP	utput	he processor protects itsel rom catastrophic o erheatin use o an internal thermal sensor. his sensor is set ell a o e the normal operatin temperature to ensure that there are no alse trips. he processor ill stop all e ecution hen the unction temperature e ceeds appro imatel 12 C. his is si nalled to the s stem the H M IP (hermal rip) pin. For termination re uirements please re er to the plat orm desi n uides.
MS	Input	MS (est Mode Select) is a G speci ication support si nal used de u tools. Please re er to the *ITP700 Debug Port Design Guide* and the plat orm desi n uides or termination re uirements and implementation details.

Table 22. Signal Description (Sheet 7 of 7)

Name	Type	Description
	Input	(ar et ead) is asserted the tar et to indicate that it is read to recei e a rite or implicit rite ack data trans er. must connect the appropriate pins o oth s stem us a ents.
S	Input	S (est eset) resets the est ccess Port (P) lo ic. S must e dri en lo durin po er on eset. Please re er to the *ITP700 Debug Port Design Guide* and the plat orm desi n uides or termination re uirements and implementation details.
V_{CC}	Input	Processor core po er suppl .
V_{CC} 3 0	Input	V_{CC} pro ides isolated po er or the internal processor core PLL s. e er to the plat orm desi n uides or complete implementation details.
V_{CCP}	Input	Processor I/ Po er Suppl .
V_{CC} 1 0	Input	uiet po er suppl or on die C MP circuitr . hese pins should e connected to V_{CCP} on the mother oard. Ho e er, these connections should ena le addition o decouplin on the V_{CC} lines i necessar .
V_{CCS} s	utput	V_{CCS} s is an isolated lo impedance connection to processor core po er (V_{CC}). It can e used to sense or measure po er near the silicon ith little noise. Please re er to the plat orm desi n uides or termination recommendations and more details.
VI 0	utput	VI 0 (Volta e I) pins are used to support automatic selection o po er suppl olta es (Vcc). nlike some pre ious enerations o processors, these are CM S si nals that are dri en the Intel Pentium M processor. he olta e suppl or these pins must e alid e ore the V can suppl Vcc to the processor. Con ersel , the V output must e disa led until the olta e suppl or the VI pins ecomes alid. he VI pins are needed to support the processor olta e speci ication ariations. See a le 3 or de initions o these pins. he V must suppl the olta e that is re uested the pins, or disa le itsel .
V_{SSS} s	utput	V_{SSS} s is an isolated lo impedance connection to processor core V_{SS}. It can e used to sense or measure round near the silicon ith little noise. Please re er to the plat orm desi n uides or termination recommendations and more details.

5 Thermal Specifications and Design Considerations

The Intel Pentium M processor requires a thermal solution to maintain temperatures within operating limits. A complete thermal solution includes both component and system level thermal management features. Component level thermal solutions include active or passive heatsinks or heat exchangers attached to the processor exposed die. The solution should make firm contact with the die while maintaining processor mechanical specifications such as pressure. A typical system level thermal solution may consist of a processor fan ducted to a heat exchanger that is thermally coupled to the processor using a heat pipe or direct die attachment. A secondary fan or air from the processor fan may also be used to cool other platform components or lower the internal ambient temperature within the system. The processor must remain within the minimum and maximum junction temperature (Tj) specifications at the corresponding Thermal Design Power (TDP) value listed in Table 23. The maximum junction temperature is defined by an activation of the processor Intel Thermal Monitor.

Refer to Section 5.1.2 for more details. Analysis indicates that real applications are unlikely to cause the processor to consume the theoretical maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP) indicated in Table 23. The Intel Thermal Monitor feature is designed to help protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained period of time. For more details on the usage of this feature, refer to Section 5.1.2. In all cases the Intel Thermal Monitor feature must be enabled for the processor to remain within specification.

Table 23. Power Specifications for the Intel Pentium M Processor

Symbol	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
P	1.70 GHz 1.484 V 1.60 GHz 1.484 V 1. 0 GHz 1.484 V 1.40 GHz 1.484 V 1.30 GHz 1.388 V 1.30 GHz 1.180 V 1.20 GHz 1.180 V 1.10 GHz 1.180 V 1.10 GHz 1.004 V 1.00 GHz 1.004 V 00 MHz 1.004V 600 MHz 0. 6 V 600 MHz 0.844 V	24. 24. 24. 22 22 12 12 12 7 7 7 6 4				t 100 C, otes 1, 4
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Notes**
P H, P SG	uto Halt, Stop-Grant Po er at 1.484 V 1.388 V (Pentium M 1.30 GHz) 1.180 V 1.004 V (LV Pentium M) 0. 6 V 0.844 V (LV Pentium M)			 7.3 7.3 3.2 1.7 1.8 0.		t 0 C, ote 2
P SLP	Sleep Po er at 1.484 V 1.388 V (Pentium M 1.30 GHz) 1.180 V 1.004 V (LV Pentium M) 0. 6 V 0.844 V (LV Pentium M)			 7.0 7.0 3.0 1. 1.7 0.8		t 0 C, ote 2
P SLP	eep Sleep Po er at 1.484 V 1.388 V (Pentium M 1.30 GHz) 1.180 V 1.004 V (LV Pentium M) 0. 6 V 0.844 V (LV Pentium M)			 .1 .4 2.2 1.0 1.1 0.		t 3 C, ote 2
P P SLP	eeper Sleep Po er			0.		t 3 C, ote 2
P P SLP LV	eeper Sleep Po er (LV Pentium M onl)			0.37		t 3 C, ote 2
	unction emperature	0		100	°C	otes 3, 4

NOTES:

1. he hermal esi n Po er (P) speci ication should e used to desi n the processor thermal solution. he P is not the ma imum theoretical po er the processor can dissipate.

2. ot 100 tested. hese po er speci ications are determined characterization o the processor currents at hi her temperatures and e trapolatin the alues or the temperature indicated.
3. s measured the on-die Intel hermal Monitor. he Intel hermal Monitor s automatic mode is used to indicate that the ma imum has een reached. e er to Section .1 or more details.
4. he Intel hermal Monitor automatic mode must e ena led or the processor to operate ithin speci ications.

5.1 Thermal Specifications

5.1.1 Thermal Diode

The Intel Pentium M processor incorporates two methods of monitoring die temperature, the Intel Thermal Monitor and the thermal diode. The Intel Thermal Monitor (detailed in Section 5.1) must be used to determine when the maximum specified processor junction temperature has been reached. The second method, the thermal diode, can be read by an off-die analog/digital converter (a thermal sensor) located on the motherboard, or a stand-alone measurement kit. The thermal diode may be used to monitor the die temperature of the processor for thermal management or instrumentation purposes but cannot be used to indicate that the maximum T_J of the processor has been reached. Please see Section 5.1.2 for thermal diode usage recommendation when the PROCHOT# signal is not asserted.

Table 24 and Table 25 provide the diode interface and specifications.

Note: The reading of the external thermal sensor (on the motherboard) connected to the processor thermal diode signals, will not necessarily reflect the temperature of the hottest location on the die. This is due to inaccuracies in the external thermal sensor, on-die temperature gradients between the location of the thermal diode and the hottest location on the die, and time based variations in the die temperature measurement. Time based variations can occur when the sampling rate of the thermal diode (by the thermal sensor) is slower than the rate at which the T_J temperature can change.

The offset between the thermal diode based temperature reading and the Intel Thermal Monitor reading can be characterized using the Intel Thermal Monitor's automatic mode activation of the thermal control circuit. This temperature offset must be taken into account when using the processor thermal diode to implement power management events.

Table 24. Thermal Diode Interface

Signal Name	Pin/Ball Number	Signal Description
H M	B18	hermal diode anode
H M C	18	hermal diode cathode

Table 25. Thermal Diode Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_F	For ard Bias Current			300	μA	ote 1
n	iode Idealit Factor	1.001 1	1.00220	1.0028		otes 2, 3, 4
	Series esistance		3.06		ohms	2, 3,

NOTES:

1. Intel does not support or recommend operation o the thermal diode under re erse ias. Intel does not support or recommend operation o the thermal diode hen the processor po er supplies are not ithin their speci ied tolerance ran e.
2. Characterized at 100 C.
3. ot 100 tested. Speci ied desi n/characterization.
4. he idealit actor, n, represents the de iation rom ideal diode eha ior as e empli ied the diode e uation
   I_F I_s ($e^{(V /nk)}$-1)
   here I_S saturation current, electronic char e, V olta e across the diode, k Boltzmann Constant, and a solute temperature (el in).
. he series resistance, , is pro ided to allo or a more accurate measurement o the diode unction temperature. as de ined, includes the pins o the processor ut does not include an socket resistance or oard trace resistance et een the socket and the e ternal remote diode thermal sensor. can e used remote diode thermal sensors ith automatic series resistance cancellation to cali rate out this error term. nother application is that a temperature o set can e manuall calculated and pro rammed into an o set re ister in the remote diode thermal sensors as e empli ied the e uation
   error (-1) $I_{F\ min}$ / (no/) ln

5.1.2 Intel Thermal Monitor

The Intel Thermal Monitor helps control the processor temperature by activating the TCC when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel Thermal Monitor activates the thermal control circuit (TCC) is not user configurable and is not software visible. Bus traffic is snooped in the normal manner, and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would not be detectable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss, and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously.

The Intel Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks or by initiating an Enhanced Intel SpeedStep® technology transition when the processor silicon reaches its maximum operating temperature. The Intel Thermal Monitor uses two modes to activate the TCC: Automatic mode and On-Demand mode. If both modes are activated, Automatic mode takes precedence. **The Intel Thermal Monitor Automatic Mode must be enabled via BIOS for the processor to be operating within specifications**.There are two Automatic modes called Intel Thermal Monitor 1 and Intel Thermal Monitor 2. These modes are selected by writing values to the Model Specific Registers (MSRs) of the processor. After Automatic mode is enabled, the TCC will activate only when the internal die temperature reaches the maximum allowed value for operation.

Likewise, when Intel Thermal Monitor 2 is enabled, and a high temperature situation exists, the processor will perform an Enhanced Intel SpeedStep technology transition to a lower operating point. When the processor temperature drops below the critical level, the processor will make an Enhanced Intel SpeedStep technology transition to the last requested operating point. Intel Thermal Monitor 2 is the recommended mode on the Intel Pentium M processor.

If a processor load-based Enhanced Intel SpeedStep technology transition (through MSR write) is initiated when an Intel Thermal Monitor 2 period is active, there are two possible results:

1. If the processor load based Enhanced Intel SpeedStep technology transition target frequency is **higher** than the Intel Thermal Monitor 2 transition based target frequency, the processor load-based transition will be deferred until the Intel Thermal Monitor 2 event has been completed.

2. If the processor load-based Enhanced Intel SpeedStep technology transition target frequency is
   lower than the Intel Thermal Monitor 2 transition based target frequency, the processor will transition to the processor load-based Enhanced Intel SpeedStep technology target frequency point.

When Intel Thermal Monitor 1 is enabled, and a high temperature situation exists, the clocks will be modulated by alternately turning the clocks off and on at a 50% duty cycle. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. After the temperature has returned to a non-critical level, modulation ceases and the TCC goes inactive. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. The duty cycle is factory configured and cannot be modified. Also, Automatic mode does not require any additional hardware, software drivers or interrupt handling routines. Processor performance will be decreased by the same amount as the duty cycle when the TCC is active, however, with a properly designed and characterized thermal solution the TCC most likely will never be activated, or will be activated only briefly during the most power intensive applications.

The TCC may also be activated using On-Demand mode. If bit 4 of the ACPI Intel Thermal Monitor Control Register is written to a "1", the TCC will be activated immediately, independent of the processor temperature. When using On-Demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI Intel Thermal Monitor Control Register. In Automatic mode, the duty cycle is fixed at 50% on, 50% off, in On-Demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-Demand mode can be used at the same time Automatic mode is enabled, however, if the system tries to enable the TCC via On-Demand mode at the same time Automatic mode is enabled **and** a high temperature condition exists, Automatic mode will take precedence.

An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is above the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active.

Note: PROCHOT# will not be asserted when the processor is in the Stop-Grant, Sleep, Deep Sleep, and Deeper Sleep low power states (internal clocks stopped), hence the thermal diode reading must be used as a safeguard to maintain the processor junction temperature within the 100 °C (maximum) specification. If the platform thermal solution is not able to maintain the processor junction temperature within the maximum specification, the system must initiate an orderly shutdown to prevent damage. If the processor enters one of the above low power states with PROCHOT# already asserted, PROCHOT# will remain asserted until the processor exits the low power state and the processor junction temperature drops below the thermal trip point.

If Automatic mode is disabled the processor will be operating out of specification. Whether the automatic or On-Demand modes are enabled or not, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 125 °C. At this point the system bus signal THERMTRIP# will go active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. When THERMTRIP# is asserted, the processor core voltage must be shut down within the time specified in Chapter 3.

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6 Debug Tools Specifications

Please refer to the *ITP700 Debug Port Design Guide* and the platform design guides for information regarding debug tools specifications.

6.1 Logic Analyzer Interface (LAI)

Intel is working with logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging Intel Pentium M processor systems. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of Intel Pentium M processor systems, the LAI is critical in providing the ability to probe and capture system bus signals. There are two sets of considerations to keep in mind when designing an Intel Pentium M processor system that can make use of an LAI: mechanical and electrical.

6.1.1 Mechanical Considerations

The LAI is installed between the processor socket and the Intel Pentium M processor. The LAI pins plug into the socket, while the Intel Pentium M processor pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the Intel Pentium M processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system.

6.1.2 Electrical Considerations

The LAI will also affect the electrical performance of the system bus; therefore, it is critical to obtain electrical load models from each of the logic analyzers to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

Intel® Pentium® M Processor LV 738 (2M Cache, 1.40 GHz, 400 MHz FSB)

SPECIFICATIONS

All
Essentials
Memory Specifications
Package Specifications
Advanced Technologies

COMPATIBLE PRODUCTS

BLOCK DIAGRAMS

ORDERING / SSPECS / STEPPINGS

Specifications

Essentials	
Status	Launched
Launch Date	Q2'04
Processor Number	738
# of Cores	1
# of Threads	1
Clock Speed	1.4 GHz
L2 Cache	2 MB
Bus/Core Ratio	14
FSB Speed	400 MHz
FSB Parity	No
Instruction Set	32-bit
Embedded Options Available	Yes
Supplemental SKU	No
Lithography	90 nm
Max TDP	10 W
VID Voltage Range	0.988V-1.116V
Recommended Customer Price	TRAY: $218

Memory Specifications	
Physical Address Extensions	32-bit
ECC Memory Supported	No

Package Specifications

$T_{JUNCTION}$	100°C
Package Size	35mm x 35mm
Processing Die Size	87 mm^2
# of Processing Die Transistors	144 million
Sockets Supported	H-PBGA479
Low Halogen Options Available	See MDDS

Advanced Technologies

Intel® Turbo Boost Technology	No
Intel® Hyper-Threading Technology	No
Intel® Virtualization Technology (VT-x)	No
Intel® Trusted Execution Technology	No
Intel® 64	No
Idle States	No
Enhanced Intel SpeedStep® Technology	Yes
Intel® Demand Based Switching	No
Execute Disable Bit	Yes

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availability.

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chipset, BIOS, operating syst
architecture. Processors will
architecture-enabled BIOS. Performance will vary depending on your hardware and software configurations. Consult with your system vend

Max Turbo Frequency refers to the maximum single-core frequency that can be achieved with Intel® Turbo Boost Technology, which requir
capability. Intel Turbo Boost Technology performance varies depending on hardware, software, and overall system configuration. Check wit
Turbo Boost Technology. See www.intel.com/technology/turboboost/ for more information.

Enabling Execute Disable Bit functionality requires a PC with a processor with Execute Disable Bit capability and a supporting operating sys
system delivers Execute Disable Bit functionality.

Intel® Virtualization Technology requires a computer system with a processor, chipset, BIOS, virtual machine monitor (VMM) and for some
performance or other benefit will vary depending on hardware and software configurations. Intel Virtualization Technology-enabled VMM ap

System and Maximum TDP is based on worst case scenarios. Actual TDP may be lower if not all I/Os for chipsets are used.

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information herein is provided "as-is" and Intel does not make any representations or warranties whatsoever regarding accuracy of the infor
compatibility of the products listed. Please contact system vendor for more information on specific products or systems.

Low Halogen: Applies only to brominated and chlorinated flame retardants (BFRs/CFRs) and PVC in the final product. Intel components as
JS-709 requirements, and the PCB / substrate meet IEC 61249-2-21 requirements. The replacement of halogenated flame retardants and/c

Some products can support AES New Instructions with a Processor Configuration update, in particular, i7-2630QM/i7-2635QM, i7-2670QM/
contact OEM for the BIOS that includes the latest Processor configuration update.

Corporation

Intel® Pentium® M Processor LV 738 (2M Cache, 1.40 GHz, 400 MHz FSB)

SP CIFIC I S

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Intel® Pentium® M Processor LV 738 (2M Cache, 1.40 GHz, 400 MHz FSB) uFCBG P -Free SLI, ra

Socket	Step	Step P	rderin Code	Spec Code	V -	CC	CC S	S H S	CP
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Intel® Pentium® M Processor LV 738 (2M Cache, 1.40 GHz, 400 MHz FSB) uFCBG P -Free SLI, ra

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Intel® Pentium® M Processor LV 738 (2M Cache, 1.40 GHz, 400 MHz FSB) uFCBG , ra

Socket	Step	Step P	rderin Code	Spec Code	V -	CC	CC S	S H S	CP
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H per- hreadin echnolo (H echnolo) re uires a computer s stem ith an Intel® processor supportin H echnolo and an H echnolo ena led chipset, BI S and operatin s stem. Per ormance ill ar dependin on the speci ic hard are and so t are ou use. See .intel.com/products/ht/h perthreadin _more.htm or more in ormation includin details on hich processors support H echnolo .

64- it computin on Intel® architecture re uires a computer s stem ith a processor, chipset, BI S, operatin s stem, de ice dri ers and applications ena led or Intel® 64 architecture. Processors ill not operate (includin 32- it operation) ithout an Intel 64 architecture-ena led BI S. Per ormance ill ar dependin on our hard are and so t are con i urations. Consult ith our s stem endor or more in ormation.

Ma ur o Fre uenc re ers to the ma imum sin le-core re uenc that can e achie ed ith Intel® ur o Boost echnolo , hich re uires a PC ith a processor ith Intel ur o Boost echnolo capa ilit . Intel ur o Boost echnolo per ormance aries dependin on hard are, so t are, and o erall s stem con i uration. Check ith our PC manu acturer on hether our s stem deli ers Intel ur o Boost echnolo . See .intel.com/technolo /tur o oost/ or more in ormation.

na lin ecute isa le Bit unctionalit re uires a PC ith a processor ith ecute isa le Bit capa ilit and a supportin operatin s stem. Check ith our PC manu acturer on hether our s stem deli ers ecute isa le Bit unctionalit .

Intel® Virtualization echnolo re uires a computer s stem ith a processor, chipset, BI S, irtual machine monitor (VMM) and or some uses, certain plat orm so t are, ena led or it. Functionalit , per ormance or other ene it ill ar dependin on hard are and so t are con i urations. Intel Virtualization echnolo -ena led VMM applications are currentl in de elopment.

S stem and Ma imum P is ased on orst case scenarios. ctual P ma e lo er i not all I/ s or chipsets are used.

ll in ormation pro ided is su ect to chan e at an time, ithout notice. Intel ma make chan es to manu acturin li e c cle, speci ications, and product descriptions at an time, ithout notice. he in ormation herein is pro ided as-is and Intel does not make an representations or arranties hatsoe er re ardin accurac o the in ormation, nor on the product eatures, a aila ilit , unctionalit , or compati ilit o the products listed. Please contact s stem endor or more in ormation on speci ic products or s stems.

Lo Halo en pplies onl to rominated and chlorinated lame retardants (BF s/CF s) and PVC in the inal product. Intel components as ell as purchased components on the inished assem l meet S-70 re uirements, and the PCB / su strate meet I C 6124 -2-21 re uirements. he replacement o halo enated lame retardants and/or PVC ma not e etter or the en ironment.

Some products can support S e Instructions ith a Processor Con i uration update, in particular, i7-2630 M/i7-263 M, i7-2670 M/i7-267 M, i -2430M/i -243 M, i -2410M/i -241 M. Please contact M or the BI S that includes the latest Processor con i uration update.

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