Radiation Hardened Adjustable Positive Voltage Regulator

**HS-117RH, HS-117EH**

The Radiation Hardened HS-117RH, HS-117EH are adjustable positive voltage linear regulator capable of operating with input voltages up to 40VDC. The output voltage is adjustable from 1.2V to 37V with two external resistors. The device is capable of sourcing from 5mA to 1.25A\textsubscript{PEAK} (0.5A\textsubscript{PEAK} for the TO-39 package). Protection is provided by the on-chip thermal shutdown and output current limiting circuitry.

The Intersil HS-117RH, HS-117EH has advantages over other industry standard types, in that circuitry is incorporated to minimize the effects of radiation and temperature on device stability.

Constructed with the Intersil dielectrically isolated Rad Hard Silicon Gate (RSG) process, the HS-117RH, HS-117EH are immune to single event latch-up and has been specifically designed to provide highly reliable performance in harsh radiation environments.

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency (DLA). The SMD numbers listed here must be used when ordering.

Detailed electrical specifications for the HS-117RH, HS-117EH are contained in SMD 5962-99547. A “hot-link” is provided on our website for downloading.

**Features**

- Electrically Screened to DLA SMD # 5962-99547
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Environment
  - 300 krad (Si) (Max)
  - Latch-up Immune
- Superior Temperature Stability
- Overcurrent and Overtemperature Protection

**Applications**

- Adjustable Linear Voltage Regulators
- Adjustable Linear Current Regulator

**Pin Configurations**

**HS2-117RH**

(TO-39 CAN)

BOTTOM VIEW

1 - ADJUST
2 - IN
3 - OUT

**HSYE-117RH**

(SMD.5 CLCC)

BOTTOM VIEW

1 - ADJUST
2 - IN
3 - OUT

**HS9S-117RH**

(TO-257AA FLANGE MOUNT)

TOP VIEW

1 - ADJUST
2 - OUT
3 - IN

**NOTE:** No current JEDEC outline for the SMD.5 package. Refer to SMD for package dimensions. The TO-257 is a totally isolated metal package.

September 4, 2012

FN4560.9
## Ordering Information

<table>
<thead>
<tr>
<th>ORDERING NUMBER</th>
<th>INTERNAL MKT. NUMBER</th>
<th>TEMP. RANGE (°C)</th>
<th>PACKAGE</th>
<th>PKG DWG. #</th>
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<tbody>
<tr>
<td>5962F9954702VUC</td>
<td>HS2-117EH-Q</td>
<td>-55 to +125</td>
<td>3 LD METAL CAN</td>
<td>T3.C</td>
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<td>DIE</td>
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<tr>
<td>5962F9954702VXC</td>
<td>HS9S-117EH-Q</td>
<td>-55 to +125</td>
<td>3 LD TO-257</td>
<td>T3.D</td>
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<td>-55 to +125</td>
<td>3 PAD LCC</td>
<td>J3.A</td>
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</tbody>
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**NOTE:**
1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
Die Characteristics

DIE DIMENSIONS
2616mm x 2794mm (103 mils x 110 mils)
483mm ±25.4mm (19 mils ±1 mil)

INTERFACE MATERIALS

Glassivation
Type: Silox (SiO₂)
Thickness: 8.0kÅ ±1.0kÅ

Top Metallization
Type: AlSiCu
Thickness: 16.0kÅ ±2kÅ

Substrate
Radiation Hardened Silicon Gate,
Dielectric Isolation

Backside Finish
Gold

ASSEMBLY RELATED INFORMATION

Substrate Potential
Unbiased (DI)

ADDITIONAL INFORMATION

Worst Case Current Density
<2.0 x 10⁵ A/cm²

Transistor Count
95

Metallization Mask Layout

For additional products, see www.intersil.com/product_tree

Intersil products are manufactured, assembled and tested utilizing ISO9000 quality systems as noted
in the quality certifications found at www.intersil.com/design/quality

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