TLE8209-4SA

SPI Programmable H-Bridge

Automotive Power

Never stop thinking

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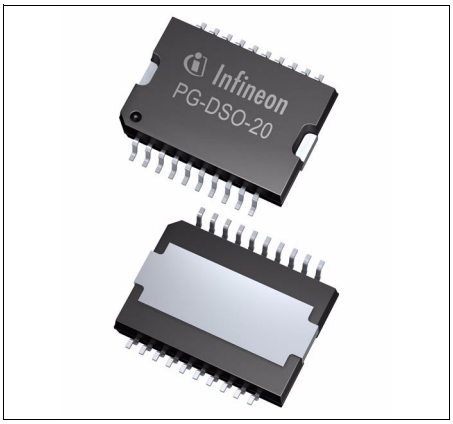
1 Overview



PG-DSO-20-65

Features

- Programmable current limitation from 1.8 to 10.6 A typ.
- Full path R_{DSon} of 240 mΩ (typ. at Tj=25°C)
- Operating battery supply voltage 4.5 V to 28 V
- Operating logic supply voltage 4.4 to 5.25 V
- Low standby current (8 µA typ.)
- Logic inputs TTL/CMOS-compatible
- All I/O pins overvoltage tolerant up to 18 V
- Enable and disable input
- Short circuit and overtemperature protection
- V_S undervoltage protection
- V_{DD} over and undervoltage protection
- Open load detection in off condition
- Temperature dependent current reduction
- Extensive diagnosis capabilities via SPI interface
- Status Flag for basic diagnosis without SPI
- Configurable as H-bridge or two independent half bridges
- Control of power stages by parallel inputs or via SPI
- Output switching frequency up to 11 kHz
- Slewrate programmable through SPI
- Excellent EMC performance
- AEC qualified
- Green product (RoHS compliant)

Functional Description

The TLE8209-4SA is a SPI programmable H-bridge, designed for the control of DC motors in safety critical automotive applications. It features four selectable current ranges, two selectable slew rate settings and extensive diagnosis via SPI. The device monitors the digital supply voltage V_{DD} and shuts down the output stages in case of V_{DD} over- or undervoltage, thus providing a safe switch off path in case of malfunction of the digital control circuitry.

In order to reduce power dissipation in extreme thermal conditions the current limitation threshold is reduced linearly for junction temperatures over 165°C. A thermal warning bit is set in the SPI.

The two half bridges can also be used independently to drive two separate loads like solenoids or unidirectional DC motors.

Type	Package	Body Width	Marking
TLE8209-4SA	PG-DSO-20-65	430 mil	TLE8209-4SA

2 Pin Configuration

2.1 Pin Assignment

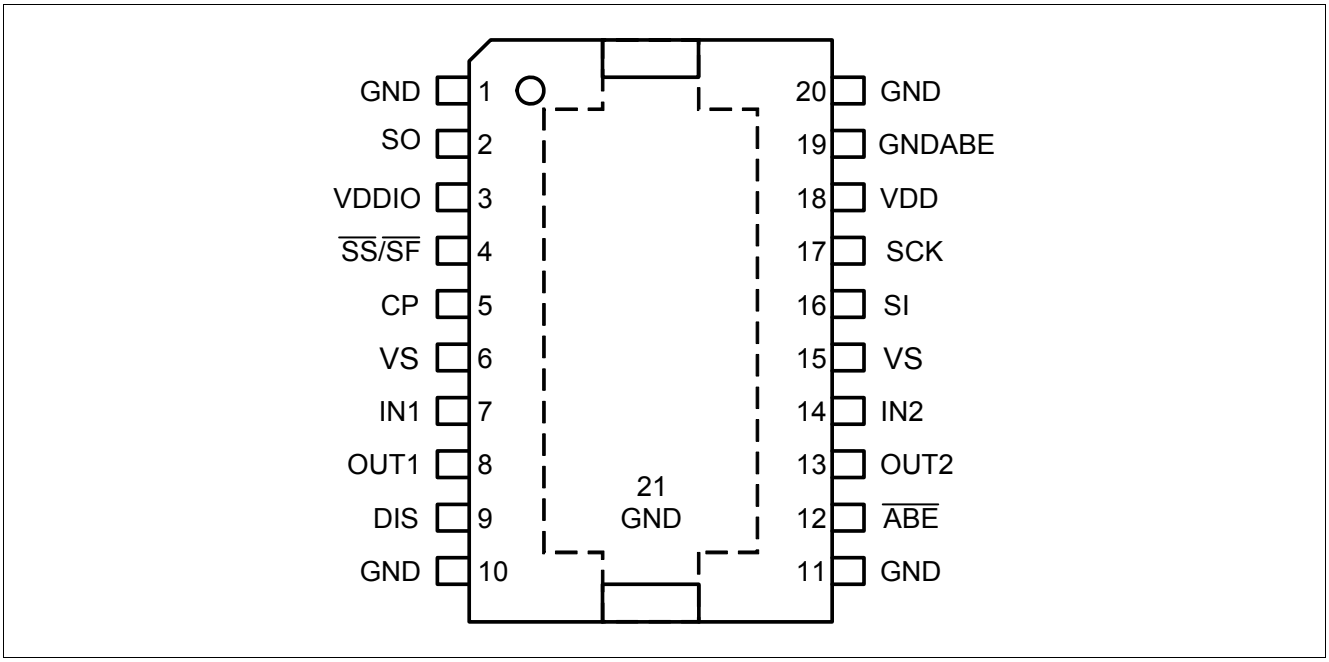


Figure 1 Pinout TLE8209-4SA

2.2 Pin Definitions and Functions

Pin	Symbol	Function in SPI Mode	Function in Status Flag Mode
1	GND	Ground	Ground
2	SO	SPI Serial Data Out	no function - connect to GND
3	VDDIO	Supply Voltage for Logic Output Buffer	Switches to SF-mode if connected to GND
4	$\overline{SS}/\overline{SF}$	Slave Select (low active)	Status Flag (low active)
5	CP	Pin for external Charge Pump Capacitor	Pin for external Charge Pump Capacitor
6	VS	Battery Supply Voltage, has to be connected to pin 15	Battery Supply Voltage, has to be connected to pin 15
7	IN1	Input 1	Input 1
8	OUT1	Output 1	Output 1
9	DIS	Disable	Disable
10	GND	Ground	Ground
11	GND	Ground	Ground
12	$\overline{ABE}$	Bidirectional Enable Pin	Bidirectional Enable Pin
13	OUT2	Output 2	Output 2
14	IN2	Input 2	Input 2
15	VS	Input battery supply voltage, has to be connected to pin 6	Input battery supply voltage, has to be connected to pin 6
16	SI	SPI Serial Data Input	no function - connect to GND

Pin	Symbol	Function in SPI Mode	Function in Status Flag Mode
17	SCK	SPI Clock	no function - connect to GND
18	VDD	V_{DD} supply	V_{DD} supply
19	GNDABE	Sense ground for V_{DD} monitoring	Sense ground for V_{DD} monitoring
20	GND	Ground	Ground
21	GND	Heatslug - connect to GND	Heatslug - connect to GND

2.3 Terms

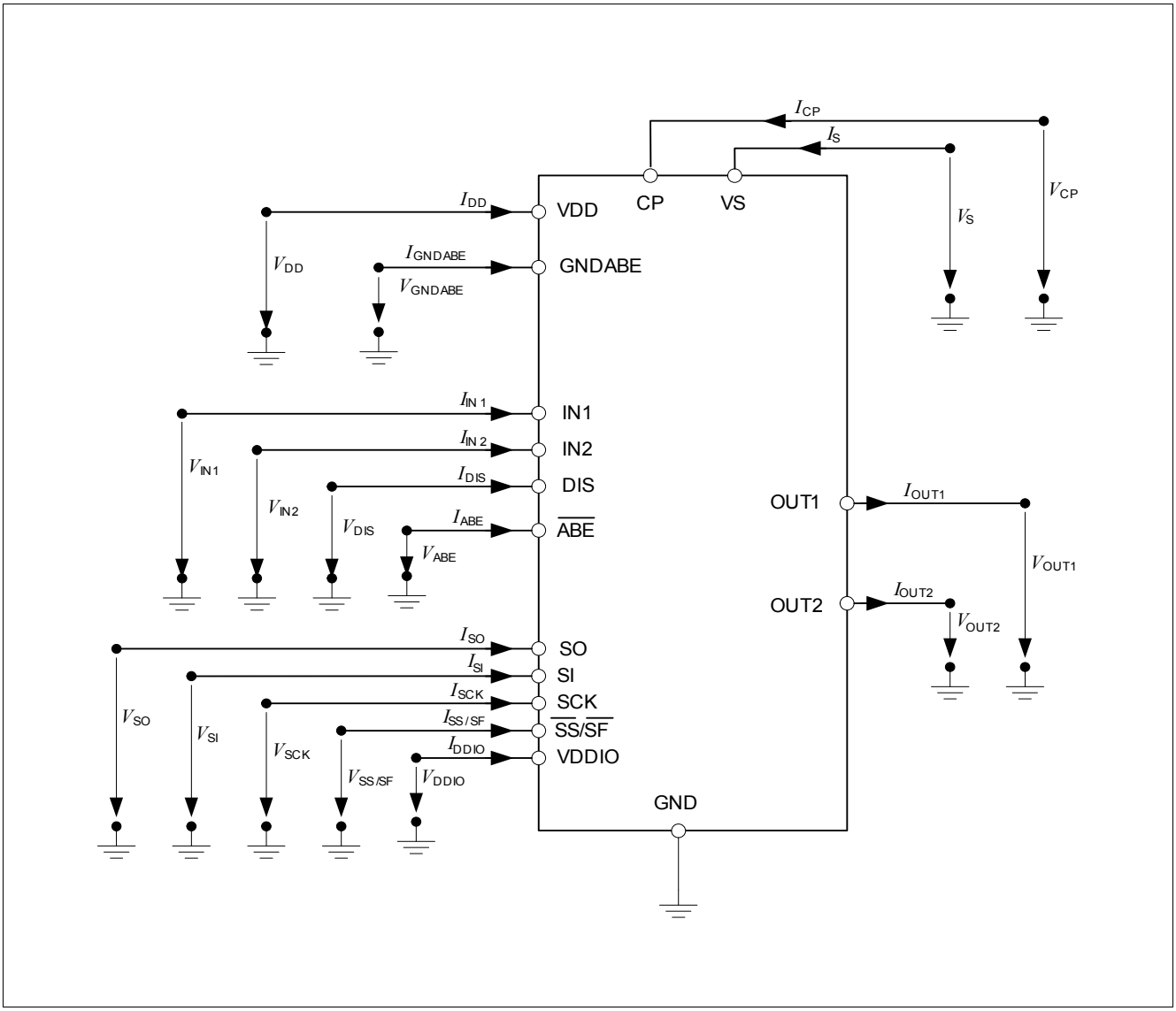


Figure 2 Terms TLE8209-4SA

3 Block Diagram

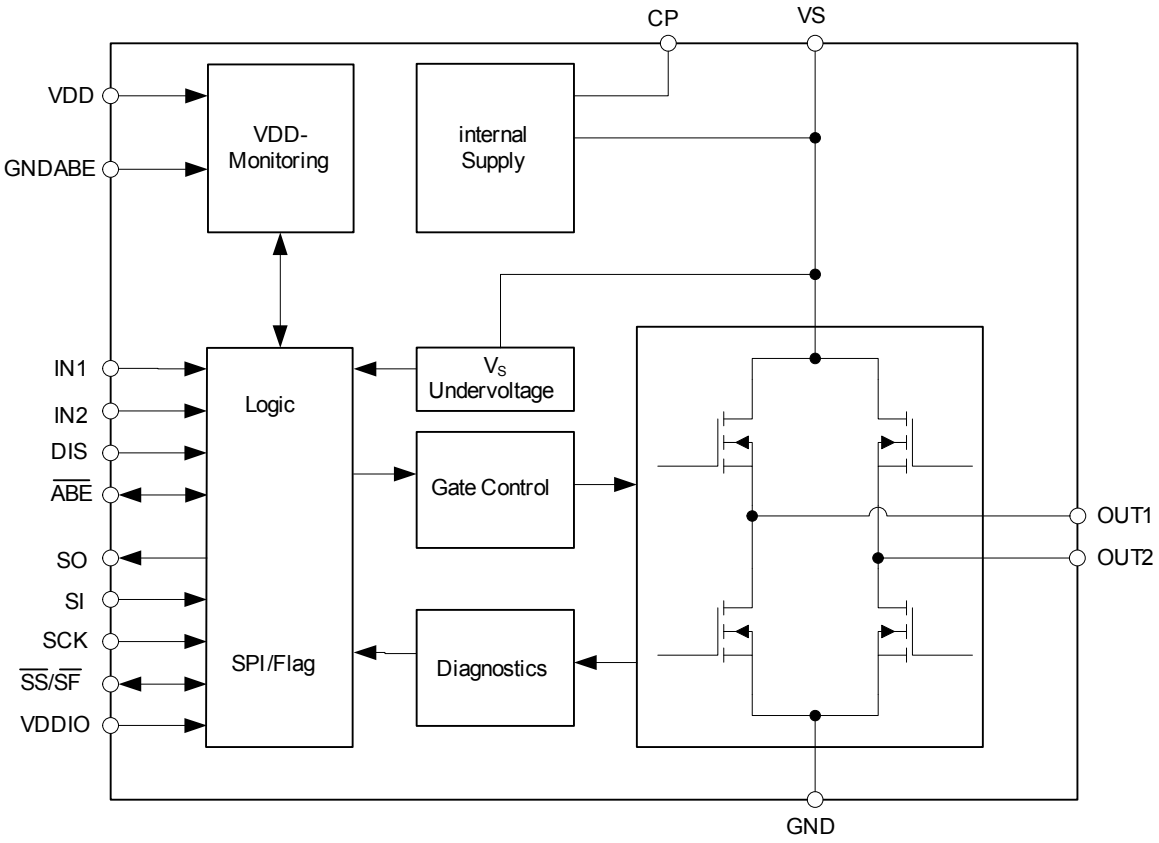


Figure 3 Block Diagram TLE8209-4SA

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 ·C to 150 ·C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Test Conditions / Comment
			Min.	Max.		
4.1.1	Junction temperature	T_j	-40 150	150 175	°C	– 100h cumulative
4.1.2	Storage temperature	T_s	-55	150	°C	–
4.1.3	Ambient temperature	T_a	-40	125	°C	–
4.1.4	Battery supply voltage	V_S	-0.5	40	V	Static destruction proof
			-2	40	V	Dynamic destruction proof t < 0.5 s (single pulse, T_{jstart} < 85 °C)
4.1.5	Logic supply voltage	V_{DD}	-0.5	18	V	–
4.1.6	Supply for logic out	V_{DDIO}	-0.5	18	V	–
4.1.7	Voltage at logic pins $\overline{ABE}$, IN1, IN2, DIS, SCK, $\overline{SS/SF}$, SI	V_{IN}	-0.5	18	V	–
4.1.8	Voltage at SO	V_{SO}	-0.5	V_{DDIO} +0.3	V	–
4.1.9	Voltage at CP	V_{CP}	V_S-0.3	V_S+5.0	V	0V < V_S < 40V
4.1.10	Voltage at GNDABE	V_{GNDABE}	V_{GND}-0.3	V_{GND}+0.3	V	
ESD Susceptibility						
4.1.11	ESD Resistivity to GND	V_{ESD}	-2	2	kV	HBM[2)]
4.1.12			-8	8	kV	HBM[2)], Pins OUT1 and OUT2
4.1.13			-500	500	V	CDM[3)]
4.1.14			-750	750	V	CDM[3)], Pins 1, 10, 11, 20

1) Not subject to production test, specified by design.

2) ESD susceptibility HBM according to EIA/JESD22-A114-B (1.5kΩ, 100pF)

3) ESD susceptibility, Charged Device Model “CDM” EIA/JESD22-C101

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Operating Range

Pos.	Parameter	Symbol	Limit Values		Unit	Remark
			Min.	Max.		
4.2.1	V_S supply voltage range	V_S	4.5	28	V	–
4.2.2	V_{DD} supply voltage	V_{DD}	4.4	5.25	V	–
4.2.3	V_{DDIO} supply voltage	V_{DDIO}	0	5.5	V	–
4.2.4	PWM frequency	f	–	11	kHz	–
4.2.5	Junction temperature	T_J	-40	150	°C	–

Note: Within the operating range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Remark
			Min.	Typ.	Max.		
4.3.6	Junction to Case[1)]	R_{thJC}	–	–	1.6	K/W	–
4.3.7	Junction to Ambient[1)]	R_{thJA}	–	17	–	K/W	[2)]

1) Not subject to production test, specified by design.

2) Simulation according to Jedec JESD51-2,-5,-7; natural convection; FR4 2s2p board 76.2 x 114.3 x 1.5 mm (2 x 70µm Cu, 2 x 35µm Cu)

5 Power Supply

5.1 Basic Supply Characteristics

The TLE8209-4SA has three different supply pins: VDD, VS and VDDIO. VDD is used to supply the internal logic circuitry. VS connects to battery voltage and supplies the output stages. The voltage at pin VDDIO defines the high level output voltage at the pin SO of the SPI interface. VDDIO is also used as a mode select pin. If VDDIO is connected to ground, the device is set to status flag mode (SPI inactive).

On power up the device will enter a functional state when V_{DD} rises above the functional reset threshold V_{DD_RES}. In this state all output stages are inactive and internal registers are cleared. When V_{DD} rises further above the power on reset threshold V_{DD_POR} the device starts operation with a delay time of t_{POR}.

5.2 VDD Monitoring

The logic supply voltage level at the pin VDD is monitored. If the voltage at pin V_{DD} is out of the permissible range of V_{DD_L} ... V_{DD_H} the power stages of TLE8209-4SA are switched off and pin $\overline{ABE}$ is pulled to ground. To suppress glitches in the V_{DD} monitoring, a glitch filter is implemented. V_{DD} is measured with reference to pin GNDABE. The state of VDD monitoring is stored in STATCON_REG and can be read out via SPI.

The output stages can also be turned off by pulling the ABE pin to ground externally.

In case of VDD failure, the output stages are switched off, even if the pin $\overline{ABE}$ should be connected to a high level signal because of external short circuit to VDD or battery voltage (up to 18V). OUT1 and OUT2 cannot be switched on in over- or undervoltage condition, switching off is always possible. A power on reset ($V_{DD} < V_{DD_POR}$) switches off all stages without delay.

Control of VDD-monitoring is possible in SPI mode only. Detailed information (differentiation of over and under-voltage detection) is only possible by SPI interface.

Behavior of VDD monitoring in SF mode:

- monitoring is present with the specified values for over- and undervoltage
- any test of over- and undervoltage threshold is not possible
- the latch for overvoltage is disabled

VDD Undervoltage

If the VDD voltage is lower than the supply voltage supervisory lower threshold (V_{DD_THL}), output stages are shut off after a filtering time (t_{FIL_OFF}) and the bi-directional pin $\overline{ABE}$ is pulled low. At the transition from undervoltage to normal voltage the signal at pin ABE goes high and the output stages will return to normal operation after a filtering time (t_{FIL_ON}) has expired. For output control via SPI the bits MUX and SINx in the config register have to be re-programmed. New failures are not stored to diagnostic registers during undervoltage, register content remains valid, writing new information to configuration registers is possible as far as they are not reset by ABE. If VDD falls below the power-on-reset supply voltage (V_{DD_POR}) all stages are shut off and ABE is switched active low. When VDD is rising above the power-on-reset supply voltage threshold (V_{DD_POR}) a power-on-reset is generated (t_{POR}), setting all registers to its default state.

VDD Overvoltage

If the VDD voltage is higher than the supply voltage supervisory upper threshold (V_{DD_THH}), all output stages are shut off after a filtering time (t_{FIL_OFF}) and the bi-directional pin ABE is pulled low. The behavior of the ABE level and output stages on the return of VDD from overvoltage to the correct range is configured in STATCON_REG, bit CONFIG0)

CONFIG0='1': ABE is latched and outputs remain off after overvoltage. Return to normal operation is only possible with power-on reset or by changing this bit via SPI.

CONFIG0=’0’: ABE is inactive after VDD returned to normal operating voltage and filtering time has expired.

At the transition from overvoltage to normal condition, the output stages will return to normal operation. For output control via SPI the bits MUX and SINx in the config register have to be re-programmed. New failures are not stored to diagnostic registers during overvoltage, register content remains valid, writing new information to configure registers is possible as far as they are not reset by ABE.

VDD Monitoring Test Mode

Testing of VDD monitoring is possible in SPI mode only. The latch function for over voltage at VDD has to be switched of (CONFIG0=0 in STATCON_REG)

Testing upper threshold:

By writing 00xxxxxxb into STATCON_REG, the overvoltage threshold is reduced to VDD_TEST_H. STATCON_REG bit 2 and 0 have to be LOW then. After writing 1xxxxxxxb to STATCON_REG, bit 2 and 0 in STATCON_REG must be HIGH again

Testing lower threshold:

By writing 01xxxxxxb into STATCON_REG, the undervoltage threshold is increased to VDD_TEST_L. STATCON_REG bit 2 and 1 have to be LOW then. After writing 1xxxxxxxb to STATCON_REG, bit 2 and 1 in STATCON_REG must be HIGH again.

5.3 VDDIO - Digital Output Supply and Diagnostic Mode Selection

The voltage at V_{DDIO} is used to supply the output buffer at the SO pin (serial output of SPI-interface). The VDDIO pin is also used to select SPI- or in status flag (SF) diagnostic mode. As soon as V_{DDIO} is lower than V_{DDIO_L}, the device is put into status flag mode.

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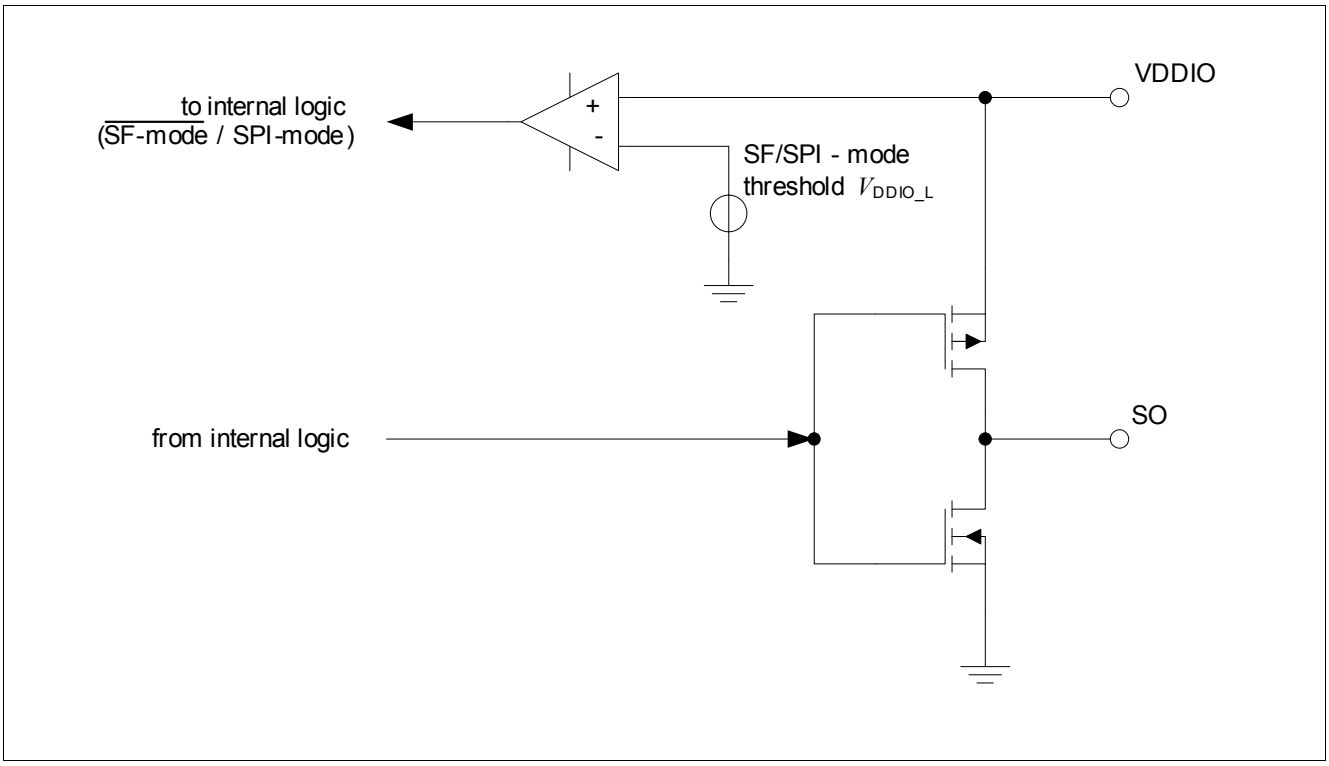


Figure 4 V_{DDIO} and SO-Pin

5.4 Electrical Characteristics Power Supply and V_{DD}-Monitoring

Electrical Characteristics: Power Supply and V_{DD}-Monitoring

V_S = 5 V to 28 V; V_{DD} = 5.0 V, T_j = -40 ·C to 150 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Supply							
5.4.1	Supply Current	I_{VS}	–	8	20	µA	I_{OUT} = 0 A, V_{DD} = 0V, V_S < 18 V, T_j < 125°C
			–	2.1	4	mA	bridge disabled, I_{OUT} = 0 A, 5 V < V_S < 18 V
			–	2.5	5	mA	f = 2 kHz, I_{OUT} = 0 A, 5 V < V_S < 18 V
			–	4	9	mA	f = 10 kHz, I_{OUT} = 0 A, 5 V < V_S < 18 V
			–	4.8	13	mA	f = 10 kHz, I_{OUT} = 0 A, 5 V < V_S < 28 V
5.4.2	Functional Reset Threshold	V_{DD_RES}	–	1.4	2.5	V	–
5.4.3	Power On Reset Threshold	V_{DD_POR}	3.5	3.75	4.0	V	–
5.4.4	Power On Reset Delay Time	t_{POR}	–	0.22	0.5	ms	V_{DD} = on --> output stage active, no load
5.4.5	VDD Input current	I_{DD}	–	7	9	mA	4.5V < V_{DD} < 5.5V
5.4.6	VDDIO Input current	I_{DDIO}	–	30	100	µA	SPI-mode no load at SO no SPI communication
5.4.7	SF-mode Threshold	V_{DDIO_L}	–	–	1.0	V	–
5.4.8	SPI-mode Threshold	V_{DDIO_H}	2.0	–	–	V	–
5.4.9	Mode selection hysteresis	V_{DDIO_HYS}	0.2	0.5	1.0	V	–
V_{DD}-Monitoring							
5.4.10	Overvoltage threshold	V_{DD_THH}	5.25	5.4	5.5	V	Voltage referred to GNDABE
5.4.11	Undervoltage threshold	V_{DD_THL}	4.2	4.3	4.4	V	
5.4.12	Test mode reduced Overvoltage threshold	$V_{DD_TEST_H}$	4.2	4.3	4.4	V	
5.4.13	Test mode increased Undervoltage threshold	$V_{DD_TEST_L}$	5.25	5.4	5.5	V	
5.4.14	Filter time for glitch suppression	t_{FIL}	60	100	135	µs	–
5.4.15	Maximum Slew Rate on VDD[1)]	V_{DD_slew}	–	–	0.5	V/µs	–

1) Not subject to production test; specified by design

6 Logic Inputs and Outputs

The threshold specifications for the logic inputs are compatible to both 5 and 3.3 V standard CMOS micro-controller ports. All inputs (except $\overline{ABE}$) feature internal pull-up current sources. The logic output SO is supplied by V_{DDIO}. V_{DDIO} can be supplied with either 5 or 3.3 V, so the output thresholds of SO can be configured to the required I/O voltage.

Electrical Characteristics: Control Inputs

V_S = 5 V to 28 V; V_{DD} = 5.0 V; T_j = -40 ·C to 150 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
IN1, IN2							
6.0.1	Low level	V_{INx_L}	-0.3	–	1.0	V	–
6.0.2	High level	V_{INx_H}	2.0	–	V_{DD}+0.3	V	–
6.0.3	Hysteresis	V_{INx_HYS}	0.2	–	1.0	V	–
6.0.4	Input Current (Pull Up)	I_{INx}	-30	-20	-10	µA	0 V < V_{INx} < 2.1 V
6.0.5			0	2	5	µA	V_{INx} > 3.0 V
6.0.6	Input Capacity[1]	C_{INx}	–	–	20	pF	[2]
DIS							
6.0.7	Low level	V_{DIS_L}	-0.3	–	1.0	V	–
6.0.8	High level	V_{DIS_H}	2.0	–	V_{DD}+0.3	V	–
6.0.9	Hysteresis	V_{DIS_HYS}	0.2	–	1.0	V	–
6.0.10	Input Current (Pull Up)	I_{DIS}	-200	-125	-50	µA	0 V < V_{DIS}< 2.1 V
6.0.11			0	2	5	µA	V_{DIS} > 3.0 V
6.0.12	Input Capacity[1]	C_{DIS}	–	–	20	pF	[2]
6.0.13	Minimum Pulse Width[1]	t_{DIS}	0.4	0.8	1.5	µs	–
$\overline{ABE}$							
6.0.14	Output low-level voltage	V_{ABE_OUTL}	–	–	1.2	V	V_{DD_THH} < V_{DD} < 18 V I_{ABE} < 5 mA
6.0.15			–	–	1.0	V	2.5 V < V_{DD} < V_{DD_THL} I_{ABE} < 1 mA
6.0.16	Input threshold high	V_{ABE_INH}	0.7*V_{DD}	–	–	V	–
6.0.17	Input threshold low	V_{ABE_INL}	–	–	0.3*V_{DD}	V	–
6.0.18	Hysteresis	V_{ABE_INHY}	0.2	–	1.0	V	–
6.0.19	Minimum pulse width[1]	t_{ABE}	0.4	0.8	1.5	µs	–
6.0.20	$\overline{ABE}$ Input current (Pull Down)	$-I_{ABE_L}$	20	40	120	µA	1.5 V < V_{ABE} < 18 V
6.0.21			0	–	60	µA	0 V < V_{ABE} < 1.5 V
SI							
6.0.22	Low level	V_{SI_L}	-0.3	–	1.0	V	–
6.0.23	High level	V_{SI_H}	2.0	–	V_{DD}+0.3	V	–
6.0.24	Hysteresis	V_{SI_HYS}	0.2	–	1.0	V	–
6.0.25	Input Current (Pull Up)	I_{SI}	-30	-20	-10	µA	0 V < V_{SI} < 2.1 V
6.0.26	Input Capacity[1]	C_{SI}			14	pF	[2]

Electrical Characteristics: Control Inputs (cont'd)

V_S = 5 V to 28 V; V_{DD} = 5.0 V; T_j = -40 ·C to 150 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
SCK							
6.0.27	Low level	V_{SCK_L}	-0.3	–	1.0	V	–
6.0.28	High level	V_{SCK_H}	2.0	–	V_{DD}+0.3	V	–
6.0.29	Hysteresis	V_{SCK_HYS}	0.2	–	1.0	V	–
6.0.30	Input Current (Pull Up)	I_{SCK}	-30	-20	-10	µA	0 V < V_{SCK} < 2.1 V
6.0.31	Input Capacity[1)]	C_{SCK}	–	–	14	pF	[2)]
SS/SF							
6.0.32	Low level	V_{SS_L}	-0.3	–	1.0	V	–
6.0.33	High level	V_{SS_H}	2.0	–	V_{DD}+0.3	V	–
6.0.34	Hysteresis	V_{SS_HYS}	0.2	–	1.0	V	–
6.0.35	Input Current in SPI mode (Pull Up)	I_{SS}	-30	-20	-10	µA	0 V < V_{SS} < 2.1 V
6.0.36			-30	–	5	µA	2.1 V < V_{SS} < 3.0 V
6.0.37			0	2	5	µA	V_{SS} > 3.0 V
6.0.38	Input Current in SF mode (Open Drain)	I_{SF}	0	2	5	µA	V_{SF} = 5.0 V, SF inactive
6.0.39			300	–	–	µA	V_{SF} = 1.0 V, SF active
6.0.40	Input Capacity[1)]	C_{SS}	–	–	15	pF	[2)]
SO							
6.0.41	Low level	V_{SO_L}	0.0	–	0.4	V	I_{SO} = 2 mA
6.0.42	High level	V_{SO_H}	V_{DDIO}-0.75	–	V_{DDIO}	V	I_{SO} = -2 mA 2.9 V < V_{DDIO} < 5.5 V
6.0.43	Output capacitance[1)]	C_{SO}	–	–	19	pF	In tristate[2)]
6.0.44	Leakage current	I_{SO}	-2	–	2	µA	In tristate 0 < V_{SO} < V_{DDIO}

1) Not subject to production test; specified by design

2) V_{bias} = 2 V; V_{test} = 20 mVpp; f = 1 MHz

7 Power Stages

The TLE8209-4SA contains four n-channel power-DMOS transistors that can be used in an H-bridge or in dual half bridge configuration.

Integrated circuits protect the outputs against overcurrent and over-temperature, in case of short-circuit to ground, to the supply voltage or across the load. Positive and negative voltage spikes, which occur when switching inductive loads, are limited by integrated freewheeling diodes (body diodes of power-DMOS).

7.1 Parallel or SPI Control

By default the setting of the power switches is controlled by the Inputs IN1, IN2 (parallel control). The outputs OUT1 and OUT2 are set to High (high-side switch ON, low-side switch OFF) or Low (high-side switch OFF, low-side switch ON) by the parallel inputs IN1 and IN2, respectively. In SPI mode there is also the option to control the outputs via the SPI bits SIN1 and SIN2 of the SPI configuration register. To switch to SPI control the bit MUX has to be set to ’0’.

In addition, the outputs can be disabled (set to tristate, high- and low-side switch OFF) by the disable input DIS and the bidirectional reset pin $\overline{\text{ABE}}$. Disabling sets the device to parallel control

Table 1 shows the different options for the output control.

7.2 H-Bridge or Single Switch Usage

The IC can be set to H-bridge mode or single-switch mode by SPI. This setting changes the behavior of the device in the following features:

- current limiting
- overcurrent shut-down
- open load diagnosis

Table 1 Functional Truth Table

Pos.	DIS	$\overline{\text{ABE}}$	IN1	IN2	SPI MUX	SPI SIN1	SPI SIN2	OUT1	OUT2
Forward, parallel ctrl.	L	H	H	L	1	X	X	H	L
Reverse, parallel ctrl.	L	H	L	H	1	X	X	L	H
Free-wheeling low, parallel ctrl.	L	H	L	L	1	X	X	L	L
Free-wheeling high, parallel ctrl.	L	H	H	H	1	X	X	H	H
Forward, SPI ctrl.	L	H	X	X	0	1	0	H	L
Reverse, SPI ctrl.	L	H	X	X	0	0	1	L	H
Free-wheeling low, SPI ctrl.	L	H	X	X	0	0	0	L	L
Free-wheeling high, SPI ctrl.	L	H	X	X	0	1	1	H	H
Disabled by DIS	H	X	X	X	X	X	X	Z	Z
Disabled by $\overline{\text{ABE}}$	X	L	X	X	X	X	X	Z	Z

Table 2 OUT States

OUT	High-Side DMOS	Low-Side DMOS
H	ON	OFF
L	OFF	ON
Z	OFF	OFF

7.3 Electrical Characteristics Power Stages

Electrical Characteristics: Power Stage

V_S = 5 V to 28 V; V_{DD} = 5.0 V, T_j = -40 ·C to 150 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Power Outputs OUT1, OUT2							
7.3.1	Switch on resistance low side	R_{OUT1L}	–	125	–	mΩ	I_{OUTx} = 3 A; T_j = 25°C
		R_{OUT2L}	–	215	250		I_{OUTx} = 3 A; T_j = 150°C
7.3.2	Switch on resistance high side	R_{OUT1H}	–	115	–	mΩ	I_{OUTx} = 3 A; T_j = 25°C
		R_{OUT2H}	–	200	240		I_{OUTx} = 3 A; T_j = 150°C
7.3.3	Leakage current	$I_{OUT1(off)}$ $I_{OUT2(off)}$	-200	–	200	µA	Output stage switched off V_S = 13 V
7.3.4	Free-wheel diode forward voltage	U_D	–	0.9	1.1	V	I_D = 3 A
7.3.5	Free-wheel diode reverse recovery time[1)]	t_{rr}	–	–	100	ns	–
Output Switching Times - Fast Slew Rate							
7.3.6	Rise time HS	$t_{r\ (HS)}$	3.5	6.0	10	µs	SPI bit SL='0' V_S = 8..18 V; I_{OUT} = 3 A
7.3.7	Fall time HS	$t_{f\ (HS)}$	3.5	6.0	10		
7.3.8	Rise time LS	$t_{r\ (LS)}$	3.5	6.0	8.5		
7.3.9	Fall time LS	$t_{f\ (LS)}$	3.5	6.0	8.5		
Output Switching Times - Slow Slew Rate							
7.3.10	Rise time HS	$t_{r\ (HS)}$	15	30	48	µs	SPI bit SL='1' V_S = 8..18 V; I_{OUT} = 3 A
7.3.11	Fall time HS	$t_{f\ (HS)}$	15	30	48		
7.3.12	Rise time LS	$t_{r\ (LS)}$	18	30	48		
7.3.13	Fall time LS	$t_{f\ (LS)}$	18	30	48		
Output Delay - Parallel Control, Fast Slew Rate							
7.3.14	Output on-delay	t_{don}	–	–	12	µs	V_S = 8..18 V; I_{OUT} = 3 A
7.3.15	Output off-delay	t_{doff}	–	–	7	µs	
Output Delay - SPI Control, Fast Slew Rate							
7.3.16	Output on-delay	t_{don}	–	–	13	µs	V_S = 8..18 V; I_{OUT} = 3 A
7.3.17	Output off-delay	t_{doff}	–	–	12		
Output Delay - Parallel Control, Slow Slew Rate							
7.3.18	Output on-delay	t_{don}	–	–	41	µs	V_S = 8..18 V; I_{OUT} = 3 A
7.3.19	Output off-delay	t_{doff}	–	–	25		
Output Delay - SPI Control, Slow Slew Rate							
7.3.20	Output on-delay	t_{don}	–	–	42	µs	V_S = 8..18 V; I_{OUT} = 3 A
7.3.21	Output off-delay	t_{doff}	–	–	26		

Electrical Characteristics: Power Stage

V_S = 5 V to 28 V; V_{DD} = 5.0 V, T_j = -40 ·C to 150 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Enable and Disable Delay Times							
7.3.22	Disable delay time, fast slew rate	t_{ddis}	–	8	20	µs	V_S = 8..18 V; I_{OUT} = 3 A
7.3.23	Disable delay time, slow slew rate	t_{ddis}	–	38	75		
7.3.24	Enable delay time, fast slew rate	t_{del}	–	8	20		
7.3.25	Enable delay time, slow slew rate	t_{del}	–	38	75		
7.3.26	Power on delay time	t_{del}	–	0.1	0.4	ms	V_S = on --> output stage active, no load

1) Not subject to production test - specified by design

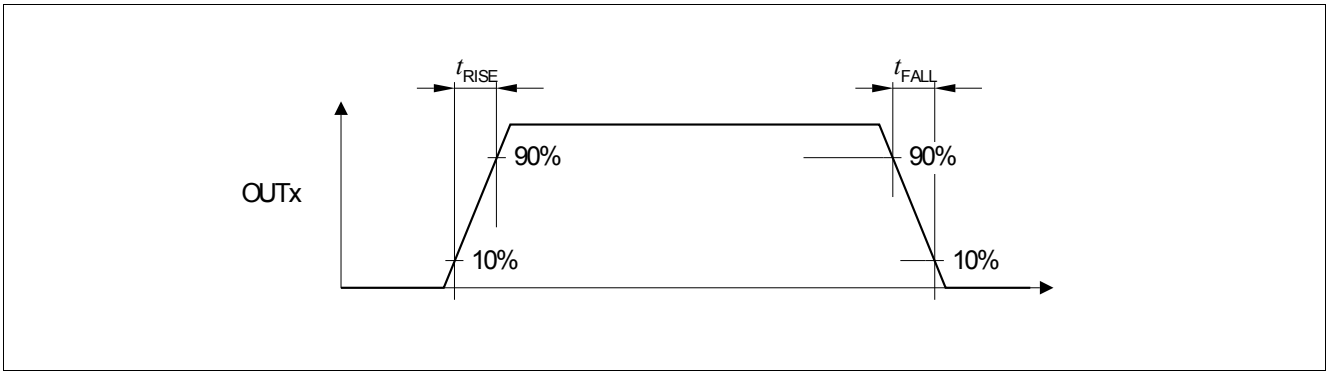


Figure 5 Output Switching Time

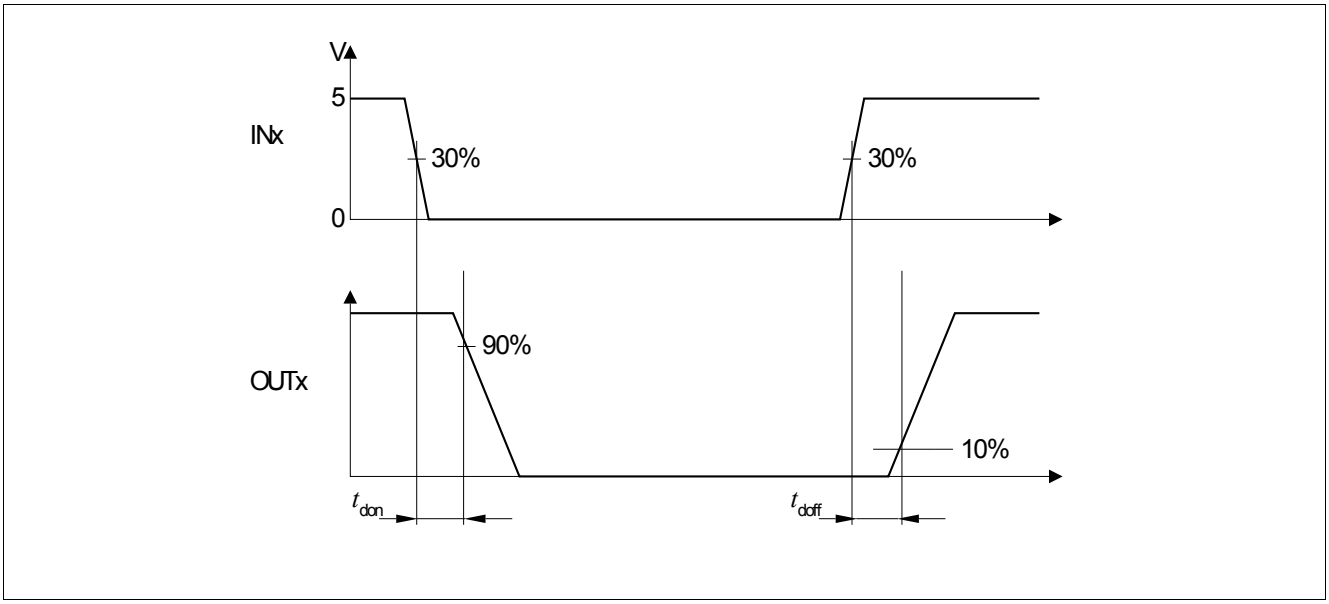


Figure 6 Output Delay Time – Low-Side FETs

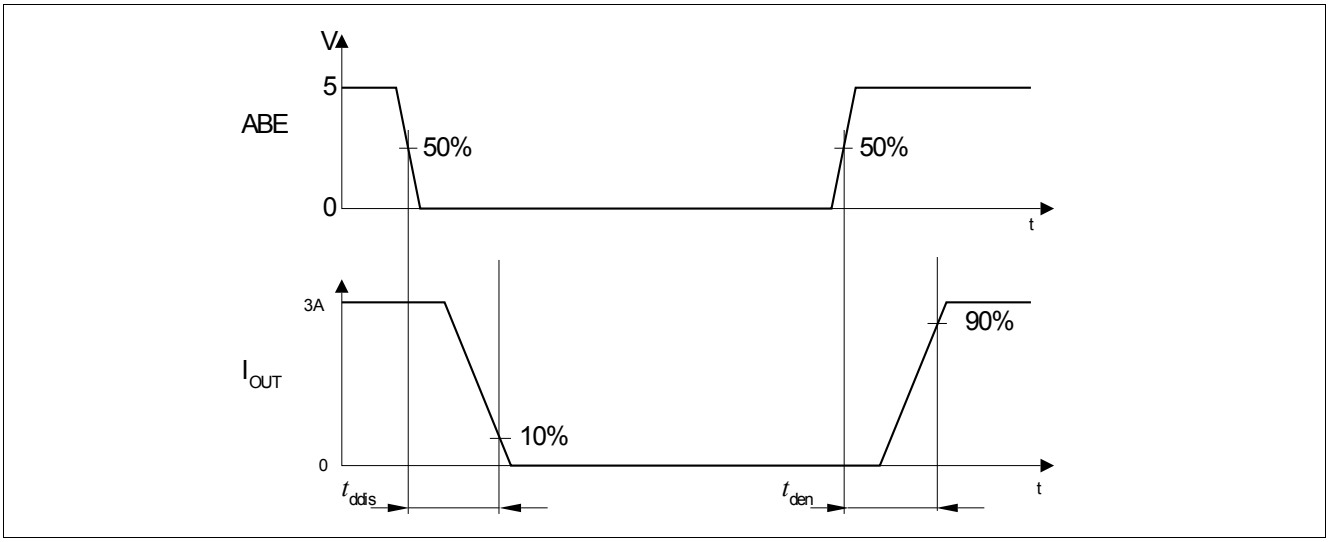


Figure 7 ABE pin - Enable and Disable Delay Time

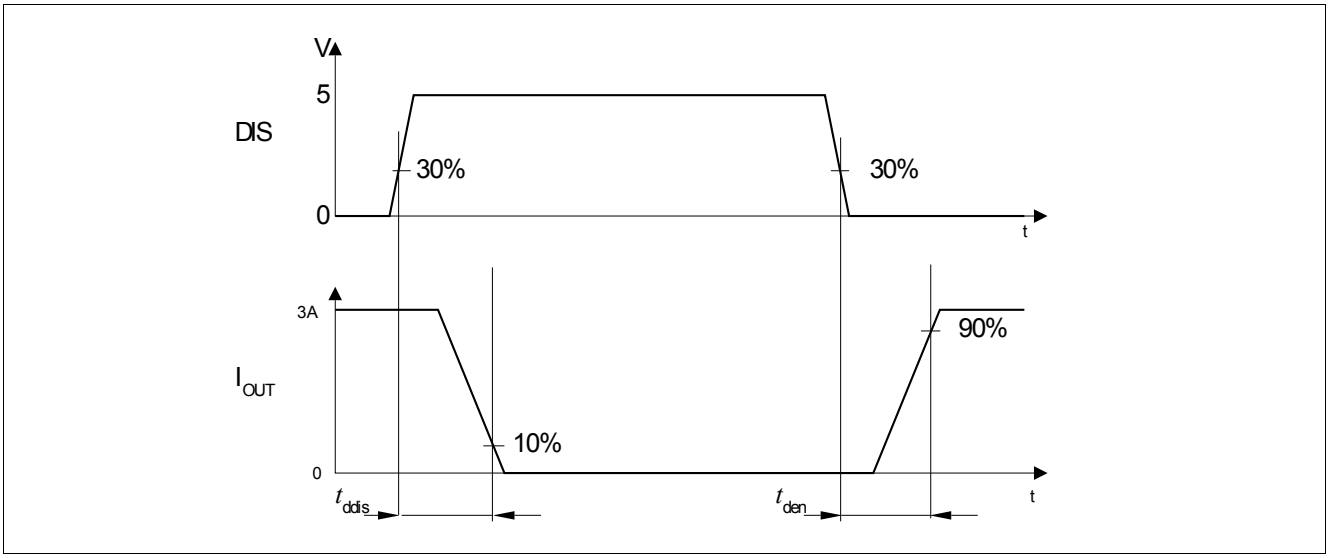


Figure 8 DIS pin - Enable and Disable Delay Time

8 Protection and Monitoring

Both output stages of the TLE8209-4SA are equipped with fault diagnostic functions:

- Short to battery voltage (SCB). Can be detected when low side-switches are turned on
- Short to ground (SCG). Can be detected when high side-switches are turned on
- Open load (OL). Can be detected in inactive mode
- Over-temperature (OT). Can be detected in active and inactive mode
- VDD over- and under voltage (**Chapter 5.2**)
- Battery under voltage detection. Can be detected in active and inactive mode

Individual detection for each output in single switch operation mode (SCB, SCG, OL) is possible. The corresponding diagnostics bits for each failure will be set in the SPI according to **Table 8 “Failure Encoding” on Page 29**.

8.1 Diagnosis in Status Flag Mode

Instead of using the SPI interface for control and diagnosis of the TLE8209-4SA, the device can also be set into status flag mode by connecting pin VDDIO to GND as described in **Chapter 5.3**.

In status flag mode the pin SF will be pulled low in the following cases:

- undervoltage at VS
- bridge disabled by $\overline{\text{ABE}}$ or DIS
- bridge disabled by VDD monitoring
- bridge disabled by short circuit detection
- overtemperature shut down

SF will not be pulled low if V_{DD} is below the power on reset threshold (VDD_POR).

8.2 Current Limitation

To limit the output current at low power loss, a chopper current limitation is integrated. Current measurement for current limitation is done in the high side path. This requires high side freewheeling in case of active current limitation.

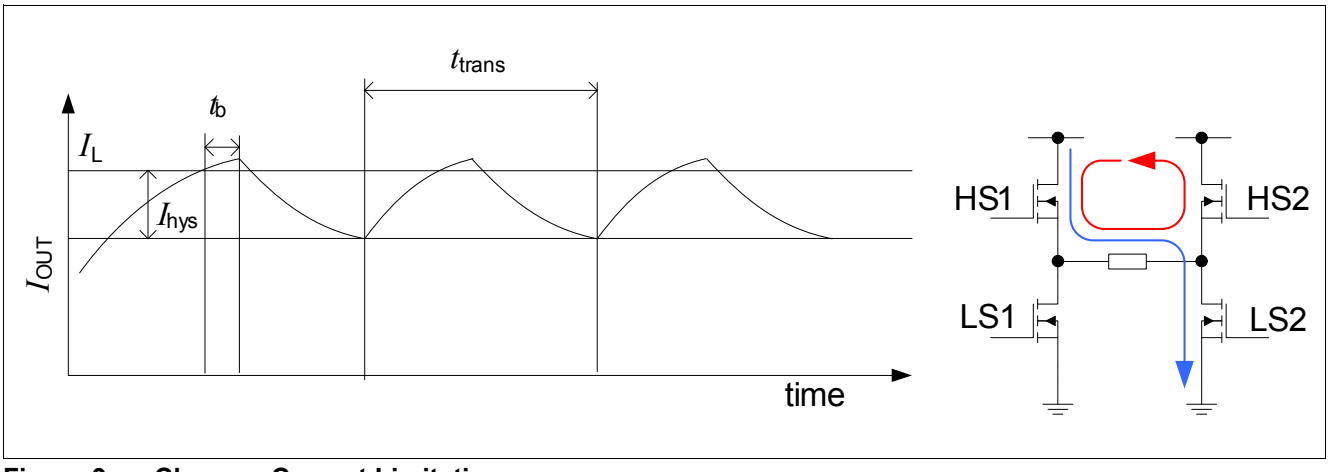


Figure 9 Chopper Current Limitation

Figure 9 shows the behavior of the current limitation for over current detection in HS1. It applies accordingly also for HS2:

When the current in high-side switch of OUT1 (HS1) exceeds the limit I_L longer than the blanking time t_b, OUT2 is switched to high (e.g. LS2->OFF, HS2->ON), independent of the input signal at IN2. This leads to a slow-decay current decrease in the load and in HS1. As soon as the current falls below I_L-I_{hys}, OUT2 is switched back to normal

operation, i.e. the outputs follow the inputs according to the truth table. The current limit I_L can be programmed to four different values by setting the SPI bits CL1 and CL2 in the SPI configuration register. To avoid high chopper frequencies the time between two transients t_{trans} is limited.

Current limitation is available in H-bridge operation mode, not in single switch operation mode. This means, that the current limit, current limit hysteresis and blanking time has no effect in single switch operation mode.

8.3 Temperature Dependent Current Reduction

For $T_{ILR} < T_j < T_{SD}$ the current limit decreases from I_L as set by the SPI to I_{L_TSD} = 2.5 A typ. as shown in **Figure 10**.

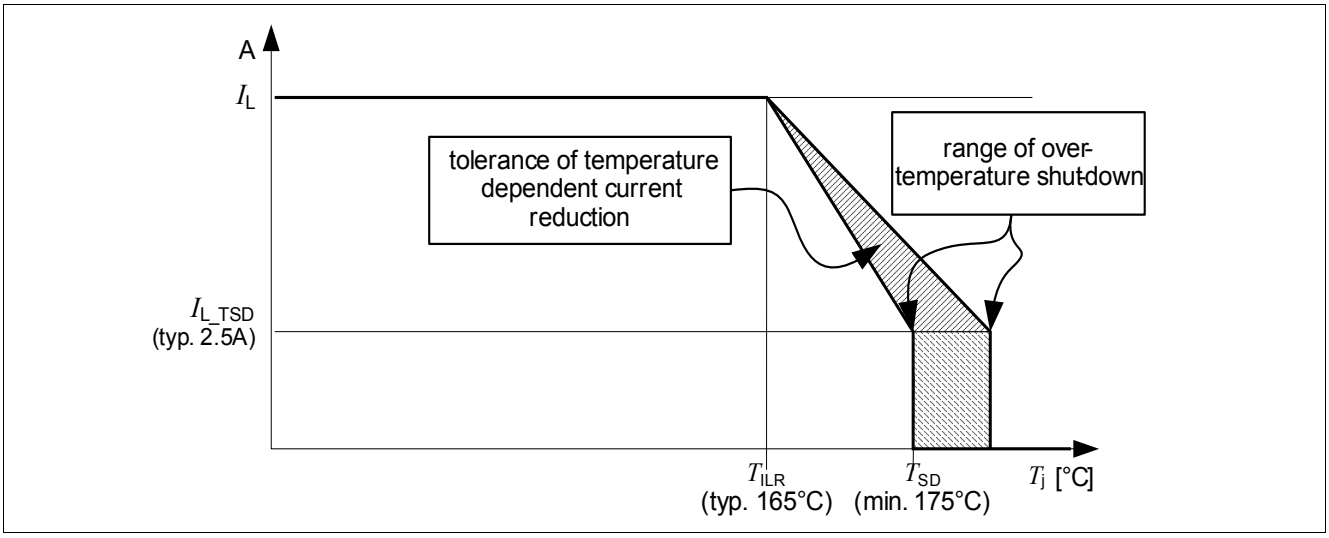


Figure 10 Temperature Dependent Current Reduction

8.4 Short Circuit to Ground

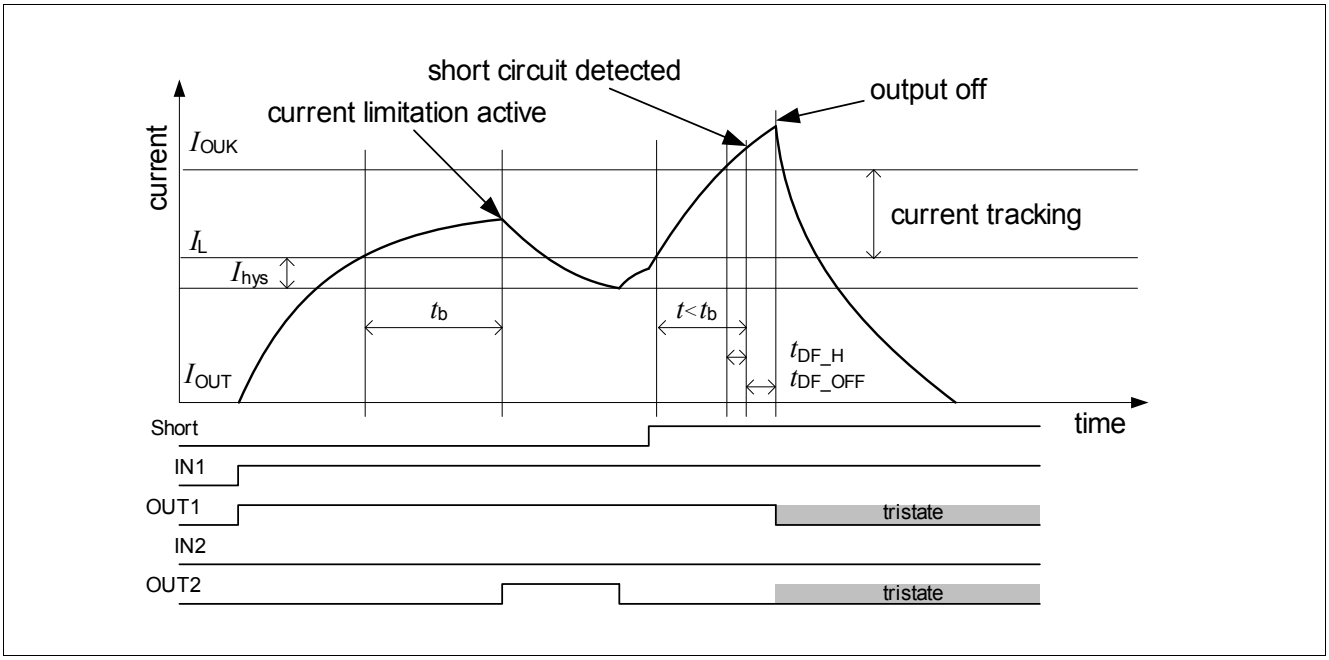


Figure 11 Short to Ground Detection

The short circuit to ground detection is activated when the current through one of the high side switches rises over the threshold I_{OUK} and remains higher than I_{OUK} for at least the filter time t_{DF_H} within the blanking time t_b.

The output stage in which the short circuit was detected will be switched off within t_{DF_OFF}.

In H-bridge mode also the other output will be switched off after a short delay of t_{DF_del} .

In single switch mode only the affected output will be switched off.

8.5 Short Circuit to Battery

A short circuit to battery is detected in the same way as a short circuit to ground, only in the low side switch instead of the high side switch.

8.6 Short Circuit across the Load

Short circuit over load is indicated by two failures - short circuit to ground on one output and short circuit to battery on the other output. Both failure bits will be set in the SPI diagnostics register. Both output stages will be turned off.

8.7 Overtemperature

In case of high DC-currents, insufficient cooling or high ambient temperature, the chip temperature may rise above the thermal shut-down temperature T_{SD} (see **Figure 10**). In that case, all output transistors are turned off.

8.8 Undervoltage Shut-Down

If the supply voltage at the VS pins falls below the undervoltage detection threshold V_{UV_OFF}, the outputs switches are turned off. As soon as V_S rises above V_{UV_ON} again, the device is returning to normal operation.

8.9 Open Load Diagnosis

Open load diagnosis is only possible if outputs are switched off by DIS or $\overline{ABE}$. The diagnostic current sources are deactivated in status flag mode. Diagnostic current sources are disconnected if outputs are active. That means that the diagnostic current sources are also disconnected if the outputs are deactivated due to short circuit. The open load detection in H-bridge mode is different from the open load detection in single switch mode.

Open Load Detection in H-Bridge mode

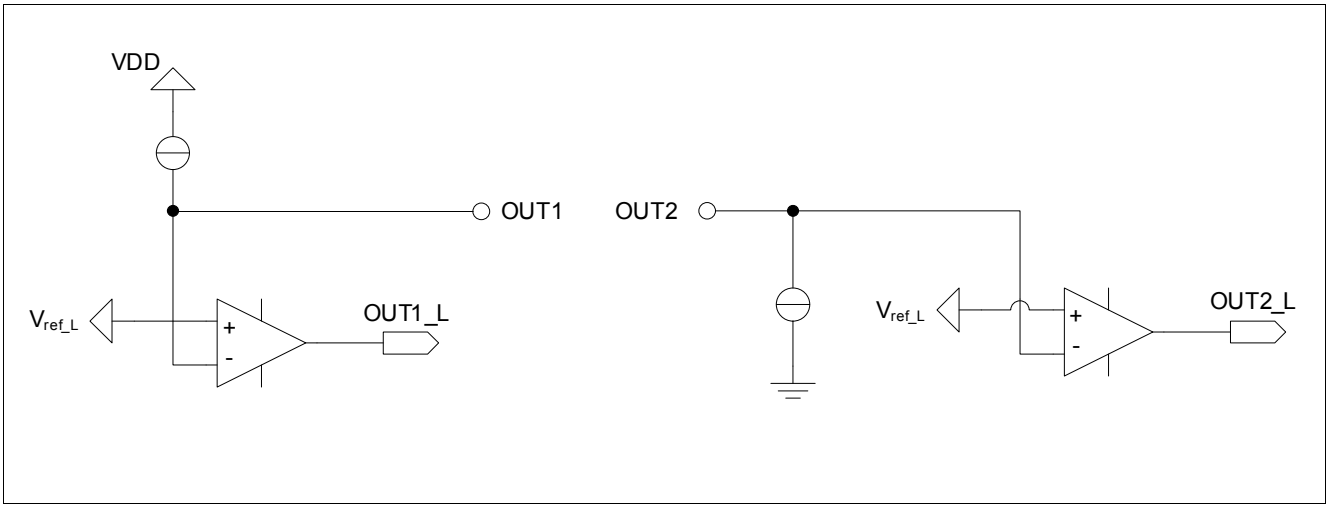


Figure 12 Open Load Detection in H-Bridge Mode

Table 3 Open Load Detection in H-Bridge Mode

VOUT1	OUT1_L	VOUT2	OUT2_L	Diagnostic	Comment
< V_{ref_L}	H	< V_{ref_L}	H	Load o.k.	pull down current is stronger
< V_{ref_L}	H	> V_{ref_L}	L	Load o.k.	transient area
> V_{ref_L}	L	< V_{ref_L}	H	Open Load	
> V_{ref_L}	L	> V_{ref_L}	L	Load o.k.	transient area

Open Load Detection in Single Switch Mode

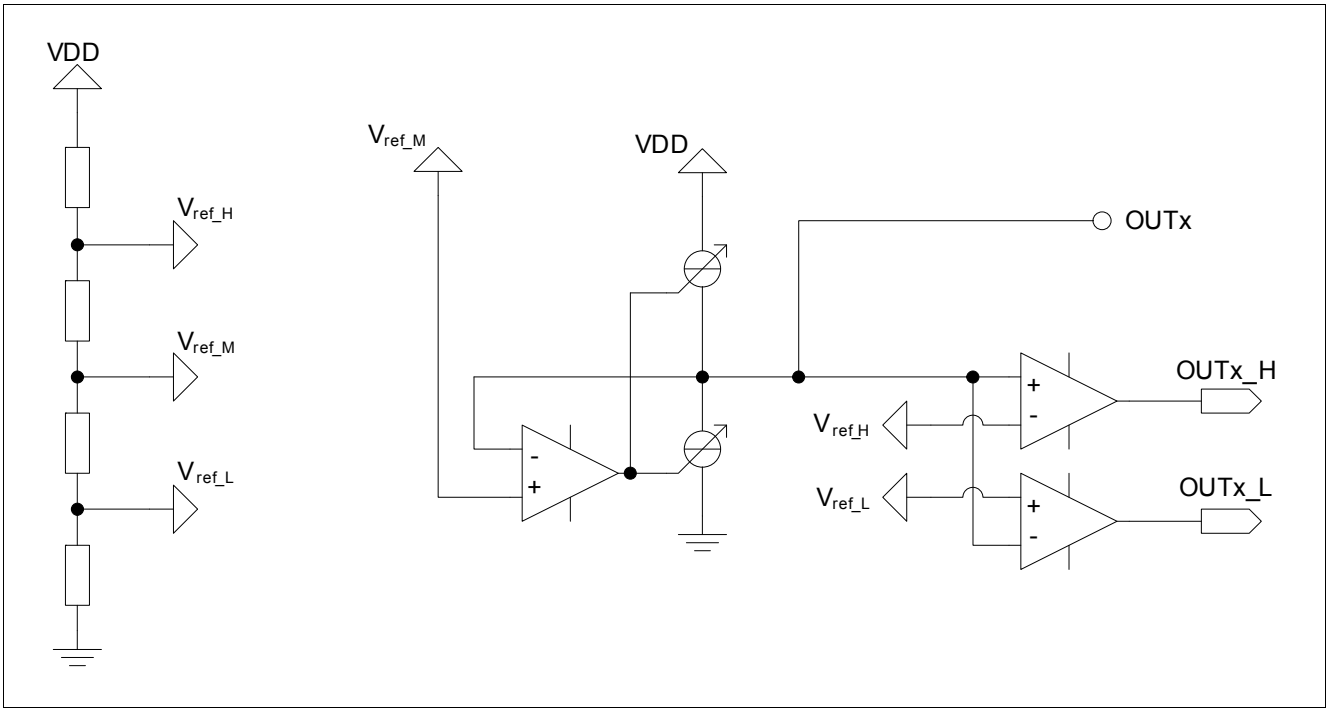


Figure 13 Open Load Detection in Single Switch Mode

Table 4 Open Load Detection in Single Switch Mode

VOUTx (OFF State)	OUTx_H	OUTx_L	Diagnostic	Comment
$V_{OUTx} < V_{ref_L}$	L	H	o.k.	Load to ground
$V_{ref_L} < V_{OUTx} < V_{ref_H}$	L	L	Open Load	Output open
$V_{OUTx} > V_{ref_H}$	H	L	o.k.	Load to V_S

8.10 Electrical Characteristics

Electrical Characteristics: Protection and Monitoring

V_S = 5 V to 28 V; V_{DD} = 5.0 V, T_j = -40 ·C to 150 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Chopper Current Limitation							
8.10.1	Current Limit	$\|I_{L1}\|$	1.0	1.8	2.7	A	-40 °C < T_j < T_{ILR} Dependent on SPI setting; Default = I_{L3}
8.10.2		$\|I_{L2}\|$	3.3	4.8	5.7		
8.10.3		$\|I_{L3}\|$	6.0	7.8	9.2		
8.10.4		$\|I_{L4}\|$	9.0	10.6	12.3		
8.10.5	Current Limit Hysteresis	I_{hys}	0.0	0.3	0.4	A	-40 °C < T_j < T_{ILR}
8.10.6	Blanking time	t_b	8	11	15	µs	–
8.10.7	Time between transients	t_{trans}	90	–	130	µs	–
Temperature Dependent Current Limitation[1)]							
8.10.8	Current Limit at T_{SD}	I_{L_TSD}	1.4	2.5	3.6	A	–
8.10.9	Start of current limit reduction	T_{ILR}	150	165	–	°C	–
8.10.10	Thermal shut-down	T_{SD}	175	–	–	°C	–
8.10.11	Range of temperature dependent current reduction	T_{SD} - T_{ILR}	20	25	30	°C	–
Short Circuit Detection to GND							
8.10.12	Short circuit detection current (HS)	$\|I_{OUKH1}\|$	2.5	6.3	7.5	A	-40 °C < T_j < T_{ILR} Dependent on SPI-setting for $\|I_L\|$; Default = I_{OUKH3}
8.10.13		$\|I_{OUKH2}\|$	5.5	9.0	11.0		
8.10.14		$\|I_{OUKH3}\|$	8.5	11.7	13.5		
8.10.15		$\|I_{OUKH4}\|$	10.5	14.2	17.4		
8.10.16	Current tracking	$\|I_{OUKH1}\|$ - $\|I_{L1}\|$	1.5	4.4	5.5	A	
8.10.17		$\|I_{OUKH2}\|$ - $\|I_{L2}\|$	2.0	4.2	5.5		
8.10.18		$\|I_{OUKH3}\|$ - $\|I_{L3}\|$	2.0	3.9	5.0		
8.10.19		$\|I_{OUKH4}\|$ - $\|I_{L4}\|$	1.5	3.7	5.0		
Short Circuit Detection to VS							
8.10.20	Short circuit detection current (LS)	$\|I_{OUKL1}\|$	2.5	4.6	6.5	A	-40 °C < T_j < T_{ILR} Dependent on SPI-setting for $\|I_L\|$; Default = I_{OUKL3}
8.10.21		$\|I_{OUKL2}\|$	5.0	8.1	10.0		
8.10.22		$\|I_{OUKL3}\|$	7.5	10.0	11.5		
8.10.23		$\|I_{OUKL4}\|$	10.5	14	17.4		
8.10.24	Current tracking	$\|I_{OUKL1}\|$ - $\|I_{L1}\|$	1.0	2.8	5.0	A	
8.10.25		$\|I_{OUKL2}\|$ - $\|I_{L2}\|$	1.0	3.3	5.5		
8.10.26		$\|I_{OUKL3}\|$ - $\|I_{L3}\|$	0.5	2.2	5.5		
8.10.27		$\|I_{OUKL4}\|$ - $\|I_{L4}\|$	0.3	3.4	7.0		

Electrical Characteristics: Protection and Monitoring

V_S = 5 V to 28 V; V_{DD} = 5.0 V, T_j = -40 ·C to 150 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Short Circuit Detection Timing							
8.10.28	Delay time for fault detection	t_{DF_H}, t_{DF_L}	1	2	5	µs	–
8.10.29	Time from detected fault to high impedance of output[1)]	t_{DF_OFF}	–	–	4	µs	–
8.10.30	Delay time between switching off of the output stages in short circuit	t_{DF_del}	5	17	40	µs	–
Open Load							
8.10.31	Open Load Diagnostic Filter Time[1)]	t_{OL_DIAG}	60	–	135	µs	–
8.10.32	Low Diagnosis Threshold	V_{ref_L}	0.4 * V_{DD} - 0.2	0.4 * V_{DD}	0.4 * V_{DD} + 0.2	V	–
8.10.33	High Diagnosis Threshold	V_{ref_H}	0.8 * V_{DD} - 0.2	0.8 * V_{DD}	0.8 * V_{DD} + 0.2	V	–
8.10.34	Diagnosis Bias Voltage	V_{ref_M}	0.6 * V_{DD} - 0.2	0.6 * V_{DD}	0.6 * V_{DD} + 0.2	V	–
8.10.35	Positive Diagnostic Current (pull down current source)	I_{DIA_P}	300	620	980	µA	V_{OUTx} = 14 V
8.10.36			270	610	980	µA	V_{OUTx} = V_{ref_H}
8.10.37	Negative Diagnostic Current	I_{DIA_N}	-350	-240	-100	µA	V_{OUTx} = 0 V
8.10.38			-350	-210	-80	µA	V_{OUTx} = V_{ref_L}
8.10.39	Ratio of current sources (Pos/Neg)	$Ratio_{I_DIA}$	2	2.9	4	–	–
Undervoltage							
8.10.40	Undervoltage at V_S	$V_{UV\ OFF}$	3.1	3.7	4.4	V	Switch off threshold
		$V_{UV\ ON}$	3.3	3.9	4.6	V	Switch on threshold
		$V_{UV\ HY}$	100	200	400	mV	Hysteresis
8.10.41	VS Undervoltage Detection Filter Time[1)]	t_{UV}	–	–	1.5	µs	

1) Not subject to production test; specified by design.

9 SPI Interface

The serial SPI interface establishes a communication link between TLE8209-4SA and the systems microcontroller. The TLE8209-4SA always operates in slave mode whereas the controller provides the master function. The maximum baud rate is 2 MBaud.

By applying an active slave select signal at $\overline{SS}$ the TLE8209-4SA is selected by the SPI-master. SI is the data input (Slave In), SO the data output (Slave Out). Via SCK (Serial Clock Input) the SPI-clock is provided by the master. In case of inactive slave select signal (High) the data output SO goes into tristate.

The first two bits of an instruction may be used to establish an extended device-addressing. This gives the opportunity to operate up to 4 Slave-devices sharing one common $\overline{SS}$ signal from the Master-Unit (see **Figure 16**).

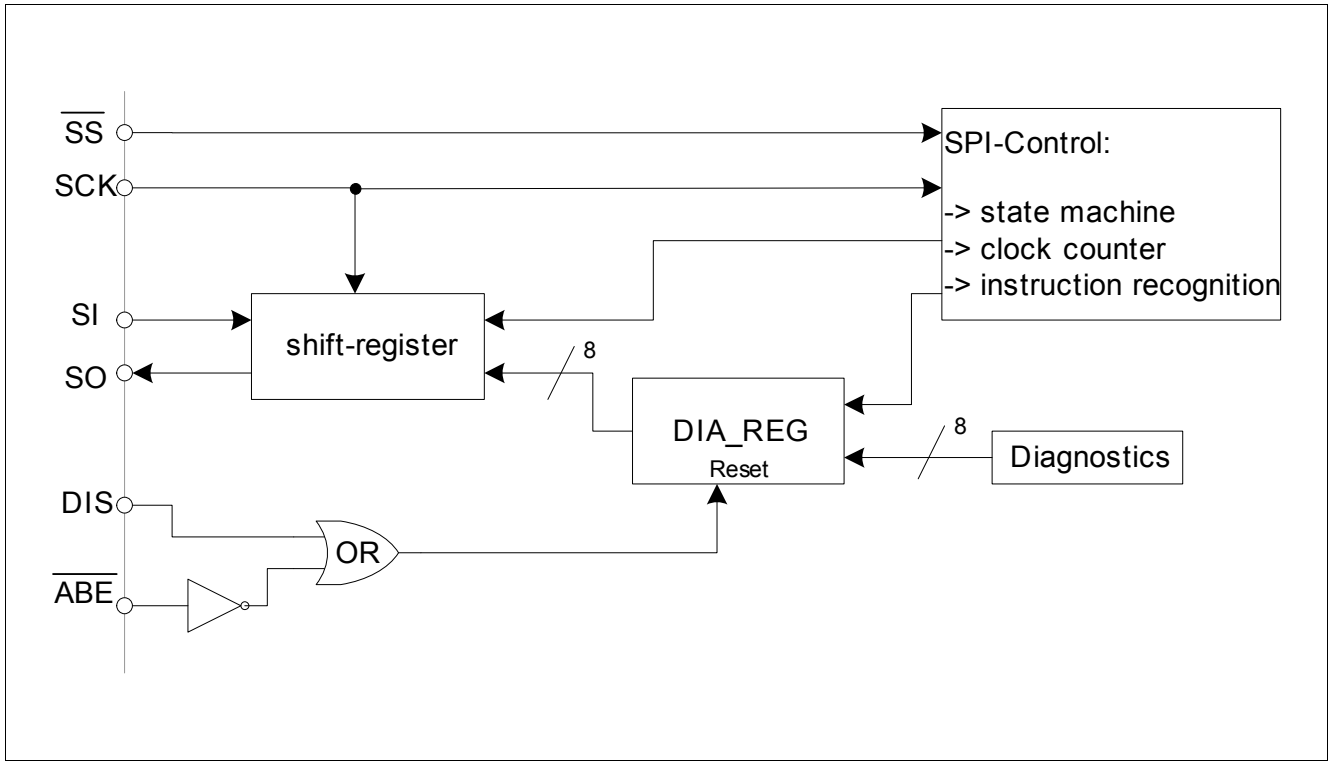


Figure 14 SPI Block Diagram

9.1 General SPI Characteristics

1. During active reset conditions the SPI is driven into its default state. The output SO is set to high impedance (tristate). When reset becomes inactive, the state machine enters into a wait state for the next instruction.

2. If the slave select signal at SS is inactive (high), the state machine is forced to wait for the following instruction.

3. During active (low) state of the select signal SS the falling edge of the serial clock signal SCK will be used to latch the input data at SI. Output data at SO are driven with the rising edge of SCK. Further processing of the data according to the instruction (i.e. modification of internal registers) will be triggered by the rising edge of the SS signal.

4. In order to establish the option of extended addressing the upper two bits of the instruction byte (i.e. the first two SI bits of a frame) are reserved to send a chip address. To avoid a bus conflict the output SO will remain tristate during the addressing phase of a frame (i.e. until the address bits are recognized as a valid chip

address). If the chip address does not match, the according frame will be ignored and SO remains tristate for the complete frame.

5. Verification byte: Simultaneously to the receipt of an SPI instruction the TLE8209-4SA transmits a verification byte via the output SO to the controller. This byte indicates regular or irregular operation of the SPI. It contains an initial bit pattern and a flag indicating an invalid instruction of the previous access.

6. On a read access the data bits at the SPI input SI are rejected. During a valid write access the SPI will transmit the data byte "00hex" at the output SO after having sent the verification byte.

7. An instruction is invalid if one of the following conditions is fulfilled:
   - an unused instruction code is detected (see tables with SPI instructions).
   - the previous transmission is not completed in terms of internal data processing.
   - the number of SPI clock pulses (falling edge) counted during active SS differs from exactly 16 clock pulses.

   If an unused instruction code occurres, the data byte “FF_{hex}” (no error) will be transmitted after having sent the verification byte. This transmission takes place within the same SPI-frame that contained the unused instruction byte.
   If an invalid instruction is detected, bit TRANS_F in the following verification byte (next SPI-transmission) is set to HIGH. The TRANS_F bit must not be cleared before it has been sent to the microcontroller.

9.2 SPI Communication

The 16 input bits consist of the SPI instruction byte and an input data byte. The 16 output bits consist of the verification byte and the output data byte (see also **Figure 15**). The definition of these bytes is given in the subsequent sections. The access mode of the registers is described in the column “Type” (r = read, w = write).

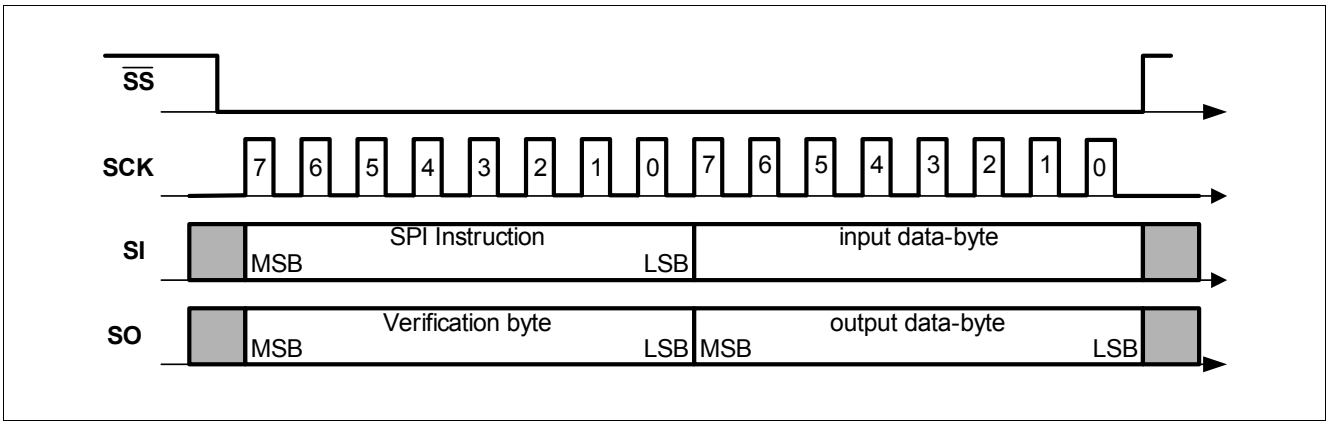


Figure 15 SPI Communication

9.2.1 Instruction Byte

The upper 2 bit of the instruction byte contain the chip address. The chip address of the TLE8209-4SA is ’00’. During read access, the output data according to the register requested in the instruction byte are applied to SO within the same SPI frame. That means, the output data corresponding to an instruction byte sent during one SPI frame are transmitted to SO during the same SPI-frame

Table 5 SPI Instruction Format

7	6	5	4	3	2	1	0
CPAD1	**CPAD0**	**INSTR5**	**INSTR4**	**INSTR3**	**INSTR2**	**INSTR1**	**INSTR0**

Field	Bits	Type	Description
CPAD1:0	7:6	w	**Chip Address (00_B)**
INSTR5:0	5:0	w	**SPI Instruction (encoding)**

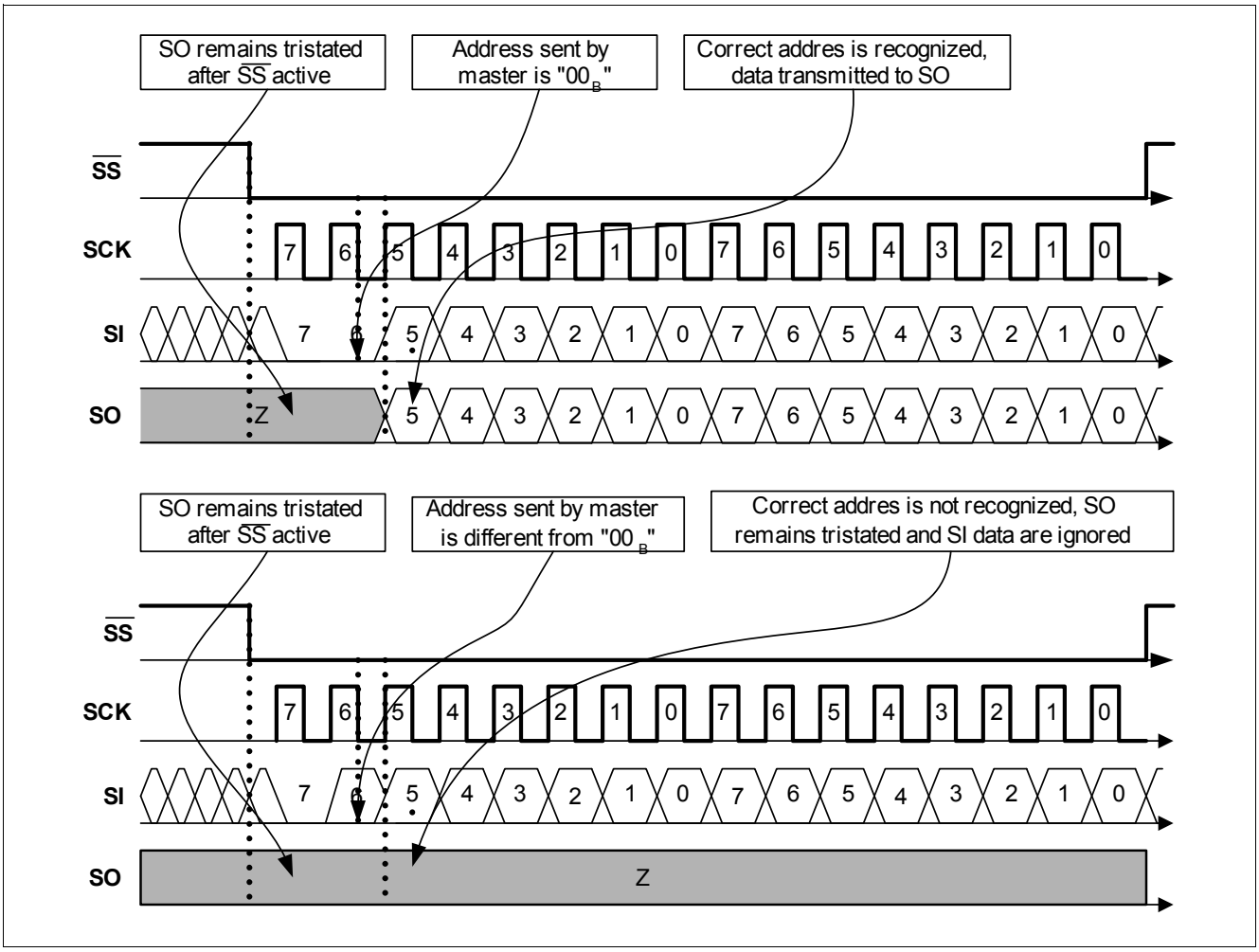


Figure 16 Bus Arbitration by Chip Address

Table 6 SPI Instruction Set

Command	SPI Instruction Byte	Description
RD_ID	0000 0000	Read identifier
RD_REV	0000 0011	Read version
RD_DIA	0000 1001	Read diagnostics register
RD_CONFIG	0011 0000	Read power stage configuration
RD_STATCON	0011 1100	Read VDD monitoring status
WR_CONFIG	0010 1000	Write power stage configuration
WR_STATCON	0001 1000	Write VDD monitoring status
all other instructions	00xx xxxx	Unused - TRANS_F is set to high, ff_hex is sent as data bit.
all other chip addr.	xxxx xxxx	Invalid address - SO remains tristate during entire SPI-frame.

9.2.2 Verification Byte

Table 7 Verification Byte Format

7	6	5	4	3	2	1	0
VER6	**VER5**	**VER4**	**VER3**	**VER2**	**VER1**	**VER0**	**TRANS_F**

Field	Bits	Type	Description
VER6	7	r	Fixed to tristate (Z)
VER5	6	r	Fixed to tristate (Z)
VER4	5	r	Fixed to high (1)
VER3	4	r	Fixed to low (0)
VER2	3	r	Fixed to high (1)
VER1	2	r	Fixed to low (0)
VER0	1	r	Fixed to high (1)
TRANS_F	0	r	Transfer failure: 1_B Error detected during previous transfer 0_B Previous transfer was recognized as valid

9.2.3 Device Identifier and Revision

The IC's identifier (device ID) and revision number are used for production test purposes and features plug & play functionality depending on the systems software release. The two numbers are read-only accessible via the SPI-instructions RD_ID and RD_REV as described in **Section 9.2.1**. The device ID is defined to allow identification of different IC-types by software and is fixed for the TLE8209-4SA.

The revision number may be utilized to distinguish different states of hardware and is updated with each redesign of the TLE8209-4SA. It is divided into an upper 4 bit field reserved to define revisions (SWR) corresponding to specific software releases and a lower 4 bit field utilized to identify the actual mask set revision (MSR).

Both (SWR and MSR) will start with 0000_B and are increased by 1 every time an according modification of the hardware is introduced.

ID_REG
Device Identifier

7	6	5	4	3	2	1	0
ID7	**ID6**	**ID5**	**ID4**	**ID3**	**ID2**	**ID1**	**ID0**

Field	Bits	Type	Description
ID7:0	7:0	r	**Device-ID** TLE8209-4SA: DE hex

REV_REG
Device Revision

7	6	5	4	3	2	1	0
SWR3	**SWR2**	**SWR1**	**SWR0**	**MSR3**	**MSR2**	**MSR1**	**MSR0**

Field	Bits	Type	Description
SWR3:0	7:4	r	Revision corresponding to software release
MSR3:0	3:0	r	Revision corresponding to mask set

9.2.4 Diagnostics Register

DIA_REG
Diagnostics Register **Reset Value: x111 1111$_B$**

7	6	5	4	3	2	1	0
$\overline{\text{ABE}}$/DIS	**OT**	**CurrRed**	**CurrLim**	**DIA21**	**DIA20**	**DIA11**	**DIA10**

Field	Bits	Type	Description
$\overline{\text{ABE}}$/DIS	7	r	Is set to “0” in case of $\overline{\text{ABE}}$ = L or DIS = H
OT	6	r	Is set to “0” in case of over temperature
CurrRed	5	r	Is set to “0” in case of temperature dependent current limitation
CurrLim	4	r	Is set to “0” in case of current limitation
DIA21	3	r	Diagnosis-Bit2 of OUT2
DIA20	2	r	Diagnosis-Bit1 of OUT2
DIA11	1	r	Diagnosis-Bit2 of OUT1
DIA10	0	r	Diagnosis-Bit1 of OUT1

Table 8 Failure Encoding

$\overline{\text{ABE}}$/DIS	DIA21	DIA20	DIA11	DIA10	Description	Comment
X	1	1	1	1	no failure	
1	X	X	0	1	short circuit to battery at OUT1 (SCB1)	latched
1	X	X	1	0	short circuit to ground at OUT1 (SCG1)	latched
1	X	X	1	1	no error detected at OUT1	
1	0	1	X	X	short circuit to battery at OUT2 (SCB2)	latched
1	1	0	X	X	short circuit to ground at OUT2 (SCG2)	latched
1	1	1	X	X	no error detected at OUT2	
1	0	1	1	0	short circuit accross load (HS1+LS2 active)	latched
1	1	0	0	1	short circuit accross load (HS2+LS1 active)	latched
X	0	0	0	0	Undervoltage at pin VS	not latched
0	1	1	0	0	open load (H-Bridge)	latched
0	1	1	X	0	open load at OUT1 (single switch operation)	latched
0	1	1	0	X	open load at OUT2 (single switch operation)	latched

Note:

The bit $\overline{\text{ABE}}$/DIS shows directly the status of inputs $\overline{\text{ABE}}$ and DIS. It is set to ‘0’ if the power stages are disabled by $\overline{\text{ABE}}$ or DIS.

The bits OT, CurrRed and CurrLim are latched. They will be reset with each read access. If the failure condition is still present the according bits are set again.

Undervoltage at VS is reported and the outputs are switched off as long as the undervoltage condition is present. The previous setting of the DIAx bits is masked but not reset. Once the supply voltage is back in the operating range the diagnostic bits DIAxx will return to their setting before VS undervoltage. The outputs will return to normal operation.

Detection of short circuit will switch of the output stages. In single half bridge operation only the affected output is switched off. In H-Bridge mode both outputs are shut down. The outputs remain off until the failure condition is removed and the diagnosis register is reset.

A short across the load may also be reported as SCG at one output and SCB at the other.

The diagnostic information DIAxx in the SPI interface is reset in the following cases:

- Read out of DIA_REG: only bit 4, 5 and 6 will be reset
- Enabling or disabling of the bridge via ABE or DIS
- Undervoltage at VDD
- Reset command via SPI

9.2.5 Configuration Register

CONFIG_REG
Configuration Register **Reset Value: 1111 1010$_B$**

7	6	5	4	3	2	1	0
MODE	MUX	SIN1	SIN2	CL1	CL2	RESET	SL

Field	Bits	Type	Description
MODE	7	wr	’1’: H-bridge mode ’0’: single output stages (for current levels 1 to 3 only)
MUX	6	wr	’1’: control by parallel inputs IN1 and IN2 ’0’: control by SPI bits SIN1 and SIN2
SIN1	5	wr	control of OUT1 if MUX=’0’
SIN2	4	wr	control of OUT2 if MUX=’0’
CL1	3	wr	current limitation level (see table below)
CL2	2	wr	current limitation level (see table below)
RESET	1	wr	’0’: reset of digital logic
SL	0	wr	slew rate setting ’1’: slow ’0’: fast

Table 9 Current Limitation Levels

CL1	CL2	Current Level	Typical Current
0	0	1	1.5A
0	1	2	4.0A
1	0	3 (default)	6.6A
1	1	4	8.6A

9.2.6 STATCON Register

STATCON_REG
STATCON Register **Reset Value: 1101 1xxx$_B$**

7	6	5	4	3	2	1	0
CONFIG2	CONFIG1	CONFIG0	DIACLR2	DIACLR1	STATUS2	STATUS1	STATUS0

Field	Bits	Type	Description
CONFIG2	7	wr	VDD threshold test mode ’1’: VDD monitoring in normal operation ’0’: VDD thresholds are changed according to CONFIG1

Field	Bits	Type	Description
CONFIG1	6	wr	changes thresholds in VDD threshold test mode (CONFIG2='0') '1': increase lower threshold of VDD monitoring to test switch off path '0': decrease upper threshold of VDD monitoring to test switch off path
CONFIG0	5	wr	latch function for overvoltage at VDD '1': overvoltage at VDD latched '0': overvoltage at VDD not latched
DIACLR2	4	wr	'0': clears diagnosis of OUT2 always returns '1' at read access
DIACLR1	3	wr	'0': clears diagnosis of OUT1 always returns '1' at read access
STATUS2	2	r	returns level at $\overline{ABE}$
STATUS1	1	r	'0': under voltage at VDD '1': VDD voltage above lower limit
STATUS0	0	r	0': over voltage at VDD '1': VDD voltage below upper limit

9.2.7 Contents of the SPI registers after a reset condition

Note: The registers for device identifier and revision (ID_REG and REV_REG) are not affected by reset.

DIA_REG

	7	6	5	4	3	2	1	0
	ABEDIS	**OT**	**CurrRed**	**CurLim**	**DIA21**	**DIA20**	**DIA11**	**DIA10**
POR	x	1	1	1	1	1	1	1
SPIR	x	1	1	1	1	1	1	1
ABEDISR	x	1	1	1	1	1	1	1
RDR	x	1	1	1	x	x	x	x
DIACLR1	x	x	x	x	x	x	1	1
DIACLR2	x	x	x	x	1	1	x	x

CONFIG_REG

	7	6	5	4	3	2	1	0
	MODE	**MUX**	**SIN1**	**SIN2**	**CL1**	**CL2**	**RESET**	**SL**
POR	1	1	1	1	1	0	1	0
SPIR	1	1	1	1	1	0	1	0
DISR	x	1	1	1	x	x	1	x
SFMODE	1	1	1	1	1	0	1	0

STATCON_REG

	7	6	5	4	3	2	1	0
	CONFIG2	**CONFIG1**	**CONFIG0**	**DIACLR2**	**DIACLR1**	**STATUS2**	**STATUS1**	**STATUS0**
POR	1	1	0	1	1	x	x	x
SPIR	1	1	0	1	1	x	x	x
SFMODE	1	1	0	1	1	x	x	x

POR: Reset due to VDD power up
SPIR: Reset via SPI by writing 0 into the RESET of CONFIG_REG
ABEDISR: Reset due to enabling or disabling the power stages via DIS or ABE (edge triggered)
DISR: Reset due to a disabled power stage by DIS or ABE (level triggered)
RDR: Reset due to a read access to DIA_REG
DIACLR1: Reset via SPI by writing 0 into the DIACLR1 of STATCON_REG
DIACLR2: Reset via SPI by writing 0 into the DIACLR2 of STATCON_REG
SFMODE: Reset by setting the TLE8209-4SA into the Status Flag Mode (VDDIO = 0V)

x: No change

Note: If a reset condition is not listed for a particular register it has no effect on the contents of this register.

9.3 Electrical Characteristics SPI

Electrical Characteristics: SPI Interface

V_S = 5 V to 28 V; V_{DD} = 5.0 V; V_{DDIO} = 2.9 V to 5.5 V, T_j = -40 ·C to 150 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
SPI-Timing (see Figure 17)[1)]							
9.3.1	Cycle-time (1)	t_{cyc}	490	–	–	ns	referred to master
9.3.2	Enable Lead Time (2)	t_{lead}	50	–	–	ns	referred to master
9.3.3	Enable Lag Time (3)	t_{lag}	150	–	–	ns	referred to master
9.3.4	Data Valid (4) H->L: V_{SCK}=2V -> V_{SO}=0.2 V_{DDIO} L->H: V_{SCK}=2V -> V_{SO}=0.8 V_{DDIO} if V_{DDIO} < 4.5V: L->H: V_{SCK}=2V -> V_{SO}=0.7 V_{DDIO}	t_v	– –	– –	150 230	ns	C_L = 200 pF C_L = 350 pF referred to TLE8209-4
9.3.5	Data Setup Time (5)	t_{su}	40	–	–	ns	referred to master
9.3.6	Data Hold Time (6)	t_h	40	–	–	ns	referred to master
9.3.7	Disable Time (7)	t_{dis}	–	–	100	ns	referred to TLE8209-4
9.3.8	Transfer Delay (8)	t_{dt}	250	–	–	ns	referred to master
9.3.9	Disable Lead Time (9)	t_{dld}	250	–	–	ns	referred to master
9.3.10	Disable Lag Time (10)	t_{dlg}	250	–	–	ns	referred to master
9.3.11	Access time (11)	t_{acc}	8.35	–	–	µs	referred to master

1) All timing parameters specified by design - not subject to production test

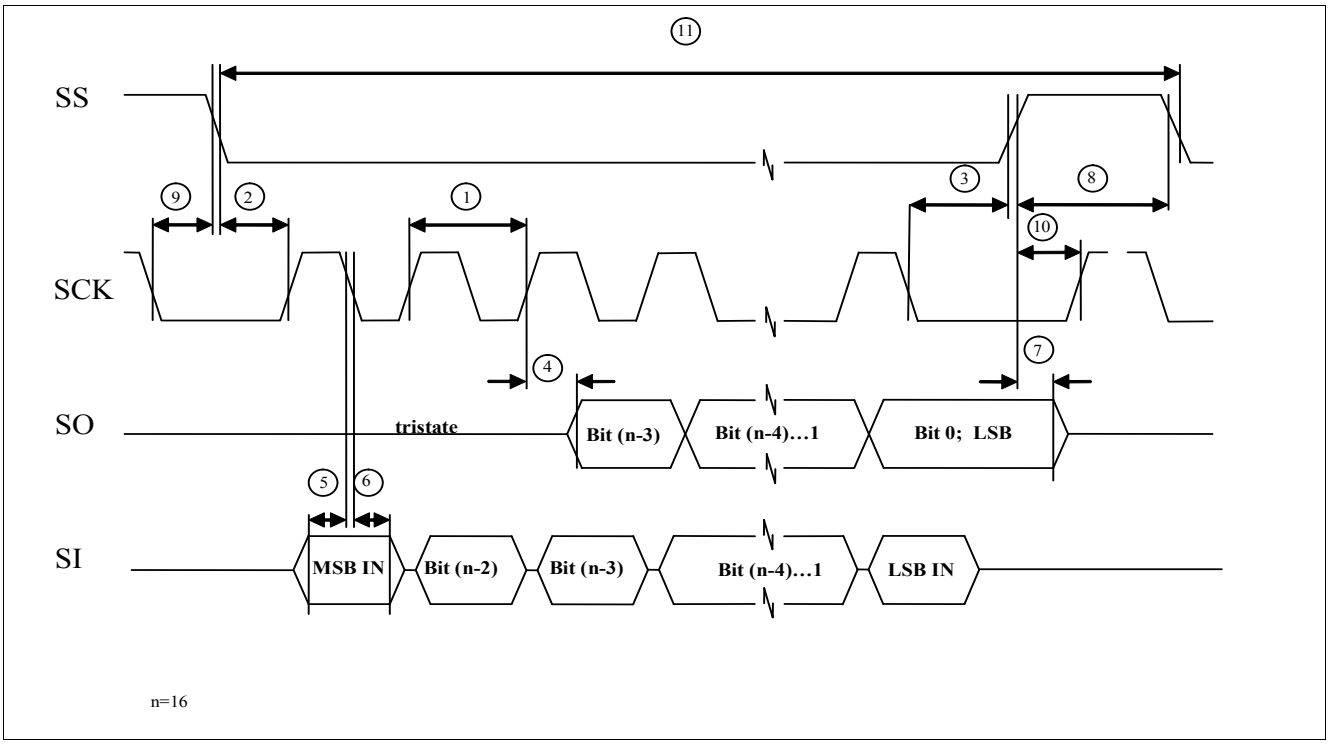


Figure 17 SPI Timing

10 Application Information

Note: The following simplified application examples are given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. The function of the described circuits must be verified in the real application

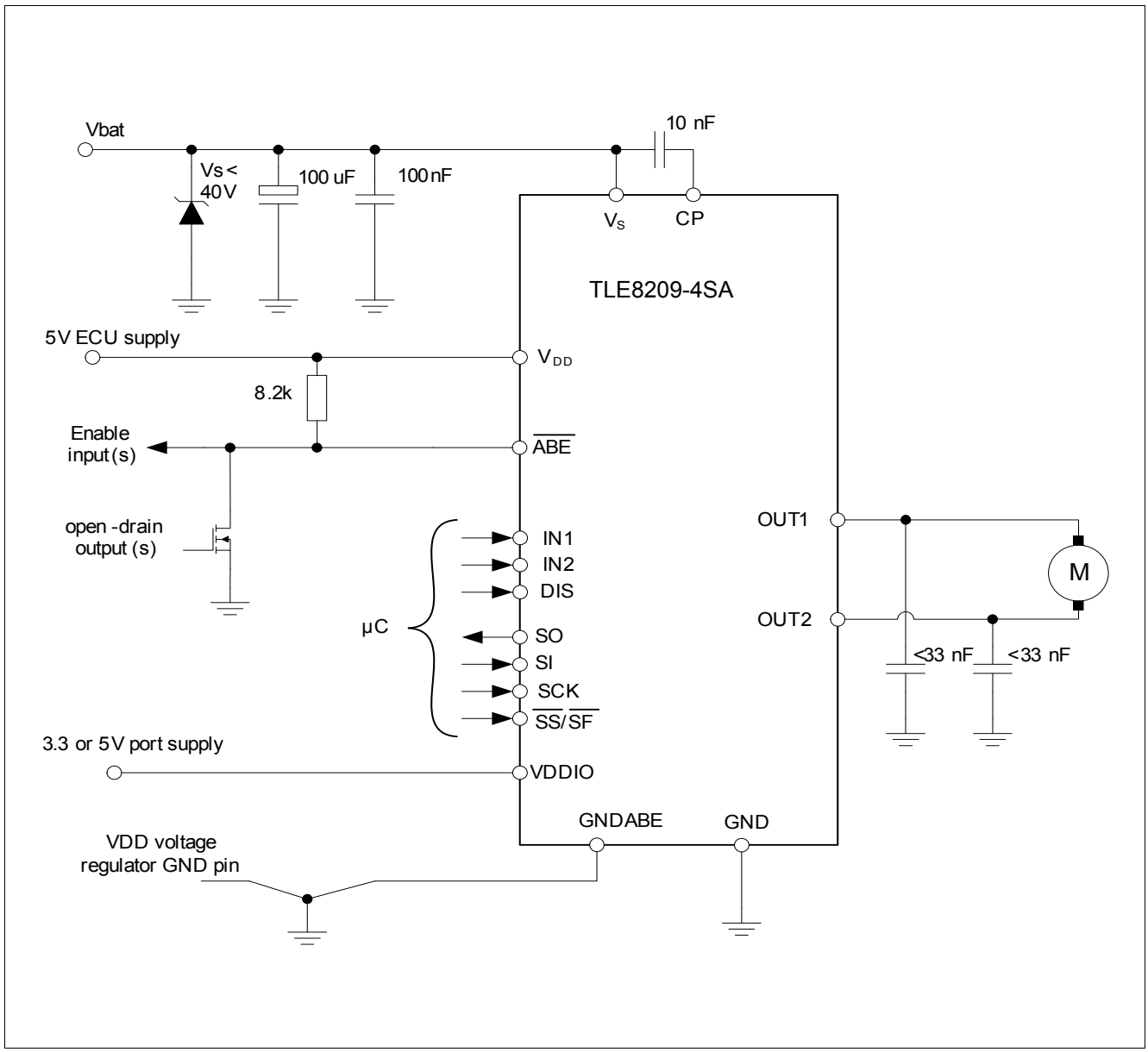


Figure 18 Application Example H-Bridge with SPI-Interface

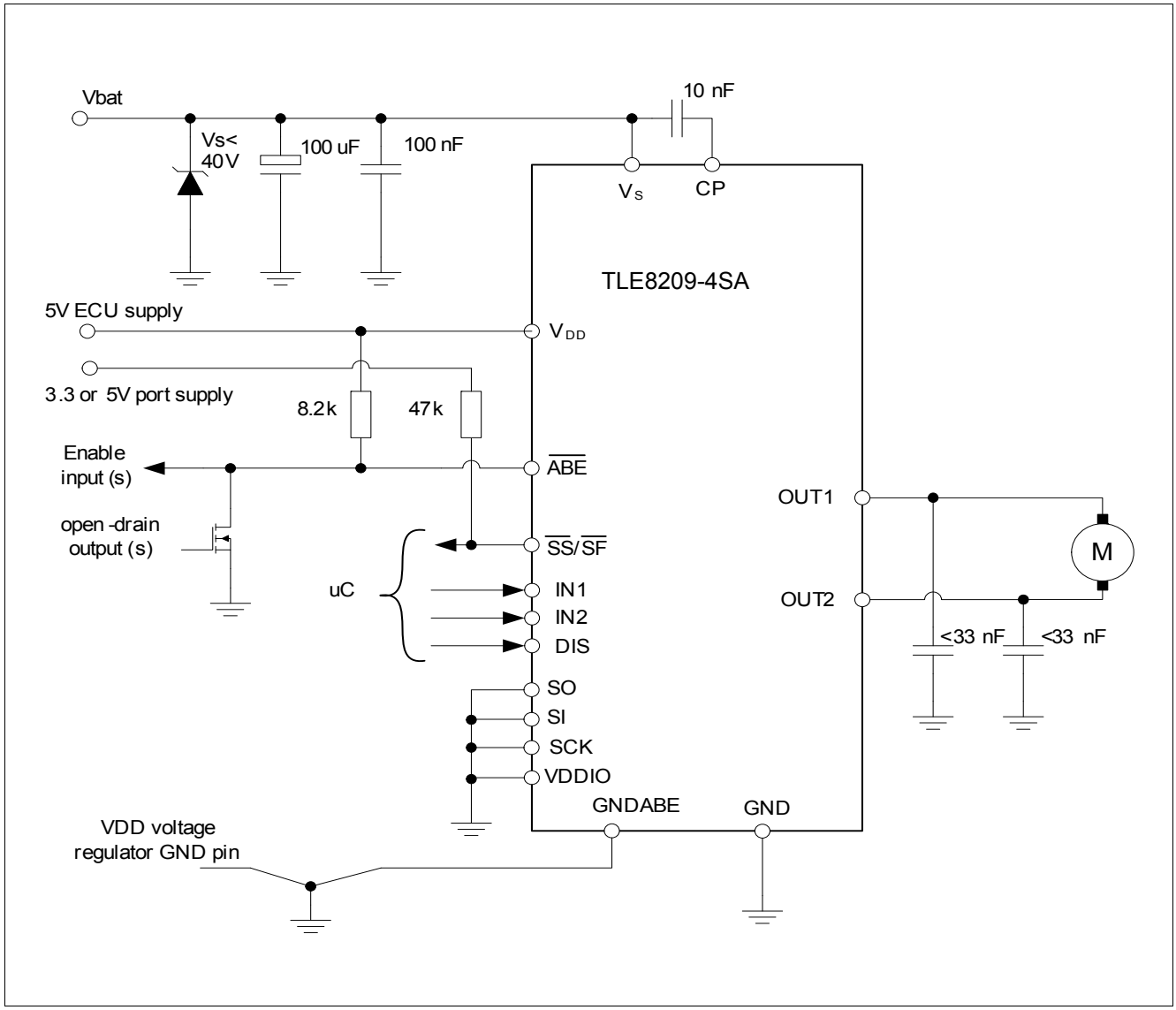


Figure 19 Application Example with Status Flag

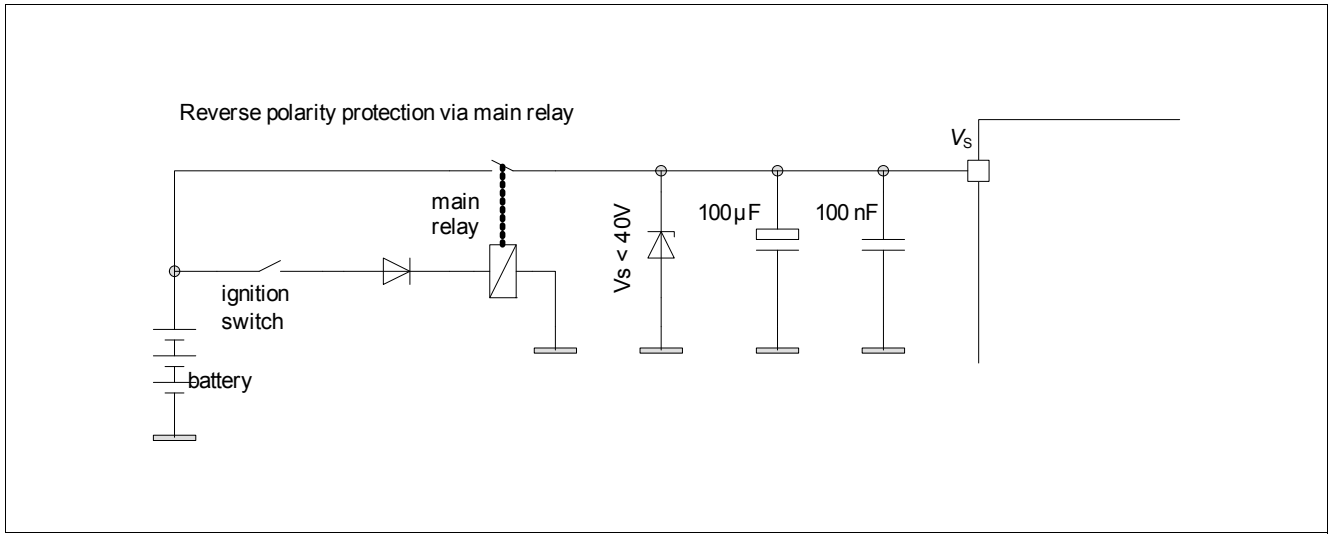
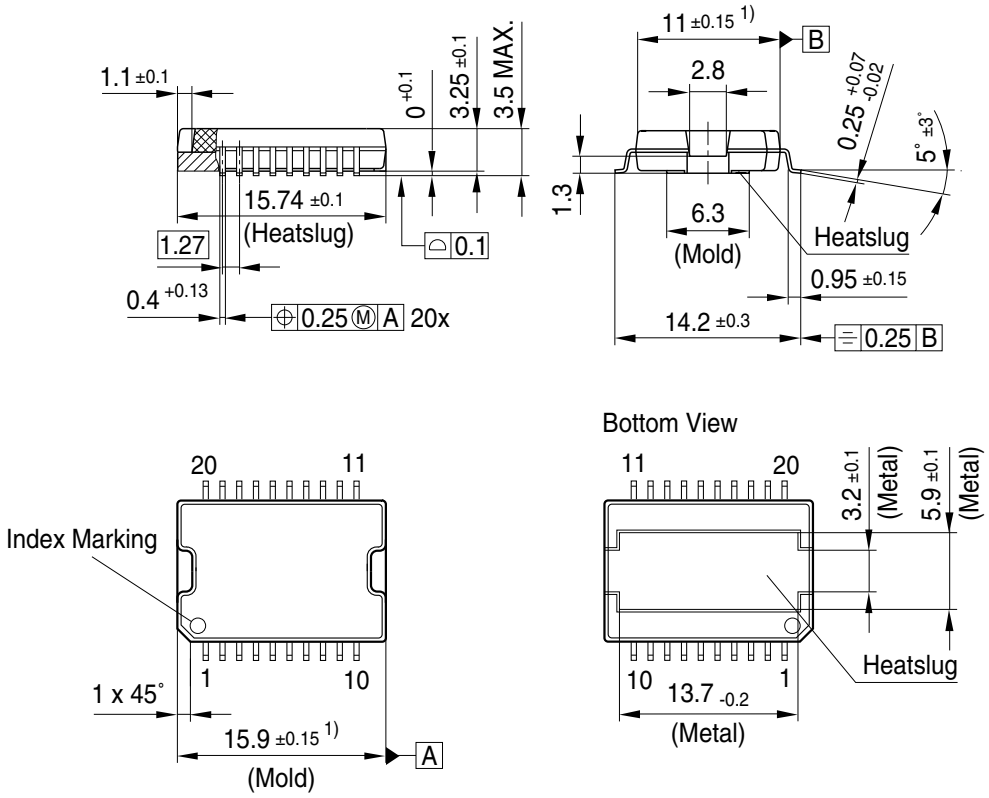


Figure 20 Application Examples for Overvoltage and Reverse-Voltage Protection

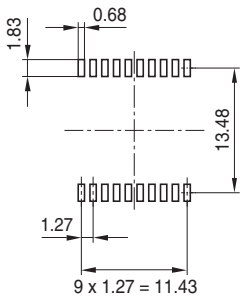
11 Package Outlines TLE8209-4SA



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPS05791

Footprint:



hlg09550

Figure 21 PG-DSO-20-65 (Plastic Dual Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

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Dimensions in mm

12 Revision History

Revision	Date	Comments / Changes
0.1	2010-08-05	Target Data Sheet based on TLE8209-2SA Data Sheet Rev. 1.0
1.0	2012-09-13	Data Sheet Current Limitation and Short Circuit Limits revised
1.1	2012-10-15	Parameter 8.10.1: Max. changed to 2.7A Parameter 8.10.12: Max. changed to 7.5A

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