February 2009

TLV4946

Value Optimized Hall Effect Latches for Industrial and Consumer Applications

TLV4946K, TLV4946-2K, TLV4946-2L



Preliminary

Datasheet

Revision 0.9

Sense and Control

Never stop thinking

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Value Optimized Hall Effect Latches for Industrial and Consumer Applications

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Page	Subjects (major changes since last revision)

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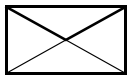


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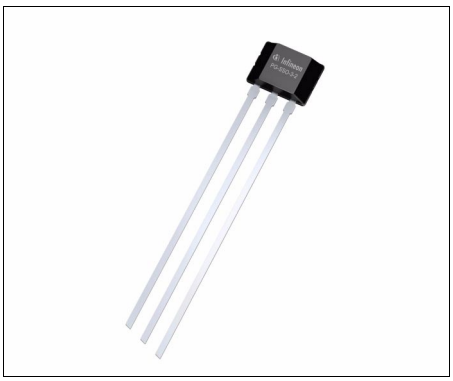
1 Product Description



1.1 Overview

The TLV4946xy is a high precision Hall Effect Latch with highly accurate switching thresholds for ambient operating temperatures up to 85°C.

The TLV4946K and the TLV4946-2K is available in a PG-SC59-3-4 package, the TLV4946-2L in a PG-SSO-3-2 package.



1.2 Features

- 2.7 V to 18 V supply voltage operation.
- Operation from unregulated power supply.
- High sensitivity and high stability of the magnetic switching points.
- High resistance to mechanical stress by active error compensation.
- Reverse battery protection (-18 V).
- Superior temperature stability.
- Low jitter (typically 1 µs).
- High ESD performance (± 4 kV HBM).
- Digital output signal (open-drain).

1.3 Target Applications

The TLV4946xy is ideally suited to detect the rotor position in Brushless DC (BLDC) Motors used in industrial and consumer applications, such as: air conditioning systems, pumps, washing machines, DVD players, rolling shutter, etc. The sensor also provides a reliable switching for index counting with small pole wheels and large air gaps. The TLV4946xy can also be used for index counting.

Product Name	Product Type	Ordering Code	Package
Hall Effect Latch	TLV4946K	SP000604402	PG-SC59-3-4
Hall Effect Latch	TLV4946-2K	SP000604332	PG-SC59-3-4
Hall Effect Latch	TLV4946-2L	SP000604340	PG-SSO-3-2

2 Functional Description

2.1 General

Precise magnetic switching thresholds and high temperature stability are achieved by active compensation circuits and chopper techniques on chip. Offset voltages generated by temperature-induced stress or overmolding are canceled so that high accuracy is achieved. The IC has an open collector output stage with 20 mA current sink capability. A wide operating voltage range from 2.7 V to 18 V with reverse polarity protection down to -18 V makes the TLV4946xysuitable for a wide range of applications. A magnetic south pole with a field strength above B_{op} turns the output on. A magnetic north pole exceeding B_{rp} turns it off.

2.2 Pin Configuration

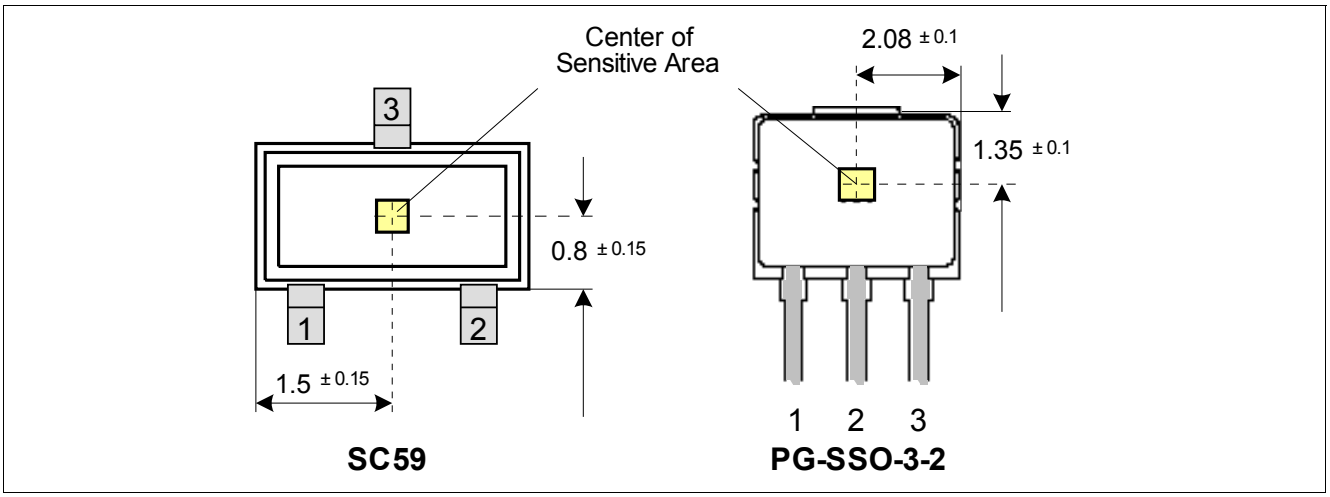


Figure 1 Pin Configuration and sensitive area (Top view, figure not to scale)

2.3 Pin Description

Table 1 PIN Definitions for the PG-SC59-3-4 package

PIN No.	Name	Function
1	V_s	Supply Voltage
2	Q	Output
3	GND	Ground

Table 2 PIN Definitions for the PG-SSO-3-2 package

PIN No.	Name	Function
1	V_s	Supply Voltage
2	GND	Ground
3	Q	Output

2.4 Block Diagram

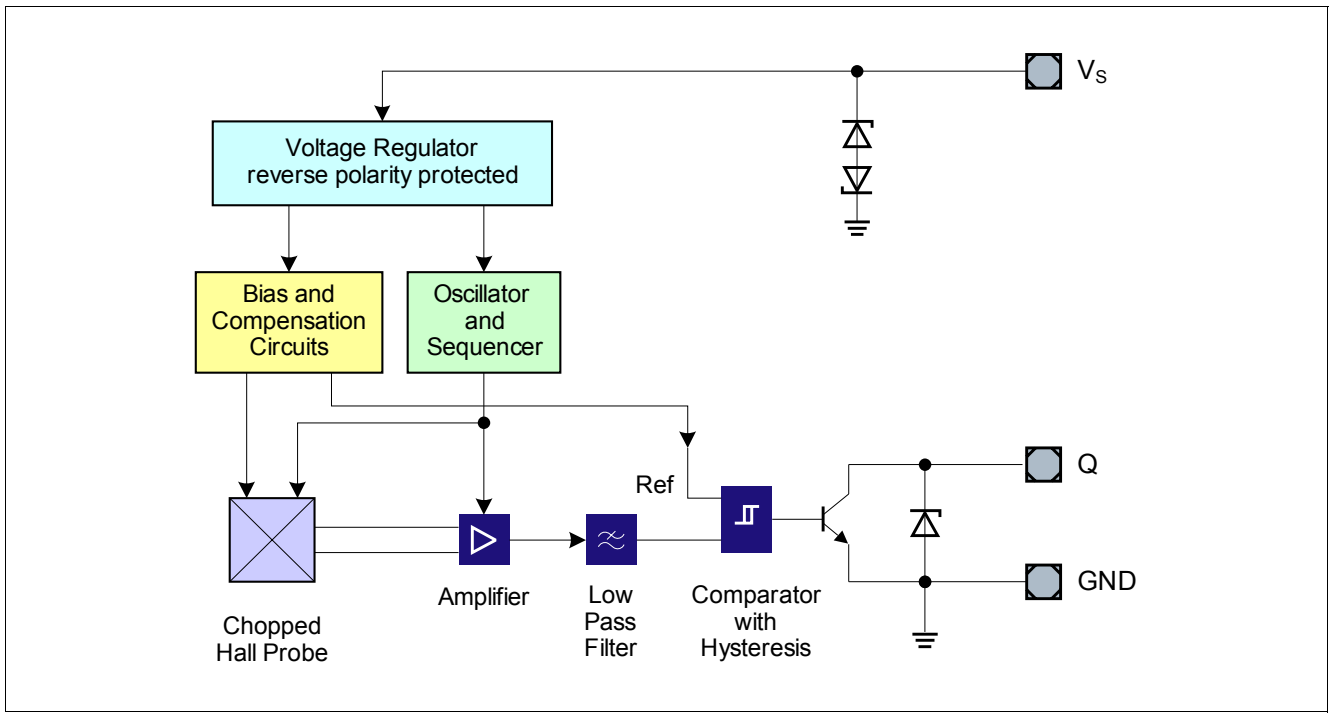


Figure 2 TLV4946xy Block Diagram

2.5 Operating Modes and States

Field Direction and Definition

Positive magnetic fields correspond to the south pole of the magnet targeting the branded side of the package.

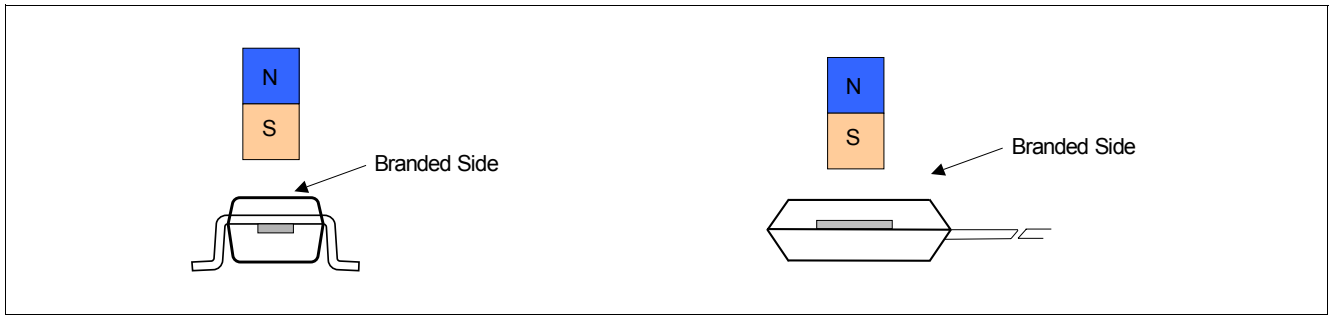


Figure 3 Definition of the Magnetic Field direction

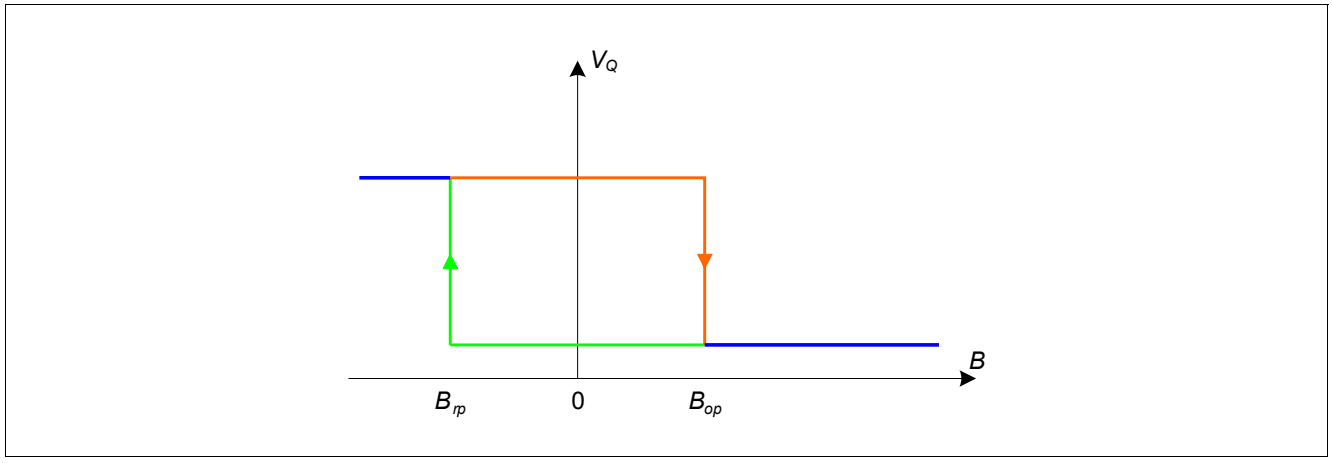


Figure 4 Output Signal

2.6 Functional Block Description

The chopped Hall Effect Latch comprises a Hall probe, a bias generator, compensation circuits, an oscillator and an output transistor. The bias generator provides currents to the Hall probe and the active circuits. Compensation circuits stabilize response of the IC over temperature and reduce the impact of process variations.

The Active Error Compensation rejects offsets in the signal path and reduces the impact of mechanical stress in the package caused by molding, soldering and thermal effects.

The chopper technique together with the threshold generator and the comparator ensure high accurate magnetic switching points.

3 Specification

3.1 Application circuit

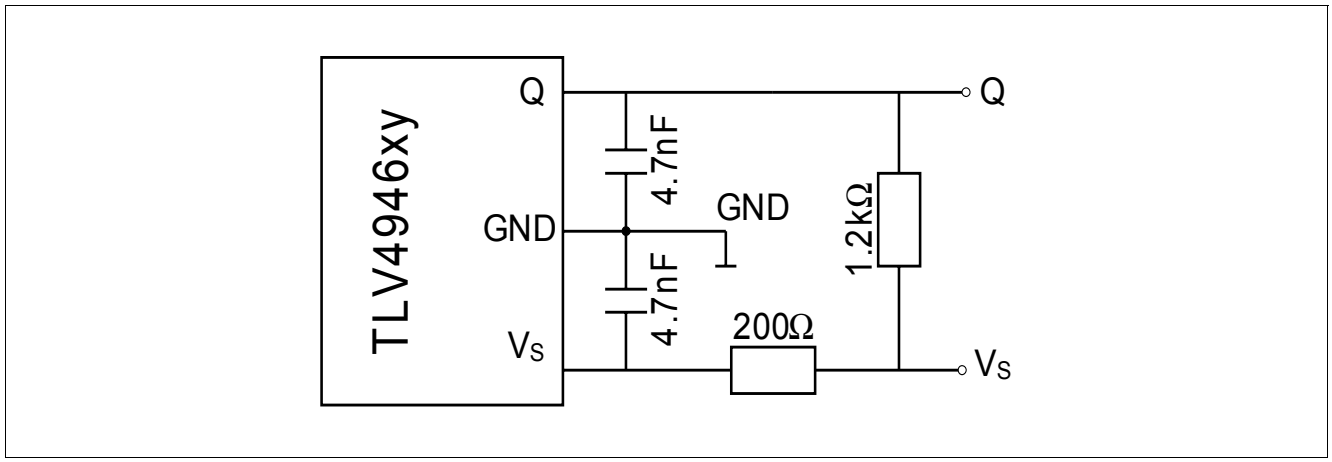


Figure 5 Application circuit

It is recommended to use a resistor of 200 Ω in the supply line for current limitation in the case of an overvoltage pulse. Two capacitors of 4.7 nF enhance the EMC performance. The pull-up of 1.2 kΩ limits the current through the output transistor.

3.2 Absolute Maximum Ratings

Stress above the maximum values listed in this section may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect the reliability of the device. Exceeding only one of these values may cause irreversible damage to the device.

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum Ambient Temperature	T_A	- 40	–	125	°C	
Maximum Junction Temperature	T_J	- 40	–	150	°C	
Supply Voltage	V_S	- 18	–	18	V	
Supply current through protection device	I_S	-50	–	50	mA	
Output Voltage	V_{OUT}	- 0.7	–	18	V	
Storage Temperature	T_S	- 40	–	150	°C	
Magnetic flux density	B	–	–	unlimited	mT	
ESD Robustness HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$ [1)]	–	–	4	kV	

1) According to EIA/JESD22-A114-E

3.3 Operating Range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLV4946xy. All parameters specified in the following sections refer to these operating conditions unless otherwise mentioned.

Table 4 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_S	2.7	–	18	V	
Output Voltage	V_Q	-0.7	–	18	V	
Output Current	I_Q	0	–	20	mA	
Maximum Ambient Temperature	T_A	-40	–	85	°C	

3.4 Electrical Characteristics

Product characteristics include the spread of values guaranteed within the specified voltage and ambient temperature range. typical characteristics are the median of the production (at V_s=12V and T_A=25°C).

Table 5 Electrical Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Current	I_S	2	4	6	mA	V_S=2.7 V...18 V
Reverse Current	I_{SR}	0	0.2	1	mA	V_S=-18 V
Output Saturation Voltage	V_{QSAT}	–	0.3	0.6	V	I_Q=20 mA
Output leakage current	I_{QLEAK}	–	0.05	10	µA	V_Q=18 V
Output fall time[1)]	t_f	–	0.02	1	µs	R_L=1.2k Ω, C_L=50 pF
Output rise time[1)]	t_r	–	0.4	1	µs	
Chopper frequency	f_{OSC}	–	320	–	kHz	
Switching frequency	f_{SW}	0	–	15[2)]	kHz	
Delay time[3)]	t_d	–	13	–	µs	
Output jitter[4)]	t_{QJ}	–	1	–	$µs_{RMS}$	Typical value for a 1 kHz square wave signal
Power-on Time[5)]	t_{PON}	–	13	–	µs	V_S > 2.7 V
Thermal Resistance junction to ambient[6)]	R_{thja}	–	100	–	K/W	TLV4946K, TLV4946-2K
		–		190	K/W	TLV4946-2L

1) See **Figure 6**
2) To operate the sensor at maximum switching frequency, the value of the magnetic signal amplitude must be 1.4 times higher than the static fields. This is due to the -3 dB corner frequency of the low pass filter in the signal path.
3) Systematic delay between magnetic threshold reached and output.
4) Jitter is the unpredictable deviation of the output switching delay.
5) Time from applying V_S. > 2.7 V to the sensor until the output state is valid.
6) Relationship between junction and ambient temperature: $T_J=T_{amb} + R_{thja} .(V_S . I_S + V_{QS} . I_Q)$.

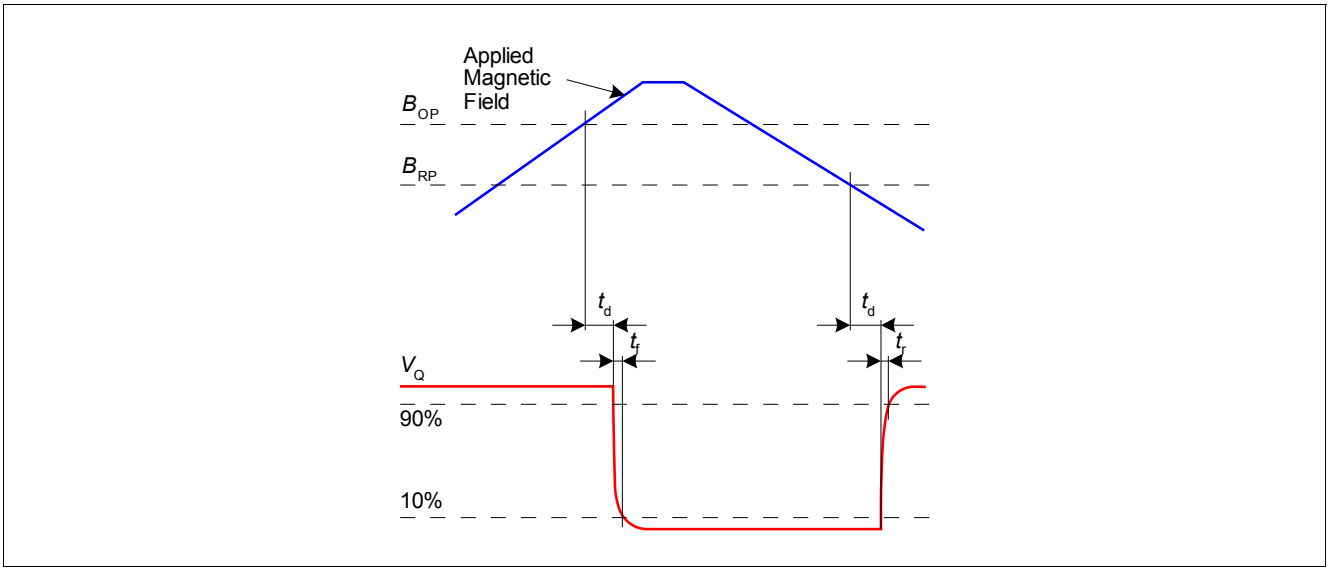


Figure 6 Timing Diagram

Table 6 Magnetic Characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operate point	B_{OP}	6.1	14.0	19.2	mT	TLV4946K
		0.5	2.0	3.5	mT	TLV4946-2K, TLV4946-2L
Release point	B_{RP}	-19.2	-14.0	-6.1	mT	TLV4946K
		-3.5	-2.0	-0.5	mT	TLV4946-2K, TLV4946-2L
Hysteresis	B_{HYS}	22.0	28.0	34.0	mT	TLV4946K[2)]
		1.0	4.0	6.0	mT	TLV4946-2K, TLV4946-2L
Magnetic offset[3)]	B_{OFF}	-3.0	–	3.0	mT	TLV4946K[2)]
		-1.5	0	1.5	mT	TLV4946-2K, TLV4946-2L
Temperature compensation of magnetic thresholds	TC	–	-2000	–	ppm/°C	TLV4946K
		–	-350	–	ppm/°C	TLV4946-2K, TLV4946-2L
Repeatability of magnetic thresholds[4)]	B_{REP}	–	20	–	μT_{RMS}	typical value for $\Delta B/\Delta t$ > 12mT/ms

1) Over all operating conditions
2) at 25°C.
3) $B_{OFF} = (B_{OP} + B_{RP}) / 2$.
4) B_{REP} is equivalent to the noise constant.

4 Package Information

4.1 TLV4946K and TLV4946-2K Package Outline

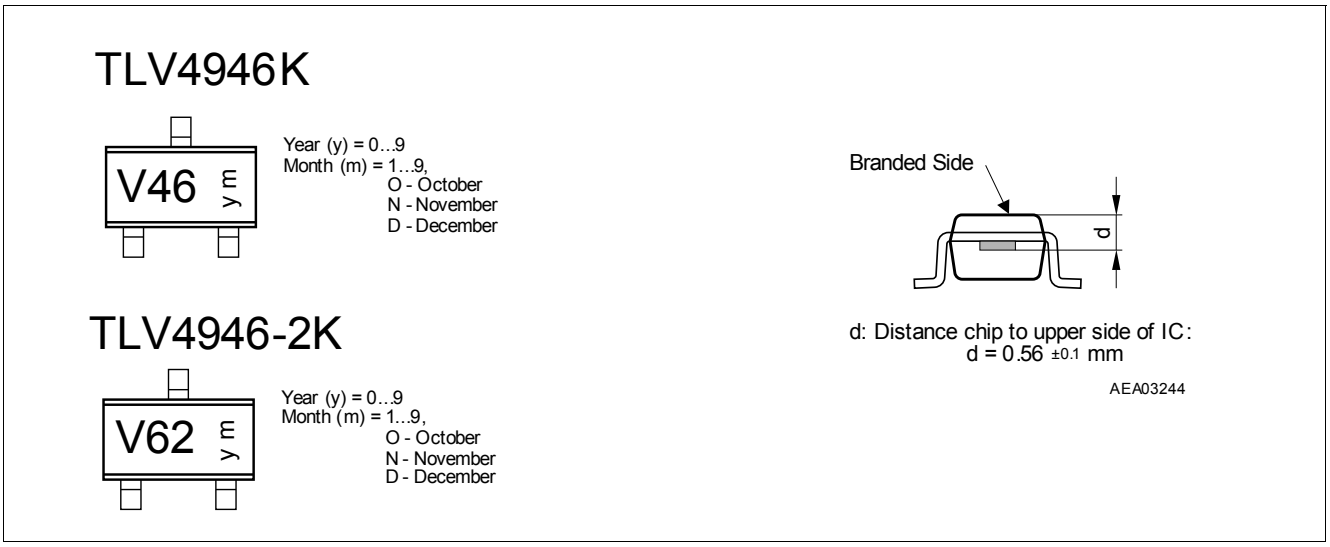


Figure 7 Marking of the TLV4946K and TLV4946-2K distance of the chip to the upper side

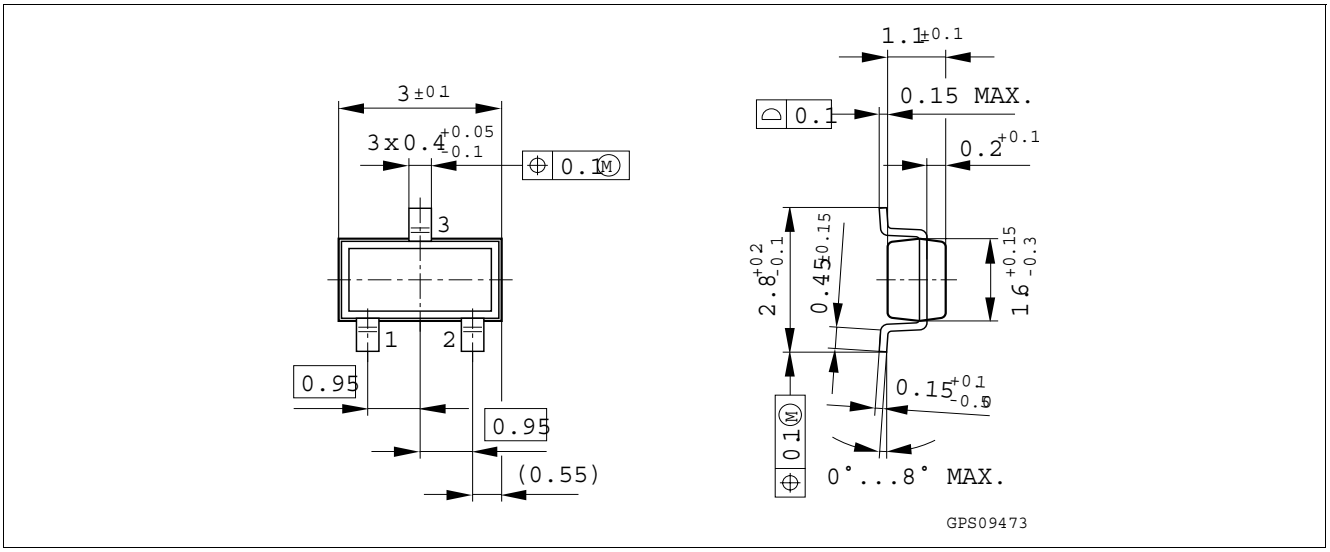


Figure 8 PG-SC59-3-4 Package Outline

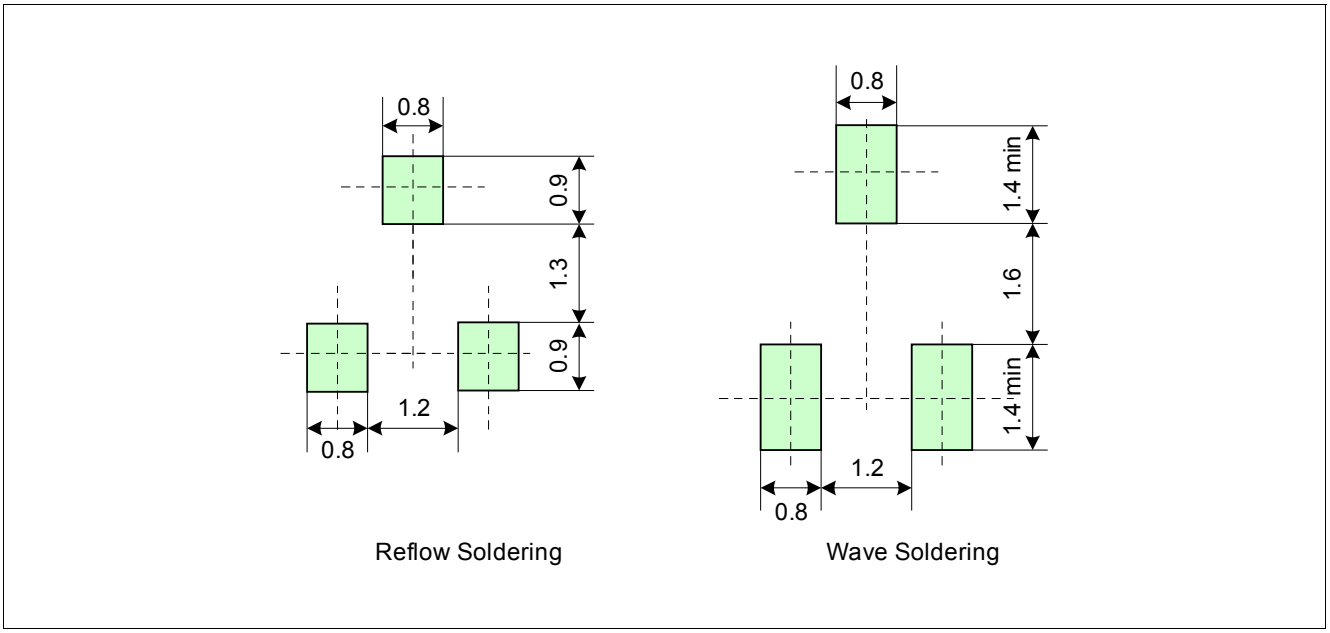


Figure 9 Footprint PG-SC59-3-4 (SOT23 compatible)

4.2 TLV4946-2L Package Outline

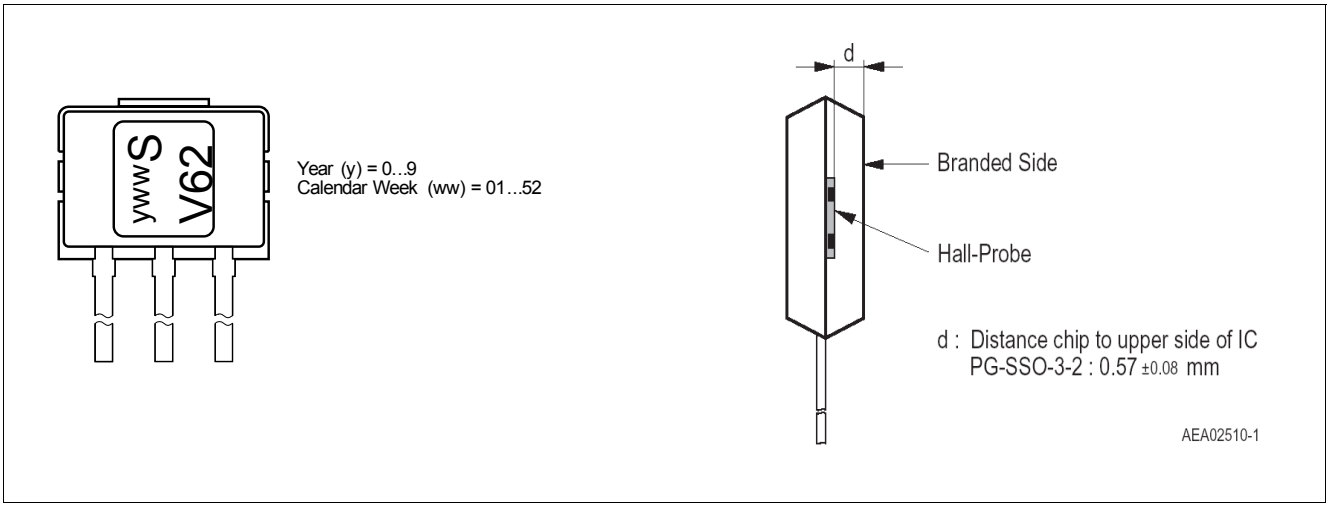


Figure 10 Marking of the TLV4946-2L and distance of the chip to the upper side

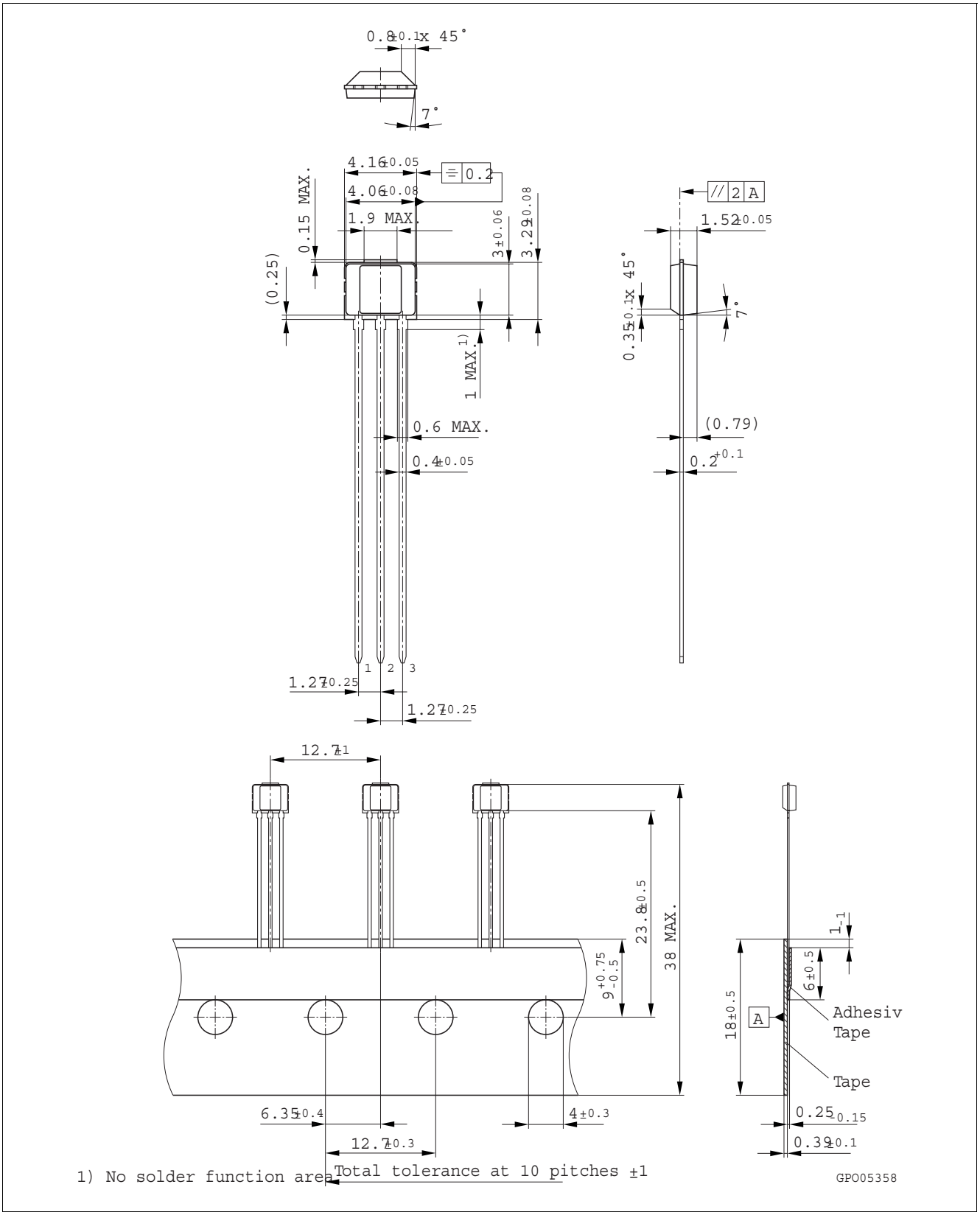


Figure 11 PG-SSO-3-2 Package Outline

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