

AIROC™ Wi-Fi & Bluetooth® combo chip

Single-chip, Tri-band, 802.11ax, 1x1, Bluetooth® 5.3 for Commercial/Consumer applications

Description

The Infineon AIROC™ CYW55571 single-chip device provides the highest level of integration for commercial and consumer IoT wireless systems with integrated tri-band 1x1 IEEE 802.11ax WLAN MAC/baseband/radio, Bluetooth® 5.3 MAC/baseband/radio, and integrated Power Management Unit. WLAN and Bluetooth® radios also include on-chip power amplifiers and low-noise amplifiers to further reduce the need for external components.

The WLAN interfaces to host processor through a PCIe v3.0 Gen2 or SDIO 3.0 interface while Bluetooth® host interface is provided through high-speed 4-wire UART interface. Additionally, the Bluetooth® section supports PCM and I2S interfaces for audio applications. CYW55571 is qualified to operate across Industrial (–40°C to +85°C) temperature range.

AIROC™ CYW55571 functional block diagram

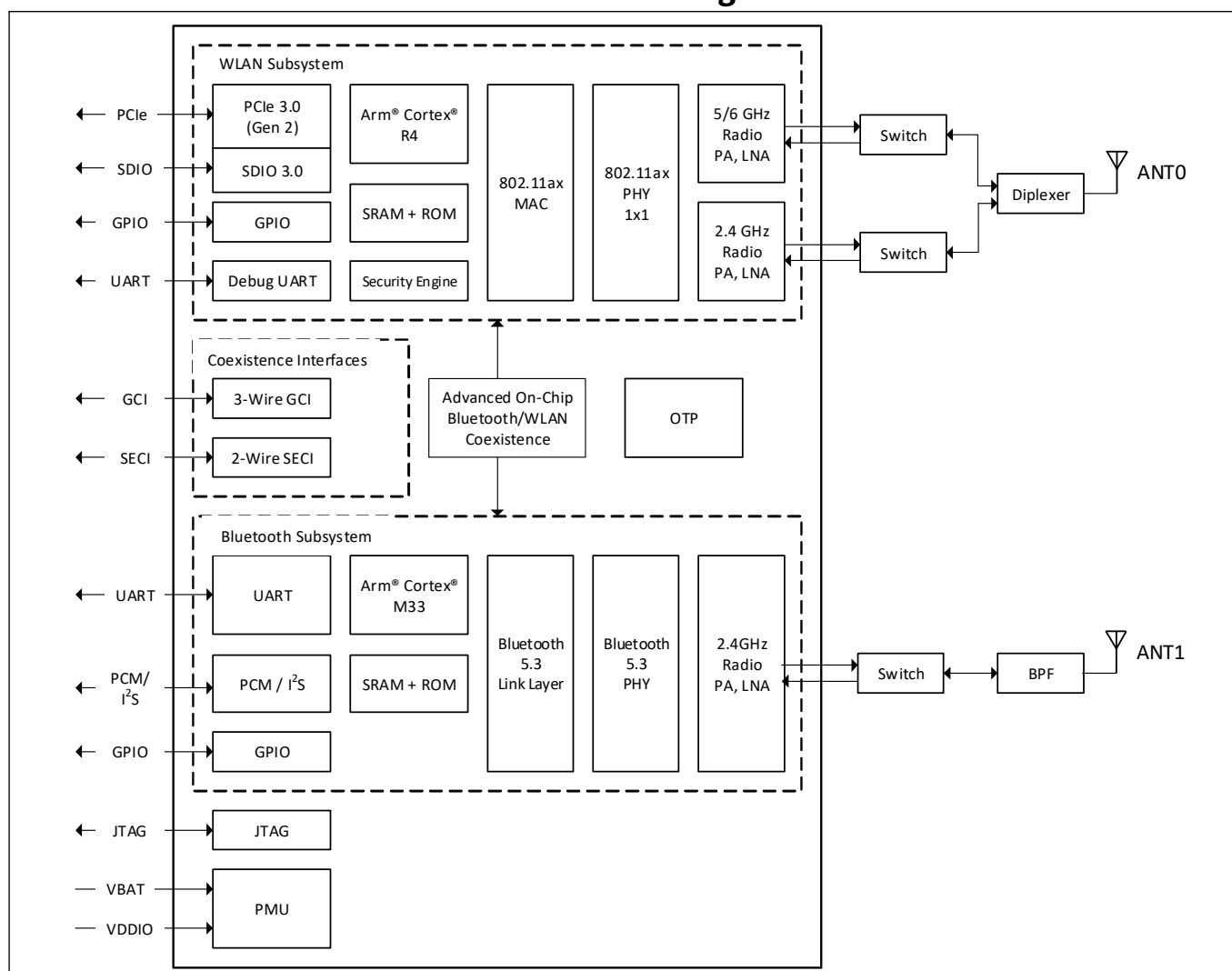


Figure 1 CYW55571 functional block diagram

Features**Features****• WLAN:**

- 802.11a/b/g/n/ac/ax compliant, tri-band capable (2.4/5/6 GHz)
- 5/6 GHz: 20/40/80 MHz channels, 1024-QAM, 1×1 providing up to 600 Mbps PHY data rate
- 2.4 GHz: 20/40^[1] MHz channels, 1024-QAM, 1×1 providing up to 287 Mbps PHY data rate
- 802.11ax STA mode and Soft AP mode with 11ax scheduled access
- Supports 802.11d, h, k, r, v, w, ai
- On-chip power amplifiers and low-noise amplifiers
- Supports one and two-antenna configurations
- Supports multi-point external coexistence interface to optimize bandwidth utilization with other co-located wireless technologies such as LTE
- Fast Virtual simultaneous dual band (VSDB)
- Security:
 - WPA/WPA2/WPA3 (Personal/Enterprise) support for powerful encryption and authentication
 - AES in hardware for faster data encryption and IEEE 802.11i compatibility
 - Reference WLAN subsystem provides Wi-Fi protected setup (WPS)
- Worldwide regulatory support: Global products supported with worldwide homologated design
- Integrated Arm® Cortex® R4 processor with tightly coupled memory for complete WLAN subsystem functionality. This architecture offloads the host processor completely from WLAN functionality.
- GPIOs: 15

• Bluetooth® :

- Qualified for Bluetooth® core specification 5.3 (BDR + EDR + Bluetooth® LE)
 - QDID: **192646**
 - Declaration ID: **D057578**
- All Bluetooth® 5.0/5.1/5.2 optional features supported including LE audio
- Dedicated Bluetooth® RF path for best Wi-Fi + Bluetooth® coexistence performance
- Bluetooth® Class 1 or Class 2 transmitter operation
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets
- Adaptive Frequency Hopping (AFH) for reducing radio frequency interference
- Interface support, Host controller interface (HCI) using a high-speed UART interface and PCM/I2S for audio data
- Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound
- On-chip memory includes 512 KB SRAM and 2 MB ROM
- GPIOs: 10

• Interfaces:

- PCIe Gen2 (3.0 compliant) for WLAN: complies with PCI express base specification revision 3.0 for ×1 lane and power management running at Gen2 speeds
- SDIO 2.0/3.0 for WLAN
- HCI-UART, PCM/I2S for Bluetooth®

• Coexistence:

- Built-in advanced algorithms for Wi-Fi + Bluetooth® coexistence
- 2-wire SECI for external third party Bluetooth®/GPS/LTE radios

Note

1. Available per request.

CYW55571 functional block diagram – two antenna system

• General:

- Fully integrated programmable dynamic power management unit (PMU)
- Supports VBAT power supply range from 3.0 V to 4.8 V with internal regulator
- Supports 1.8 V VDDIO
- Supports 1340 bytes of OTP shared between Bluetooth® and WLAN for storing board parameters

- Package:

- FCBGA 12 x12 mm (0.65 mm ball pitch),
- WLCSP 5.3 x 5.7 mm (0.2 mm bump pitch)
- WLBGA 5.32 x 5.67 mm (0.35 mm ball pitch)
- 4-layer reference PCB design with FCBGA part with no blind and buried VIAs and only through hole VIAs
- 6-layer reference PCB design with WLBGA part is with blind and buried VIAs only

CYW55571 functional block diagram – two antenna system

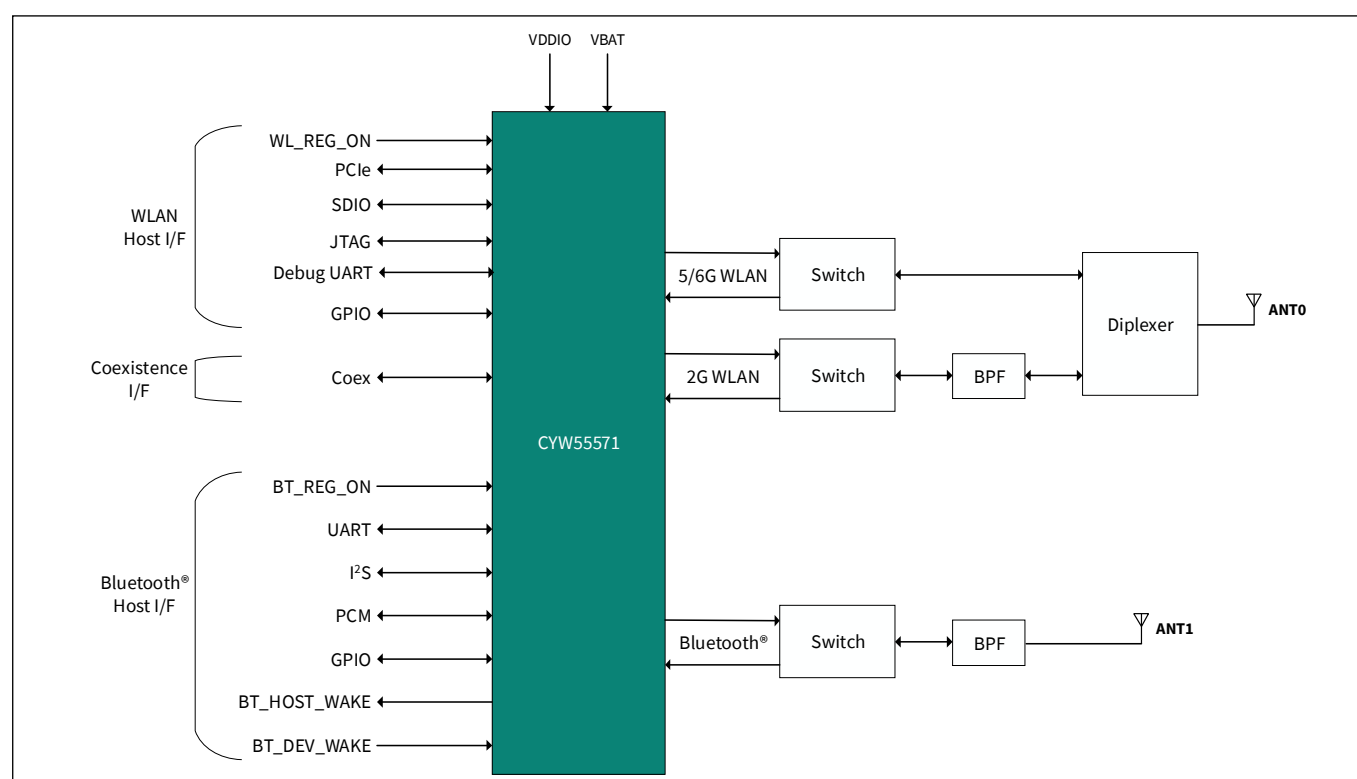


Figure 2 CYW55571 functional block diagram – two antenna system

CYW55571 functional block diagram — one antenna system

CYW55571 functional block diagram — one antenna system

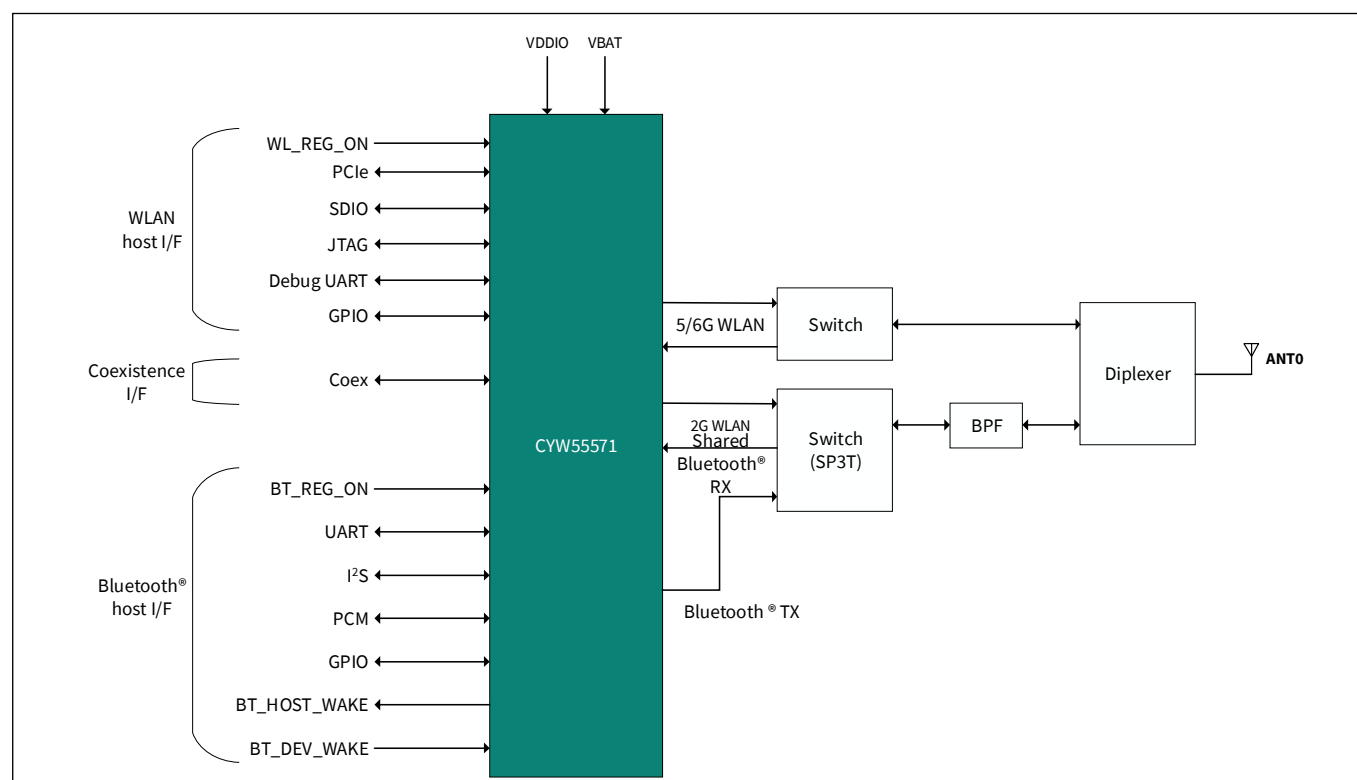


Figure 3 CYW55571 functional block diagram — one antenna system

Note

- Infineon recommends using a 2-antenna system to utilize the device's complete functionality: WLAN 1×1 2.4/5/6 GHz bands and Bluetooth® concurrently.

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Overview

1 Overview

1.1 Overview

The Infineon AIROC™ CYW55571 single-chip device provides the highest level of integration for commercial and consumer systems, with integrated IEEE 802.11 a/b/g/n/ac/ax MAC/baseband/radio (1×1), Bluetooth® 5.3+ Isochronous. It provides a small form-factor solution with minimal external components to drive down cost and allows for platform design flexibility in size, form, and function.

Table 1 Device options and features

Feature	FCFBGA	WLCSP	WLBGA
Package ball count	289-balls	486-balls	225-balls
PCIe	Yes	Yes	Yes
SDIO	Yes	Yes	Yes
UART	Yes	Yes	Yes
I ² S	Yes	Yes	Yes
GPIO	25	25	25

Figure 4 shows the interconnection of all the major physical blocks in CYW55571.

The Interconnection interfaces are described in greater detail in the subsequent sections of this document.

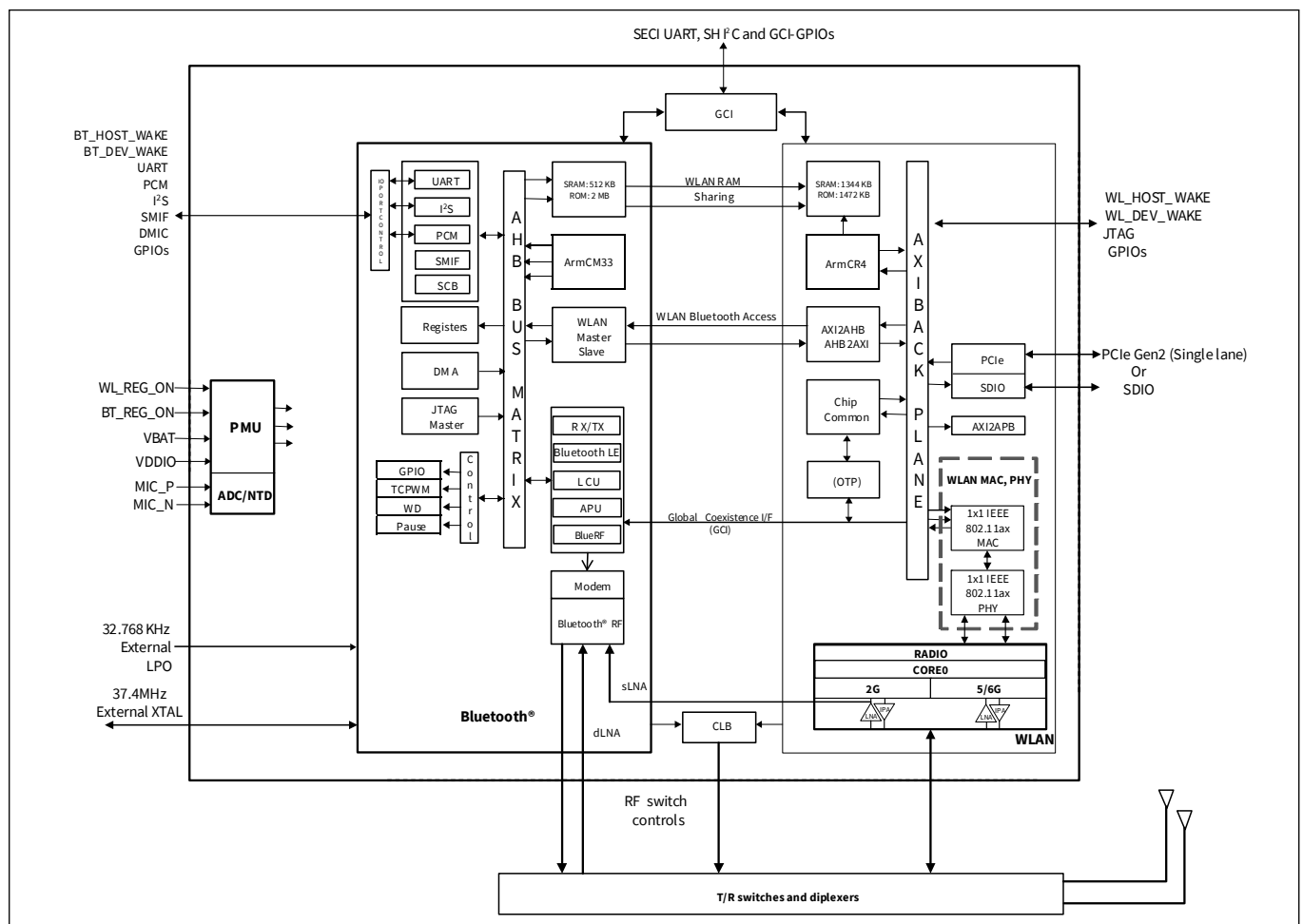


Figure 4 CYW55571 system block diagram

Overview**1.2 Standards compliance**

CYW55571 supports the following standards:

- Bluetooth® 2.1 + EDR, 3.0, 4.2, 5.0, 5.1, 5.2, 5.3
- IEEE 802.11ax
- IEEE 802.11ac mandatory and optional requirements for 20 MHz, 40 MHz, and 80 MHz channels
- IEEE 802.11a/b/g/n
- IEEE 802.11d/h
- IEEE 802.11i
- **Security:**
 - WPA/WPA2/WPA3 (Personal/Enterprise) with 192-bit encryption, Hardware accelerator (AES), and software support (CKIP)
- **WMM:**
 - IEEE 802.11r (Fast Roaming between APs)
 - IEEE 802.11w (Secure Management Frames)
- **IEEE 802.11 extensions:**
 - IEEE 802.11e QoS enhancements (In accordance with the WMM specification, QoS is already supported)
 - IEEE 802.11h 5/6 GHz extensions
 - IEEE 802.11i MAC enhancements

2 Power supplies and power management

2.1 Power supply topology

Two buck regulators, multiple LDO regulators, and a power management unit (PMU) are integrated into CYW55571. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth® and WLAN functions in embedded designs.

CYW55571 only requires two power supplies, VBAT and VDDIO, to be provided, with all additional voltages being generated by on-chip regulators.

Two control signals, BT_REG_ON and WL_REG_ON, are used to power-up the regulators and take the respective section out of reset. The two core Buck regulators, CBUCK and ABUCK, power up when either BT_REG_ON or WL_REG_ON are asserted. All regulators, Buck and LDO, are powered down when both BT_REG_ON and WL_REG_ON are deasserted.

CYW55571 allows for an extremely Low-power consumption mode by completely shutting down the CBUCK and ABUCK regulators. In this extremely low power state, MEMLPLDO and LPLDO (which are a low-power linear regulators supplied by the system VDDIO supply) provide CYW55571 with all the voltages it requires, thereby reducing leakage currents.

2.2 CYW55571 PMU features

- Core switching regulator (400 mA)
- Analog switching regulator (400 mA)
- BTLDO (400 mA)
- PALDO (800 mA)
- RFLDO (200 mA)
- VDDOUT_MISC (60 mA)

Figure 5 and **WLAN power management** illustrate the typical power topology for CYW55571. The shaded areas are external to CYW55571.



2.3 WLAN power management

CYW55571 has been designed with the stringent performance requirements of commercial/consumer applications in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the CYW55571 integrated RAM is a high-Vt memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. CYW55571 includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting CYW55571 into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power up sequences are fully programmable. Configurable, free-running counters (running at 32.768 kHz LPO clock) in the PMU sequencer are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. The slower clock speeds are used wherever possible.

CYW55571 WLAN power states are described as follows:

- **Active mode**— All WLAN blocks in CYW55571 are powered up and fully functional with active carrier sensing and frame transmission and reception. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- **Deep Sleep mode**— Most of the chip including both analog and digital domains and most of the regulators are powered off. All main clocks (PLL, crystal oscillator, or TCXO) are shutdown to reduce active power to the minimum. The PMU sequencer uses the 32.768 kHz LPO clock to keep track of time and wake up the chip and transition to Active mode as scheduled. The logic states in the digital core are saved and preserved into a retention memory in the always-ON domain before the digital core is powered off. Upon a wake-up event triggered by the PMU timers, an external interrupt, logic states in the digital core are restored to their pre-Deep Sleep settings to avoid lengthy HW reinitialization. In Deep Sleep mode, the primary source of power consumption is leakage current.
- **Power-down mode**— CYW55571 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

2.4 Power management unit (PMU) sequencing

The PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them.

The resource requests may come from several sources: clock requests from cores, the minimum resources defined in the ResourceMin register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of four states: enabled, disabled, transition_on, and transition_off and has a timer that contains '0' when the resource is enabled or disabled and a non-zero value in the transition states. The timer is loaded with the time_on or time_off value of the resource when the PMU determines that the resource must be enabled or disabled. That timer decrements on each 32.768 kHz PMU clock. When it reaches '0', the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is '0', the resource can go immediately from disabled to enabled. Similarly, a time_off value of '0' indicates that the resource can go immediately from enabled to disabled. The terms enable sequence and disable sequence refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

- Computes the required resource set based on requests and the resource dependency table.
- Decrements all timers whose values are non zero. If a timer reaches '0', the PMU clears the ResourcePending bit for the resource and inverts the Resource State bit.
- Compares the request with the current resource status and determines which resources must be enabled or disabled.

Power supplies and power management

- Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered-up dependents.
- Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

2.5 Power-off shutdown

CYW55571 provides a low-power shutdown feature that allows the device to be turned off while the host, and any other devices in the system, remain operational. When CYW55571 is not needed in the system, VDDIO_RF and VDDC are shut down while VDDIO remains powered. This allows CYW55571 to be effectively OFF while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shutdown state, provided VDDIO remains applied to CYW55571, all outputs are tristated, and most inputs signals are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, and enables CYW55571 to be fully integrated in an embedded device and take full advantage of the lowest power-savings modes.

When CYW55571 is powered ON from this state, it is the same as a normal power-up and the device does not retain any information about its state from before it was powered down.

2.6 Power-up/Power-down/Reset circuits

CYW55571 has two signals (see [Table 2](#)) that enable or disable Bluetooth® and WLAN circuits and internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see [Power-up sequence and timing](#).

Table 2 Power-up/Power-down/Reset control signals

Signal	Description
WL_REG_ON	This signal is used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW55571 regulators. When this pin is HIGH, the regulators are enabled and the WLAN section is out of reset. When this pin is LOW, all the WLAN section is in reset. If BT_REG_ON and WL_REG_ON are both low, all the regulators are disabled. This pin has an internal 50 kΩ pull-down resistor that is enabled by default and it can be disabled through programming.
BT_REG_ON	This signal is used by the PMU to power up the Bluetooth® section. It is also OR-gated with the WL_REG_ON input to control the internal CYW55571 regulators. When this pin is HIGH, the regulators are enabled and the Bluetooth® section is out of reset. When this pin is low, the Bluetooth® section is in reset. If BT_REG_ON and WL_REG_ON are both LOW, all the regulators are disabled. This pin has an internal 50 kΩ pull-down resistor that is enabled by default and can be disabled through programming.

Frequency references

3 Frequency references

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference may be used. A 32.768 kHz clock is also required for Low-power mode timing.

3.1 Crystal interface and clock generation

The AIROC™ CYW55571 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in **Figure 6**. See the reference schematics for the latest configuration.

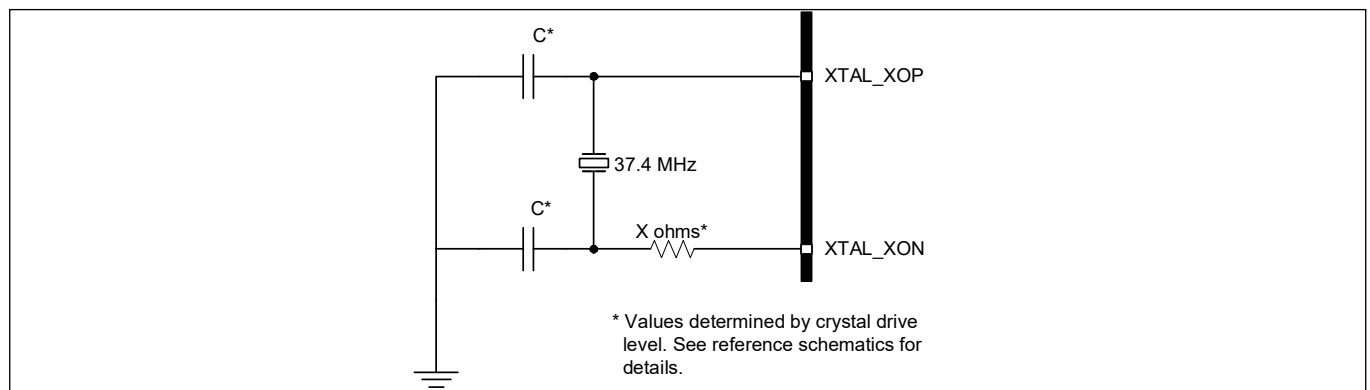


Figure 6 Recommended crystal oscillator configuration

The recommended default frequency reference is a 37.4 MHz crystal. The signal characteristics for the crystal oscillator interface are listed in **Table 3**.

Table 3 Crystal oscillator— requirements and performance

Parameter	Conditions/Notes	Crystal ^[3]			Unit
		Min	Typ	Max	
Frequency	2.4G, 5G, and 6G bands: IEEE 802.11ac/ax operation	–	37.4	–	MHz
Frequency tolerance over the lifetime of the equipment, including temperature ^[4]	Without trimming	-20.0	–	20.0	ppm
Crystal load capacitance	–	–	12.0	–	pF
ESR	–	–	–	60.0	Ω
Drive level	External crystal must be able to tolerate this drive level	200	–	–	μW
Input impedance XTAL_XOP	Resistive	–	–	–	kΩ
	Capacitive	–	–	7.5	pF

Notes

3. Use XTAL_XOP and XTAL_XON.
4. It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.

Frequency references

3.2 External frequency reference

As an alternative to a crystal, an external precision frequency reference can be provided. The recommended default frequency is 37.4 MHz, and it must meet the requirements listed in [Table 4](#).

The external frequency reference should be connected to the XTAL_XOP pin through an external 1000 pF coupling capacitor, as shown in [Figure 7](#). The internal clock buffer connected to this pin will be turned OFF when CYW55571 goes into sleep mode.

When the clock buffer turns ON and OFF there will be a small impedance variation. Power must be supplied to the XTAL_VDD_1P12 pin.

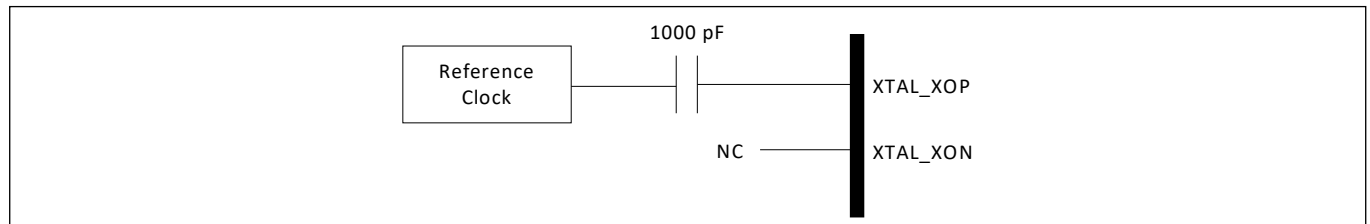


Figure 7 Recommended circuit to use with an external reference clock

Table 4 External clock—requirements and performance

Parameter	Conditions/Notes	External frequency reference			Unit
		Min	Typ	Max	
Frequency	2.4G, 5G, and 6G: IEEE 802.11ac/ax operation	–	37.4	–	MHz
Frequency tolerance over the lifetime of the equipment, including temperature ^[5]	Without trimming	-20.0	–	20	ppm
Input impedance (XTAL_XOP)	Resistive	30.0	100	–	kΩ
	Capacitive	–	–	7.5	pF
XTAL_XOP input low level	DC-coupled digital signal	0	–	0.2	V
XTAL_XOP input high level	DC-coupled digital signal	0.8	–	1.0	V
XTAL_XOP input voltage (see Figure 7)	AC-coupled analog signal	400	–	1000	mV _{p-p}
Duty cycle	37.4 MHz clock	40.0	50.0	60.0	%
Phase noise (IEEE 802.11b/g)	37.4 MHz clock at 10 kHz offset	–	–	-129	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	-136	dBc/Hz
Phase noise ^[6] (IEEE 802.11a)	37.4 MHz clock at 10 kHz offset	–	–	-137	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	-144	dBc/Hz
Phase noise ^[6] (IEEE 802.11n, 2.4 GHz)	37.4 MHz clock at 10 kHz offset	–	–	-134	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	-141	dBc/Hz
Phase noise ^[6] (IEEE 802.11n, 5/6 GHz)	37.4 MHz clock at 10 kHz offset	–	–	-142	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	-149	dBc/Hz

Notes

- It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.
- Assumes that external clock has a flat phase noise response above 100 kHz.

Frequency references
Table 4 External clock—requirements and performance *(continued)*

Parameter	Conditions/Notes	External frequency reference			Unit
		Min	Typ	Max	
Phase noise ^[6] (IEEE 802.11ac, 5/6 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–150	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–157	dBc/Hz
Phase noise ^[6] (IEEE 802.11ax, 5/6 GHz)	37.4 MHz clock at 10 kHz offset	–	–	–152	dBc/Hz
	37.4 MHz clock at 100 kHz offset	–	–	–159	dBc/Hz

Notes

5. It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.
6. Assumes that external clock has a flat phase noise response above 100 kHz.

3.3 External 32.768 kHz low-power oscillator

CYW55571 requires an external low-frequency clock for low-power mode timing. An external 32.768 kHz precision oscillator which meets the requirements listed in [Table 5](#) must be used.

Table 5 External 32.768 kHz sleep clock specifications

Parameter	LPO clock	Unit
Nominal input frequency	32.768	kHz
Frequency accuracy	±250	ppm
Duty cycle	30–70	%
Input signal amplitude	200–1800	mV, p–p
Signal type	Square-wave or sine-wave	–
Input impedance ^[7]	> 100k	Ω
	< 5	pF
Clock jitter ^[8] (during initial startup)	< 10,000	ppm

Notes

7. When power is applied or switched OFF.
8. The LPO_IN input receiver has ac-coupled capacitance on the input with the feedback resistor to maintain the common mode around VDDIO/2 and power supply noise should be maintained less than 100 mV to avoid any false glitches before the time constant (ac-coupled capacitance * feedback resistor, i.e., 100 μs) settles down.

4 Bluetooth® subsystem overview

The Infineon AIROC™ CYW55571 is a Bluetooth® 5.3 + EDR-compliant, baseband processor and 2.4 GHz transceiver. It features the highest level of integration and eliminates the need for all critical external components, thus minimizing the footprint, power consumption, and system cost of a Bluetooth® solution.

CYW55571 is the optimal solution for any Bluetooth® voice and/or data application. The Bluetooth® subsystem presents a standard Host controller interface (HCI) via a high-speed UART and PCM for audio. CYW55571 incorporates all Bluetooth® 5.2 features including LE-Audio and LE Isochronous channels.

The Bluetooth® transmitter also features a power amplifier with programmable Class 1 and Class 2 capabilities.

4.1 Features

- Supports features of Bluetooth® core specification v5.3:
 - LE Asynchronous channels
 - LE Power control
- Supports features of Bluetooth® core specification v5.1:
 - Additional advertising channels
 - Periodic advertising sync transfer (PAST)
 - GATT caching
- Supports features of Bluetooth® core specification v5.0:
 - LE 2Mbps
 - LE long range (LE-LR)
 - LE advertising extension
 - Slot availability masks (SAM)
 - Channel selection algorithm #2
 - High duty cycle non-connectable advertising
- Supports features of Bluetooth® core specification v4.0 + EDR:
 - Adaptive frequency hopping (AFH)
 - Quality of service (QoS)
 - Extended synchronous connections (eSCO)—Voice connections
 - Fast connect (interlaced page and inquiry scans)
 - Secure simple pairing (SSP)
 - Sniff subrating (SSR)
 - Encryption pause resume (EPR)
 - Extended inquiry response (EIR)
 - Link supervision timeout (LST)
- UART baud rates up to 4 Mbps
- Supports all Bluetooth® 4.2, 5.0, 5.1, 5.2, and 5.3 packet types
- Supports maximum Bluetooth® data rates over HCI UART
- Multi-point operation with up to seven active peripherals
 - Maximum of seven simultaneous active ACL links
 - Maximum of three simultaneous active SCO and eSCO connections with scatternet support
- Supports narrowband and wideband packet loss concealment
- Scatternet operation with up to four active piconets with background scan and support for scatter mode
- High-speed HCI UART transport support with low-power out-of-band BT_DEV_WAKE and BT_HOST_WAKE signaling (see [Host controller power management](#))

Bluetooth® subsystem overview

- Channel quality driven data rate and packet type selection
- Standard Bluetooth® test modes
- Extended radio and production test mode features
- Full support for power savings modes
 - Bluetooth® clock request
 - Bluetooth® standard sniff
 - Deep Sleep modes and software regulator shutdown
- TCXO input and auto-detection of all standard handset clock frequencies. Also supports a low-power crystal, which can be used during power save mode for better timing accuracy.

4.2 Bluetooth® radio

CYW55571 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth® wireless frequency band. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. It is fully compliant with the Bluetooth® radio specification and EDR specification and meets or exceeds the requirements to provide the highest communication link quality of service.

4.2.1 Transmit (TX)

CYW55571 features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates $\pi/4$ -DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support EDR. The transmitter is compatible with Bluetooth® Low Energy specification. The transmitter PA can be programmed to provide Bluetooth® class 1 or class 2 operation.

4.2.2 Digital modulator

The digital modulator performs the data modulation and filtering required for the GFSK, $\pi/4$ -DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

4.2.3 Digital demodulator and bit synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit-synchronization algorithm.

4.2.4 Power amplifier (PA)

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. For applications in which Bluetooth® is integrated next to a cellular radio, external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

4.2.5 Receiver (RX)

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology with built-in out-of-band attenuation enables CYW55571 to be used in most applications with minimal off-chip filtering. For applications, in which the Bluetooth® function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

4.2.6 Digital demodulator and bit synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

4.2.7 Receiver Signal Strength Indicator (RSSI)

The radio portion of CYW55571 provides a RSSI signal to the baseband, so that the controller can take part in a Bluetooth® power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

4.2.8 Local oscillator (LO) generation

The LO generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. CYW55571 uses an internal RF and IF loop filter.

4.2.9 Calibration

CYW55571 radio transceiver features an automated calibration scheme that is fully self contained in the radio. No user interaction is required during normal operation or during manufacturing to provide the optimal performance. The calibration optimizes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. The calibration occurs transparently during normal operation during the settling time of the hops and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

5 Bluetooth® baseband core (BBC)

The BBC implements all of the time-critical functions required for high-performance Bluetooth® operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth® slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, Data Deframing, Forward Error Correction (FEC), Header Error Control (HEC), Cyclic Redundancy Check (CRC), Data Decryption, and Data Dewhitening in the receiver
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter

5.1 Bluetooth® 5.2 and 4.2 features

The BBC supports all Bluetooth® 5.2 and 4.2 features, with the following benefits:

- Dual-mode Bluetooth® low energy (Bluetooth® and Bluetooth® LE operation)
- Bluetooth® LE LE-2Mbps mode, LE-Long Range mode, Advertising Extensions, Slot Availability Masks.
- Extended inquiry response (EIR): Shortens the time to retrieve the device name, specific profile, and operating mode.
- Encryption pause resume (EPR): Enables the use of Bluetooth® technology in a much more secure environment. Sniff subrating (SSR): Optimizes power consumption for low duty cycle asymmetric data flow, which subsequently extends battery life.
- Secure simple pairing (SSP): Reduces the number of steps for connecting two devices, with minimal or no user interaction required.
- Link supervision time out (LSTO): Additional commands added to HCI and link management protocol (LMP) for improved link time-out supervision.
- QoS enhancements: Changes to data traffic control, which results in better link performance. Audio, human interface device (HID), bulk traffic, SCO, and enhanced SCO (eSCO) are improved with the erroneous data (ED) and packet boundary flag (PBF) enhancements.

5.2 Link control layer

The link control layer is part of the Bluetooth® link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task performs a different state in the Bluetooth® link controller.

- Major states:
 - Standby
 - Connection
- Substates
 - Page
 - Page Scan
 - Inquiry
 - Inquiry Scan
 - Sniff

5.3 Test mode support

The AIROC™ CYW55571 fully supports Bluetooth® Test mode as described in Part I:1 of the Specification of the Bluetooth® System v3.0. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth® Test mode, CYW55571 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
 - Simplifies some type-approval measurements (Japan)
 - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
 - Receiver output directed to I/O pin
 - Allows for direct BER measurements using standard RF test equipment
 - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
 - Eight-bit fixed pattern or PRBS-9
 - Enables modulated signal measurements with standard RF test equipment

5.4 Bluetooth® power management unit (PMU)

The Bluetooth® PMU provides power management features that can be invoked by either software through power management registers or packet handling in the baseband core.

The power management functions provided by CYW55571 are:

- **RF power management**
- **Host controller power management**
- **BBC power management**

5.4.1 RF power management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver. The transceiver then processes the power-down functions accordingly.

5.4.2 Host controller power management

When running in UART mode, CYW55571 may be configured so that dedicated signals are used for power management hand-shake between CYW55571 and host. The basic power saving functions supported by those hand-shake signals include the standard Bluetooth® defined power savings modes and standby modes of operation.

Table 6 describes the power-control hand-shake signals used with the UART interface.

Table 6 Power control pin description

Signal	Type	Description
BT_DEV_WAKE	I	Bluetooth® device wake-up: Signal from host to CYW55571 indicating that the host requires attention. • Asserted: The Bluetooth® device must wake-up or remain awake. • Deasserted: The Bluetooth® device may Sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted HIGH or LOW.
BT_HOST_WAKE	O	Host wake up. Signal from CYW55571 to the host indicating that CYW55571 requires attention. • Asserted: host device must wake-up or remain awake. • Deasserted: host device may sleep when Sleep criteria are met. The polarity of this signal is software configurable and can be asserted HIGH or LOW.

Note

9. Pad function Control register is set to 0 for these pins. See [DC characteristics](#) for more details.

5.4.3 BBC power management

The following are low-power operations for the BBC:

- Physical layer packet-handling turns the RF on and off dynamically within transmit/receive packets.
- Bluetooth®-specified low-power connection modes: sniff, hold, and park. While in these modes, CYW55571 runs on the low-power oscillator and wakes up after a predefined time period.
- A low-power shutdown feature allows the device to be turned off while the host and any other devices in the system remain operational. When CYW55571 is not needed in the system, the RF and core supplies are shut down while the I/O remains powered. This allows CYW55571 to effectively be off while keeping the I/O pins powered so they do not draw extra current from any other devices connected to the I/O. During the low-power shut-down state, provided VDDIO remains applied to CYW55571, all outputs are tristated, and most input signals are disabled. The input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system and enables CYW55571 to be fully integrated in an embedded device to take full advantage of the lowest power-saving modes. Two CYW55571 input signals are designed to be high-impedance inputs that do not load the driving signal even if the chip does not have VDDIO power supplied to it: the frequency reference input (XTAL_XOP) and the 32.768 kHz input (LPO_IN). When CYW55571 is powered on from this state, it is the same as a normal power-up, and the device does not contain any information about its state from the time before it was powered down.

5.4.4 Wideband speech (WBS)

CYW55571 provides support for WBS using on-chip SmartAudio technology. CYW55571 can perform subband codec (SBC), as well as mSBC, encoding and decoding of linear 16 bits at 16 kHz (256 Kbps rate) transferred over the PCM bus.

5.4.5 Packet loss concealment (PLC)

The PLC improves apparent audio quality for systems with marginal link performance. Bluetooth® messages are sent in packets. When a packet is lost, it creates a gap in the received audio bit-stream.

Packet loss can be mitigated in several ways:

- Fill in zeros
- Ramp down the output audio signal toward zero (this is the method used in current Bluetooth® headsets)
- Repeat the last frame (or packet) of the received bit-stream and decode it as usual (frame repeat)

These techniques cause distortion and popping in the audio stream. CYW55571 uses a proprietary waveform extension algorithm to provide dramatic improvement in the audio quality. **Figure 8** and **Figure 9** show audio waveforms without and with PLC. The PLC/BEC algorithms also support wideband speech.

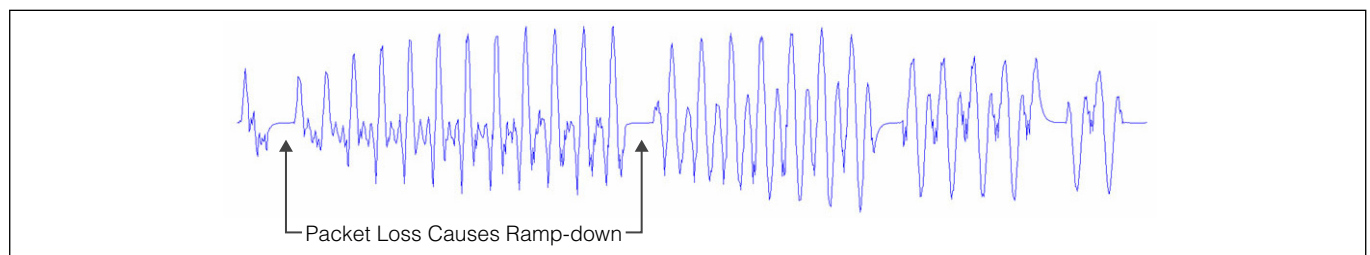


Figure 8 CVSD decoder output waveform without PLC

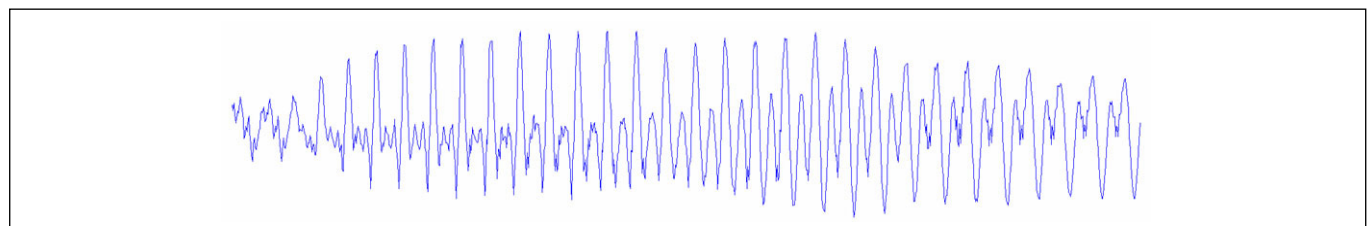


Figure 9 CVSD decoder output waveform after applying PLC

5.4.6 Audio rate-matching algorithms

CYW55571 has an enhanced rate-matching algorithm that uses interpolation algorithms to reduce audio stream jitter that may be present when the rate of audio data coming from the host is not the same as the Bluetooth® data rates.

5.4.7 Codec encoding

CYW55571 can support SBC and mSBC encoding and decoding for wideband speech.

5.4.8 Multiple simultaneous A2DP audio stream

CYW55571 has the ability to take a single audio stream and output it to multiple Bluetooth® devices simultaneously. This allows a user to share his or her music (or any audio stream) with a friend.

5.4.9 Burst buffer operation

CYW55571 has a data buffer that can buffer data being sent over the HCI and audio transports, then send the data at an increased rate. This mode of operation allows the host to sleep for the maximum amount of time, dramatically reducing system current consumption.

5.5 Adaptive frequency hopping

CYW55571 gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency-hop map.

5.6 Advanced Bluetooth®/WLAN coexistence

CYW55571 includes advanced coexistence technologies that are only possible with a Bluetooth®/WLAN integrated die solution. These coexistence technologies are targeted at Commercial/Consumer applications such as WLAN + eSCO and WLAN + High fidelity Bluetooth® Stereo.

It is recommended that WLAN and Bluetooth® have separate dedicated antenna for maximum simultaneous traffic. However, CYW55571 is also capable of supporting platforms that share an antenna between WLAN and Bluetooth®. Advanced Bluetooth®/WLAN coexistence algorithms allow for simultaneous WLAN and Bluetooth® reception and transmit antenna arbitration.

CYW55571 integrated solution enables MAC-layer signaling (firmware) and a greater degree of sharing via an enhanced coexistence interface. Information is exchanged between the Bluetooth® and WLAN cores without host processor involvement.

CYW55571 also supports Transmit Power Control on the WLAN STA together with standard Bluetooth® TPC to limit mutual interference and receiver desensitization. Preemption mechanisms are utilized to prevent AP transmissions from colliding with Bluetooth® frames. Improved channel classification techniques have been implemented in Bluetooth® for faster and more accurate detection and elimination of interferers (including non-WLAN 2.4 GHz interference).

The Bluetooth® AFH classification is also enhanced by the WLAN core's channel information.

5.7 Fast connection (Interlaced page and inquiry Scans)

CYW55571 supports page scan and inquiry scan modes that significantly reduce the average inquiry response and connection times. These scanning modes are compatible with the Bluetooth® v2.1 page and inquiry procedures.

6 Microprocessor and memory unit for Bluetooth®

The Bluetooth® microprocessor core is based on the Arm® Cortex®-M33 with embedded ICE-RT debug and JTAG interface units.

The Arm® core is paired with a memory unit that contains 2 MB of ROM memory for program storage and boot ROM, and 512 KB of RAM for data scratch-pad and patch RAM code. At power-up, the lower-layer protocol stack is executed from the internal ROM memory.

The external patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or features additions. These patches may be downloaded from the host to CYW55571 through the UART transports.

6.1 RAM, ROM, and Patch memory

CYW55571 Bluetooth® core has 512 KB of internal RAM which is mapped between general purpose scratch pad memory and patch memory and 2 MB of ROM used for the lower-layer protocol stack, test mode software, and boot ROM. The patch memory capability enables the addition of code changes for purposes of feature additions and bug fixes to the ROM memory.

6.2 Reset

CYW55571 has an integrated power-on reset circuit that resets all circuits to a known power-on state. The Bluetooth® power-on reset (POR) circuit is out of reset after BT_REG_ON goes High. If BT_REG_ON is LOW, then the POR circuit is held in reset.

7 Bluetooth® peripheral transport units

7.1 Media transports

The AIROC™ CYW55571 supports HFP and A2DP codec controllers with optimized I²S and PCM transports for Bluetooth® audio.

HFP codec interface controller

- Supported by PCM and I²S transports and bi-directional operations
- PCM
 - Sample rates 8k for NBS and 16k for WBS supported
 - Dual stream use cases can concurrently use NBS and WBS
 - Sample width is limited to 16 bits
 - Synchronization clock width of 1 or 3 (short or long)
 - Bit clocks of 128k, 256k, 512k, 1024k and 2024k, the only difference being the number of 16 bit slots
 - HFP samples can be taken from any available slot. Slot 0 is the default slot
- I²S
 - Supports bit clocks of 256k (NBS) and 512K (WBS).
 - HFP samples can be taken from either left or right. Left is the default

A2DP codec controller

- Supported by I²S transport in a single direction, either in or out but not both
- Two channels, left and right. Mono is not supported.
- Sample rates: 44.1k or 48k
- Sample width is limited to 16 bits
- Supports bit clocks of 32 times the sample rate, 1.411200 (44.1k) or 1536000 (48k) and not adjustable

7.2 PCM interface

CYW55571 supports two independent PCM interfaces that share the pins with the I²S interfaces. The PCM Interface on CYW55571 can connect to linear PCM codec devices in Master/Slave mode. In Master mode, CYW55571 generates the BT_PCM_CLK and BT_PCM_SYNC signals, and in Slave mode, these signals are provided by another master on the PCM interface and are inputs to CYW55571.

The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

7.2.1 Slot mapping

CYW55571 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate of 128 kHz, 512 kHz, or 1024 kHz. The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16 respectively. The transmit and receive PCM data from a SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

7.2.2 Frame synchronization

CYW55571 supports both short and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the

Bluetooth® peripheral transport units

audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

7.2.3 Data formatting

CYW55571 may be configured to generate and accept several different data formats. For conventional Narrowband speech mode, CYW55571 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked Most Significant Bit (MSb) first.

7.2.4 Wideband speech support

When the host encodes WBS packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64 Kbps bit rate. CYW55571 also supports slave transparent mode using a proprietary rate-matching scheme. In SBCCode mode, linear 16-bit data at 16 kHz (256 Kbps rate) is transferred over the PCM bus.

7.2.5 Burst PCM mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24 MHz. This mode of operation is initiated with an HCI command from the host.

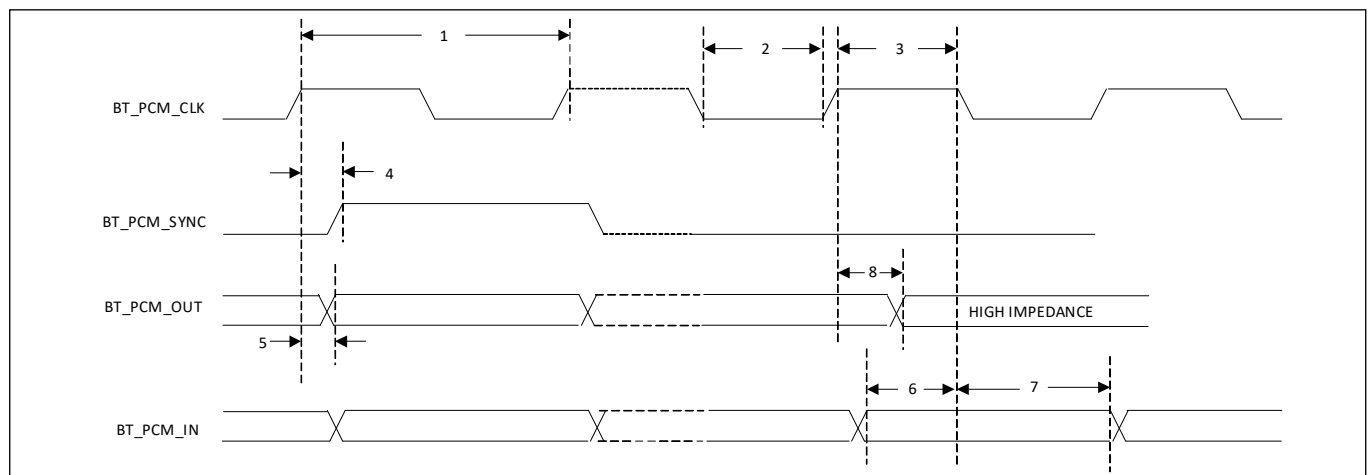
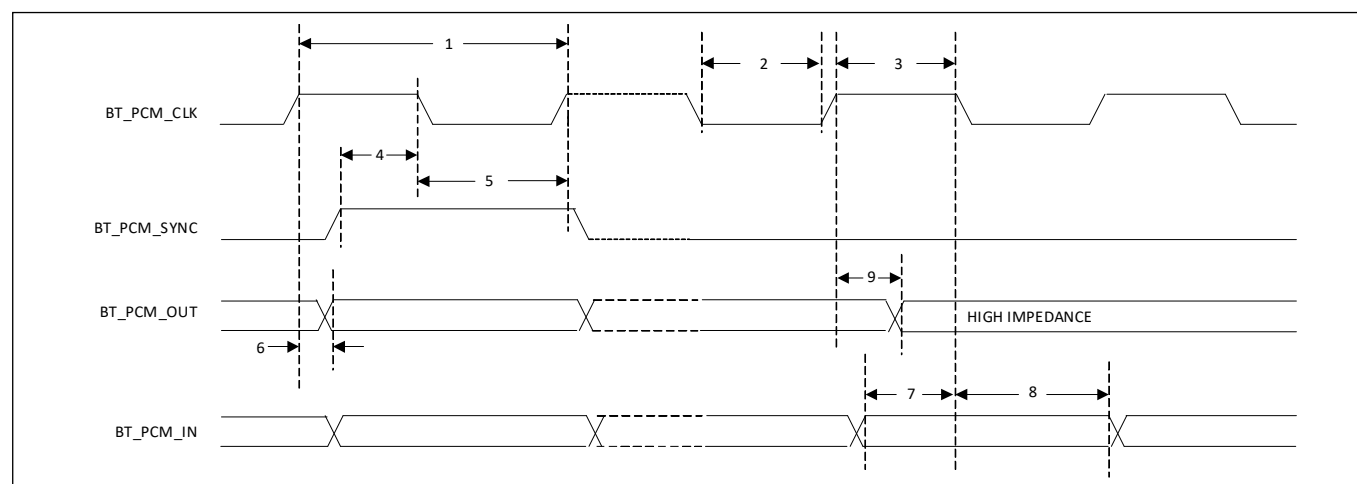
7.2.6 PCM interface timing**7.2.6.1 Short frame sync, master mode**

Figure 10 PCM timing diagram (short frame sync, master mode)

Bluetooth® peripheral transport units
Table 7 PCM interface timing specifications (short frame sync, master mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	BT_PCM_SYNC delay	0	–	25.0	ns
5	BT_PCM_OUT delay	0	–	25.0	ns
6	BT_PCM_IN setup	8.0	–	–	ns
7	BT_PCM_IN hold	8.0	–	–	ns
8	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high-Z	0	–	25.0	ns

7.2.6.2 Short frame sync, slave mode

Figure 11 PCM timing diagram (short frame sync, slave mode)
Table 8 PCM interface timing specifications (short frame sync, slave mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	BT_PCM_SYNC setup	8.0	–	–	ns
5	BT_PCM_SYNC hold	8.0	–	–	ns
6	BT_PCM_OUT delay	0	–	25.0	ns
7	BT_PCM_IN setup	8.0	–	–	ns
8	BT_PCM_IN hold	8.0	–	–	ns
9	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high-Z	0	–	25.0	ns

7.2.6.3 Long frame sync, master mode

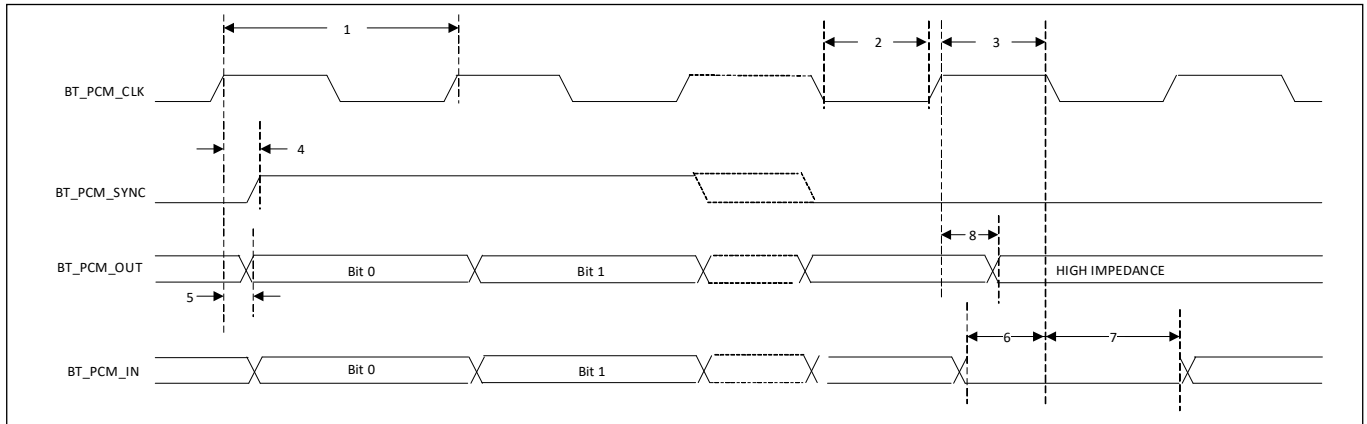


Figure 12 PCM timing diagram (long frame sync, master mode)

Table 9 PCM interface timing specifications (long frame sync, master mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	BT_PCM_SYNC delay	0	–	25.0	ns
5	BT_PCM_OUT delay	0	–	25.0	ns
6	BT_PCM_IN setup	8.0	–	–	ns
7	BT_PCM_IN hold	8.0	–	–	ns
8	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high-Z	0	–	25.0	ns

7.2.6.4 Long frame sync, slave mode

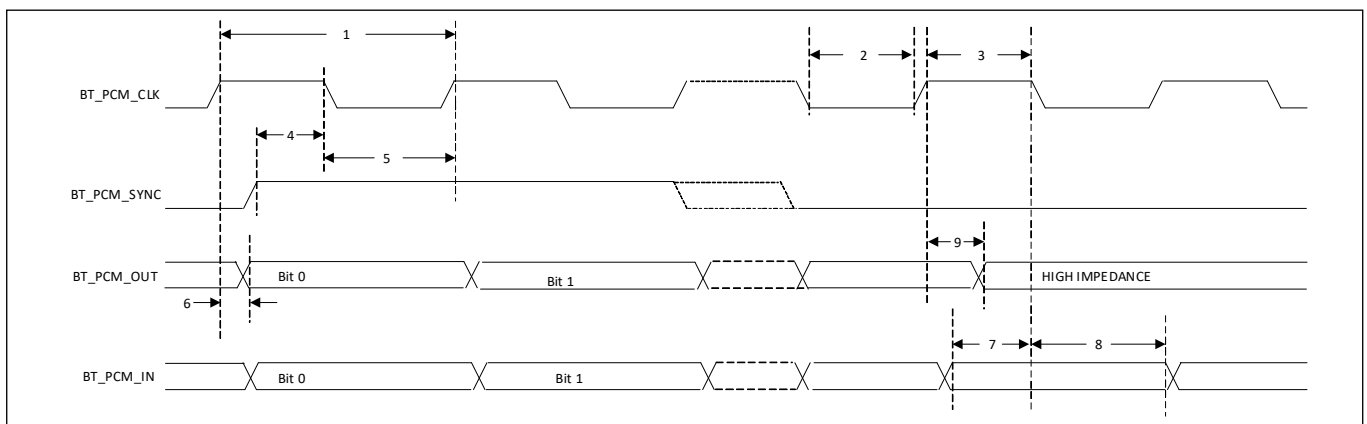
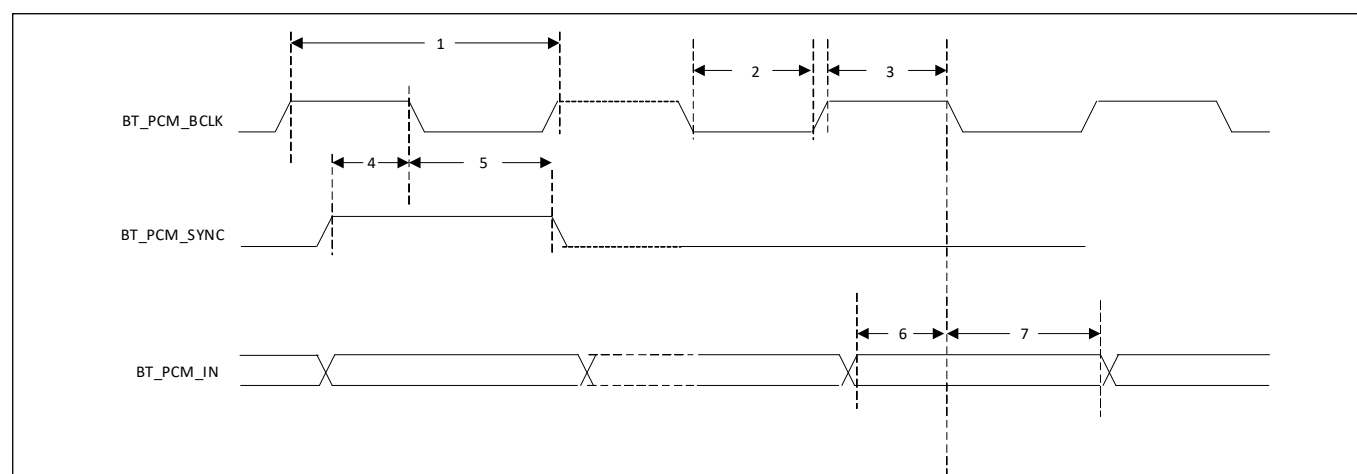


Figure 13 PCM timing diagram (long frame sync, slave mode)

Bluetooth® peripheral transport units
Table 10 PCM interface timing specifications (long frame sync, slave mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	12.0	MHz
2	PCM bit clock LOW	41.0	–	–	ns
3	PCM bit clock HIGH	41.0	–	–	ns
4	BT_PCM_SYNC setup	8.0	–	–	ns
5	BT_PCM_SYNC hold	8.0	–	–	ns
6	BT_PCM_OUT delay	0	–	25.0	ns
7	BT_PCM_IN setup	8.0	–	–	ns
8	BT_PCM_IN hold	8.0	–	–	ns
9	Delay from rising edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high-Z	0	–	25.0	ns

7.2.6.5 Short frame sync, burst mode

Figure 14 PCM burst mode timing diagram (receive only, short frame sync)
Figure 15 PCM burst mode (receive only, short frame sync)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	24.0	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	BT_PCM_SYNC setup	8.0	–	–	ns
5	BT_PCM_SYNC hold	8.0	–	–	ns
6	BT_PCM_IN setup	8.0	–	–	ns
7	BT_PCM_IN hold	8.0	–	–	ns

7.2.6.6 Long frame sync, burst mode

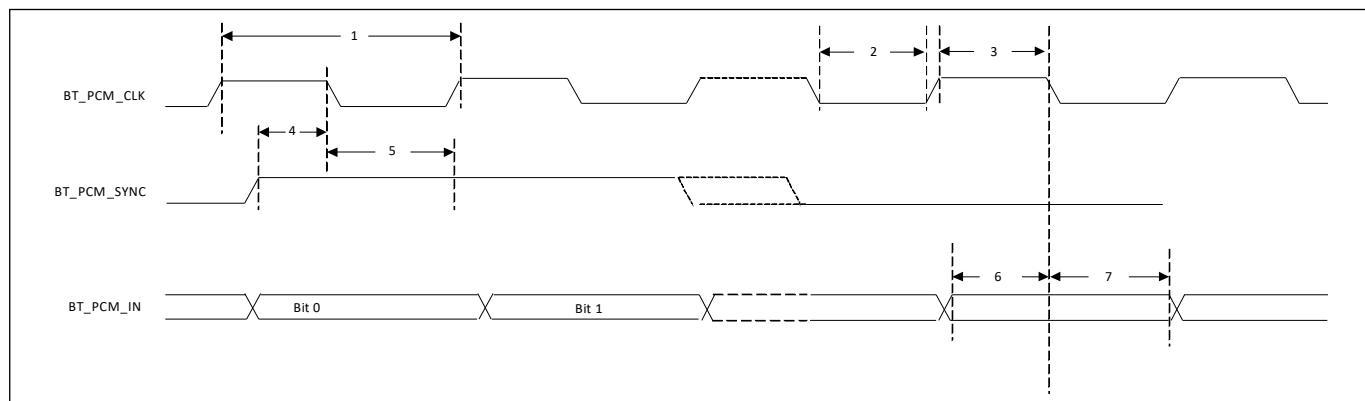


Figure 16 PCM burst mode timing diagram (receive only, long frame sync)

Table 11 PCM burst mode (receive only, long frame sync)

Reference	Characteristics	Min	Typ	Max	Unit
1	PCM bit clock frequency	–	–	24.0	MHz
2	PCM bit clock LOW	20.8	–	–	ns
3	PCM bit clock HIGH	20.8	–	–	ns
4	BT_PCM_SYNC setup	8.0	–	–	ns
5	BT_PCM_SYNC hold	8.0	–	–	ns
6	BT_PCM_IN setup	8.0	–	–	ns
7	BT_PCM_IN hold	8.0	–	–	ns

7.2.7 I²S interface

CYW55571 has the following I²S signals:

- I²S clock: BT_I2S_CLK
- I²S Word Select: BT_I2S_WS
- I²S Data Out: BT_I2S_DO
- I²S Data In: BT_I2S_DI

BT_I2S_CLK and BT_I2S_WS become outputs in Master mode and inputs in Slave mode, whereas BT_I2S_DO always stays as an output. The channel word length is 16 bits, and the data is justified so that the MSb of the left-channel data is aligned with the MSb of the I²S bus, in accord with the I²S specification. The MSb of each data word is transmitted one bit clock cycle after the BT_I2S_WS transition, synchronous with the falling edge of the bit clock. Left-channel data is transmitted when BT_I2S_WS is LOW, and right-channel data is transmitted when BT_I2S_WS is HIGH. Data bits sent by CYW55571 are synchronized with the falling edge of BT_I2S_CLK and should be sampled by the receiver on the rising edge of BT_I2S_CLK.

Bluetooth® peripheral transport units
7.2.7.1 I²S timing

Note Timing values specified in [Table 12](#) are relative to high and low threshold levels.

Table 12 Timing for I²S transmitters and receivers

	Transmitter				Receiver				Notes
	Lower limit		Upper limit		Lower limit		Upper limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock period T	T _{tr}	–	–	–	T _r	–	–	–	[10]
Master mode: Clock generated by transmitter or receiver									
HIGH t _{HC}	0.35 × T _{tr}	–	–	–	0.35 × T _{tr}	–	–	–	[11]
LOW t _{LC}	0.35 × T _{tr}	–	–	–	0.35 × T _{tr}	–	–	–	[11]
Slave mode: Clock accepted by transmitter or receiver									
HIGH t _{HC}	–	0.35 × T _{tr}	–	–	–	0.35 × T _{tr}	–	–	[12]
LOW t _{LC}	–	0.35 × T _{tr}	–	–	–	0.35 × T _{tr}	–	–	[12]
Rise time t _{RC}	–	–	0.15 × T _{tr}	–	–	–	–	–	[13]
Transmitter									
Delay t _{dtr}	–	–	–	0.8 × T	–	–	–	–	[14]
Hold time t _{htr}	0	–	–	–	–	–	–	–	[13]
Receiver									
Setup time t _{sr}	–	–	–	–	0.2 × T _r	–	–	–	[15]
Hold time t _{hr}	–	–	–	–	0.2 × T _r	–	–	–	[15]

Notes

- The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
- At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
- In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35 \times T_r$, any clock that meets the requirements can be used.
- Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax} , where t_{RCmax} is not less than $0.15 \times T_{tr}$.
- To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
- The data setup and hold time must not be less than the specified receiver setup and hold time.

Note The time periods specified in [Figure 17](#) and [Figure 18](#) are defined by the transmitter speed. The receiver specifications must match transmitter performance.

Bluetooth® peripheral transport units

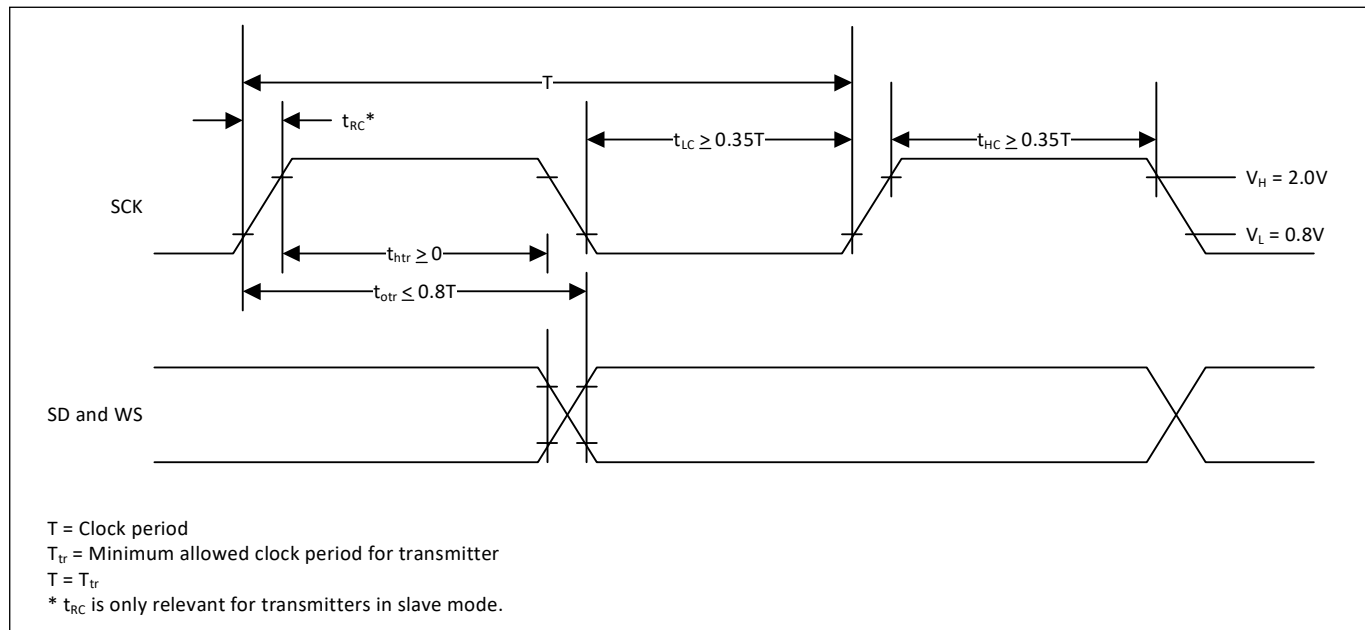


Figure 17 I²S transmitter timing

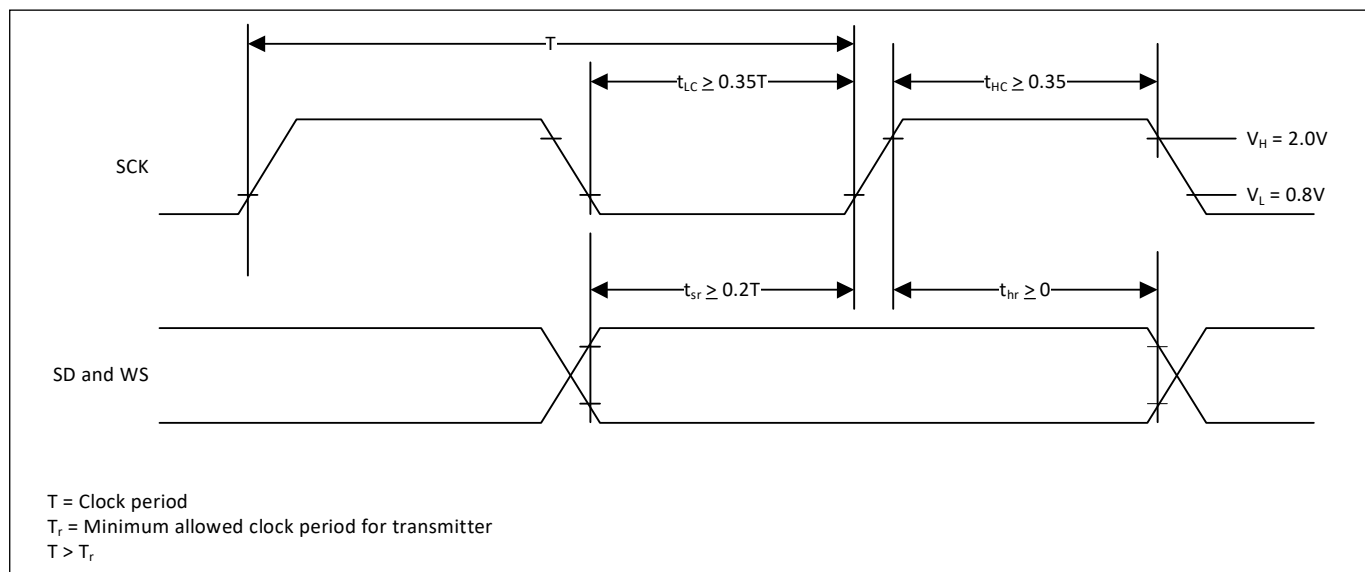


Figure 18 I²S receiver timing

7.3 UART interface

The CYW55571 UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The baud rate may be selected through a vendor-specific UART HCI command.

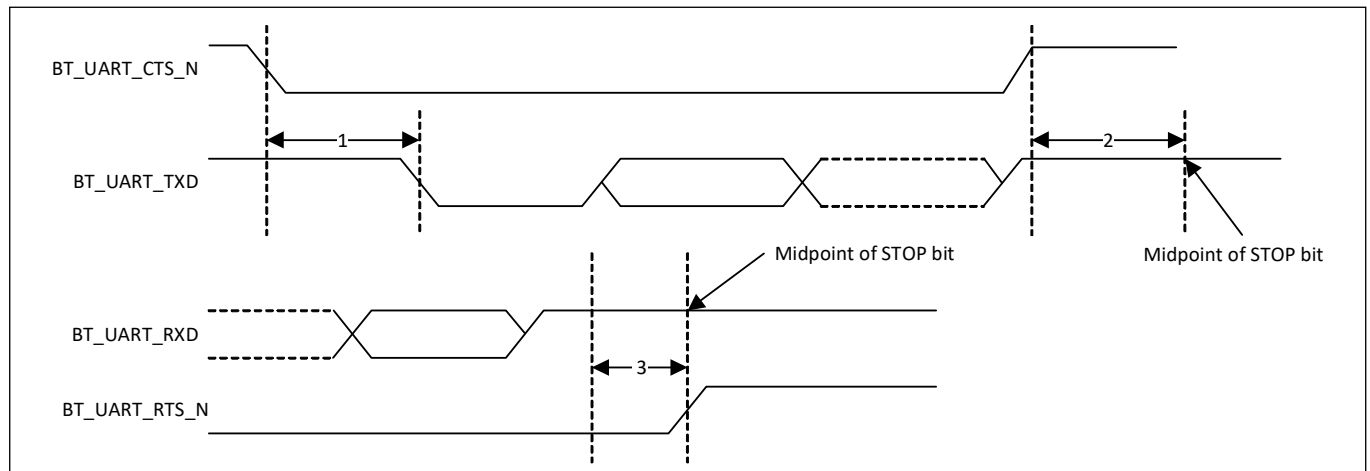
UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA/CPU. The UART supports the Bluetooth® 5.0 UART HCI specification. The default baud rate is 115.2 Kbaud.

The CYW55571 UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The CYW55571 UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within $\pm 2\%$.

Table 13 Example of common baud rates

Desired rate	Actual rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

Bluetooth® peripheral transport units

Figure 19 **UART timing**
Table 14 **UART timing specifications**

Reference	Characteristics	Min	Typ	Max	Unit
1	Delay time, BT_UART_CTS_N LOW to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N HIGH before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N HIGH	–	–	0.5	Bit periods

8 WLAN Global functions

8.1 WLAN CPU and Memory subsystem

The AIROC™ CYW55571 WLAN section includes an integrated Arm® Cortex®-R4 32-bit processor with internal RAM and ROM. The on-chip memory for the CPU includes 1344 KB SRAM and 1472 KB ROM. The Arm® Cortex®-R4 processor implements the Arm® v7-R architecture with support for the Thumb-2 instruction set.

Using multiple technologies to reduce cost, the Arm® Cortex®-R4 offers improved memory utilization, reduced pin overhead, and reduced silicon area. It supports independent buses for Code and Data access (Icode/Dcode and system buses), integrated sleep modes, and extensive debug features including real-time tracing of program execution.

8.2 One-Time programmable (OTP) memory

Various hardware configuration parameters may be stored in an internal one-time programmable (OTP) memory, which is read by the system software after device reset. In addition, customer-specific parameters, including the system vendor ID and the MAC address can be stored, depending on the specific board design. Up to 348 bytes of user-accessible OTP are available.

The initial state of all bits in an unprogrammed OTP device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with the Infineon WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package.

8.3 GPIO interface

CYW55571 has fifteen GPIO pins in the WLAN section that can be used to connect to various external devices. Upon power-up and reset, these pins become tristated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. In addition, the GPIO pins can be assigned to various other functions, see [Table 22](#).

8.4 External coexistence interface

An external handshake interface is available to enable signaling between the device and an external co-located wireless device, such as LTE to manage wireless medium sharing for optimal performance. [Figure 20](#) shows the LTE coexistence interface (including UART). See [Table 22](#) for further details on multiplexed signals, such as the GPIO pins.

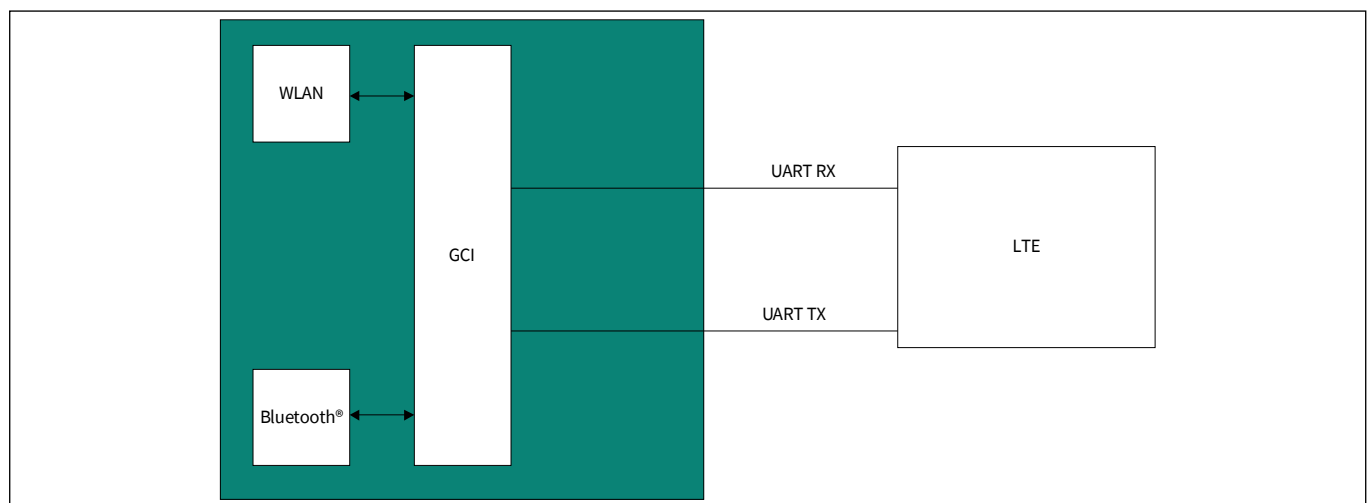


Figure 20 Multi-point global coexistence interface

WLAN Global functions

Baud rates are derived from the crystal clock. For rates higher than a crystal_frequency/16, the baud rate is an integer divide of the crystal frequency. [Table 15](#) shows the values for a 37.4 MHz crystal.

Table 15 Baud rates for a 37.4 MHz crystal

Division	XTAL	Baud rate (Mbps)
12	37.4/12	3.116667
13	37.4/13	2.876923
14	37.4/14	2.671429
15	37.4/15	2.493333
16	37.4/16	2.3375

8.5 Debug UART interface

One 2-wire UART interface can be enabled by software as an alternate function on GPIO pins. See [Table 22](#). Provided primarily for debugging during development, this UART enables CYW55571 to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and provides a FIFO size of 64 × 8 in each direction.

8.6 FAST UART interface

A high-speed 4-wire CTS/RTS UART interface can be enabled by software as an alternate function on GPIO pins. Refer to [Table 22](#). Provided primarily for control word exchange, this UART enables the chip to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and provides a FIFO size of 64 × 8 in each direction.

8.7 JTAG interface

CYW55571 supports the IEEE 1149.1 JTAG boundary scan standard for performing device package and PCB assembly testing during manufacturing. In addition, the JTAG interface allows Infineon to assist customers by using proprietary debug and characterization test tools during board bring-up. Therefore, it is highly recommended to provide access to the JTAG pins by means of test points or a header on all PCB designs. See [Table 22](#) for JTAG pin assignments.

WLAN host interface

9 WLAN host interface

9.1 SDIO v3.0

The following SDIO v3.0 modes are supported:

- DS: Default speed (DS) up to 25 MHz, including 1 and 4-bit modes (1.8 V signaling)
- SDR12: SDR up to 25 MHz (1.8 V signaling)
- SDR25: SDR up to 50 MHz (1.8 V signaling)
- SDR50: SDR up to 100 MHz (1.8 V signaling)
- SDR104: SDR up to 208 MHz (1.8 V signaling)
- DDR50: DDR up to 50 MHz (1.8 V signaling)

Note CYW55571 is backward compatible with SDIO v2.0 host interfaces.

The SDIO interface also has the ability to map the interrupt signal on to a GPIO pin for applications requiring an interrupt different from the one provided by the SDIO interface. The ability to force control of the gated clocks from within the device is also provided. SDIO mode is enabled by strapping options. See [Table 21](#) WLAN GPIO Functions and Strapping options.

The following three functions are supported:

- Function 0 Standard SDIO function (Max. BlockSize/ByteCount = 32B)
- Function 1 Backplane Function to access the internal system-on-chip (SoC) address space (Max. BlockSize/ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max. BlockSize/ByteCount = 512B)

9.1.1 SDIO pins

Table 16 SDIO pin descriptions

SD 4-bit mode		SD 1-bit mode	
DATA0	Data line 0	DATA	Data line
DATA1	Data line 1 or Interrupt	IRQ	Interrupt
DATA2	Data line 2 or Read Wait	RW	Read Wait
DATA3	Data line 3	N/C	Not used
CLK	Clock	CLK	Clock
CMD	Command line	CMD	Command line

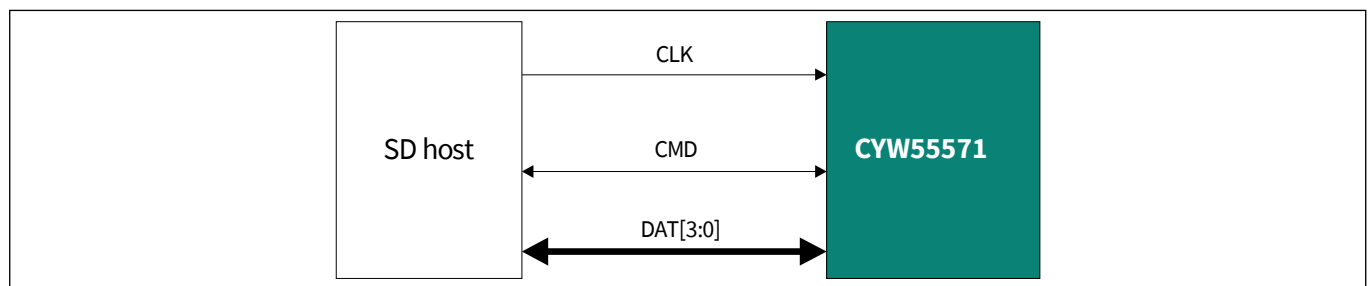
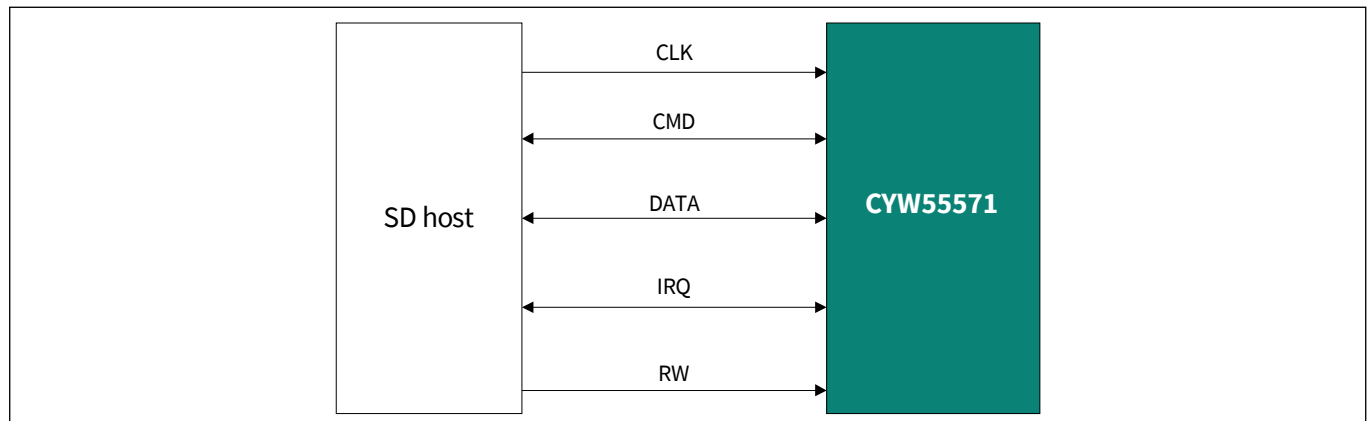


Figure 21 Signal connections to SDIO host (SD 4-bit mode)

WLAN host interface

Figure 22 Signal connections to SDIO host (SD 1-bit mode)

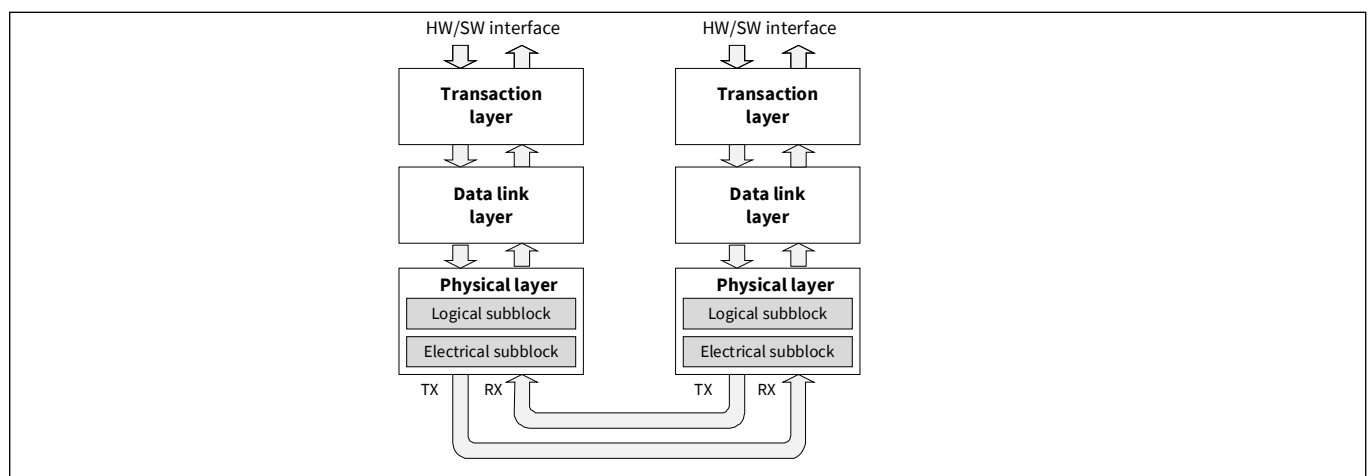
Note Per Section 6 of the SDIO specification, pull-ups in the 10 kΩ to 100 kΩ range are required on the four DATA lines and the CMD line. This requirement must be met during all operating states either through the use of external pull-up resistors or through proper programming of the SDIO host's internal pull-ups.

9.2 PCI express interface (PCIe)

The PCIe core in CYW55571 is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the PCI Express Base Specification v3.0 running at Gen2 speeds. This core contains all the necessary blocks, including logical and electrical functional subblocks to perform PCIe functionality and maintain high-speed links, using existing PCI system configuration software implementations without modification.

The organization of the PCIe core is in logical layers: Transaction Layer, Data Link Layer, and Physical Layer, as shown in [Figure 23](#). A configuration or link management block is provided for enumerating the PCIe configuration space and supporting generation and reception of System Management Messages by communicating with PCIe layers.

Each layer is partitioned into dedicated transmit and receive units that allow point-to-point communication between the host and CYW55571 device. The transmit side processes outbound packets whereas the receive side processes inbound packets. Packets are formed and generated in the Transaction and Data Link Layer for transmission onto the high-speed links and onto the receiving device. A header is added at the beginning to indicate the packet type and any other optional fields.


Figure 23 PCIe layer model

9.2.1 Transaction layer interface

The PCIe core employs a packet-based protocol to transfer data between the host and CYW55571 device, delivering new levels of performance and features. The upper layer of the PCIe is the transaction layer. The transaction layer is primarily responsible for assembly and disassembly of transaction layer packets (TLPs). TLP structure contains header, data payload, and end-to-end CRC (ECRC) fields, which are used to communicate transactions, such as read and write requests and other events.

A pipelined full split-transaction protocol is implemented in this layer to maximize efficient communication between devices with credit-based flow control of TLP, which eliminates wasted link bandwidth due to retries.

9.2.2 Data link layer

The data link layer serves as an intermediate stage between the transaction layer and the physical layer. Its primary responsibility is to provide reliable, efficient mechanism for the exchange of TLPs between two directly connected components on the link. Services provided by the data link layer include data exchange, initialization, error detection and correction, and retry services.

The data link layer packets (DLLPs) are generated and consumed by the data link layer. DLLPs are the mechanism used to transfer link management information between data link layers of the two directly connected components on the link, including TLP acknowledgement, power management, and flow control.

9.2.3 Physical layer

The physical layer of the PCIe provides a handshake mechanism between the data link layer and the high-speed signaling used for Link data interchange. This layer is divided into the logical and electrical functional subblocks. Both subblocks have dedicated transmit and receive units that allow for point-to-point communication between the host and CYW55571 device. The transmit section prepares outgoing information passed from the data link layer for transmission, and the receiver section identifies and prepares received information before passing it to the data link layer. This process involves link initialization, configuration, scrambler, and data conversion into a specific format.

9.2.4 Logical subblock

The logical sub block primary functions are to prepare outgoing data from the data link layer for transmission and identify received data before passing it to the data link layer.

9.2.5 Scrambler/descrambler

This PCIe PHY component generates pseudo-random sequence for scrambling of data bytes and the idle sequence. On the transmit side, scrambling is applied to characters prior to the 8b/10b encoding. On the receive side, descrambling is applied to characters after 8b/10b decoding. Scrambling may be disabled in polling and recovery for testing and debugging purposes.

9.2.6 8B/10B-encoder/decoder

The PCIe core on CYW55571 uses an 8b/10b encoder/decoder scheme to provide DC balancing, synchronizing clock and data recovery, and error detection. The transmission code is specified in the ANSI X3.230-1994, clause 11 and in IEEE 802.3z, 36.2.4.

Using this scheme, 8-bit data characters are treated as 3 bits and 5 bits mapped onto a 4-bit code group and a 6-bit code group, respectively. The control bit in conjunction with the data character is used to identify when to encode one of the 12 special symbols included in the 8b/10b transmission code. These code groups are concatenated to form a 10-bit symbol, which is then transmitted serially. The special symbols are used for link management, frame TLPs, and DLLPs, allowing these packets to be quickly identified and easily distinguished.

9.2.7 Elastic FIFO

An elastic FIFO is implemented in the receiver side to compensate for the differences between the transmit clock domain and the receive clock domain, with worse case clock frequency specified at 600 ppm tolerance. As a result, the transmit and receive clocks can shift one clock every 1666 clocks. In addition, the FIFO adaptively adjusts the elastic level based on the relative frequency difference of the write and read clock. This technique reduces the elastic FIFO size and the average receiver latency by half.

9.2.8 Electrical subblock

The high-speed signals utilize the common mode logic (CML) signaling interface with on-chip termination and deemphasis for best-in-class signal integrity. A deemphasis technique is employed to reduce the effects of intersymbol interference (ISI) due to the interconnect by optimizing voltage and timing margins for worst case channel loss. This results in a maximally open “eye” at the detection point, thereby allowing the receiver to receive data with acceptable bit-error rate (BER).

To further minimize ISI, multiple bits of the same polarity that are output in succession are deemphasized. Subsequent same bits are reduced by a factor of 3.5 dB in power. This amount is specified by PCIe to allow for maximum interoperability while minimizing the complexity of controlling the deemphasis values. The high-speed interface requires AC coupling on the transmit side to eliminate the DC common mode voltage from the receiver. The range of AC capacitance allowed is 75 nF to 200 nF.

9.2.9 Configuration space

The PCIe function in CYW55571 implements the configuration space as defined in the **PCI Express Base Specification v3.0**.

10 Wireless LAN MAC and PHY

10.1 IEEE 802.11ax MAC

The AIROC™ CYW55571 WLAN MAC is designed to support high-throughput operation with low-power consumption. It does so without compromising the Bluetooth® coexistence policies, thereby enabling optimal performance over both networks. In addition, several power saving modes have been implemented that allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in [Figure 24](#).

The following sections provide an overview of the important modules in the MAC.

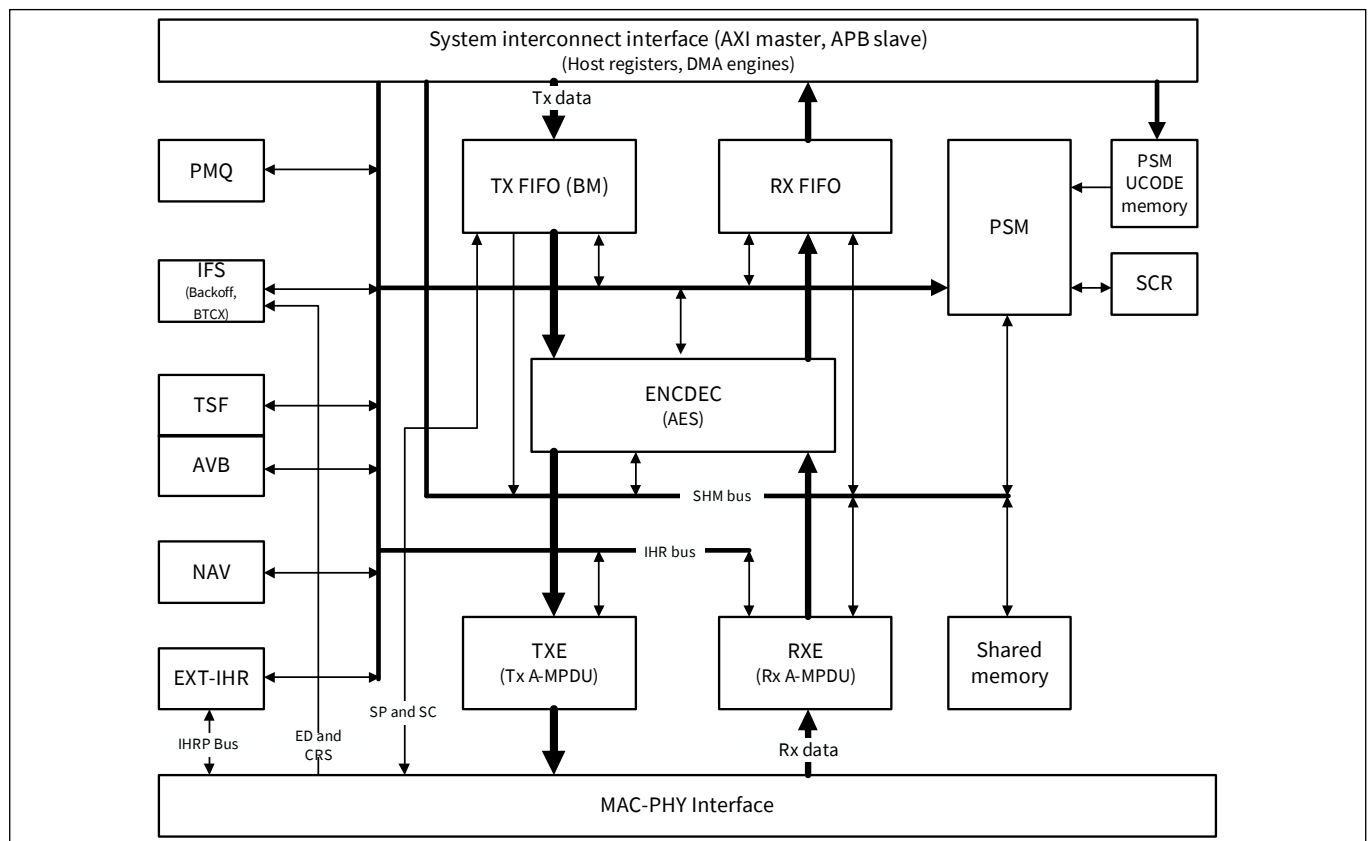


Figure 24 WLAN MAC Architecture

The CYW55571 WLAN media access controller (MAC) supports features specified in the IEEE 802.11-2016 standard and amended draft 2.0 of 802.11ax specification.

Key MAC features include:

- 802.11a/b/g/n/ac/ax
- 1x1 11ax-80 MHz
- Support 11ax STA
- Transmission and reception of HE-SU and HE-ER-SU PPDU
- Reception of HE-MU PPDU-OFDMA/MU-MIMO Frame
- Transmission of HE-TB PPDU (Uplink MU OFDMA)
- Trigger frame reception
- NDP for triggered/non-triggered formats

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- Multi-TID AMPDU
- MU RTS and MU BA reception
- Dual NAV
- Intra PPDU power save
- Spatial reuse support per specification
- Target wake time
- Transmission and reception of AMPDUs/AMSDUs for very high throughput (VHT)
- Supports power management schemes, including WMM power-save
- Supports all ACK and Block-ACK policies as per standard
- Supports interframe space timing, including RIFS
- Supports RTS/CTS and CTS-to-nowhere frame sequences for protecting frame exchanges
- Supports WMM/802.11e/802.11w
- Supports 802.11mc and 802.11v
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware and capturing the TSF timer on an external time synchronization pulse
- Hardware offload for cipher suites/encryption types AES(WPA2), support for WPA3-SAE and key management
- Supports MBSS, P2P Wi-Fi Direct
- Support coexistence with Bluetooth® and other external radios
- Supports RTS-CTS based BW signaling mechanism
- Support statistics counters

10.1.1 System interconnect interface

The system interconnect interface consists of registers for controlling and monitoring the status of the MAC core and interfacing with the TX and RX FIFOs.

10.1.2 Programmable state machine (PSM)

The PSM is a microcode engine that provides most of the low-level control to the hardware to implement the IEEE 802.11 specification. It is a MCU that is highly optimized for flow-control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

In the event of multiple back-off counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM. The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power saving mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. Once the timer expires, the MAC is restored to its functional state. The PSM updates the TSF timer-based on the sleep duration, ensuring that the TSF is synchronized to the network.

10.1.3 Encryption and decryption (ENCDEC)

The ENCDEC engine encapsulates all the hardware accelerators to perform the encryption and decryption, as well as the MIC computation and verification. The accelerators implement the following cipher algorithms: WPA2 AES-CCMP and WPA-3. Based on the frame type and association information, the PSM determines the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The ENCDEC interfaces with the transmit engine (TXE) to encrypt and compute the MIC on transmit frames and the receive engine (RXE) to decrypt and verify the MIC on receive frames. WAPI is also supported.

10.1.4 Transmit engine (TXE)

The TXE constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with ENCDEC module to encrypt frames, and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

10.1.5 Receive engine (RXE)

The RXE constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RX FIFO. It transfers bytes across the MAC-PHY interface and interfaces with the ENCDEC module to decrypt frames. The decrypted data is stored in the RX FIFO. The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types. The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

10.1.6 Interframe space (IFS) timing

The IFS module contains the timers required to determine interframe space timing including RIFS timing. It also contains multiple back-off engines required to support prioritized access to the medium as specified by WMM. The interframe spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP). The back-off engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the back-off counters. When the back-off counters reach 0, the TXE gets notified so that it may commence frame transmission.

10.1.7 Timing synchronization function (TSF)

The TSF module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, can adopt timestamps received from beacon and probe response frames to maintain synchronization with the network. The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

10.1.8 AVB module

The AVB module contains free running timer that runs on AVB clock. It captures the Tx and Rx Time Stamps for calculation of Round trip time (RTT).

10.1.9 Network allocation vector (NAV)

The NAV timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard. The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

10.1.10 Power management queue (PMQ)

The PMQ is a mechanism to watch associated STA's sleep transitions. It is also used to suppress frames to a STA that went to sleep that were queued on the DMA queues before that STA went to sleep. These will be reported with a corresponding suppression reason in the transmit status.

10.1.11 MAC-PHY interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. There is a programming interface, which can be controlled either by the host or the PSM to configure and control the PHY. In addition, it has Sample Play and Sample Collect (SP and SC) interface to Tx/Rx sample directly from/to Buffer Memory (BM). Also has control signals for ED and CRS (per each 20 MHz).

10.1.12 IHR bus

The internal bus used by uCode (PSM) to access MAC registers.

10.1.13 SHM bus

The internal bus used by uCode (PSM) to access Shared memory inside the MAC.

10.1.14 Shared memory (SHM)

The single port RAM used for either reading or writing on each cycle. Shared by RXE, buffer memory, driver and PSM.

10.1.15 SCR

The memory for storing temporary variables and state (64 locations) of 16-bit width. Acts as a dual-read port memory.

10.2 IEEE 802.11ax/ac PHY

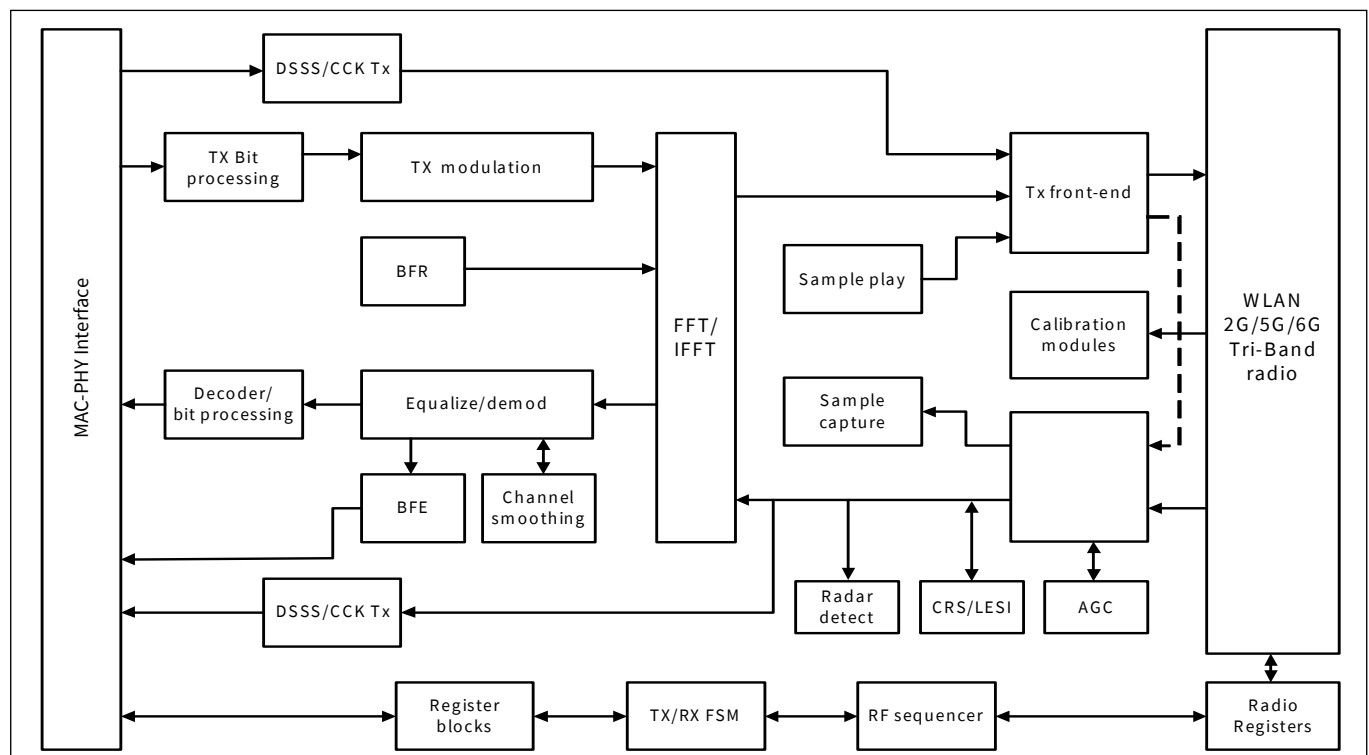
CYW55571 WLAN PHY supports features specified in the IEEE 802.11-2016 standard and amended 802.11ax specification. The PHY has been designed to work in the presence of interference, radio nonlinearity, and various other impairments. It incorporates optimized implementations of the filters, FFT, and Viterbi decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking and channel estimation and tracking. The PHY receiver also contains a robust IEEE 802.11b demodulator. The PHY carrier sense has been tuned to provide high throughput for IEEE 802.11g/11b hybrid networks with Bluetooth® coexistence. It has also been designed for sharing an antenna between WLAN and Bluetooth®.

Key PHY features include:

- One stream HE-11ax STA support (based on draft 2.0 11ax)
- Supports 20/40/80 MHz channels
- Supports 11ax MCS0-11
- Supports transmission and reception of HE-SU and HE-ER-SU PPDU
- Supports reception of HE-MU PPDU
 - Downlink MU OFDMA
 - Downlink MU-MIMO on full band (non-OFDMARU)

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- Supports transmission of HE-TB PPDU (Uplink MU OFDMA)
- Supports dual carrier modulation (DCM)
- Supports transmission and reception of HE-SIG-B at HE-MCS0-5
- Support for all mandatory GI-LTF combinations
- Supports 20 MHz only STA
- Supports reception of frame with preamble puncturing
- Supports responding to HE-sounding frame with up to 8 spatial streams
- Supports MU-MIMO STA capability with full band RU – Required to allow AP (with up to 8 antenna) to use MU-MIMO when transmitting to the STA, improving network efficiency
- Supports legacy 802.11a/b/g/n/ac
- Supports RTT 802.11mc
- Time domain channel smoothing (TDCS) for improved receiver performance
- Low-end sensitivity improvement (LESI) for improving sensitivity for low rate/MCS
- Wideband PAPD (WBPA PD) for improved calibration time and regulatory radiation requirement compliance
- Hardware based adjacent channel detection (HWACI) for improved receiver performance under congested environment
- Narrowband detection to improve Rx sensitivity in presence of spurs or narrow band signal
- Supports 11ax soft-AP mode with capability to receive single user allocation TB-PPDU frames
- Temperature sensing during packet transmission to accurately measure chip temperature

**Figure 25 WLAN PHY block diagram**

11 WLAN radio subsystem

CYW55571 includes an integrated tri-band WLAN RF transceiver that has been optimized for use in 2.4 GHz, 5 GHz, and 6 GHz Wireless LAN systems. It has been designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM or 5–7 GHz U-NII bands. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

Twenty RF control signals are available (10 per core) to drive external RF switches and support optional external power amplifiers and low-noise amplifiers for each band. See the reference board schematics for further details.

11.1 Receiver path

CYW55571 has a wide dynamic range, direct conversion receiver that employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the entire 5–7 GHz U-NII band. An on-chip low-noise amplifier (LNA) in the 2.4 GHz path is shared between the Bluetooth® and WLAN receivers, while the 5/6 GHz receive path has a dedicated on-chip LNA. Control signals are available that can support the use of optional external LNAs for each band.

11.2 Transmit path

The baseband data is modulated and upconverted to the 2.4 GHz ISM or 5–7 GHz U-NII bands, respectively. Linear on-chip power amplifiers are included, which are capable of delivering high output power while meeting IEEE 802.11a/b/g/n/ac/ax specifications without the need for external PAs. When using the internal PAs, closed-loop output power control is completely integrated. As an option, external PAs can be used for even higher output power, in which case the closed-loop power control is provided by means of a-band and g-band TSSI inputs from external power detectors.

11.3 Calibration

CYW55571 features dynamic and automatic on-chip calibration to continually compensate for temperature and process variations across components. These calibration routines are performed periodically in the course of normal radio operation. Examples of some of the automatic calibration algorithms are baseband filter calibration for optimum transmit and receive performance, and LOFT calibration for carrier leakage reduction. In addition, I/Q Calibration, R Calibration, and VCO Calibration are performed on-chip. No per-board calibration is required in manufacturing test, which helps to minimize the test time and cost in large volume production.

Pinout and signal descriptions

12 Pinout and signal descriptions

12.1 WLCSP coordinates

Table 17 lists the CYW55571 WLCSP coordinates by bump number. The table pertains to a bump-side view (i.e., with the die facing up).

Note Bump coordinates origin is die center.

Table 17 CYW55571 WLCSP coordinates by bump number

Bump #	Bump name	X COORD	Y COORD
1	WRF_LOGEN_GND	-1868.932	745.041
2	WRF_TX_GND_C1	-2402.8435	1741.4175
3	WRF_VCO_VDD_1P12	-1292.563	1099.353
4	WRF_SYNTG_GND	-1032.6835	448.5675
5	WRF_AFE_LPF_TIA_GND_C1	-1232.0335	1953.4035
6	WRF_DFSCVO_GND	-1670.419	2361.8595
7	WRF_TX5G_GND_C0	-2420.1325	386.553
8	WRF_VDD_V1P8_C0	-1472.2705	-236.175
9	WRF_PAOUT_5G_C0	-2608.2685	308.046
10	WRF_GPAIO_TSSI2G_OUT_C0	-1650.8845	236.1675
11	NC ^[17]	-1969.4755	918.39
12	WRF_VCO_VDD_3P3	-1498.645	470.109
13	WRF_AFE_VDD_1P22_C1	-1247.32	1388.865
14	WRF_TSSI5G_OUT_C0	-1676.656	-425.868
15	WRF_PA_GND_C1	-2659.1545	1862.5035
16	WRF_PMU_TX_VDD_1P22_C1	-1120.1005	1567.398
17	WRF_LO_GND_C1	-1940.734	1373.592
18	WRF_TX_GND_C1	-1976.9725	1726.536
19	WRF_SYNTG_VDD_1P12	-1492.696	1148.052
20	NC1 ^[17]	-2602.3105	2402.004
21	WRF_VDD_1P8_C1	-1489.5055	2186.0445
22	WRF_PA_VDD_3P3_C0	-2254.0375	-176.4555
23	WRF_VCO_GND	-1538.7085	952.635
24	WRF_TX2G_GND_C0	-2358.3385	-359.5785
25	WRF_PA_VDD_3P3_C1	-2277.235	1933.4145
26	WRF_PA_GND_C1	-2670.355	1661.934
27	WRF_TX5G_GND_C1	-2420.1325	2136.558
28	WRF_PA_VDD_3P3_C1	-2177.9965	1758.567
29	NC2 ^[17]	-2625.6295	1465.8555
30	WRF_PAOUT_2G_C0	-2625.6295	-284.1495
31	WRF_PMU_TX_VDD_1P22_C0	-1129.4965	-204.162

Notes

16.No routing of the signal under this ball.

17.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 17 CYW55571 WLCSP coordinates by bump number (continued)

Bump #	Bump name	X COORD	Y COORD
32	WRF_PA_VDD_3P3_C0	-2177.9965	8.562
33	WRF_PA_VDD_3P3_C1	-2254.0375	1573.5
34	WRF_TX2G_GND_C1	-2358.3385	1390.4265
35	WRF_TX_GND_C0	-1976.9725	-23.469
36	WRF_PA_GND_C0	-2659.1545	112.4985
37	WRF_PA_VDD_3P3_C0	-2277.235	183.4095
38	WRF_LO_GND_C0	-1910.755	-704.4855
39	WRF_PMU_GND_C1	-1473.157	1415.874
40	WRF_SYNTG_GND	-1232.6635	236.3565
41	WRF_RFIN_2G_C0	-2624.9995	-752.649
42	WRF_TX_GND_C0	-2402.8435	-8.5875
43	WRF_SYNTG_VDD_3P3	-1444.708	276.555
44	WRF_LO_GND_C0	-1949.8645	-385.971
45	WRF_RX5G_GND_C1	-2259.4915	2443.7145
46	NC3 ^[17]	-2624.9995	1004.619
47	WRF_PMU_GND_C1	-1518.904	1716.258
48	WRF_RX5G_GND_C0	-2259.4915	695.0595
49	WRF_RFIN_5G_C0	-2602.3105	651.999
50	WRF_AFE_LPF_TIA_GND_C1	-1230.868	1751.0385
51	WRF_LO_GND_C1	-1831.717	1888.3515
52	WRF_PA_GND_C0	-2670.355	-88.071
53	WRF_LO_GND_C0	-1851.3325	-190.5855
54	WRF_PMU_VDD_3P3_C1	-1673.2225	1577.316
55	WRF_AFE_LPF_TIA_GND_C0	-1262.332	-388.3605
56	WRF_PMU_VDD_3P3_C0	-1356.112	-70.233
57	WRF_PMU_GND_C0	-1588.825	-68.5365
58	WRF_RX2G_GND_C1	-2274.9985	1000.4205
59	WRF_RX2G_GND_C0	-2274.9985	-749.2155
60	WRF_AFE_VDD_1P22_C0	-1139.4955	17.904
61	WRF_DFSPLL_GND	-1130.3785	2323.362
62	NC ^[16]	-1738.0045	2169.1785
63	WRF_VCO_GND	-989.6185	952.635
64	NC4 ^[17]	-2608.2685	2058.051
65	WRF_AFE_LPF_TIA_GND_C0	-1277.3935	-655.0845
66	XTAL_XOP	-983.4085	-2499.999
67	XTAL_GND	-1183.4065	-2300.001
68	XTAL_XON	-1183.4065	-2499.999

Notes

16.No routing of the signal under this ball.

17.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 17 **CYW55571 WLCSP coordinates by bump number** *(continued)*

Bump #	Bump name	X COORD	Y COORD
69	VDD_XTAL	-783.4105	-2499.999
70	XTAL_VDD_1P12	-783.4105	-2300.001
71	XTAL_GND	-1383.4045	-2494.599
72	XTAL_GND	-983.4085	-2300.001
73	BTRF_VSS	-2688.5395	-1175.0415
74	BT_PAVDD_3P3	-1813.843	-2499.324
75	BTRF_VSS	-2221.2145	-1954.9095
76	BTRF_VSS	-2185.4575	-2374.3725
77	BTRF_VSS	-2338.2325	-1081.6395
78	BTRF_VSS	-2285.5555	-2159.466
79	BTRF_VSS	-1934.5735	-1404.5325
80	BTRF_VSS	-2126.215	-992.8185
81	BTRF_VSS	-1759.42	-2100.876
82	BTRF_VSS	-1896.202	-976.6545
83	BTRF_VSS	-1572.7645	-2219.604
84	BTRF_VSS	-1964.2915	-2114.16
85	BTRF_VSS	-2679.7555	-1575.0375
86	BTRF_VSS	-1630.7245	-2411.5425
87	BTRF_VSS	-2274.9985	-1706.5185
88	BTRF_VSS	-1991.4625	-1155.138
89	BTRF_VSS	-2373.013	-2485.23
90	BT_RFTEST	-2131.1965	-1455.567
91	BT_RFop	-2641.6675	-976.281
92	BT_PLLVSS	-1907.7445	-1630.824
93	BT_PAVDD_3P3	-2014.471	-2499.324
94	BT_13dBmOP	-2646.2125	-1784.4405
95	BT_LDOVDD_1P12	-1605.9295	-1749.9975
96	BT_RFVSS	-2676.907	-1375.0395
97	BT_20dBmOP	-2581.282	-2472.126
98	VSSC	324.998	299.973
99	PMU_VDD1P8P	2070.998	-274.956
100	RF3P3_SNS	2670.992	-274.956
101	VDDOUT_MISC	2070.998	1325.028
102	PMU_VDD1P8A	2270.996	-274.956
103	PA3P3_SNS	2670.992	725.034
104	VDDOUT_PA3P3	2670.992	525.036
105	VDDOUT_PA3P3	2470.994	525.036

Notes

16.No routing of the signal under this ball.

17.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 17 **CYW55571 WLCSP coordinates by bump number** *(continued)*

Bump #	Bump name	X COORD	Y COORD
106	VDDOUT_PA3P3	2270.996	525.036
107	VDDOUT_PA3P3	2070.998	525.036
108	VDDOUT_PA3P3	2470.994	725.034
109	VDDOUT_PA3P3	2270.996	725.034
110	VDDOUT_PA3P3	2070.998	725.034
111	WLLDO_VDDBAT	2470.994	325.038
112	WLLDO_VDDBAT	2270.996	325.038
113	WLLDO_VDDBAT	2070.998	325.038
114	WLLDO_VDDBAT	2670.992	325.038
115	WLLDO_VDDBAT	2670.992	125.04
116	WLLDO_VDDBAT	2470.994	125.04
117	WLLDO_VDDBAT	2270.996	125.04
118	WLLDO_VDDBAT	2070.998	125.04
119	VDDOUT_RF3P3	2670.992	-74.958
120	VDDOUT_RF3P3	2470.994	-74.958
121	VSSC	1871	125.04
122	MIC_P	2070.998	-74.958
123	VSSC	1871	-274.956
124	VSSC	1871	-74.958
125	WLREG_ON	1871	325.038
126	ASR_VDDBAT	2016.998	1925.022
127	ASR_VDDBAT	2216.996	1925.022
128	ASR_VDDBAT	2416.994	1925.022
129	ASR_VDDBAT	2670.992	1925.022
130	ASR_VLX	2416.994	1725.024
131	ASR_VLX	2216.996	1725.024
132	ASR_VLX	2016.998	1725.024
133	ASR_VLX	2670.992	1725.024
134	PVSSA	2016.998	1525.026
135	PVSSA	2216.996	1525.026
136	PVSSA	2416.994	1525.026
137	PVSSA	2670.992	1525.026
138	MIC_N	2270.996	-74.958
139	ASR_VDD1P12	2270.996	1325.028
140	VSSC	2324.978	-500.019
141	VDD_TOP	-674.992	2099.955
142	VDDOUT_MISC	1871	1325.028

Notes

16.No routing of the signal under this ball.

17.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 17 **CYW55571 WLCSP coordinates by bump number** *(continued)*

Bump #	Bump name	X COORD	Y COORD
143	VDD_RET_GL	1817	1925.022
144	PMU_AVSS	1871	925.032
145	BTREG_ON	1871	1125.03
146	BTLDO_VDDBAT	2670.992	1125.03
147	BTLDO_VDDBAT	2470.994	1125.03
148	VDDOUT_BT3P3	2270.996	1125.03
149	MISC_SNS	2070.998	1125.03
150	VDDOUT_BT3P3	2270.996	925.032
151	VDDOUT_BT3P3	2070.998	925.032
152	VDDOUT_BT3P3	2470.994	925.032
153	PMU_AVSS	1871	725.034
154	BT3P3_SNS	2670.992	925.032
155	PMU_AVSS	1871	525.036
156	CSR_VDDBAT	2216.996	2125.02
157	PVSSC	2416.994	2525.016
158	VDD_DIG	2524.976	-500.019
159	CSR_VDDBAT	2016.998	2125.02
160	CSR_VDDBAT	2670.992	2125.02
161	CSR_VDDBAT	2416.994	2125.02
162	CSR_VLX	2416.994	2325.018
163	PVSSC	2216.996	2525.016
164	CSR_VLX	2216.996	2325.018
165	PVSSC	2016.998	2525.016
166	CSR_VLX	2016.998	2325.018
167	CSR_VLX	2670.992	2325.018
168	VSSC	924.992	299.973
169	DMIC_CK	1324.988	-1700.007
170	VDD_DIG	125	-700.017
171	BT_GPIO_18	1924.982	-2499.999
172	SDIO_DATA_2	924.992	-500.019
173	VSSC	924.992	-1900.005
174	VDD_DIG	1324.988	-1300.011
175	GPIO_13	1724.984	-1900.005
176	VSSC	1924.982	-1500.009
177	VSSC	524.996	-100.023
178	VSSC	1524.986	-1900.005
179	BT_VDDO	-74.998	-1500.009

Notes

16.No routing of the signal under this ball.

17.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 17 **CYW55571 WLCSP coordinates by bump number** *(continued)*

Bump #	Bump name	X COORD	Y COORD
180	VSSC	324.998	499.971
181	VSSC	-274.996	-100.023
182	VDD_TOP	924.992	99.975
183	SMIF_SPHB_CS1_N	-474.994	2499.951
184	SMIF_SPHB_CS0_N	-274.996	2499.951
185	RF_SW_CTRL_16	-274.996	2099.955
186	SMIF_SPHB_DQ2	-74.998	2299.953
187	RF_SW_CTRL_14	125	2099.955
188	SMIF_SPHB_CK	-474.994	2299.953
189	VSSC	-674.992	1899.957
190	SMIF_SPHB_DQ0	-74.998	2499.951
191	SMIF_SPHB_DQ1	125	2499.951
192	VDD_AON	-674.992	1499.961
193	VSSO_SMIF	-74.998	-900.015
194	VDD_TOP	-674.992	1099.965
195	RF_SW_CTRL_15	324.998	2299.953
196	VDDP_RFSW	524.996	2299.953
197	RF_SW_CTRL_5	724.994	1699.959
198	VDDIO_RFSW	924.992	1899.957
199	VDD_AON	-674.992	899.967
200	BT_VDDO_SMIF	328.058	-900.357
201	VDD_TOP	724.994	-300.021
202	VDD_AON	924.992	-300.021
203	BT_GPIO_3	-474.994	-2100.003
204	VDD_MAIN	724.994	2299.953
205	RF_SW_CTRL_9	1124.99	2299.953
206	RF_SW_CTRL_7	1324.988	2299.953
207	VSSC	1124.99	2099.955
208	VSSO	924.992	-2100.003
209	GPIO_1	524.996	1499.961
210	BT_VDDO	724.994	-1900.005
211	VSSC	924.992	-2300.001
212	VSSO	1324.988	1899.957
213	RF_SW_CTRL_2	1124.99	1499.961
214	RF_SW_CTRL_0	1524.986	1696.854
215	VDDIO	1637.486	2431.452
216	I2S_MCK	1124.99	-2300.001

Notes

16.No routing of the signal under this ball.

17.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 17 **CYW55571 WLCSP coordinates by bump number** *(continued)*

Bump #	Bump name	X COORD	Y COORD
217	VSSO_SMIF	924.992	-1500.009
218	VSSC	1524.986	-2300.001
219	VSSC	1324.988	1499.961
220	RF_SW_CTRL_6	1324.988	2099.955
221	VDD_MAIN	1525.247	2097.381
222	RF_SW_CTRL_1	1324.988	1699.959
223	BT_VDDO	724.994	-2300.001
224	VDD_DIG	1524.986	-1700.007
225	BT_VDDC	-874.99	-1300.011
226	RF_SW_CTRL_10	324.998	1899.957
227	VSSC	524.996	-1100.013
228	I2S_DO	1324.988	-1500.009
229	VSSC	1324.988	-1100.013
230	BTLDO_VDDBAT	2670.992	1325.028
231	VSSC	1524.986	-1500.009
232	VSSC	128.06	-900.357
233	VSSC	-74.998	2099.955
234	VSSC	-1274.986	-1100.013
235	VDDIO_SD	1924.982	-1300.011
236	VSSC	1924.982	-500.019
237	I2S_SCK	1124.99	-1900.005
238	BT_VDDC	-1474.984	-1100.013
239	BT_VDDC	-874.99	-1700.007
240	BT_AJTAG_TDI	-1674.982	-1100.013
241	VDD_DIG	724.994	-2100.003
242	VSSC	-1674.982	-1300.011
243	BT_AJTAG_TDO	-1474.984	-1300.011
244	BT_VDDC	-1274.986	-1300.011
245	BT_AJTAG_TMS	-1274.986	-1500.009
246	BT_TM1	-1274.986	-1700.007
247	VDD_TOP	324.413	-1100.355
248	DMIC_DQ	1324.988	-1900.005
249	VDD_DIG	1324.988	-2100.003
250	VSSC	-1274.986	-1900.005
251	VDD_DIG	-674.992	-900.015
252	VDD_MAIN	-274.996	1499.961
253	VDD_RET_GL_IN	-674.992	-500.019

Notes

16.No routing of the signal under this ball.

17.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 17 **CYW55571 WLCSP coordinates by bump number** *(continued)*

Bump #	Bump name	X COORD	Y COORD
254	VSSO	-1074.988	-1900.005
255	VSSC	1924.982	-1900.005
256	VSSC	-674.992	-300.021
257	VSSC	-674.992	-100.023
258	VSSC	-74.998	-100.023
259	VSSC	-674.992	-700.017
260	BT_UART_CTS_N	125	-2300.001
261	I2S_DI	1324.988	-2300.001
262	VDD_DIG	924.992	-2499.999
263	SDIO_CLK	1724.984	-900.015
264	VSSO	1924.982	-900.015
265	PCI_PME_L	1724.984	-2300.001
266	BT_GPIO_17	1724.984	-2499.999
267	BT_GPIO_16	1324.988	-2499.999
268	VDDP_RFSW	724.994	1899.957
269	BT_VDDO	924.992	-900.015
270	GPIO_12	324.998	1299.963
271	VSSC	125	-100.023
272	BTLDO_VDDBAT	2470.994	1325.028
273	GPIO_2	724.994	1299.963
274	VSSO	125	1899.957
275	SDIO_DATA_1	1324.988	-500.019
276	VSSC	-874.99	-1100.013
277	VSSC	-674.992	-1500.009
278	BT_GPIO_2	-874.99	-1900.005
279	BT_GPIO_4	-474.994	-1900.005
280	VSSC	1324.988	-100.023
281	VDD_TOP	-674.992	1699.959
282	LHL_GPIO5	1324.988	299.973
283	BT_VDDC	-674.992	-2100.003
284	BT_GPIO_20	-474.994	-2300.001
285	BT_HOST_WAKE	-474.994	-2499.999
286	LHL_GPIO7	1524.986	299.973
287	VDDIO	1524.986	499.971
288	RF_SW_CTRL_4	924.992	1699.959
289	VSSC	1124.99	1699.959
290	VSSC	-274.996	-2100.003

Notes

16.No routing of the signal under this ball.

17.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 17 **CYW55571 WLCSP coordinates by bump number** *(continued)*

Bump #	Bump name	X COORD	Y COORD
291	BT_DEV_WAKE	-274.996	-2499.999
292	VSSC	-274.996	-1700.007
293	VSSC	-274.996	-1500.009
294	VDD_TOP	125	1499.961
295	VDD_AON	924.992	2099.955
296	VSSC	125	-1500.009
297	BTPLL_AVDD1P0	125	-1900.005
298	BT_VDDC	324.998	-1500.009
299	AVDD_RX_1P0	2468.582	-845.5425
300	AVSS_PCIE_PLL	2268.584	-845.5425
301	AVSS_PCIE_RX	2668.58	-845.5425
302	PCIE_RDP	2668.58	-1045.545
303	AVDD_PLL_1P0	2468.582	-1045.545
304	VSSC	125	1099.965
305	PCIE_REFCLKP	2268.584	-1045.545
306	PCIE_REFCLKN	2268.584	-1245.543
307	ARMPLL_AVSS	1124.99	-100.023
308	ARMPLL_AVDD1P0	1124.99	-300.021
309	VSSC	1124.99	-500.019
310	PCIE_RDN	2668.58	-1245.543
311	PCIE_TDP	2668.58	-1445.541
312	AVDD_TX_1P0	2468.582	-1445.541
313	VSSC	1124.99	-700.017
314	VDD_DIG	1324.988	-700.017
315	SDIO_CMD	1724.984	-700.017
316	PCIE_TESTN	2268.584	-1445.541
317	PCIE_TESTP	2268.584	-1645.539
318	VDD_TOP	1924.982	-700.017
319	VDDIO_SD	1524.986	-1300.011
320	VDDIO_SD	1724.984	-1300.011
321	AVSS_PCIE_TX	2468.582	-1645.539
322	PCIE_TDN	2668.58	-1645.539
323	BT_VDDO	724.994	-2499.999
324	VSSC	-274.996	99.975
325	VDD_DIG	1724.984	-500.019
326	VDDIO_RFSW	724.994	2099.955
327	I2S_IRCK	1124.99	-1500.009

Notes

16.No routing of the signal under this ball.

17.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 17 **CYW55571 WLCSP coordinates by bump number** *(continued)*

Bump #	Bump name	X COORD	Y COORD
328	VSSO	1724.984	-1700.007
329	BT_GPIO_11	-674.992	-1700.007
330	BT_GPIO_9	-874.99	-1500.009
331	VSSC	1924.982	-1700.007
332	VDD_DIG	1724.984	-1500.009
333	VSSC	924.992	-700.017
334	VSSC	1524.986	99.975
335	VDD_DIG	2124.98	-500.019
336	LHL_GPIO4	724.994	299.973
337	BT_UART_RXD	324.998	-2499.999
338	VSSC	-74.998	99.975
339	VSSC	524.996	1099.965
340	VSSC	1324.988	99.975
341	JTAG_SEL	1124.99	699.969
342	VSSC	125	99.975
343	VSSC	324.998	99.975
344	VSSC	524.996	99.975
345	LHL_GPIO6	1324.988	499.971
346	LHL_VDDO	1124.99	299.973
347	VSSC	524.996	-500.019
348	VSSC	724.994	99.975
349	VSSC	-474.994	99.975
350	VDD_MAIN	524.996	899.967
351	LHL_XTALO	524.996	299.973
352	LHL_GPIO3	924.992	699.969
353	VSSC	-674.992	99.975
354	VDD_TOP	-674.992	299.973
355	VSSC	1524.986	-100.023
356	VSSC	324.998	-500.019
357	VSSC	324.998	-700.017
358	RF_SW_CTRL_13	324.998	2099.955
359	VDD_TOP	1606.49	1900.344
360	VSSC	924.992	1099.965
361	GPIO_4	924.992	899.967
362	VDDIO	1668.284	1426.539
363	VDD_AON	1670.984	1226.541
364	GPIO_0	1124.99	899.967

Notes

16.No routing of the signal under this ball.

17.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 17 **CYW55571 WLCSP coordinates by bump number** *(continued)*

Bump #	Bump name	X COORD	Y COORD
365	VSSO	1670.984	1026.543
366	VDDIO	1670.984	826.545
367	GPIO_10	1324.988	1099.965
368	VDD_MAIN	1324.988	899.967
369	PVSSC	1817	2525.016
370	VDDOUT_SWCORE	1817	2125.02
371	VSSC	324.998	-300.021
372	VSSC	125	-300.021
373	CSR_VDD0P9	1817	2325.018
374	RF_SW_CTRL_12	924.992	2299.953
375	VDDOUT_RF3P3	2470.994	-274.956
376	BT_VDDC	524.996	-900.015
377	VSSC	524.996	1299.963
378	LHL_GPIO2	724.994	699.969
379	VSSC	-474.994	299.973
380	SDIO_DATA_0	1324.988	-300.021
381	BT_VDDO_SMIF	-474.994	-900.015
382	VSSO	924.992	-1100.013
383	VSSC	-474.994	-100.023
384	VDD_TOP	1524.986	-300.021
385	VSSC	-474.994	-500.019
386	VDD_DIG	-274.996	-500.019
387	VDD_DIG	-74.998	-500.019
388	VDD_DIG	125	-500.019
389	VSSC	1524.986	-500.019
390	VDD_DIG	2124.98	-1900.005
391	GPIO_14	1524.986	-2100.003
392	PCIE_CLKREQ_L	1924.982	-2300.001
393	VDD_DIG	2124.98	-2300.001
394	BT_GPIO_12	2324.978	-2300.001
395	BT_GPIO_14	2524.976	-2300.001
396	BT_GPIO_19	1524.986	-2499.999
397	RF_SW_CTRL_19	-474.994	1899.957
398	RF_SW_CTRL_17	-274.996	1899.957
399	VDD_MAIN	-74.998	1899.957
400	VDD_AON	-74.998	1499.961
401	RF_SW_CTRL_3	724.994	1499.961

Notes

16.No routing of the signal under this ball.

17.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 17 **CYW55571 WLCSP coordinates by bump number** *(continued)*

Bump #	Bump name	X COORD	Y COORD
402	VDD_MAIN	924.992	1499.961
403	VSSC	-74.998	1299.963
404	GPIO_11	125	1299.963
405	GPIO_3	724.994	899.967
406	NC	-474.994	1099.965
407	VSSC	-274.996	1099.965
408	VDD_MAIN	-74.998	1099.965
409	VDD_MAIN	-474.994	699.969
410	VSSC	-274.996	699.969
411	VSSC	-74.998	699.969
412	LHL_GPIO0	125	699.969
413	LHL_GPIO1	324.998	699.969
414	BT_VDDC	524.996	-700.017
415	VSSC	324.998	-100.023
416	GPIO_8	524.996	1699.959
417	VSSC	-274.996	1299.963
418	VSSC	724.994	499.971
419	LPO_IN	924.992	499.971
420	VSSC	-274.996	299.973
421	VDD_TOP	-74.998	299.973
422	VSSO_SMIF	-274.996	-900.015
423	VSSC	1124.99	-1100.013
424	VDD_MAIN	524.996	1899.957
425	BT_VDDO	724.994	-1100.013
426	BT_GPIO_10	-674.992	-1300.011
427	BT_VDDC	-474.994	-1300.011
428	BT_VDDC	-1074.988	-1500.009
429	BT_VDDO_SMIF	724.994	-1500.009
430	VSSC	-1074.988	-1700.007
431	BT_VDDC	-74.998	-1700.007
432	VSSC	125	-1700.007
433	BT_VDDC	324.998	-1700.007
434	BT_UART_TXD	-74.998	-2499.999
435	BT_UART_RTS_N	125	-2499.999
436	BT_VDDC	324.998	-2300.001
437	RF_SW_CTRL_18	-474.994	1699.959
438	VDD_MAIN	-474.994	2099.955

Notes

16.No routing of the signal under this ball.

17.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 17 **CYW55571 WLCSP coordinates by bump number** *(continued)*

Bump #	Bump name	X COORD	Y COORD
439	GPIO_5	-274.996	1699.959
440	RF_SW_CTRL_11	-74.998	1699.959
441	VSSC	125	1699.959
442	RF_SW_CTRL_8	324.998	1699.959
443	VSSC	324.998	1499.961
444	GPIO_9	924.992	1299.963
445	GPIO_7	1124.99	1299.963
446	GPIO_6	1324.988	1299.963
447	VSSC	-474.994	899.967
448	VDD_MAIN	-274.996	899.967
449	VSSC	-74.998	899.967
450	VDD_MAIN	125	899.967
451	VSSC	324.998	899.967
452	VSSC	524.996	699.969
453	FLL_VDDIO	1324.988	699.969
454	VSSC	-474.994	499.971
455	VSSC	-274.996	499.971
456	LHL_XTALI	125	499.971
457	VDD_AON	125	299.973
458	VSSC	-474.994	-300.021
459	VSSC	-274.996	-300.021
460	VDD_DIG	-74.998	-300.021
461	BT_VDDO_SMIF	-274.996	-700.017
462	VDD_DIG	-74.998	-700.017
463	SDIO_DATA_3	1124.99	-900.015
464	VDD_AON	1524.986	-900.015
465	BT_AJTAG_TCK	-1074.988	-1100.013
466	VSSC	-539.992	-1100.013
467	VSSC	-1074.988	-1300.011
468	SMIF_SPHB_DQ3	-274.996	2299.953
469	VSSO_SMIF	724.994	-1700.007
470	VSSC	-674.992	-1900.005
471	BT_GPIO_5	-274.996	-1900.005
472	BT_GPIO_8	-74.998	-1900.005
473	BT_GPIO_6	125	-2100.003
474	VSSC	324.998	-2100.003
475	PERST_L	2324.978	-2100.003

Notes

16.No routing of the signal under this ball.

17.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions**Table 17** CYW55571 WLCSP coordinates by bump number *(continued)*

Bump #	Bump name	X COORD	Y COORD
476	VSSC	2524.976	-2100.003
477	BT_VDDC	-274.996	-2300.001
478	BT_GPIO_7	-74.998	-2300.001
479	BT_GPIO_13	2124.98	-2499.999
480	BT_GPIO_15	2324.978	-2499.999
481	VSSC	2524.976	-2499.999
482	VSSC	728.324	-100.023
483	VSSC	524.996	-300.021
484	VDD_AON	1124.99	99.975
485	VDD_MAIN	125	2299.953
486	VSSC	324.998	-1900.005

Notes

16.No routing of the signal under this ball.

17.Need to have a 50 Ω termination to ground.

12.2 486 bump map WLCSP (5.32 × 5.67 × 0.33 mm)

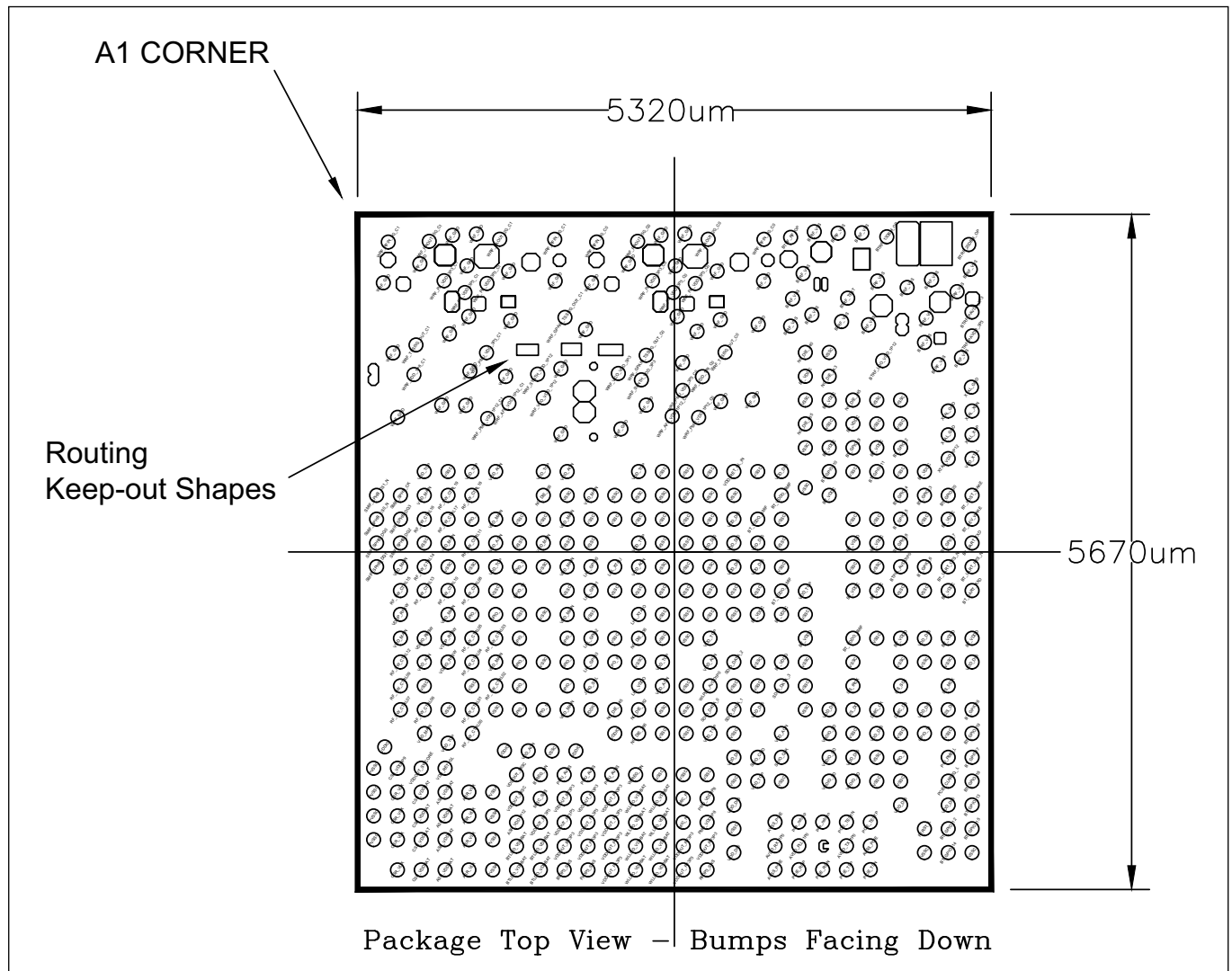


Figure 26 486 bump map WLCSP (5.32 × 5.67 × 0.33 mm)

Pinout and signal descriptions
12.3 WLCSP package signal descriptions

The signal name, type, and description of each pin in the CYW55571 is listed in [Table 18](#). The symbols shown under Type indicate pin directions (I/O = Bidirectional, I = Input, O = Output, PWR = Power, GND = Ground, OD = Open-Drain) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

Table 18 CYW55571 WLCSP signal descriptions

Bump #	Bump name	Type	Description
1	WRF_GND	GND	WLAN radio ground
2	WRF_GND	GND	WLAN radio ground
3	WRF_VCO_VDD_1P12	PWR	WLAN radio 1.12 V supply
4	WRF_GND	GND	WLAN radio ground
5	WRF_GND	GND	WLAN radio ground
6	WRF_GND	GND	WLAN radio ground
7	WRF_GND	GND	WLAN radio ground
8	WRF_VDD_1P8_C0	PWR	WLAN radio 1.8 V Core0 supply
9	WRF_PAOUT_5G_C0	O	WLAN radio Core0 5/6 GHz PA output
10	WRF_GPAIO_TSSI2G_OUT_C0	O	WLAN radio 2.4 GHz TSSI Core0
11	NC ^[19]	O	WLAN radio 2.4 GHz TSSI Core1
12	WRF_VCO_VDD_3P3	PWR	WLAN radio 3.3 V supply
13	WRF_AFE_VDD_1P12_C1	PWR	WLAN radio 1.12 V supply
14	WRF_TSSI5G_OUT_C0	O	WLAN radio 5/6 GHz TSSI Core0
15	WRF_GND	GND	WLAN radio ground
16	WRF_PMU_VDD_1P12_C1	PWR	WLAN radio 1.12 V supply
17	WRF_GND	GND	WLAN radio ground
18	WRF_GND	GND	WLAN radio ground
19	WRF_SYNTH_VDD_1P12	PWR	WLAN radio 1.12 V supply
20	NC1 ^[20]	I	WLAN radio 5/6 GHz Core1 receiver input
21	WRF_VDD_1P8_C1	PWR	WLAN radio 1.8 V Core1 supply
22	WRF_PA_VDD_3P3_C0	PWR	WLAN radio 3.3 V Core0 PA supply
23	WRF_GND	GND	WLAN radioo ground
24	WRF_GND	GND	WLAN radio ground
25	WRF_PA_VDD_3P3_C1	PWR	WLAN radio 3.3 V Core1 PA Supply
26	WRF_GND	GND	WLAN radio ground
27	WRF_GND	GND	WLAN radio ground
28	WRF_PA_VDD_3P3_C1	PWR	WLAN radio 3.3 V Core1 PA supply
29	NC2 ^[20]	O	WLAN radio Core1 2.4 GHz PA output
30	WRF_PAOUT_2G_C0	O	WLAN radio Core0 2.4 GHz PA output
31	WRF_PMU_VDD_1P12_C0	PWR	WLAN radio 1.12 V supply
32	WRF_PA_VDD_3P3_C0	PWR	WLAN radio 3.3 V Core0 PA supply

Notes

18. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.

19. No routing of the signal under this ball.

20. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 18 **CYW55571 WLCSP signal descriptions** *(continued)*

Bump #	Bump name	Type	Description
33	WRF_PA_VDD_3P3_C1	PWR	WLAN radio 3.3 V Core1 PA supply
34	WRF_GND	GND	WLAN radio ground
35	WRF_GND	GND	WLAN radio ground
36	WRF_GND	GND	WLAN radio ground
37	WRF_PA_VDD_3P3_C0	PWR	WLAN radio 3.3 V Core0 PA supply
38	WRF_GND	GND	WLAN radio ground
39	WRF_GND	GND	WLAN radio ground
40	WRF_GND	GND	WLAN radio ground
41	WRF_RFIN_2G_C0	I	WLAN radio 2.4 GHz Core0 receiver input
42	WRF_GND	GND	WLAN radio ground
43	WRF_SYNTH_VDD_3P3	PWR	WLAN radio 3.3 V supply
44	WRF_GND	GND	WLAN radio ground
45	WRF_GND	GND	WLAN radio ground
46	NC3 ^[20]	I	WLAN radio 2.4 GHz Core1 receiver input
47	WRF_GND	GND	WLAN radio ground
48	WRF_GND	GND	WLAN radio ground
49	WRF_RFIN_5G_C0	I	WLAN radio 5/6 GHz Core0 receiver input
50	WRF_GND	GND	WLAN radio ground
51	WRF_GND	GND	WLAN radio ground
52	WRF_GND	GND	WLAN radio ground
53	WRF_GND	GND	WLAN radio ground
54	WRF_PMU_VDD_3P3_C1	PWR	WLAN radio 3.3 V supply
55	WRF_GND	GND	WLAN radio ground
56	WRF_PMU_VDD_3P3_C0	PWR	WLAN radio 3.3 V supply
57	WRF_GND	GND	WLAN radio ground
58	WRF_GND	GND	WLAN radio ground
59	WRF_GND	GND	WLAN radio ground
60	WRF_AFE_VDD_1P12_C0	PWR	WLAN radio 1.12 V supply
61	WRF_GND	GND	WLAN radio ground
62	NC ^[19]	O	WLAN radio 5/6 GHz TSSI Core1
63	WRF_GND	GND	WLAN radio ground
64	NC4 ^[20]	O	WLAN radio Core1 5/6 GHz PA output
65	WRF_GND	GND	WLAN radio ground
66	XTAL_XOP	I	XTAL oscillator input
67	XTAL_GND	GND	XTAL oscillator ground
68	XTAL_XON	O	XTAL oscillator output

Notes

18. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.

19. No routing of the signal under this ball.

20. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 18 **CYW55571 WLCSP signal descriptions** *(continued)*

Bump #	Bump name	Type	Description
69	VDD_XTAL	PWR	XTAL oscillator 1.0 V supply
70	XTAL_VDD_1P12	PWR	XTAL oscillator 1.12 V supply
71	XTAL_GND	GND	XTAL oscillator ground
72	XTAL_GND	GND	XTAL oscillator ground
73	BTRF_VSS	GND	Bluetooth® radio ground
74	BTRF_PAVDD_3P3	PWR	Bluetooth® radio 3.3 V PA supply
75	BTRF_VSS	GND	Bluetooth® radio ground
76	BTRF_VSS	GND	Bluetooth® radio ground
77	BTRF_VSS	GND	Bluetooth® radio ground
78	BTRF_VSS	GND	Bluetooth® radio ground
79	BTRF_VSS	GND	Bluetooth® radio ground
80	BTRF_VSS	GND	Bluetooth® radio ground
81	BTRF_VSS	GND	Bluetooth® radio ground
82	BTRF_VSS	GND	Bluetooth® radio ground
83	BTRF_VSS	GND	Bluetooth® radio ground
84	BTRF_VSS	GND	Bluetooth® radio ground
85	BTRF_VSS	GND	Bluetooth® radio ground
86	BTRF_VSS	GND	Bluetooth® radio ground
87	BTRF_VSS	GND	Bluetooth® radio ground
88	BTRF_VSS	GND	Bluetooth® radio ground
89	BTRF_VSS	GND	Bluetooth® radio ground
90	BTRF_TEST	I/O	Bluetooth® radio test input/output pin
91	BTRF_RF_OP	I/O	Bluetooth® BDR/LE 0DBM radio output and BDR/LE/EDR radio input
92	BTRF_VSS	GND	Bluetooth® radio ground
93	BTRF_PAVDD_3P3	PWR	Bluetooth® radio 3.3 V PA supply
94	BTRF_13DBM_OP	O	Bluetooth® BDR/LE13DBM and EDR 9DBM radio output
95	BTRF_LDO_VDD_1P12	PWR	Bluetooth® radio 1.12 V Input supply
96	BTRF_VSS	GND	Bluetooth® radio ground
97	BTRF_20DBM_OP	O	Bluetooth® BDR/LE 20DBM and EDR 13DBM radio output
98	VSSC	GND	Core ground for WLAN and Bluetooth®
99	PMU_VDD1P8	PWR	1.8 V PMU supply input
100	RF3P3_SNS	I	Feedback input of RF3P3 LDO
101	VDDOUT_MISC	O	Output of VDDOUT_MISC
102	PMU_VDD1P8	PWR	1.8 V PMU supply input

Notes

18. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.
19. No routing of the signal under this ball.
20. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 18 **CYW55571 WLCSP signal descriptions** (continued)

Bump #	Bump name	Type	Description
103	PA3P3_SNS	I	Feedback input of PA3P3 LDO
104	VDDOUT_PA3P3	PWR	3.3 V output to supply WLAN PA
105	VDDOUT_PA3P3		
106	VDDOUT_PA3P3		
107	VDDOUT_PA3P3		
108	VDDOUT_PA3P3		
109	VDDOUT_PA3P3		
110	VDDOUT_PA3P3		
111	WLLDO_VDDBAT	PWR	Battery supply input for WLAN PA and RF LDO
112	WLLDO_VDDBAT		
113	WLLDO_VDDBAT		
114	WLLDO_VDDBAT		
115	WLLDO_VDDBAT		
116	WLLDO_VDDBAT		
117	WLLDO_VDDBAT		
118	WLLDO_VDDBAT		
119	VDDOUT_RF3P3	PWR	3.3 V output to supply WLAN RF
120	VDDOUT_RF3P3		
121	VSSC	GND	Core ground for WLAN and Bluetooth®
122	MIC_P	I	ADC microphone positive input
123	VSSC	GND	Core ground for WLAN and Bluetooth®
124	VSSC	GND	Core ground for WLAN and Bluetooth®
125	WLREG_ON	I	Used by the PMU to power up or power down the internal CYW55571 regulators used by the WLAN section. When deasserted, this pin holds the WLAN section in reset. This pin has an internal 50 kΩ pull-down resistor that is auto enabled/disabled by programming.
126	ASR_VDDBAT	PWR	Battery supply Input for ASR power stage
127	ASR_VDDBAT		
128	ASR_VDDBAT		
129	ASR_VDDBAT		
130	ASR_VLX	O	ASR power stage output to inductor
131	ASR_VLX		
132	ASR_VLX		
133	ASR_VLX		
134	PVSSA	GND	Ground input of ASR power stage
135	PVSSA	GND	Ground input of ASR power stage

Notes

18. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.

19. No routing of the signal under this ball.

20. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 18 **CYW55571 WLCSP signal descriptions** *(continued)*

Bump #	Bump name	Type	Description
136	PVSSA	GND	Ground input of ASR power stage
137	PVSSA	GND	Ground input of ASR power stage
138	MIC_N	I	ADC microphone negative input
139	ASR_VDD1P12	I	Sense or feedback input of ASR power stage
140	VSSC	GND	Core ground for WLAN and Bluetooth®
141	VDD_TOP	PWR	0.9 V digital Core supply for WLAN/Bluetooth®
142	VDDOUT_MISC	O	output of VDDOUT_MISC
143	VDD_RET_GL	O	Power MUX output Supply for VDD_RET_GL_IN power supply input
144	PMU_AVSS	GND	PMU analog ground
145	BTREG_ON	I	Used by the PMU to power up or power down the internal CYW55571 regulators used by the Bluetooth® section. When deasserted, this pin holds the Bluetooth® section in reset. This pin has an internal 50 kΩ pull-down resistor that is auto enabled/disabled by programming.
146	BTLDO_VDDBAT	PWR	Battery supply input for Bluetooth® PA LDO
147	BTLDO_VDDBAT	PWR	Battery supply input for Bluetooth® PA LDO
148	VDDOUT_BT3P3	PWR	3.3 V output to supply Bluetooth® PA
149	MISC_SNS	I	Feedback input of MISC LDO
150	VDDOUT_BT3P3	PWR	3.3 V output to supply Bluetooth® PA
151	VDDOUT_BT3P3		
152	VDDOUT_BT3P3		
153	PMU_AVSS	GND	PMU analog ground
154	BT3P3_SNS	I	Feedback input of BT3P3 LDO
155	PMU_AVSS	GND	PMU analog ground
156	CSR_VDDBAT	PWR	Battery supply input for ASR power stage
157	PVSSC	GND	Ground input of CSR power stage
158	VDD_DIG	PWR	0.9 V digital core supply for WLAN
159	CSR_VDDBAT	PWR	Battery supply input for CSR power stage
160	CSR_VDDBAT		
161	CSR_VDDBAT		
162	CSR_VLX	O	CSR power stage output to inductor
163	PVSSC	GND	Ground input of CSR power stage
164	CSR_VLX	O	CSR power stage output to inductor
165	PVSSC	GND	Ground input of CSR power stage
166	CSR_VLX	O	CSR power stage output to inductor
167	CSR_VLX	O	CSR power stage output to inductor

Notes

18. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.

19. No routing of the signal under this ball.

20. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 18 **CYW55571 WLCSP signal descriptions** (continued)

Bump #	Bump name	Type	Description
168	VSSC	GND	Core ground for WLAN and Bluetooth®
169	DMIC_CK	I/O	Digital Mic clock
170	VDD_DIG	PWR	0.9 V digital core supply for WLAN
171	BT_GPIO_18	I/O	Bluetooth® general purpose I/O
172	SDIO_DATA_2	I/O	SDIO data line 2
173	VSSC	GND	Core ground for WLAN and Bluetooth®
174	VDD_DIG	PWR	0.9 V digital core supply for WLAN
175	GPIO_13	I/O	WLAN general purpose I/O
176	PACKAGEOPTION_0	I	Should be connected to VSSC
177	VSSC	GND	Core ground for WLAN and Bluetooth®
178	VSSC	GND	Core ground for WLAN and Bluetooth®
179	BT_VDDO	PWR	1.8 V IO supply for Bluetooth® GPIOs
180	VSSC	GND	Core ground for WLAN and Bluetooth®
181	VSSC	GND	Core ground for WLAN and Bluetooth®
182	VDD_TOP	PWR	0.9 V digital core supply for WLAN/Bluetooth®
183	SMIF_SPHB_CS1_N	O	SMIF Chip Select1 active LOW output
184	SMIF_SPHB_CS0_N	O	SMIF Chip Select0 active LOW output
185	RF_SW_CTRL16	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
186	SMIF_SPHB_DQ2	I/O	SMIF data line 2
187	RF_SW_CTRL14	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
188	SMIF_SPHB_CK	O	SMIF clock output
189	VSSC	GND	Core ground for WLAN and Bluetooth®
190	SMIF_SPHB_DQ0	I/O	SMIF data line 0
191	SMIF_SPHB_DQ1	I/O	SMIF data line 1
192	VDD_AON	PWR	0.9 V digital core supply for WLAN/Bluetooth®
193	VSSO_SMIF	GND	IO ground
194	VDD_TOP	PWR	0.9 V digital core supply for WLAN/Bluetooth®
195	RF_SW_CTRL15	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
196	VDDP_RFSW	O	VDDP power switch output
197	RF_SW_CTRL05	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
198	VDDIO_RFSW	PWR	IO Supply for RF switch control pads
199	VDD_AON	PWR	0.9 V Digital core supply for WLAN/Bluetooth®
200	BT_VDDO_SMIF	PWR	1.8 V SMIF interface IO supply

Notes

18. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.

19. No routing of the signal under this ball.

20. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 18 **CYW55571 WLCSP signal descriptions** *(continued)*

Bump #	Bump name	Type	Description
201	VDD_TOP	PWR	0.9 V digital core supply for WLAN/Bluetooth®
202	VDD_AON	PWR	0.9 V digital core supply for WLAN/Bluetooth®
203	BT_GPIO_3	I/O	Bluetooth® general purpose I/O
204	VDD_MAIN	PWR	0.9 V digital core supply for WLAN
205	RF_SW_CTRL09	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
206	RF_SW_CTRL07	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
207	VSSC	GND	Core ground for WLAN and Bluetooth®
208	VSSO	GND	IO ground
209	GPIO_1	I/O	WLAN general purpose I/O
210	BT_VDDO	PWR	1.8 V IO supply for Bluetooth® GPIOs
211	VSSC	GND	Core ground for WLAN and Bluetooth®
212	VSSO	GND	IO ground
213	RF_SW_CTRL02	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
214	RF_SW_CTRL00	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
215	VDDIO	PWR	1.8 V IO supply for WLAN GPIOs
216	I2S_MCK	I/O	I2S master clock
217	VSSO_SMIF	GND	IO ground
218	VSSC	GND	Core ground for WLAN and Bluetooth®
219	VSSC	GND	Core ground for WLAN and Bluetooth®
220	RF_SW_CTRL06	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
221	VDD_MAIN	PWR	0.9 V digital core supply for WLAN
222	RF_SW_CTRL01	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
223	BT_VDDO	PWR	1.8 V IO supply for Bluetooth® GPIOs
224	VDD_DIG	PWR	0.9 V digital core supply for WLAN
225	BT_VDDC	PWR	0.9 V digital core supply for Bluetooth®
226	RF_SW_CTRL10	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
227	VSSC	GND	Core ground for WLAN and Bluetooth®
228	I2S_DO	I/O	I2S serial data output
229	VSSC	GND	Core ground for WLAN and Bluetooth®
230	BTLDO_VDDBAT	PWR	Battery supply input for Bluetooth® PA LDO
231	VSSC	GND	Core ground for WLAN and Bluetooth®

Notes

- 18. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.
- 19. No routing of the signal under this ball.
- 20. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 18 **CYW55571 WLCSP signal descriptions** (continued)

Bump #	Bump name	Type	Description
232	VSSC	GND	Core ground for WLAN and Bluetooth®
233	VSSC	GND	Core ground for WLAN and Bluetooth®
234	VSSC	GND	Core ground for WLAN and Bluetooth®
235	VDDIO_SD	PWR	1.8 V IO supply for SDIO Interface
236	VSSC	GND	Core ground for WLAN and Bluetooth®
237	I2S_SCK	I/O	I2S bit or serial clock
238	BT_VDDC	PWR	0.9 V digital core supply for Bluetooth®
239	BT_VDDC	PWR	0.9 V digital core supply for Bluetooth®
240	BT_AJTAG_TDI	–	–
241	VDD_DIG	PWR	0.9 V digital core supply for WLAN
242	VSSC	GND	Core ground for WLAN and Bluetooth®
243	BT_AJTAG_TDO	–	–
244	BT_VDDC	PWR	0.9 V digital core supply for Bluetooth®
245	BT_AJTAG_TMS	–	–
246	BT_TM1	I	Bluetooth® Core Test Mode Input and should be connected to VSSC
247	VDD_TOP	PWR	0.9 V digital core supply for WLAN/Bluetooth®
248	DMIC_DQ	I/O	Digital Mic Data
249	VDD_DIG	PWR	0.9 V digital core supply for WLAN
250	VSSC	GND	Core ground for WLAN and Bluetooth®
251	VDD_DIG	PWR	0.9 V digital core supply for WLAN
252	VDD_MAIN	PWR	0.9 V digital core supply for WLAN
253	VDD_RET_GL_IN	PWR	0.9 V digital core supply for WLAN
254	VSSO	GND	IO ground
255	VSSC	GND	Core ground for WLAN and Bluetooth®
256	VSSC	GND	Core ground for WLAN and Bluetooth®
257	VSSC	GND	Core ground for WLAN and Bluetooth®
258	VSSC	GND	Core ground for WLAN and Bluetooth®
259	VSSC	GND	Core ground for WLAN and Bluetooth®
260	BT_UART_CTS_N	I	UART clear-to-send. Active LOW clear-to-send signal for the HCI UART interface
261	I2S_DI	I/O	I2S serial data input
262	VDD_DIG	PWR	0.9 V digital core supply for WLAN
263	SDIO_CLK	I	SDIO clock input
264	VSSO	GND	IO ground

Notes

18.Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.

19.No routing of the signal under this ball.

20.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 18 **CYW55571 WLCSP signal descriptions** (continued)

Bump #	Bump name	Type	Description
265	PCI_PME_L	OD	PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal is asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the PCI bus local bus specification, revision 2.3.
266	BT_GPIO_17	I/O	Bluetooth® general purpose I/O
267	BT_GPIO_16	I/O	Bluetooth® general purpose I/O
268	VDDP_RFSW	O	VDDP power switch output
269	BT_VDDO	PWR	1.8 V IO supply for Bluetooth® GPIOs
270	GPIO_12	I/O	WLAN general purpose I/O
271	VSSC	GND	Core ground for WLAN and Bluetooth®
272	BT_LDO_VDDBAT	PWR	Battery supply input for Bluetooth® PA LDO
273	GPIO_2	I/O	WLAN general purpose I/O
274	VSSO	GND	IO ground
275	SDIO_DATA_1	I/O	SDIO data line 1
276	VSSC	GND	Core ground for WLAN and Bluetooth®
277	VSSC	GND	Core ground for WLAN and Bluetooth®
278	BT_GPIO_2	I/O	Bluetooth® general purpose I/O
279	BT_GPIO_4	I/O	Bluetooth® general purpose I/O
280	PACKAGEOPTION_1	I	Should be connected to VSSC
281	VDD_TOP	PWR	0.9 V digital core supply for WLAN/Bluetooth®
282	LHL_GPIO5	I/O	Miscellaneous general purpose I/O
283	BT_VDDC	PWR	0.9 V digital core supply for Bluetooth®
284	BT_GPIO_20	I/O	Bluetooth® general purpose I/O
285	BT_HOST_WAKE	I/O	Bluetooth® HOST WAKE
286	LHL_GPIO7	I/O	Miscellaneous general purpose I/O
287	VDDIO	PWR	1.8 V IO supply for WLAN GPIOs
288	RF_SW_CTRL04	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
289	VSSC	GND	Core ground for WLAN and Bluetooth®
290	VSSC	GND	Core ground for WLAN and Bluetooth®
291	BT_DEV_WAKE	I/O	Bluetooth® DEVICE WAKE
292	VSSC	GND	Core ground for WLAN and Bluetooth®
293	VSSC	GND	Core ground for WLAN and Bluetooth®
294	VDD_TOP	PWR	0.9 V digital core supply for WLAN/Bluetooth®
295	VDD_AON	PWR	0.9 V digital core supply for WLAN/Bluetooth®
296	VSSC	GND	Core ground for WLAN and Bluetooth®

Notes

18. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.

19. No routing of the signal under this ball.

20. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 18 **CYW55571 WLCSP signal descriptions** (continued)

Bump #	Bump name	Type	Description
297	BTPLL_AVDD1P0	PWR	1.0 V BTPLL analog supply
298	BT_VDDC	PWR	0.9 V digital core supply for Bluetooth®
299	AVDD_RX_1P0	PWR	1.0 V PCIe receiver supply input
300	AVSS_PCIE	GND	PCIe analog ground
301	AVSS_PCIE	GND	PCIe analog ground
302	PCIE_RDP	I	PCIe receiver differential pair positive input
303	AVDD_PLL_1P0	PWR	1.0 V PCIe analog supply
304	VSSC	GND	Core Gground for WLAN and Bluetooth®
305	PCIE_REFCLKP	I	PCIe differential pair clock source (100 MHz) positive input
306	PCIE_REFCLKN	I	PCIe differential pair clock source (100 MHz) negative input
307	ARMPLL_AVSS	PWR	1.0 V ARMPLL analog supply
308	WLPLL_AVDD1P0	PWR	1.0 V WLPLL analog supply
309	VSSC	GND	Core ground for WLAN and Bluetooth®
310	PCIE_RDN	I	PCIe receiver differential pair negative input
311	PCIE_TDP	O	PCIe transmitter differential pair positive output
312	AVDD_TX_1P0	PWR	1.0 V PCIe transmitter supply input
313	VSSC	GND	Core ground for WLAN and Bluetooth®
314	VDD_DIG	PWR	0.9 V digital core supply for WLAN
315	SDIO_CMD	I/O	SDIO command line
316	PCIE_TESTN	I/O	PCIe test differential pair negative pin
317	PCIE_TESTP	I/O	PCIe test differential pair positive pin
318	VDD_TOP	PWR	0.9 V digital core supply for WLAN/Bluetooth®
319	VDDIO_SD	PWR	1.8 V IO supply for SDIO Interface
320	VDDIO_SD	PWR	1.8 V IO supply for SDIO Interface
321	AVSS_PCIE	GND	PCIe analog ground
322	PCIE_TDN	O	PCIe transmitter differential pair negative output
323	BT_VDDO	PWR	1.8 V IO supply for Bluetooth® GPIOs
324	VSSC	GND	Core ground for WLAN and Bluetooth®
325	VDD_DIG	PWR	0.9 V digital core supply for WLAN
326	VDDIO_RFSW	PWR	IO supply for RF switch control pads
327	I2S_IRCK	I/O	I2S Word Clock or left/right clock
328	VSSO	GND	IO ground
329	BT_GPIO_11	I/O	Bluetooth® general purpose I/O
330	BT_GPIO_9	I/O	Bluetooth® general purpose I/O
331	VSSC	GND	Core ground for WLAN and Bluetooth®

Notes

18. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.
19. No routing of the signal under this ball.
20. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 18 CYW55571 WLCSP signal descriptions (continued)

Bump #	Bump name	Type	Description
332	VDD_DIG	PWR	0.9 V digital core supply for WLAN
333	VSSC	GND	Core ground for WLAN and Bluetooth®
334	VSSC	GND	Core ground for WLAN and Bluetooth®
335	VDD_DIG	PWR	0.9 V digital core supply for WLAN
336	LHL_GPIO4	I/O	Miscellaneous general purpose I/O
337	BT_UART_RXD	I	UART serial input. Serial data input for the HCI UART interface.
338	VSSC	GND	Core ground for WLAN and Bluetooth®
339	VSSC	GND	Core ground for WLAN and Bluetooth®
340	VSSC	GND	Core ground for WLAN and Bluetooth®
341	JTAG_SEL	I	JTAG Select input: Pull high to select the JTAG interface. If the JTAG interface is not used this pin should be connected to ground.
342	VSSC	GND	Core ground for WLAN and Bluetooth®
343	VSSC	GND	Core ground for WLAN and Bluetooth®
344	VSSC	GND	Core ground for WLAN and Bluetooth®
345	LHL_GPIO6	I/O	Miscellaneous general purpose I/O
346	LHL_VDDO	PWR	1.8 V IO supply for miscellaneous GPIO
347	VSSC	GND	Core ground for WLAN and Bluetooth®
348	VSSC	GND	Core ground for WLAN and Bluetooth®
349	VSSC	GND	Core ground for WLAN and Bluetooth®
350	VDD_MAIN	PWR	0.9 V digital core supply for WLAN
351	LHL_XTALO	O	32.768 kHz crystal oscillator output
352	LHL_GPIO3	I/O	Miscellaneous general purpose I/O
353	VSSC	GND	Core ground for WLAN and Bluetooth®
354	VDD_TOP	PWR	0.9 V digital core Supply for WLAN/Bluetooth®
355	PACKAGEOPTION_2	I	Should be connected to VSSC
356	VSSC	GND	Core ground for WLAN and Bluetooth®
357	VSSC	GND	Core ground for WLAN and Bluetooth®
358	RF_SW_CTRL13	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
359	VDD_TOP	PWR	0.9 V digital core supply for WLAN/Bluetooth®
360	VSSC	GND	Core ground for WLAN and Bluetooth®
361	GPIO_4	I/O	WLAN general purpose I/O
362	VDDIO	PWR	1.8 V IO supply for WLAN GPIOs
363	VDD_AON	PWR	0.9 V digital core supply for WLAN/Bluetooth®
364	GPIO_0	I/O	WLAN general purpose I/O

Notes

18. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.

19. No routing of the signal under this ball.

20. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 18 **CYW55571 WLCSP signal descriptions** (continued)

Bump #	Bump name	Type	Description
365	VSSO	GND	IO ground
366	VDDIO	PWR	1.8 V IO supply for WLAN GPIOs
367	GPIO_10	I/O	WLAN general purpose I/O
368	VDD_MAIN	PWR	0.9 V digital core supply for WLAN
369	PVSSC	GND	Ground input of CSR power stage
370	VDDOUT_SWCORE	O	–
371	VSSC	GND	–
372	VSSC	GND	Power switch output supply for VDD_TOP power supply input
373	CSR_VDD0P9	I	Core ground for WLAN and Bluetooth®
374	RF_SW_CTRL12	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
375	VDDOUT_RF3P3	PWR	3.3 V output to supply Bluetooth® PA
376	BT_VDDC	PWR	0.9 V digital core supply for Bluetooth®
377	VSSC	GND	Core ground for WLAN and Bluetooth®
378	LHL_GPIO2	I/O	Miscellaneous general purpose I/O
379	VSSC	GND	Core ground for WLAN and Bluetooth®
380	SDIO_DATA_0	I/O	SDIO data line 0
381	BT_VDDO_SMIF	PWR	1.8 V SMIF interface IO supply
382	VSSO	GND	IO ground
383	VSSC	GND	Core ground for WLAN and Bluetooth®
384	VDD_TOP	PWR	0.9 V digital core supply for WLAN/Bluetooth®
385	VSSC	GND	Core ground for WLAN and Bluetooth®
386	VDD_DIG	PWR	0.9 V digital core supply for WLAN
387	VDD_DIG	PWR	0.9 V digital core supply for WLAN
388	VDD_DIG	PWR	0.9 V digital core supply for WLAN
389	VSSC	GND	Core ground for WLAN and Bluetooth®
390	VDD_DIG	PWR	0.9 V digital core supply for WLAN
391	GPIO_14	I/O	WLAN general purpose I/O
392	PCIE_CLKREQ_L	OD	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated 0 = the clock is required
393	VDD_DIG	PWR	0.9 V Digital core supply for WLAN
394	BT_GPIO_12	I/O	Bluetooth® general purpose I/O
395	BT_GPIO_14	I/O	Bluetooth® general purpose I/O
396	BT_GPIO_19	I/O	Bluetooth® general purpose I/O

Notes

18. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.

19. No routing of the signal under this ball.

20. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 18 **CYW55571 WLCSP signal descriptions** (continued)

Bump #	Bump name	Type	Description
397	RF_SW_CTRL19	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
398	RF_SW_CTRL17	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
399	VDD_MAIN	PWR	0.9 V digital core supply for WLAN
400	VDD_AON	PWR	0.9 V digital core supply for WLAN/Bluetooth®
401	RF_SW_CTRL03	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
402	VDD_MAIN	PWR	0.9 V digital core supply for WLAN
403	VSSC	GND	Core ground for WLAN and Bluetooth®
404	GPIO_11	I/O	WLAN general purpose I/O
405	GPIO_3	I/O	WLAN general purpose I/O
406	MON_RF_PGNDREG	O	PGNDREG monitor output
407	VSSC	GND	Core ground for WLAN and Bluetooth®
408	VDD_MAIN	PWR	0.9 V digital core supply for WLAN
409	VDD_MAIN	PWR	0.9 V digital core supply for WLAN
410	VSSC	GND	Core ground for WLAN and Bluetooth®
411	VSSC	GND	Core ground for WLAN and Bluetooth®
412	LHL_GPIO0	I/O	Miscellaneous general purpose I/O
413	LHL_GPIO1	I/O	Miscellaneous general purpose I/O
414	BT_VDDC	PWR	0.9 V digital core supply for Bluetooth®
415	VSSC	GND	Core ground for WLAN and Bluetooth®
416	GPIO_8	I/O	WLAN general purpose I/O
417	VSSC	GND	Core ground for WLAN and Bluetooth®
418	VSSC	GND	Core ground for WLAN and Bluetooth®
419	LPO_IN	I	External Sleep clock input (32.768 kHz)
420	VSSC	GND	Core ground for WLAN and Bluetooth®
421	VDD_TOP	PWR	0.9 V digital core supply for WLAN/Bluetooth®
422	VSSO_SMIF	GND	IO ground
423	VSSC	GND	Core ground for WLAN and Bluetooth®
424	VDD_MAIN	PWR	0.9 V digital core supply for WLAN
425	BT_VDDO	PWR	1.8 V IO supply for Bluetooth® GPIOs
426	BT_GPIO_10	I/O	Bluetooth® general purpose I/O
427	BT_VDDC	PWR	0.9 V digital core supply for Bluetooth®
428	BT_VDDC	PWR	0.9 V digital core supply for Bluetooth®
429	BT_VDDO_SMIF	PWR	1.8 V SMIF interface IO Supply
430	VSSC	GND	Core ground for WLAN and Bluetooth®

Notes

18. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.
19. No routing of the signal under this ball.
20. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 18 **CYW55571 WLCSP signal descriptions** *(continued)*

Bump #	Bump name	Type	Description
431	BT_VDDC	PWR	0.9 V digital core supply for Bluetooth®
432	VSSC	GND	Core ground for WLAN and Bluetooth®
433	BT_VDDC	PWR	0.9 V Ddigital core supply for Bluetooth®
434	BT_UART_TXD	O	UART serial output. Serial data output for the HCI UART interface.
435	BT_UART_RTS_N	O	UART request-to-send. Active LOW request-to-send signal for the HCI UART interface. Bluetooth® LED control pin.
436	BT_VDDC	PWR	0.9 V digital core supply for Bluetooth®
437	RF_SW_CTRL18	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
438	VDD_MAIN	PWR	0.9 V digital core supply for WLAN
439	GPIO_5	I/O	WLAN general purpose I/O
440	RF_SW_CTRL11	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
441	VSSC	GND	Core ground for WLAN and Bluetooth®
442	RF_SW_CTRL08	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
443	VSSC	GND	Core ground for WLAN and Bluetooth®
444	GPIO_9	I/O	WLAN general purpose I/O
445	GPIO_7	I/O	WLAN general purpose I/O
446	GPIO_6	I/O	WLAN general purpose I/O
447	VSSC	GND	Core ground for WLAN and Bluetooth®
448	VDD_MAIN	PWR	0.9 V digital core supply for WLAN
449	VSSC	GND	Core ground for WLAN and Bluetooth®
450	VDD_MAIN	PWR	0.9 V digital core supply for WLAN
451	VSSC	GND	Core ground for WLAN and Bluetooth®
452	VSSC	GND	Core ground for WLAN and Bluetooth®
453	FLL_VDDIO	PWR	1.8 V supply for FLL
454	VSSC	GND	Core ground for WLAN and Bluetooth®
455	VSSC	GND	Core ground for WLAN and Bluetooth®
456	LHL_XTALI	I	32.768 kHz crystal oscillatorinput
457	VDD_AON	PWR	0.9 V digital core supply for WLAN/Bluetooth®
458	VSSC	GND	Core ground for WLAN and Bluetooth®
459	VSSC	GND	Core ground for WLAN and Bluetooth®
460	VDD_DIG	PWR	0.9 V digital core supply for WLAN
461	BT_VDDO_SMIF	PWR	1.8 V SMIF interface IO supply
462	VDD_DIG	PWR	0.9 V digital core supply for WLAN

Notes

18. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.

19. No routing of the signal under this ball.

20. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 18 **CYW55571 WLCSP signal descriptions** *(continued)*

Bump #	Bump name	Type	Description
463	SDIO_DATA_3	I/O	SDIO data line 3
464	VDD_AON	PWR	0.9 V digital core supply for WLAN/Bluetooth®
465	BT_AJTAG_TCK	–	–
466	VSSC	GND	Core ground for WLAN and Bluetooth®
467	VSSC	GND	Core ground for WLAN and Bluetooth®
468	SMIF_SPHB_DQ3	I/O	SMIF data Line 3
469	VSSO_SMIF	GND	IO ground
470	VSSC	GND	Core ground for WLAN and Bluetooth®
471	BT_GPIO_5	I/O	Bluetooth® general purpose I/O
472	BT_GPIO_8	I/O	Bluetooth® general purpose I/O
473	BT_GPIO_6	I/O	Bluetooth® general purpose I/O
474	VSSC	GND	Core ground for WLAN and Bluetooth®
475	PCIE_PERST_L	I	PCIe system reset: This input is the PCIe reset as defined in the PCIe base specification v1.1.
476	VSSC	GND	Core ground for WLAN and Bluetooth®
477	BT_VDDC	PWR	0.9 V digital core supply for Bluetooth®
478	BT_GPIO_7	I/O	Bluetooth® general purpose I/O
479	BT_GPIO_13	I/O	Bluetooth® general purpose I/O
480	BT_GPIO_15	I/O	Bluetooth® general purpose I/O
481	VSSC	GND	Core ground for WLAN and Bluetooth®
482	VSSC	GND	Core ground for WLAN and Bluetooth®
483	VSSC	GND	Core ground for WLAN and Bluetooth®
484	VDD_AON	PWR	0.9 V digital core supply for WLAN/Bluetooth®
485	VDD_MAIN	PWR	0.9 V digital core supply for WLAN
486	VSSC	GND	Core ground for WLAN and Bluetooth®

Notes

- 18. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.
- 19. No routing of the signal under this ball.
- 20. Need to have a 50 Ω termination to ground.

12.4 CYW55571 FCFBGA package ball map

Figure 27 shows the CYW55571 FCFBGA package ball map.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	CSR_VDDBAT	CSR_VDDBAT	CSR_VLX	CSR_VLX	PVSSC	PVSSC	SMIF_SPHB_DQ2	SMIF_SPHB_CK	RF_SW_CTRL02	RF_SW_CTRL04	RF_SW_CTRL14	VDDP_RFSW	VDDIO_RFSW	RF_SW_CTRL16	WRF_PMU_VDD_3P3_C1	WRF_GND	WRF_GND	A
B	ASR_VDDBAT	ASR_VDDBAT	ASR_VDD1P12	CSR_VDD0P9	SMIF_SPHB_CS0_N	SMIF_SPHB_CS1_N	SMIF_SPHB_DQ3	SMIF_SPHB_DQ0	RF_SW_CTRL12	RF_SW_CTRL15	RF_SW_CTRL13	RF_SW_CTRL08	RF_SW_CTRL18	RF_SW_CTRL11	WRF_GND	WRF_GND	NC1	B
C	ASR_VLX	ASR_VLX	ASR_VLX	VDDOUT_MISC	RF_SW_CTRL07	RF_SW_CTRL06	RF_SW_CTRL09	SMIF_SPHB_DQ1	GPIO_2	GPIO_11	RF_SW_CTRL17	GPIO_5	RF_SW_CTRL10	NC	WRF_GND	WRF_GND	NC4	C
D	PVSSA	PVSSA	MISC_SNS	BTREG_ON	RF_SW_CTRL03	RF_SW_CTRL05	RF_SW_CTRL00	RF_SW_CTRL01	GPIO_8	GPIO_3	LHL_GPIO0	RF_SW_CTRL19	WRF_VDD_1P8_C1	WRF_GND	WRF_GND	WRF_PA_VDD_3P3_C1	WRF_GND	D
E	BTLDO_VDDBAT	BTLDO_VDDBAT	VDDOUT_SWCORE	PMU_AVSS	VDD_RET_GL	GPIO_9	GPIO_1	VDDIO	VSSC	VDD_AON	VSSC	WRF_GND	WRF_GND	NC	WRF_GND	WRF_PA_VDD_3P3_C1	NC2	E
F	VDDOUT_BT3P3	VDDOUT_BT3P3	BT3P3_SNS	PMU_AVSS	WLREG_ON	GPIO_6	GPIO_7	VSSC	VDD_MAIN	VDD_AON	VDD_MAIN	WRF_GND	WRF_PMU_VDD_1P12_C1	WRF_GND	WRF_GND	WRF_GND	NC3	F
G	VDDOUT_PA3P3	VDDOUT_PA3P3	VDDOUT_PA3P3	PA3P3_SNS	MIC_N	VSSC	GPIO_10	GPIO_12	GPIO_4	VDD_MAIN	VSSC	WRF_AFE_VDD_1P12_C1	WRF_SYNTH_VDD_1P12	WRF_GND	WRF_GND	WRF_GND	WRF_RFIN_5G_C0	G
H	WLLDO_VDDBAT	WLLDO_VDDBAT	WLLDO_VDDBAT	RF3P3_SNS	MIC_P	LHL_GPIO3	GPIO_0	JTAG_SEL	LHL_GPIO1	VDD_MAIN	VSSC	WRF_GND	WRF_VCO_VDD_1P12	WRF_VCO_VDD_3P3	WRF_GND	WRF_GND	WRF_PAOUT_5G_C0	H
J	VDDOUT_RF3P3	VDDOUT_RF3P3	PMU_VDD1P8	VSSC	LPO_IN	VSSC	VSSC	WLPLL_AVDD1P0	LHL_XTAL1	VDD_TOP	VSSC	WRF_GND	WRF_SYNTH_VDD_3P3	WRF_PMU_VDD_3P3_C0	WRF_GND	WRF_PA_VDD_3P3_C0	WRF_GND	J
K	SDIO_CLK	SDIO_DATA_0	SDIO_DATA_2	SDIO_CMD	LHL_GPIO2	VDDIO_SD	VSSC	VDD_DIG	LHL_XTAL0	VDD_TOP	VDD_TOP	WRF_AFE_VDD_1P12_C0	WRF_PMU_VDD_1P12_C0	WRF_VDD_1P8_C0	WRF_GND	WRF_PA_VDD_3P3_C0	WRF_PAOUT_2G_C0	K
L	PCIE_RDP	SDIO_DATA_1	SDIO_DATA_3	AVSS_PCIE	PCIE_PERST_L	VSSC	VDD_AON	LHL_VDD0	VDD_RET_GL_IN	BT_VDDC	VDD_DIG	WRF_TSS1G_OUT_C0	WRF_GPAIO_TS1G2G_OUT_C0	BTRF_VSS	BTRF_VSS	WRF_GND	WRF_RFIN_2G_C0	L
M	PCIE_RDN	AVSS_PCIE	PCIE_TESTP	AVSS_PCIE	PCI_PME_L	VDD_DIG	VSSC	VDD_DIG	BT_GPIO_10	BT_VDDC	BT_GPIO_9	NC	BTRF_LDO_VDD_1P12	BTRF_VSS	BTRF_VSS	BTRF_VSS	BTRF_VSS	M
N	PCIE_TDP	AVSS_PCIE	PCIE_TESTN	AVSS_PCIE	PCIE_CLKREQ_L	VSSC	I2S_DI	VSSC	BTPLL_AVDD1P0	BT_VDD0_SMIF	VSSC	XTAL_GND	BTRF_TEST	BTRF_VSS	BTRF_VSS	BTRF_VSS	BTRF_RF_OP	N
P	PCIE_TDN	AVSS_PCIE	AVDD_TX_1P0	AVSS_PCIE	GPIO_13	BT_GPIO_19	I2S_DO	BT_UART_RXD	BT_GPIO_2	BT_GPIO_8	BT_GPIO_11	XTAL_GND	XTAL_GND	BTRF_VSS	BTRF_PAVDD_3P3	BTRF_VSS	BTRF_13DBM_OP	P
R	AVSS_PCIE	AVSS_PCIE	AVDD_PLL_1P0	AVDD_RX_1P0	BT_GPIO_18	GPIO_14	I2S_IRCK	BT_UART_CTS_N	BT_GPIO_3	BT_GPIO_7	BT_GPIO_20	XTAL_VDD_1P12	VDD_XTAL	XTAL_GND	BTRF_VSS	BTRF_VSS	BTRF_VSS	R
T	PCIE_REFCLKP	AVSS_PCIE	BT_GPIO_12	BT_GPIO_14	BT_GPIO_17	DMIC_DQ	I2S_SCK	BT_UART_RTS_N	BT_GPIO_4	BT_GPIO_6	BT_DEV_WAKE	XTAL_GND	XTAL_GND	XTAL_GND	XTAL_GND	BTRF_VSS	BTRF_20DBM_OP	T
U	PCIE_REFCLKN	AVSS_PCIE	BT_GPIO_13	BT_GPIO_15	BT_GPIO_16	DMIC_CK	I2S_MCK	BT_UART_TXD	BT_GPIO_5	BT_VDD0	BT_HOST_WAKE	XTAL_GND	XTAL_XOP	XTAL_XON	XTAL_GND	BTRF_VSS	BTRF_VSS	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 27 12 × 12 mm FCFBGA package ball map

Pinout and signal descriptions
12.5 FCFBGA package signal descriptions

The signal name, type, and description of each pin in CYW55571 is listed in [Table 19](#). The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, O = output, PWR = power, GND = ground, OD = open-drain) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

Table 19 CYW55571 FCFBGA signal descriptions

Ball #	Ball name	Type	Description
B15	WRF_GND	GND	WLAN radio ground
A16	WRF_GND	GND	WLAN radio ground
H13	WRF_VCO_VDD_1P12	PWR	WLAN radio 1.12 V supply
D17	WRF_GND	GND	WLAN radio ground
A17	WRF_GND	GND	WLAN radio ground
J17	WRF_GND	GND	WLAN radio ground
E13	WRF_GND	GND	WLAN radio ground
K14	WRF_VDD_1P8_C0	PWR	WLAN radio 1.8 V Core0 supply
H17	WRF_PAOUT_5G_C0	O	WLAN radio Core0 5/6 GHz PA output
L13	WRF_GPAIO_TSSI2G_OUT_C0	O	WLAN radio 2.4 GHz TSSI Core0
E14	NC ^[22]	O	WLAN radio 2.4 GHz TSSI Core1
H14	WRF_VCO_VDD_3P3	PWR	WLAN radio 3.3 V Supply
G12	WRF_AFE_VDD_1P12_C1	PWR	WLAN radio 1.12 V Core1 supply
L12	WRF_TSSI5G_OUT_C0	O	WLAN radio 5/6 GHz TSSI Core0
C15	WRF_GND	GND	WLAN radio ground
F13	WRF_PMU_VDD_1P12_C1	PWR	WLAN radio 1.12 V Core1 supply
F14	WRF_GND	GND	WLAN radio ground
B16	WRF_GND	GND	WLAN radio ground
G13	WRF_SYNTH_VDD_1P12	PWR	WLAN radio 1.12 V supply
B17	NC1 ^[23]	I	WLAN radio 5/6 GHz Core1 receiver input
D13	WRF_VDD_1P8_C1	PWR	WLAN radio 1.8 V Core1 supply
K16	WRF_PA_VDD_3P3_C0	PWR	WLAN radio 3.3 V Core0 PA supply
C16	WRF_GND	GND	WLAN radio ground
D15	WRF_GND	GND	WLAN radio ground
D16	WRF_PA_VDD_3P3_C1	PWR	WLAN radio 3.3 V Core1 PA supply
F16	WRF_GND	GND	WLAN radio ground
H15	WRF_GND	GND	WLAN radio ground
E16	WRF_PA_VDD_3P3_C1	PWR	WLAN radio 3.3 V Core1 PA supply
E17	NC2 ^[23]	O	WLAN radio Core1 2.4 GHz PA output
K17	WRF_PAOUT_2G_C0	O	WLAN radio Core0 2.4 GHz PA output
K13	WRF_PMU_VDD_1P12_C0	PWR	WLAN radio 1.12 V Core0 supply

Notes

21. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.

22. No routing of the signal under this ball.

23. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 19 **CYW55571 FCFBGA signal descriptions** *(continued)*

Ball #	Ball name	Type	Description
G16	WRF_GND	GND	WLAN radio ground
H16	WRF_GND	GND	WLAN radio ground
K15	WRF_GND	GND	WLAN radio ground
J16	WRF_PA_VDD_3P3_C0	PWR	WLAN radio 3.3 V Core0 PA supply
L16	WRF_GND	GND	WLAN radio ground
J15	WRF_GND	GND	WLAN radio ground
L17	WRF_RFIN_2G_C0	I	WLAN radio 2.4 GHz Core0 receiver input
G15	WRF_GND	GND	WLAN radio ground
J13	WRF_SYNTN_VDD_3P3	PWR	WLAN radio 3.3 V Supply
F15	WRF_GND	GND	WLAN radio ground
E15	WRF_GND	GND	WLAN radio ground
F17	NC3 ^[23]	I	WLAN radio 2.4 GHz Core1 receiver input
G14	WRF_GND	GND	WLAN radio ground
E12	WRF_GND	GND	WLAN radio ground
G17	WRF_RFIN_5G_C0	I	WLAN radio 5/6 GHz Core0 receiver input
F12	WRF_GND	GND	WLAN radio ground
D14	WRF_GND	GND	WLAN radio ground
H12	WRF_GND	GND	WLAN radio ground
A15	WRF_PMU_VDD_3P3_C1	PWR	WLAN radio 3.3 V Core1 Supply
J12	WRF_GND	GND	WLAN radio ground
J14	WRF_PMU_VDD_3P3_C0	PWR	WLAN radio 3.3 V Core0 supply
K12	WRF_AFE_VDD_1P12_C0	PWR	WLAN radio 1.12 V Core0 supply
C14	NC ^[22]	O	WLAN radio 5/6 GHz TSSI Core1
C17	NC4 ^[23]	O	WLAN radio Core1 5/6 GHz PA output
U13	XTAL_XOP	I	XTAL oscillator input
U15	XTAL_GND	GND	XTAL oscillator ground
U14	XTAL_XON	O	XTAL oscillator output
R13	VDD_XTAL	PWR	XTAL oscillator 1.0 V supply
R12	XTAL_VDD_1P12	PWR	XTAL oscillator 1.12 V supply
T13	XTAL_GND	GND	XTAL oscillator ground
U12	XTAL_GND	GND	XTAL oscillator ground
P15	BTRF_PAVDD_3P3	PWR	Bluetooth® radio 3.3 V PA supply
P16	BTRF_VSS	GND	Bluetooth® radio ground
P14	BTRF_VSS	GND	Bluetooth® radio ground
L14	BTRF_VSS	GND	Bluetooth® radio ground
N16	BTRF_VSS	GND	Bluetooth® radio ground

Notes

21. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.

22. No routing of the signal under this ball.

23. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 19 **CYW55571 FCFBGA signal descriptions** *(continued)*

Ball #	Ball name	Type	Description
N14	BTRF_VSS	GND	Bluetooth® radio ground
M17	BTRF_VSS	GND	Bluetooth® radio ground
N15	BTRF_VSS	GND	Bluetooth® radio ground
T16	BTRF_VSS	GND	Bluetooth® radio ground
U16	BTRF_VSS	GND	Bluetooth® radio ground
R15	BTRF_VSS	GND	Bluetooth® radio ground
L15	BTRF_VSS	GND	Bluetooth® radio ground
M14	BTRF_VSS	GND	Bluetooth® radio ground
M15	BTRF_VSS	GND	Bluetooth® radio ground
M16	BTRF_VSS	GND	Bluetooth® radio ground
U17	BTRF_VSS	GND	Bluetooth® radio ground
N13	BTRF_TEST	I/O	Bluetooth® radio test input/output pin
N17	BTRF_RF_OP	I/O	Bluetooth® BDR/LE 0DBM radio output and BDR/LE/EDR radio input
R17	BTRF_VSS	GND	Bluetooth® radio ground
P17	BTRF_13DBM_OP	O	Bluetooth® BDR/LE13DBM and EDR 9DBM radio output
M13	BTRF_LDO_VDD_1P12	PWR	Bluetooth® radio 1.12 V input supply
R16	BTRF_VSS	GND	Bluetooth® radio ground
T17	BTRF_20DBM_OP	O	Bluetooth® BDR/LE 20DBM and EDR 13DBM radio output
A6	PVSSC	GND	Ground input of CSR power stage
G1	VDDOUT_PA3P3	PWR	3.3 V Output to Supply WLAN PA
E4	PMU_AVSS	GND	PMU analog ground
F3	BT3P3_SNS	I	Feedback input of BT3P3 LDO
A1	CSR_VDDBAT	PWR	Battery supply input for CSR power stage
A2	CSR_VDDBAT	PWR	Battery supply input for CSR power stage
E3	VDDOUT_SWCORE	O	Power switch output supply for VDD_TOP power supply input
E5	VDD_RET_GL	O	Power MUX output supply for VDD_RET_GL_IN power supply input
E1	BTLDO_VDDBAT	PWR	Battery supply input for Bluetooth® PA LDO
E2	BTLDO_VDDBAT	PWR	Battery supply input for Bluetooth® PA LDO
F1	VDDOUT_BT3P3	PWR	3.3 V output to supply Bluetooth® PA
D1	PVSSA	GND	Ground input of ASR power stage
G5	MIC_N	I	ADC Microphone negative input
F4	PMU_AVSS	GND	PMU analog ground
D3	MISC_SNS	I	Feedback input of MISC LDO

Notes

21. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.
22. No routing of the signal under this ball.
23. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 19 CYW55571 FCFBGA signal descriptions (continued)

Ball #	Ball name	Type	Description
D2	PVSSA	GND	Ground input of ASR power stage
A5	PVSSC	GND	Ground input of CSR power stage
B3	ASR_VDD1P12	I	Sense or feedback input of ASR power stage
F2	VDDOUT_BT3P3	PWR	3.3 V output to supply Bluetooth® PA
G2	VDDOUT_PA3P3	PWR	3.3 V output to supply WLAN PA
A4	CSR_VLX	O	CSR power stage output to inductor
A3	CSR_VLX	O	CSR power stage output to inductor
J1	VDDOUT_RF3P3	PWR	3.3 V output to supply WLAN radio
C1	ASR_VLX	O	ASR power stage output to inductor
J3	PMU_VDD1P8	PWR	1.8 V PMU supply input
C2	ASR_VLX	O	ASR power stage output to inductor
H1	WLLDO_VDDBAT	PWR	Battery supply input for WLAN PA and RF LDO
F5	WLREG_ON	I	Used by the PMU to power up or power down the internal CYW55571 regulators used by the WLAN section. When deasserted, this pin holds the WLAN section in reset. This pin has an internal 50 kΩ pull-down resistor that is auto enabled/disabled by programming.
B1	ASR_VDDBAT	PWR	Battery supply input for ASR power stage
H2	WLLDO_VDDBAT	PWR	Battery supply input for WLAN PA LDO and RF LDO
H3	WLLDO_VDDBAT	PWR	Battery supply input for WLAN PA LDO and RF LDO
B2	ASR_VDDBAT	PWR	Battery supply input for ASR power stage
H5	MIC_P	I	ADC Microphone positive input
J4	VSSC	GND	Core ground for WLAN and Bluetooth®
C3	ASR_VLX		ASR power stage output to inductor
J2	VDDOUT_RF3P3	PWR	3.3 V output to supply WLAN radio
D4	BTREG_ON	I	Used by the PMU to power up or power down the internal CYW55571 regulators used by the Bluetooth® section. When deasserted, this pin holds the Bluetooth® section in reset. This pin has an internal 50 kΩ pull-down resistor that is auto enabled/disabled by programming.
B4	CSR_VDD0P9	I	Sense or feedback Input of CSR power stage
H4	RF3P3_SNS	I	Feedback input of RF3P3 LDO
C4	VDDOUT_MISC	O	Output of VDDOUT_MISC
G4	PA3P3_SNS	I	Feedback input of PA3P3 LDO
G3	VDDOUT_PA3P3	PWR	3.3 V output to supply WLAN PA
N1	PCIE_TDP	O	PCIe transmitter differential pair positive output
P1	PCIE_TDN	O	PCIe transmitter differential pair negative output

Notes

21. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.
22. No routing of the signal under this ball.
23. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 19 CYW55571 FCBGA signal descriptions (continued)

Ball #	Ball name	Type	Description
T1	PCIE_REFCLKP	I	PCIe differential pair clock source (100 MHz) positive input
U1	PCIE_REFCLKN	I	PCIe differential pair clock source (100 MHz) negative input
L1	PCIE_RDP	I	PCIe receiver differential pair positive input
M1	PCIE_RDN	I	PCIe receiver differential pair negative input
N3	PCIE_TESTN	I/O	PCIe test differential pair negative pin
M3	PCIE_TESTP	I/O	PCIe test differential pair positive pin
R3	AVDD_PLL_1P0	PWR	1.0 V PCIe analog supply
P3	AVDD_TX_1P0	PWR	1.0 V PCIe transmitter supply input
M2	AVSS_PCIE	GND	PCIe analog ground
R4	AVDD_RX_1P0	PWR	1.0 V PCIe receiver supply input
J11	VSSC	GND	Core ground for WLAN and Bluetooth®
D12	RF_SW_CTRL19	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
B13	RF_SW_CTRL18	O	
C11	RF_SW_CTRL17	O	
A14	RF_SW_CTRL16	O	
B10	RF_SW_CTRL15	O	
A11	RF_SW_CTRL14	O	
B11	RF_SW_CTRL13	O	
B9	RF_SW_CTRL12	O	
B14	RF_SW_CTRL11	O	
C13	RF_SW_CTRL10	O	
C7	RF_SW_CTRL09	O	
B12	RF_SW_CTRL08	O	
C5	RF_SW_CTRL07	O	
C6	RF_SW_CTRL06	O	
D6	RF_SW_CTRL05	O	
A10	RF_SW_CTRL04	O	
D5	RF_SW_CTRL03	O	
A9	RF_SW_CTRL02	O	
D8	RF_SW_CTRL01	O	
D7	RF_SW_CTRL00	O	
G11	VSSC	GND	Core ground for WLAN and Bluetooth®
E10	VDD_AON	PWR	0.9 V digital core supply for WLAN/Bluetooth®
A13	VDDIO_RFSW	PWR	IO supply for RF switch control pads
E9	VSSC	GND	Core ground for WLAN and Bluetooth®

Notes

21. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.
22. No routing of the signal under this ball.
23. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 19 **CYW55571 FCFBGA signal descriptions** *(continued)*

Ball #	Ball name	Type	Description
A12	VDDP_RFSW	O	VDDP power switch output
E11	VSSC	GND	Core ground for WLAN and Bluetooth®
G6	VSSC	GND	Core ground for WLAN and Bluetooth®
J6	VSSC	GND	Core ground for WLAN and Bluetooth®
M7	VSSC	GND	Core ground for WLAN and Bluetooth®
J7	VSSC	GND	Core ground for WLAN and Bluetooth®
F8	VSSC	GND	Core ground for WLAN and Bluetooth®
N10	BT_VDDO_SMIF	PWR	1.8 V SMIF interface IO supply
A8	SMIF_SPHB_CK	O	SMIF clock output
B7	SMIF_SPHB_DQ3	I/O	SMIF data line 3
A7	SMIF_SPHB_DQ2	I/O	SMIF data line 2
C8	SMIF_SPHB_DQ1	I/O	SMIF data line 1
B8	SMIF_SPHB_DQ0	I/O	SMIF data line 0
B5	SMIF_SPHB_CS0_N	O	SMIF Chip Select0 active LOW output
B6	SMIF_SPHB_CS1_N	O	SMIF Chip Select0 active LOW output
H11	VSSC	GND	Core ground for WLAN and Bluetooth®
N6	VSSC	GND	Core ground for WLAN and Bluetooth®
L6	VSSC	GND	Core ground for WLAN and Bluetooth®
K7	VSSC	GND	Core ground for WLAN and Bluetooth®
R8	BT_UART_CTS_N	I	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
U8	BT_UART_TXD	O	UART Serial Output. Serial data output for the HCI UART interface.
T8	BT_UART_RTS_N	O	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. Bluetooth® LED control pin.
P8	BT_UART_RXD	I	UART serial input. Serial data input for the HCI UART interface.

Notes

21. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.

22. No routing of the signal under this ball.

23. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 19 **CYW55571 FCFBGA signal descriptions** *(continued)*

Ball #	Ball name	Type	Description
R11	BT_GPIO_20	I/O	Bluetooth® general purpose I/O
P6	BT_GPIO_19	I/O	
R5	BT_GPIO_18	I/O	
T5	BT_GPIO_17	I/O	
U5	BT_GPIO_16	I/O	
U4	BT_GPIO_15	I/O	
T4	BT_GPIO_14	I/O	
U3	BT_GPIO_13	I/O	
T3	BT_GPIO_12	I/O	
P11	BT_GPIO_11	I/O	
M9	BT_GPIO_10	I/O	
M11	BT_GPIO_9	I/O	
P10	BT_GPIO_8	I/O	
R10	BT_GPIO_7	I/O	
T10	BT_GPIO_6	I/O	
U9	BT_GPIO_5	I/O	
T9	BT_GPIO_4	I/O	
R9	BT_GPIO_3	I/O	
P9	BT_GPIO_2	I/O	
T11	BT_DEV_WAKE	I/O	Bluetooth® DEVICE WAKE
U11	BT_HOST_WAKE	I/O	Bluetooth® HOST WAKE
U10	BT_VDDO	PWR	1.8 V IO supply for Bluetooth® GPIOs
M10	BT_VDDC	PWR	0.9 V Digital core supply for Bluetooth®
R7	I2S_IRCK	I/O	I2S Word Clock or left/right clock
T7	I2S_SCK	I/O	I2S bit or serial clock
U7	I2S_MCK	I/O	I2S master clock
N7	I2S_DI	I/O	I2S serial data input
P7	I2S_DO	I/O	I2S serial data iutput
U6	DMIC_CK	I/O	Digital mic clock
T6	DMIC_DQ	I/O	Digital mic data
L10	BT_VDDC	PWR	0.9 V Digital core supply for Bluetooth®
K6	VDDIO_SD	PWR	1.8 V IO supply For SDIO interface
L3	SDIO_DATA_3	I/O	SDIO data line 3
K3	SDIO_DATA_2	I/O	SDIO data line 2
L2	SDIO_DATA_1	I/O	SDIO data line 1
K2	SDIO_DATA_0	I/O	SDIO data line 0

Notes

21. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.
22. No routing of the signal under this ball.
23. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 19 **CYW55571 FCFBGA signal descriptions** *(continued)*

Ball #	Ball name	Type	Description
K4	SDIO_CMD	I/O	SDIO command line
K1	SDIO_CLK	I	SDIO clock input
L7	VDD_AON	PWR	0.9 V Digital core supply for WLAN/Bluetooth®
F10	VDD_AON	PWR	0.9 V Digital core supply for WLAN/Bluetooth®
M5	PCI_PME_L	OD	PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal is asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the PCI Bus Local Bus Specification, revision 2.3.
N5	PCIE_CLKREQ_L	OD	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated 0 = the clock is required
L5	PCIE_PERST_L	I	PCIe system reset: This input is the PCIe reset as defined in the PCIe base specification v1.1.
R6	GPIO_14	I/O	WLAN general purpose I/O
P5	GPIO_13	I/O	
G8	GPIO_12	I/O	
C10	GPIO_11	I/O	
G7	GPIO_10	I/O	
E6	GPIO_9	I/O	
D9	GPIO_8	I/O	
F7	GPIO_7	I/O	
F6	GPIO_6	I/O	
C12	GPIO_5	I/O	
G9	GPIO_4	I/O	
D10	GPIO_3	I/O	
C9	GPIO_2	I/O	
E7	GPIO_1	I/O	
H7	GPIO_0	I/O	
E8	VDDIO	PWR	1.8 V IO supply for WLAN GPIOs
H8	JTAG_SEL	I	JTAG Select Input: Pull high to select the JTAG interface. If the JTAG interface is not used this pin should be connected to ground.
J5	LPO_IN	I	External Sleep clock input (32.768 kHz)
J9	LHL_XTALI	I	32.768 kHz crystal oscillator input
K9	LHL_XTALO	O	32.768 kHz crystal oscillator output
L8	LHL_VDDO	PWR	1.8 V IO supply for miscellaneous GPIO

Notes

21. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.
22. No routing of the signal under this ball.
23. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 19 **CYW55571 FCFBGA signal descriptions** *(continued)*

Ball #	Ball name	Type	Description
D11	LHL_GPIO0	I/O	Miscellaneous general purpose I/O
H9	LHL_GPIO1	I/O	
K5	LHL_GPIO2	I/O	
H6	LHL_GPIO3	I/O	
N11	VSSC	GND	Core ground for WLAN and Bluetooth®
N8	VSSC	GND	
K8	VDD_DIG	PWR	0.9 V Digital core supply for WLAN
L11	VDD_DIG	PWR	
M6	VDD_DIG	PWR	
M8	VDD_DIG	PWR	
F9	VDD_MAIN	PWR	0.9 V Digital core supply for WLAN
F11	VDD_MAIN	PWR	
G10	VDD_MAIN	PWR	
H10	VDD_MAIN	PWR	
L9	VDD_RET_GL_IN	PWR	0.9 V Digital core supply for WLAN
K11	VDD_TOP	PWR	0.9 V Digital core supply for WLAN/Bluetooth®
K10	VDD_TOP	PWR	
J10	VDD_TOP	PWR	
J8	WLPLL_AVDD1P0	PWR	1.0 V WLPLL analog supply
N9	BTPLL_AVDD1P0	PWR	1.0 V BTPLL analog supply
N2	AVSS_PCIE	GND	PCIe analog ground
P2	AVSS_PCIE	GND	
R1	AVSS_PCIE	GND	
R2	AVSS_PCIE	GND	
T2	AVSS_PCIE	GND	
U2	AVSS_PCIE	GND	
L4	AVSS_PCIE	GND	
M4	AVSS_PCIE	GND	
N4	AVSS_PCIE	GND	
P4	AVSS_PCIE	GND	

Notes

21. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.

22. No routing of the signal under this ball.

23. Need to have a 50 Ω termination to ground.

Pinout and signal descriptions**Table 19** **CYW55571 FCFBGA signal descriptions** *(continued)*

Ball #	Ball name	Type	Description
T15	XTAL_GND	GND	XTAL oscillator ground
T12	XTAL_GND	GND	
R14	XTAL_GND	GND	
P12	XTAL_GND	GND	
P13	XTAL_GND	GND	
T14	XTAL_GND	GND	
N12	XTAL_GND	GND	

Notes

21. Use SPDT or SP3T to combine Bluetooth® RF ports to fully support BDR/EDR/LE features.

22. No routing of the signal under this ball.

23. Need to have a 50 Ω termination to ground.

12.6 CYW55571 WLBGA package ball map

Figure 28 shows the CYW55571 WLBGA package ball map.

	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
15	NC1	WRF_RX5G_GND_C1	WRF_DFSVCO_GND		WRF_DFSPLL_GND		VDDP_RFSW	VDDC	VDDIO_RFSW	SMIF_SPHB_CK	SMIF_SPHB_DQ1	SMIF_SPHB_DQ0	VDDC	CSR_VDD0P9	PVSSC	CSR_VLX	15
14	NC4	WRF_TX5G_GND_C1	NC	WRF_VDD_1P8_C1	WRF_AFE_LPF_TIA_GND_C1	VSSC	RFSW_CTRL19	VSSC	RFSW_CTRL11	SMIF_SPHB_DQ3	SMIF_SPHB_DQ2	VSSC	JTAG_SEL	VDDOUT_SWCOR_E	CSR_VDDBAT	ASR_VDDBAT	14
13	WRF_PA_GND_C1	WRF_PA_VDD_3P3_C1	WRF_TX_GND_C1	WRF_PMU_GND_C1	WRF_PMU_VDD_1P12_C1	VSSC	RFSW_CTRL18	RFSW_CTRL12	RFSW_CTRL10	SMIF_SPHB_CS1_N	SMIF_SPHB_CS0_N	LHL_GPIO0	LHL_GPIO1	VDD_RET_GL	ASR_VDD1P12	ASR_VLX	13
12	NC2	WRF_TX2G_GND_C1	WRF_LO_GND_C1	WRF_PMU_VDD_3P3_C1	WRF_AFE_VDD_1P12_C1	NC1	VDDC	RFSW_CTRL13	RFSW_CTRL09	VSSC	VDDC	LHL_XTALI	LHL_XTALO	VDDOUT_MISC	BTREG_ON	PVSSA	12
11	NC3	WRF_RX2G_GND_C1	NC	WRF_SYNTH_VDD_1P12	WRF_VCO_GND		VSSC	RFSW_CTRL14	RFSW_CTRL08	RFSW_CTRL06	RFSW_CTRL00	VDDIO	LPO_IN	PMU_AVSS	VDDOUT_BT3P3	BT_LDO_VDDBAT	11
10	WRF_RFIN_5G_C0	WRF_RX5G_GND_C0	WRF_LOGEN_GND				RFSW_CTRL17	RFSW_CTRL15	VDDC	RFSW_CTRL07	RFSW_CTRL02	RFSW_CTRL05	VDDC_TOP	VSSC	WLREG_ON	VDDOUT_PA3P3	10
9	WRF_PAOUT_5G_C0	WRF_TX5G_GND_C0	WRF_GPAIO_TSS_I2G_OUT_C0	WRF_SYNTH_VDD_3P3	WRF_SYNTH_GND		RFSW_CTRL16	VDD_RET_GL_IN	GPIO_12	VSSC	GPIO_3	RFSW_CTRL01	RFSW_CTRL03	PMU_VDD1P8P	MIC_P	WLDO_VDDBAT	9
8	WRF_PA_GND_C0	WRF_PA_VDD_3P3_C0	WRF_TX_GND_C0	WRF_PMU_VDD_3P3_C0	WRF_AFE_VDD_1P12_C0	NC2	VDDC	VSSC	GPIO_5	AVDD_BBPLL_1P0	RFSW_CTRL04	VDDC_TOP	GPIO_2	PMU_VDD1P8A	MIC_N	VDDOUT_RF3P3	8
7	WRF_PAOUT_2G_C0	WRF_TX2G_GND_C0	WRF_LO_GND_C0	WRF_PMU_GND_C0	WRF_PMU_VDD_1P12_C0		BT_GPIO_5	GPIO_10	BT_GPIO_14	GPIO_9	VDDC	VDDC	VDDIO	SDIO_DATA_3	VSSC	SDIO_CLK	7
6	WRF_RFIN_2G_C0	WRF_RX2G_GND_C0	WRF_TSSI5G_OUT_C0	WRF_VDD_1P8_C0	WRF_AFE_LPF_TIA_GND_C0	VSSC	BT_GPIO_4	GPIO_1	BT_GPIO_12	GPIO_8	BT_GPIO_11	GPIO_4	SDIO_CMD	SDIO_DATA_2	AVSS_PLL	PCIE_RDP	6
5	BT_RF_OP	BT_RF_VSS	BT_RF_IF_VSS			VSSC	GPIO_0	GPIO_11	BT_GPIO_15	GPIO_6	BT_GPIO_3	GPIO_7	VDDC	SDIO_DATA_1	AVSS_RXTX	PCIE_RDN	5
4	BT_RF_VSS	BT_RF_TEST	BT_RF_PLL_VSS	BT_RF_RX_DVSS	VSSC	VSSC	BT_VDDC	BT_UART_RXD	BT_VDD0	VSSC	BT_GPIO_2	DMIC_DQ	VSSC	SDIO_DATA_0	AVDD_RXTX_1P0	PCIE_TDP	4
3	BT_RF_13DBM_OP	BT_RF_VCO_VSS		BT_RF_LDO_VDD_1P12			BT_HOST_WAKE	BT_UART_RTS_N	BT_VDDC	BT_GPIO_16	BT_GPIO_17	DMIC_CK	I2S_IRCK	PCIE_CLKREQ_L	AVDD_PLL_1P0	PCIE_TDN	3
2		BT_RF_PA_VSS	BT_RF_TX_VSS	BT_RF_TX_DVSS	XTAL_GND	VDD_XTAL	BT_DEV_WAKE	BT_UART_CTS_N	BT_UART_TXD	BT_GPIO_19	BT_GPIO_18	I2S_MCK	I2S_SCK	VSSC	PCIE_PERST_L	PCIE_REFCLKP	2
1	BT_RF_20DBM_OP	BT_RF_PA_VSS	BT_RF_PA_VDD_3P3	BT_RF_TXIF_VSS	XTAL_XON	XTAL_XOP		VSSC	AVDD_BTPLL_1P0	BT_GPIO_13	BT_VDD0	I2S_DI	I2S_DO	VDDC	PCIE_PME_L	PCIE_REFCLKN	1
	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

Figure 28 5.32 × 5.67 mm WLBGA package ball map

Pinout and signal descriptions
12.7 CYW55571 WLBGA package signal descriptions

The signal name, type, and description of each pin in the CYW55571 is listed in [Table 20](#). The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, O = output, PWR = power, GND = ground, OD = open-drain) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

Table 20 CYW55571 WLBGA signal descriptions

Ball #	Ball name	Type	Description
T8	WRF_PA_GND_C0	GND	WLAN radio ground
R13	WRF_PA_VDD_3P3_C1	PWR	WLAN radio 3.3 V Core1 PA supply
R8	WRF_PA_VDD_3P3_C0	PWR	WLAN radio 3.3 V Core0 PA supply
R15	WRF_RX5G_GND_C1	GND	WLAN radio ground
R14	WRF_TX5G_GND_C1	GND	WLAN radio ground
R12	WRF_TX2G_GND_C1	GND	WLAN radio ground
R11	WRF_RX2G_GND_C1	GND	WLAN radio ground
N6	WRF_VDD_1P8_C0	PWR	WLAN radio 1.8 V Core0 supply
T9	WRF_PAOUT_5G_C0	O	WLAN radio Core0 5 GHz PA output
P9	WRF_GPAIO_TSSI2G_OUT_C0	O	WLAN radio 2.4 GHz TSSI Core0
P11	NC ^[24]	O	WLAN radio 2.4 GHz TSSI Core1
M12	WRF_AFE_VDD_1P12_C1	PWR	WLAN radio 1.12 V Core1 supply
P6	WRF_TSSI5G_OUT_C0	O	WLAN radio 5 GHz TSSI Core0
N13	WRF_PMU_GND_C1	GND	WLAN radio ground
M13	WRF_PMU_VDD_1P12_C1	PWR	WLAN radio 1.12 V Core1 supply
R10	WRF_RX5G_GND_C0	GND	WLAN radio ground
R9	WRF_TX5G_GND_C0	GND	WLAN radio ground
N11	WRF_SYNTH_VDD_1P12	PWR	WLAN radio 1.12 V supply
T15	NC1 ^[25]	I	WLAN radio 5 GHz Core1 receiver input
N14	WRF_VDD_1P8_C1	PWR	WLAN radio 1.8 V Core1 supply
P13	WRF_TX_GND_C1	GND	WLAN radio ground
P12	WRF_LO_GND_C1	GND	WLAN radio ground
P8	WRF_TX_GND_C0	GND	WLAN radio ground
P7	WRF_LO_GND_C0	GND	WLAN radio ground
T12	NC2 ^[25]	O	WLAN radio Core1 2.4 GHz PA output
T7	WRF_PAOUT_2G_C0	O	WLAN radio Core0 2.4 GHz PA output
M7	WRF_PMU_VDD1P12_C0	PWR	WLAN radio 1.12 V Core0 supply
M15	WRF_DFSPLL_GND	GND	WLAN radio ground
M14	WRF_AFE_LPF_TIA_GND_C1	GND	WLAN radio ground
M6	WRF_AFE_LPF_TIA_GND_C0	GND	WLAN radio ground
M11	WRF_VCO_GND	GND	WLAN radio ground
M9	WRF_SYNTH_GND	GND	WLAN radio ground
T6	WRF_RFIN_2G_C0	I	WLAN radio 2.4 GHz Core0 receiver input

Notes

24.No routing of the signal under this ball.

25.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 20 **CYW55571 WLPGA signal descriptions** *(continued)*

Ball #	Ball name	Type	Description
P10	WRF_LOGEN_GND	GND	WLAN radio ground
N9	WRF_SYNTH_VDD_3P3	PWR	WLAN radio 3.3 V supply
T11	NC3 ^[25]	I	WLAN radio 2.4 GHz Core1 receiver input
T10	WRF_RFIN_5G_C0	I	WLAN radio 5 GHz Core0 receiver input
R7	WRF_TX2G_GND_C0	GND	WLAN radio ground
R6	WRF_RX2G_GND_C0	GND	WLAN radio ground
P15	WRF_DFSVCO_GND	GND	WLAN radio ground
N12	WRF_PMU_VDD_3P3_C1	PWR	WLAN radio 3.3 V Core1 supply
T13	WRF_PA_GND_C1	GND	WLAN radio ground
N8	WRF_PMU_VDD_3P3_C0	PWR	WLAN radio 3.3 V Core0 supply
M8	WRF_AFE_VDD_1P12_C0	PWR	WLAN radio 1.12 V Core0 supply
P14	NC ^[24]	O	WLAN radio 5 GHz TSSI Core1
N7	WRF_PMU_GND_C0	GND	WLAN radio ground
T14	NC4 ^[25]	O	WLAN radio Core1 5 GHz PA output
L2	VDD_XTAL	PWR	XTAL oscillator 1.0 V supply
L1	XTAL_XOP	O	XTAL oscillator output
M2	XTAL_GND	GND	XTAL oscillator ground
M1	XTAL_XON	I	XTAL oscillator input
T5	BTRF_OP	I/O	Bluetooth® radio input
T4	BTRF_VSS	GND	Bluetooth® radio ground
T3	BTRF_13DBM_OP	O	Bluetooth® radio (13 DBM) output
T1	BTRF_20DBM_OP	O	Bluetooth® radio (20 DBM) output
R5	BTRF_VSS	GND	Bluetooth® radio ground
R4	BTRF_TEST	I/O	Bluetooth® radio test input/output pin
R3	BTRF_VCO_VSS	GND	Bluetooth® radio ground
R2	BTRF_PA_VSS	GND	Bluetooth® radio ground
R1	BTRF_PA_VSS	GND	Bluetooth® radio ground
P5	BTRF_IF_VSS	GND	Bluetooth® radio ground
P4	BTRF_PLL_VSS	GND	Bluetooth® radio ground
P2	BTRF_TX_VSS	GND	Bluetooth® radio ground
P1	BTRF_PA_VDD_3P3	PWR	Bluetooth® radio 3.3 V PA supply
N4	BTRF_RX_DVSS	GND	Bluetooth® radio ground
N3	BTRF_LDO_VDD_1P12	PWR	Bluetooth® radio 1.12 V input supply
N2	BTRF_TX_DVSS	GND	Bluetooth® radio ground
N1	BTRF_TXIF_VSS	GND	Bluetooth® radio ground
B15	PVSSC	GND	Ground input of CSR power stage
A15	CSR_VLX	O	CSR power stage output to inductor

Notes

24.No routing of the signal under this ball.

25.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 20 **CYW55571 WLBGA signal descriptions** *(continued)*

Ball #	Ball name	Type	Description
C15	CSR_VDD0P9	I	Sense or feedback input of CSR power stage
A14	ASR_VDDBAT	PWR	Battery supply input for ASR power stage
B14	CSR_VDDBAT	PWR	Battery supply input for CSR power stage
C14	VDDOUT_SWCORE	O	Power switch output supply for VDD_TOP power supply input
A13	ASR_VLX	O	ASR power stage output to Inductor
B13	ASR_VDD1P12	I	Sense or feedback input of ASR power stage
C13	VDD_RET_GL	O	Power MUX output supply for VDD_RET_GL_IN Power supply input
A12	PVSSA	GND	Ground input of ASR power stage
B12	BTREG_ON	I	Used by the PMU to power up or power down the internal regulators used by the Bluetooth® section. When deasserted, this pin holds the Bluetooth® section in reset. This pin has an internal 50 kΩ pull-down resistor that is auto enabled/disabled by programming.
A11	BTLDO_VDDBAT	PWR	Battery supply input for Bluetooth® PA LDO
B11	VDDOUT_BT3P3	PWR	3.3 V output to supply Bluetooth® PA
C11	PMU_AVSS	GND	PMU analog ground
A10	VDDOUT_PA3P3	PWR	3.3 V output to supply WLAN PA
B10	WLREG_ON	I	Used by the PMU to power up or power down the internal regulators used by the WLAN section. When deasserted, this pin holds the WLAN section in reset. This pin has an internal 50 kΩ pull-down resistor that is auto enabled/disabled by programming.
C9	PMU_VDD1P8P	PWR	1.8 V PMU supply input
A9	WLLDO_VDDBAT	PWR	Battery supply input for WLAN PA and RF LDO
B9	MIC_P	I	ADC microphone positive input
C8	PMU_VDD1P8A	PWR	1.8 V PMU supply input
A8	VDDOUT_RF3P3	PWR	3.3 V output to supply WLAN radio
B8	MIC_N	I	ADC microphone negative input
C12	VDDOUT_MISC	O	Output of MISCLDO
A5	PCIE_RDN	I	PCIe receiver differential pair negative input
A6	PCIE_RDP	I	PCIe receiver differential pair positive input
A1	PCIE_REFCLKN	I	PCIe differential pair clock source (100 MHz) negative input
A2	PCIE_REFCLKP	I	PCIe differential pair clock source (100 MHz) positive input
A3	PCIE_TDN	O	PCIe transmitter differential pair negative output
A4	PCIE_TDP	O	PCIe transmitter differential pair positive output
B3	AVDD_PLL_1P0	PWR	1.0 V PCIe analog supply

Notes

24.No routing of the signal under this ball.

25.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 20 **CYW55571 WLBGA signal descriptions** *(continued)*

Ball #	Ball name	Type	Description
B4	AVDD_RXTX_1P0	PWR	1.0 V PCIe receiver and transmitter supply input
B5	AVSS_RXTX	GND	PCIe analog ground
B6	AVSS_PLL	GND	PCIe analog ground
K14	RFSW_CTRL19	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
K13	RFSW_CTRL18		
K10	RFSW_CTRL17		
K9	RFSW_CTRL16		
J10	RFSW_CTRL15		
J11	RFSW_CTRL14		
J12	RFSW_CTRL13		
J13	RFSW_CTRL12		
H14	RFSW_CTRL11		
H13	RFSW_CTRL10		
H12	RFSW_CTRL09		
H11	RFSW_CTRL08		
G10	RFSW_CTRL07		
G11	RFSW_CTRL06		
E10	RFSW_CTRL05		
F8	RFSW_CTRL04		
D9	RFSW_CTRL03		
F10	RFSW_CTRL02		
E9	RFSW_CTRL01		
F11	RFSW_CTRL00		
G15	SMIF_SPHB_CK	O	SMIF Clock output
G14	SMIF_SPHB_DQ3	I/O	SMIF data line 3
F14	SMIF_SPHB_DQ2	I/O	SMIF data line 2
F15	SMIF_SPHB_DQ1	I/O	SMIF data line 1
E15	SMIF_SPHB_DQ0	I/O	SMIF data line 0
F13	SMIF_SPHB_CS0_N	O	SMIF Chip Select0 active LOW output
G13	SMIF_SPHB_CS1_N	O	SMIF Chip Select1 active LOW output
J2	BT_UART_CTS_N	I	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
H2	BT_UART_TXD	O	UART serial output: Serial data output for the HCI UART interface.
J3	BT_UART_RTS_N	O	UART request-to-send. Active LOW request-to-send signal for the HCI UART interface. Bluetooth® LED control pin.

Notes

24.No routing of the signal under this ball.

25.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 20 **CYW55571 WLBGA signal descriptions** *(continued)*

Ball #	Ball name	Type	Description
J4	BT_UART_RXD	I	UART serial input. Serial data input for the HCI UART interface.
G2	BT_GPIO_19	I/O	Bluetooth® general purpose I/O
F2	BT_GPIO_18		
F3	BT_GPIO_17		
G3	BT_GPIO_16		
H5	BT_GPIO_15		
H7	BT_GPIO_14		
G1	BT_GPIO_13		
H6	BT_GPIO_12		
F6	BT_GPIO_11		
K7	BT_GPIO_5		
K6	BT_GPIO_4		
F5	BT_GPIO_3		
F4	BT_GPIO_2		
K2	BT_DEV_WAKE	I/O	Bluetooth® DEVICE WAKE
K3	BT_HOST_WAKE	I/O	Bluetooth® HOST WAKE
D3	I2S_IRCK	I/O	I2S Word Clock or left/right clock
D2	I2S_SCK	I/O	I2S bit or serial clock
E2	I2S_MCK	I/O	I2S masterclock
E1	I2S_DI	I/O	I2S serial data input
D1	I2S_DO	I/O	I2S serial data output
E3	DMIC_CK	I/O	Digital Mic clock
E4	DMIC_DQ	I/O	Digital Mic data
C7	SDIO_DATA_3	I/O	SDIO data line 3
C6	SDIO_DATA_2	I/O	SDIO data line 2
C5	SDIO_DATA_1	I/O	SDIO data line 1
C4	SDIO_DATA_0	I/O	SDIO data line 0
D6	SDIO_CMD	I/O	SDIO Command line
A7	SDIO_CLK	I	SDIO Clock input
B1	PCIE_PME_L	OD	PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal is asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the PCI Bus Local Bus specification, revision 2.3.
C3	PCIE_CLKREQ_L	OD	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated 0 = the clock is required

Notes

24.No routing of the signal under this ball.

25.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 20 **CYW55571 WLBGA signal descriptions** *(continued)*

Ball #	Ball name	Type	Description
B2	PCIE_PERST_L	I	PCIe System Reset. This input is the PCIe reset as defined in the PCIe base specification v1.1.
K5	GPIO_0	I/O	WLAN general purpose I/O
J6	GPIO_1		
D8	GPIO_2		
F9	GPIO_3		
E6	GPIO_4		
H8	GPIO_5		
G5	GPIO_6		
E5	GPIO_7		
G6	GPIO_8		
G7	GPIO_9		
J7	GPIO_10		
J5	GPIO_11		
H9	GPIO_12		
D14	JTAG_SEL	I	JTAG Select input: Pull high to select the JTAG interface. If the JTAG interface is not used this pin should be connected to ground.
D11	LPO_IN	I	External Sleep clock input (32.768 kHz)
E12	LHL_XTALI	I	32.768 kHz crystal oscillator input
D12	LHL_XTALO	O	32.768 kHz crystal oscillator output
E13	LHL_GPIO0	I/O	Miscellaneous general purpose I/O
D13	LHL_GPIO1	I/O	

Notes

24.No routing of the signal under this ball.

25.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions
Table 20 **CYW55571 WLBGA signal descriptions** *(continued)*

Ball #	Ball name	Type	Description
C10	VSSC	GND	Digital ground for WLAN and Bluetooth®
K11	VSSC		
C2	VSSC		
J14	VSSC		
J8	VSSC		
E14	VSSC		
B7	VSSC		
J1	VSSC		
G4	VSSC		
G9	VSSC		
L4	VSSC		
D4	VSSC		
G12	VSSC		
L14	VSSC		
L13	VSSC		
L5	VSSC		
M4	VSSC		
L6	VSSC		
K8	VDDC	PWR	0.9 V Digital Core supply for WLAN
D5	VDDC		
J15	VDDC		
D15	VDDC		
F12	VDDC		
F7	VDDC		
H10	VDDC		
C1	VDDC		
K12	VDDC		
E7	VDDC		
D10	VDDC_TOP	PWR	0.9 V Digital Core supply for WLAN and Bluetooth®
E8	VDDC_TOP		
H15	VDDIO_RFSW	PWR	IO supply for RF Switch Control Pads
K15	VDDP_RFSW	O	VDDP Power Switch Output
E11	VDDIO	PWR	1.8 V IO supply for WLAN GPIOs
D7	VDDIO		
F1	BT_VDDO	PWR	1.8 V IO supply for Bluetooth® GPIOs
H4	BT_VDDO		

Notes

24.No routing of the signal under this ball.

25.Need to have a 50 Ω termination to ground.

Pinout and signal descriptions**Table 20** CYW55571 WLBGA signal descriptions (continued)

Ball #	Ball name	Type	Description
H3	BT_VDDC	PWR	0.9 V Digital Core supply for Bluetooth®
K4	BT_VDDC		
J9	VDD_RET_GL_IN	PWR	0.9 V Digital Core supply for WLAN
H1	AVDD_BTPLL_1P0	PWR	1.0 V WLPLL analog supply
G8	AVDD_BBPLL_1P0	PWR	1.0 V BTPLL analog supply

Notes

24.No routing of the signal under this ball.

25.Need to have a 50 Ω termination to ground.

12.8 WLAN/Bluetooth® GPIO signals and strapping options

The pins listed in [Table 21](#) are sampled at power-on reset (POR) to determine the various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less.

Note See the reference board schematics for more information.

12.8.1 Strapping options**Table 21** GPIO strap pins

Ball/bump name	Default pull during Strapping	All packages
GPIO_1	1	1 = PCIe 0 = SDIO
GPIO_12	1	1 = Bluetooth® over UART 0 = RESERVED

12.9 GPIO alternative signal functions

Table 22 GPIO alternative signal functions

Pin name	HW decid- ed/Power ON default	Same as pin function name	GPIO-0	FAST_UA RT/ GPIO_1	GCI-0	GCI-1	DBG_UART	SPI/I2C	BT-0	MISC-0	MISC-1
Function Sel											
	0	1	2	3	4	5	6	7	8	9	10
GPIO_0	TRISTATE_IND	WL_HOST_WAKE/ GPIO_0	GPIO_8	-	GCI_G- PIO_0	GCI_G- PIO_11	-	-	BT_DEV_WA KE	-	SDIO_SEP_INT
GPIO_1	TRISTATE_IND	WL_DEV_WA KE/ GPIO_1	GPIO_9	-	GCI_G- PIO_1	GCI_G- PIO_12	-	-	BT_HOST_WA KE	RF_DIS- ABLE_L	-
GPIO_2	JTAG_SEL ? Tessent TAPTCK : ARM DAP TCKI ^[26]	GPIO_2	GPIO_1 0	FAST_UAR T_RX	GCI_G- PIO_2	GCI_G- PIO_13	UART_D- BG_RX	-	BT_GPIO_2	DAP_SEL ? ARM DAP TCK : Tessent TAP TCKI ^[26]	MUXED_RF_S W_CTRL0
GPIO_3	JTAG_SEL ? Tessent TAP TMS : ARM DAP TMSI ^[26]	GPIO_3	GPIO_1 1	FAST_UAR T_TX	GCI_G- PIO_3	GCI_G- PIO_14	UART_D- BG_TX	-	BT_GPIO_3	DAP_SEL ? ARM DAP TMS : Tessent TAP TMSI ^[26]	MUXED_RF_S W_CTRL1
GPIO_4	JTAG_SEL ? Tessent TAP TDI : ARM DAP TDI ^[26]	GPIO_4	GPIO_1 2	FAST_UAR T_ CTS_IN	GCI_G- PIO_4	GCI_G- PIO_15	-	-	BT_GPIO_4	DAP_SEL ? ARM DAP TDI : Tessent TAP TDI ^[26]	MUXED_RF_S W_CTRL2

Note

26.A ternary operator (condition ? value if condition is true: value if condition is false) is used to represent a conditional assignment.

Table 22 GPIO alternative signal functions (continued)

Pin name	HW decided/Power ON default	Same as pin function name	GPIO-0	FAST_UART/ GPIO_1	GCI-0	GCI-1	DBG_UART	SPI/I2C	BT-0	MISC-0	MISC-1
Function Sel											
	0	1	2	3	4	5	6	7	8	9	10
GPIO_5	JTAG_SEL ? Tessent TAP TDO : ARM DAP TDO ^[26]	GPIO_5	GPIO_1 3	FAST_UART T_RT _S _OUT	GCI_G- PIO_0	GCI_G- PIO_5	-	-	BT_GPIO_5	DAP_SEL ? ARM DAP TDO : Tessent TAP TDO ^[26]	MUXED_RF_S W_CTRL3
GPIO_6	JTAG_SEL ? Tessent TAP TRST_L : ARM DAP TRST_LI ^[26]	GPIO_6	GPIO_1 4	-	GCI_G- PIO_1	GCI_G- PIO_6	-	-	BT_GPIO_1 1	DAP_SEL ? ARM DAP TRST_L : Tessent TAP TRST_LI ^[26]	MUXED_RF_S W_CTRL4
GPIO_7	TRISTATE_IND	GPIO_7	GPIO_1 5	-	GCI_G- PIO_2	GCI_G- PIO_7	-	-	BT_GPIO_7	-	SWD/JTAG SELECT.
GPIO_8	TRISTATE_IND	GPIO_8	GPIO_0	FAST_UART T_C _T S_IN	GCI_G- PIO_3	GCI_G- PIO_8	-	GSIO_S DI	BT_GPIO_8	-	-
GPIO_9	TRISTATE_IND	GPIO_9	GPIO_1	FAST_UART T_RT _S _OUT	GCI_G- PIO_4	GCI_G- PIO_9	-	GSIO_S DO	BT_GPIO_9	-	-
GPIO_10	TRISTATE_IND	GPIO_10	GPIO_2	FAST_UART T_RX	GCI_G- PIO_0	GCI_G- PIO_10	UART_D- BG_RX	GSIO_C SN	BT_GPIO_1 0	-	-
GPIO_11	TRISTATE_IND	GPIO_11	GPIO_3	FAST_UART T_TX	GCI_G- PIO_1	GCI_G- PIO_11	UART_D- BG_TX	GSIO_C LK	BT_GPIO_6	-	-
GPIO_12	TRISTATE_IND	WL_LED1/G PIO_12	GPIO_4	-	GCI_G- PIO_2	GCI_G- PIO_12	-	-	BT_GPIO_1 2	-	-
GPIO_13	TRISTATE_IND	WL_LED0/G PIO_13	GPIO_5	-	GCI_G- PIO_3	GCI_G- PIO_13	-	-	BT_GPIO_1 3	-	-

Note

26.A ternary operator (condition ? value if condition is true: value if condition is false) is used to represent a conditional assignment.

Table 22 GPIO alternative signal functions (continued)

Pin name	HW decid- ed/Power ON default	Same as pin function name	GPIO-0	FAST_UA RT/ GPIO_1	GCI-0	GCI-1	DBG_UART	SPI/I2C	BT-0	MISC-0	MISC-1
Function Sel											
	0	1	2	3	4	5	6	7	8	9	10
GPIO_1 4	TRISTATE_IND	GPIO_14	GPIO_6	–	GCI_G- PIO_4	GCI_G- PIO_14	–	–	BT_GPIO_1 4	–	–
SDIO_C LK	SDIO_EN ? SDIO_ CLK ;TRISTATE_IND ^[26]	SDIO_CLK	GPIO_2	–	–	–	–	–	BT_GPIO_1 5	SDIO_AOS _CLK	–
SDIO_C MD	SDIO_EN ? SDIO_CMD: TRISTATE_IND ^[26]	SDIO_CMD	GPIO_3	GPIO_11	GCI_G- PIO_0	GCI_G- PIO_15	–	–	BT_GPIO_1 6	SDIO_AOS _CMD	–
SDIO_ DATA_0	SDIO_EN ? SDIO_DATA_0: TRISTATE_IND ^[26]	SDIO_ DATA_0	GPIO_4	GPIO_12	GCI_G- PIO_1	–	–	–	BT_GPIO_1 7	SDIO_AOS _D0	–
SDIO_ DATA_1	SDIO_EN ? SDIO_DATA_1: TRISTATE_IND ^[26]	SDIO_ DATA_1	GPIO_5	GPIO_13	GCI_G- PIO_2	–	–	–	BT_GPIO_1 8	SDIO_AOS _D1	–
SDIO_ DATA_2	SDIO_EN ? SDIO_DATA_2: TRISTATE_IND ^[26]	SDIO_ DATA_2	GPIO_6	GPIO_14	GCI_G- PIO_3	–	–	–	BT_GPIO_1 9	SDIO_AOS _D2	–
SDIO_ DATA_3	SDIO_EN ? SDIO_DATA_3: TRISTATE_IND ^[26]	SDIO_ DATA_3	GPIO_7	GPIO_15	GCI_G- PIO_4	–	–	–	BT_GPIO_2 0	SDIO_AOS _D3	–

Note

26.A ternary operator (condition ? value if condition is true: value if condition is false) is used to represent a conditional assignment.

12.10 I/O states

The following notations are used in [Table 23](#):

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- PU = Pulled up
- PD = Pulled down
- No pull = Neither pulled up nor pulled down
- Where applicable, the default value is shown in bold brackets (for example, **[default value]**)

Table 23 I/O states

Name	I/O	Keeper	Active mode	Low-power State/Sleep (All power present)	Power-down (BT_REG_ON and WL_REG_ON Held LOW)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON HIGH)	(WL_REG_ON HIGH and BT_REG_ON = 0) and VDDIOs are present	Power rail
WL_REG_ON BT_REG_ON	I	N	I: PD Pull-down auto disabled	I: PD Pull-down auto disabled	I: PD (of 50K)	I: PD (of 50K)	I: PD (of 50K)	–
GPIO_0	I/O	Y	I/O: PU, PD, No pull Programmable [PD]	I/O: PU, PD, No pull Programmable [PD]	High-Z, No pull	High-Z, No pull	High Z, No pull	VDDIO
GPIO_1	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High Z, No pull	High-Z, No pull	High Z, No pull	VDDIO
GPIO_2	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I:PU	I:PU	VDDIO
GPIO_3	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I:PU	I:PU	VDDIO

Note

27. When JTAG is not enabled on the GPIO.

Table 23 I/O states (continued)

Name	I/O	Keeper	Active mode	Low-power State/Sleep (All power present)	Power-down (BT_REG_ON and WL_REG_ON Held LOW)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON HIGH)	(WL_REG_ON HIGH and BT_REG_ON = 0) and VDDIOs are present	Power rail
GPIO_4	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I:PU	I:PU	VDDIO
GPIO_5	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: No pull ^[27]	I: No pull	VDDIO
GPIO_6	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PU	I:PU	VDDIO
GPIO_7	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: No pull	I: No pull	VDDIO
GPIO_8	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: No pull	I: No pull	VDDIO
GPIO_9	I/O	Y	I/O: PU, PD, No pull Programmable [PU]	I/O: PU, PD, No pull Programmable [PU]	High-Z, No pull	I: No pull	I: No pull	VDDIO
GPIO_10	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: No pull	I: No pull	VDDIO
GPIO_11	I/O	Y	I/O: PU, PD, No pull Programmable [PU]	I/O: PU, PD, No pull Programmable [PU]	High Z, No pull	I: No pull	I: No pull	VDDIO
GPIO_12	I/O	N	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	High Z, No pull	High Z, No pull	VDDIO
GPIO_13	I/O	N	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: No pull	I: No pull	VDDIO

Note

27. When JTAG is not enabled on the GPIO.

Table 23 I/O states (continued)

Name	I/O	Keeper	Active mode	Low-power State/Sleep (All power present)	Power-down (BT_REG_ON and WL_REG_ON Held LOW)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON HIGH)	(WL_REG_ON HIGH and BT_REG_ON = 0) and VDDIOs are present	Power rail
GPIO_14	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: No pull	I: No pull	VDDIO
RF_SW_CTRL_X	O	N	O: No pull	O: No pull	High-Z, No pull	O: No pull	O: No pull	VDDIO_RF
I2S_IRCK	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VD-DO_SMIF
I2S_SCK	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VD-DO_SMIF
I2S_MCK	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VD-DO_SMIF
I2S_DI	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VD-DO_SMIF
I2S_DO	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VD-DO_SMIF
BT_GPIO_2	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VDDO
BT_GPIO_3	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PU	I: PU	BT_VDDO
BT_GPIO_4	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PU	I: PU	BT_VDDO

Note

27.When JTAG is not enabled on the GPIO.

Table 23 I/O states (continued)

Name	I/O	Keeper	Active mode	Low-power State/Sleep (All power present)	Power-down (BT_REG_ON and WL_REG_ON Held LOW)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON HIGH)	(WL_REG_ON HIGH and BT_REG_ON = 0) and VDDIOs are present	Power rail
BT_GPIO_5	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PU	I: PU	BT_VDDO
BT_GPIO_6	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VDDO
BT_GPIO_7	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VDDO
BT_GPIO_8	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VDDO
BT_GPIO_9	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VDDO
BT_GPIO_10	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VDDO
BT_GPIO_11	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VDDO
BT_GPIO_12	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VDDO
BT_GPIO_13	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VDDO
BT_GPIO_14	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VDDO

Note

27. When JTAG is not enabled on the GPIO.

Table 23 I/O states (continued)

Name	I/O	Keeper	Active mode	Low-power State/Sleep (All power present)	Power-down (BT_REG_ON and WL_REG_ON Held LOW)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON HIGH)	(WL_REG_ON HIGH and BT_REG_ON = 0) and VDDIOs are present	Power rail
BT_GPIO_15	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VDDO
BT_GPIO_16	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VDDO
BT_GPIO_17	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VDDO
BT_GPIO_18	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VDDO
BT_GPIO_19	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VDDO
BT_GPIO_20	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	I: PD	O: No pull	O: No pull	BT_VDDO
BT_DEV_WAKE	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VDDO
BT_HOST_WAKE	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: PD	I: PD	BT_VDDO
LHL_GPIO0	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: No pull	I: No pull	LHL_VDDIO
LHL_GPIO1	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: No pull	I: No pull	LHL_VDDIO

Note

27. When JTAG is not enabled on the GPIO.

Table 23 I/O states (continued)

Name	I/O	Keeper	Active mode	Low-power State/Sleep (All power present)	Power-down (BT_REG_ON and WL_REG_ON Held LOW)	Out-of-Reset; Before SW Download (BT_REG_ON High; WL_REG_ON HIGH)	(WL_REG_ON HIGH and BT_REG_ON = 0) and VDDIOs are present	Power rail
LHL_GPIO2	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: No pull	I: No pull	LHL_VDDIO
LHL_GPIO3	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: No pull	I: No pull	LHL_VDDIO
LHL_GPIO4	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: No pull	I: No pull	LHL_VDDIO
LHL_GPIO5	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: No pull	I: No pull	LHL_VDDIO
LHL_GPIO6	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: No pull	I: No pull	LHL_VDDIO
LHL_GPIO7	I/O	Y	I/O: PU, PD, No pull Programmable [No pull]	I/O: PU, PD, No pull Programmable [No pull]	High-Z, No pull	I: No pull	I: No pull	LHL_VDDIO

Note

27.When JTAG is not enabled on the GPIO.

DC characteristics

13 DC characteristics

13.1 Absolute maximum ratings

Table 24 Absolute maximum ratings

Rating	Symbol	Value	Unit
DC supply for VBAT and PA driver supply	CSR_VDDBAT, ASR_VDDBAT, BTLDO_VDDBAT, WLLDO_VDDBAT	−0.5 to +6.0	V
DC supply voltage for digital I/O	VDDIO, VDDIO_SD, BT_VDDO, BT_VDDO_SMIF, LHL_VDDO, PMU_VDD1P8	−0.5 to 2.2	V
DC supply voltage for RF switch I/Os	VDDIO_RFSW	−0.5 to 3.9	V
DC supply voltage for core	VDD_AON, VDD_MAIN, VDD_DIG, VDD_RET_GL_IN, VDD_TOP, BT_VDDC	−0.5 to 1.1	V
Maximum undershoot voltage for I/O ^[28]	V _{undershoot}	−0.5	V
Maximum overshoot voltage for I/O ^[28]	V _{overshoot}	VDDIO + 0.5	V
Maximum junction temperature	T _j	125	°C
Maximum input power for RX input ports ^[29]	–	13	dBm

Notes

28.Duration not to exceed 25% of the duty cycle.

29.Devices incur a maximum of 3 dB reduction in LNA gain with a maximum input level of 13 dBm at a 1.5% duty-cycle derated from a 7-year lifetime.

13.2 Environmental ratings

 The environmental ratings are shown in [Table 25](#).

Table 25 Environmental ratings

Characteristic	Value	Unit	Conditions/comments
Ambient temperature (T _A)	−40 to +85	°C	Functional operation ^[30]
Storage temperature	−40 to +125	°C	–
Relative humidity	Less than 60	%	Storage
	Less than 85	%	Operation

Note

30.The device is functional across this range of temperature.The device autonomously monitors its junction temperature and employs transmit throughput throttling to regulate power dissipation and ensure that the junction temperature is held below maximum ratings for device reliability.

DC characteristics
13.3 Recommended operating conditions and DC characteristics

Functional operation is not guaranteed outside of the limits shown in [Table 26](#), and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 26 Recommended operating conditions and DC characteristics

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
DC supply voltage for VBAT	CSR_VDDBAT, ASR_VDDBAT, BTLDO_VDDBAT, WLLDO_VDDBAT	3.0 ^[31]	3.3	4.8 ^[32]	V
DC supply voltage for core	VDD_AON, VDD_MAIN, VDD_DIG, VDD_RET_GL_IN, VDD_TOP, BT_VDDC	0.86	–	0.94	V
DC supply voltage for digital I/O	VDDIO, VDDIO_SD, BT_VDDO, BT_VDDO_SMIF, LHL_VDDO, PMU_VDD1P8	1.71	1.8	1.89	V
DC supply voltage for RF switch I/Os when supporting 3.3 V RF_SW_CTRL pads	VDDIO_RFSW	3.13	3.3	3.47	V
External TSSI input	TSSI	0.15	–	0.95	V
Internal POR threshold	Vth_POR	0.4	–	0.7	V

Digital I/O pins^[33]
PCIe out-of-band signals (PCIE_PERST_L, PCIE_PME_L, and PCIE_CLKREQ_L)^[34]

For VDDIO, VDDIO_SD, BT_VDDO, BT_VDDO_SMIF = 1.8 V:

Input HIGH voltage	VIH	$0.65 \times \text{VDDIO}$	–	–	V
Input LOW voltage	VIL	–	–	$0.35 \times \text{VDDIO}$	V
Output HIGH voltage @ 2 mA	VOH	$\text{VDDIO} - 0.40$	–	–	V
Output LOW voltage @ 2 mA	VOL	–	–	0.45	V

RF switch control output pins^[33]

For VDDIO_RFSW = 3.3 V:

Output HIGH voltage @ 2 mA	VOH	$\text{VDDIO_RFSW} - 0.4$	–	–	V
Output LOW voltage @ 2 mA	VOL	–	–	0.40	V
Input capacitance	C _{IN}	–	–	5	pF

WL_REG_ON & BT_REG_ON Pins

Input HIGH voltage	–	1.2	–	VBAT	V
Input LOW voltage	–	–	–	0.3	V

Notes

31. CYW55571 is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for $3.13 \text{ V} < \text{VBAT} < 3.5 \text{ V}$.

32. The maximum continuous voltage is 5.25 V. Voltage transients up to 6.0 V for up to 10 seconds, cumulative duration over the lifetime of the device, are allowed. Voltage transients as high as 5.5 V for up to 250 seconds, cumulative duration over the lifetime of the device, are allowed.

33. Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

34. V_{OH} specification is not applicable for PCIE_PME_L and PCIE_CLKREQ_L signals as they are open-drain outputs.

13.4 Electrostatic discharge specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 27 ESD specifications

Pin type	Symbol	Condition	ESD rating	Unit
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	+/-2	kV
CDM	ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	+/-250	V
Latch-up	–	At 125°C	+/-200	mA

14 Bluetooth® RF specifications

Unless otherwise stated, limit values apply for the conditions specified in [Table 28](#) and [Table 29](#). Typical values apply for an ambient temperature of +25°C.

Unless otherwise stated, the values in this section are design targets, to be confirmed by silicon characterization.

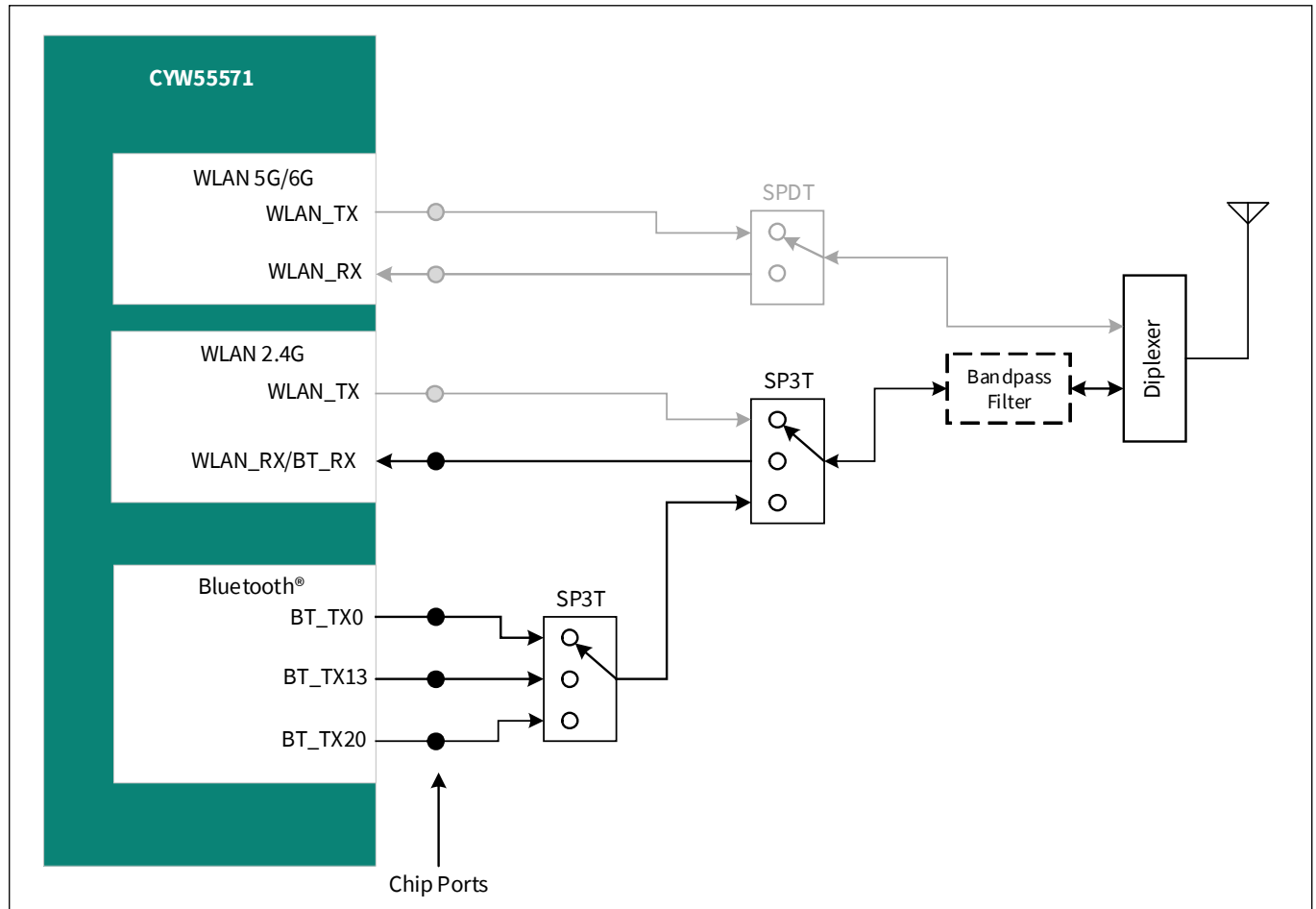


Figure 29 Port locations for Bluetooth® RF Testing – Shared WLAN/Bluetooth® antenna with shared Bluetooth® LNA

Bluetooth® RF specifications

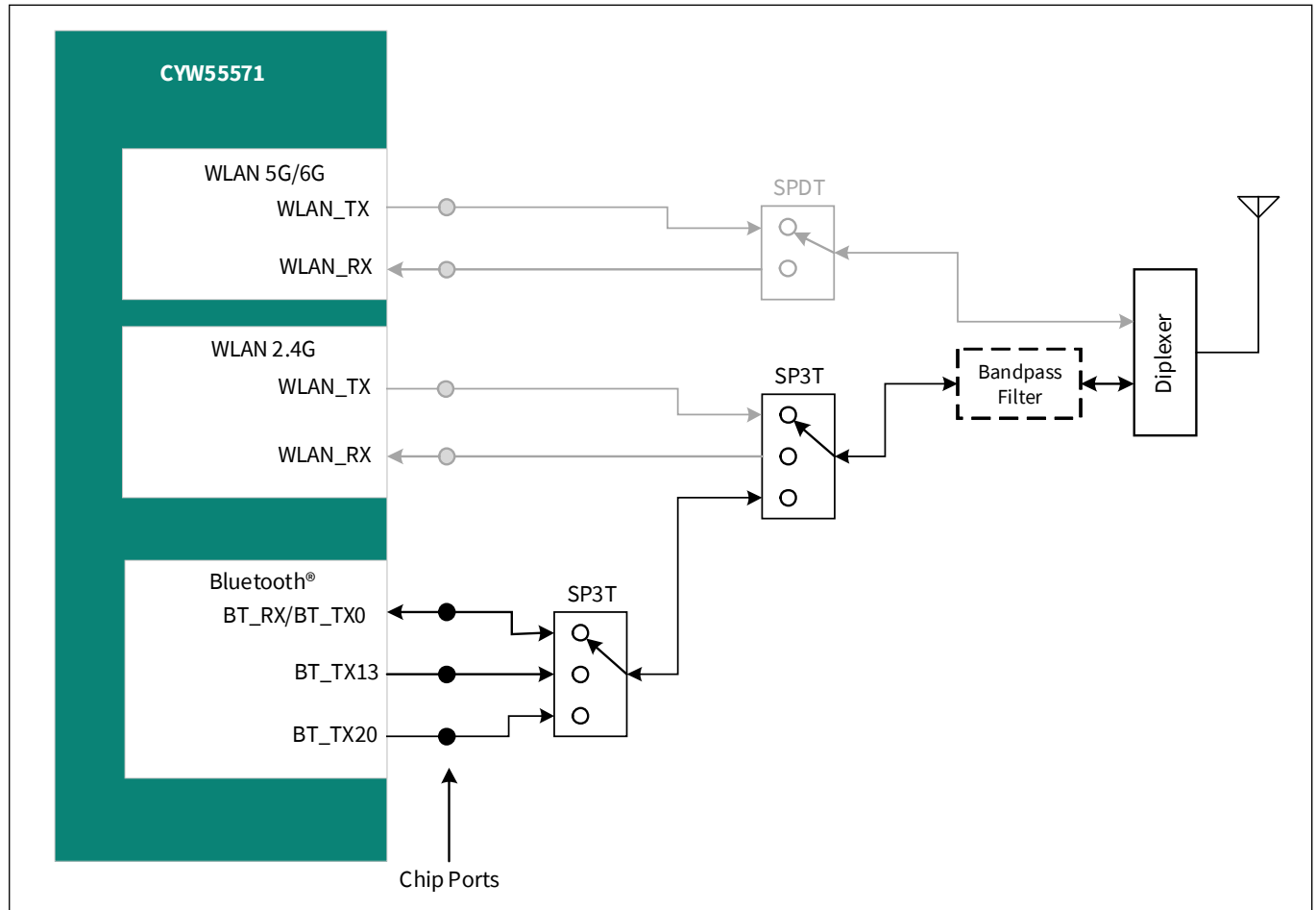


Figure 30 Port locations for Bluetooth® RF testing – shared WLAN/Bluetooth® antenna with dedicated Bluetooth® LNA

Bluetooth® RF specifications

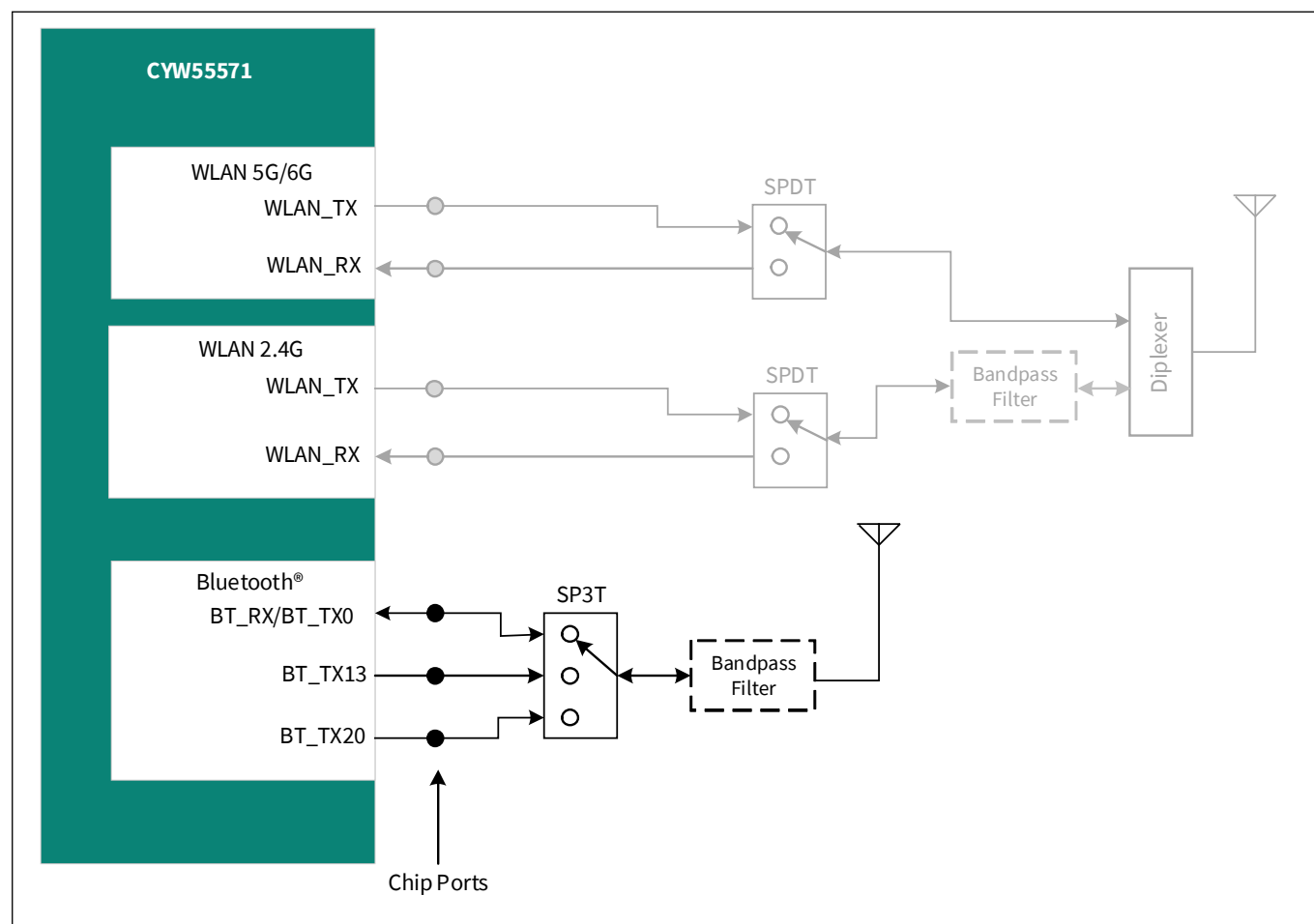


Figure 31 Port locations for Bluetooth® RF testing – dedicated Bluetooth® antenna

Note All Bluetooth® specifications are measured at the chip port unless otherwise specified.

Bluetooth® RF specifications
Table 28 Bluetooth® receiver RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
Note The specifications in this table are measured at the chip port output unless otherwise specified.					
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity (dLNA)	GFSK, 0.1% BER, 1 Mbps	–	–94.0	–	dBm
	$\pi/4$ -DQPSK, 0.01% BER, 2 Mbps	–	–96.5	–	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–90.0	–	dBm
RX sensitivity (sLNA)	GFSK, 0.1% BER, 1 Mbps	–	–94.5	–	dBm
	$\pi/4$ -DQPSK, 0.01% BER, 2 Mbps	–	–97.0	–	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–90.5	–	dBm
Maximum input	–	–	–	–20	dBm
RX LO leakage					
2.4 GHz band	–	–	–90.0	–80.0	dBm
Interference performance ^[35]					
C/I co-channel	GFSK, 0.1% BER	–	8.5	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–1.4	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–41.0	–30	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER	–	–42.5	–40	dB
C/I image channel	GFSK, 0.1% BER	–	–31.5	–9.0	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	–	–44.5	–20	dB
C/I co-channel	$\pi/4$ -DQPSK, 0.1% BER	–	10.5	13.0	dB
C/I 1 MHz adjacent channel	$\pi/4$ -DQPSK, 0.1% BER	–	–6.5	0	dB
C/I 2 MHz adjacent channel	$\pi/4$ -DQPSK, 0.1% BER	–	–38.5	–30.0	dB
C/I ≥ 3 MHz adjacent channel	$\pi/4$ -DQPSK, 0.1% BER	–	–42.5	–40.0	dB
C/I image channel	$\pi/4$ -DQPSK, 0.1% BER	–	–30.0	–7.0	dB
C/I 1 MHz adjacent to image channel	$\pi/4$ -DQPSK, 0.1% BER	–	–47.5	–20.0	dB
C/I co-channel	8-DPSK, 0.1% BER	–	18.0	21.0	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	–	–1.0	5.0	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	–	–36.5	–25.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–41.5	–33.0	dB
C/I Image channel	8-DPSK, 0.1% BER	–	–22.5	0	dB

Notes

35. The maximum value represents the actual Bluetooth® specification required for Bluetooth® qualification as defined in the version 4.0 specification.

36. Bluetooth® reference level for the wanted signal at the Bluetooth® Chip port = –84.5 dBm.

37. Interferer: 2560 MHz, BW = 10 MHz; measured at 2480 MHz.

38. Interferer: 2360 MHz, BW = 10 MHz; measured at 2402 MHz.

39. Interferer: 2380 MHz, BW = 10 MHz; measured at 2480 MHz.

40. Interferer: 2355 MHz, BW = 10 MHz; measured at 2480 MHz.

41. Bluetooth® reference level for the wanted signal at the Bluetooth® chip port = –79.5 dBm.

Bluetooth® RF specifications
Table 28 Bluetooth® receiver RF specifications (continued)

Parameter	Conditions	Min	Typ	Max	Unit
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	–	–41.5	–13.0	dB
Out-of-band blocking performance (CW)					
30 MHz–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000 MHz–2399 MHz	0.1% BER	–	–27.0	–	dBm
2498 MHz–3000 MHz	0.1% BER	–	–27.0	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm
Out-of-band blocking performance, modulated interferer					
GFSK (1 Mbps)^[36]					
698 MHz–716 MHz	WCDMA	–	–13.0	–	dBm
776 MHz–849 MHz	WCDMA	–	–14.0	–	dBm
824 MHz–849 MHz	GSM850	–	–13.0	–	dBm
824 MHz–849 MHz	WCDMA	–	–14.0	–	dBm
880 MHz–915 MHz	E-GSM	–	–13.0	–	dBm
880 MHz–915 MHz	WCDMA	–	–13.0	–	dBm
1710 MHz–1785 MHz	GSM1800	–	–18.0	–	dBm
1710 MHz–1785 MHz	WCDMA	–	–17.0	–	dBm
1850 MHz–1910 MHz	GSM1900	–	–19.0	–	dBm
1850 MHz–1910 MHz	WCDMA	–	–19.0	–	dBm
1880 MHz–1920 MHz	TD-SCDMA	–	–20.0	–	dBm
1920 MHz–1980 MHz	WCDMA	–	–20.0	–	dBm
2010 MHz–2025 MHz	TD-SCDMA	–	–20.0	–	dBm
2500 MHz–2570 MHz	WCDMA	–	–26.0	–	dBm
2510 MHz ^[37]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2530 MHz ^[37]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2550 MHz ^[37]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2570 MHz ^[37]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2310 MHz ^[38]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2330 MHz ^[38]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2350 MHz ^[38]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2370 MHz ^[38]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2570 MHz–2620 MHz ^[39]	Band 38	–	–33.0	–	dBm
2545 MHz–2575 MHz ^[40]	XGP Band	–	–33.0	–	dBm

Notes

35. The maximum value represents the actual Bluetooth® specification required for Bluetooth® qualification as defined in the version 4.0 specification.

36. Bluetooth® reference level for the wanted signal at the Bluetooth® Chip port = –84.5 dBm.

37. Interferer: 2560 MHz, BW = 10 MHz; measured at 2480 MHz.

38. Interferer: 2360 MHz, BW = 10 MHz; measured at 2402 MHz.

39. Interferer: 2380 MHz, BW = 10 MHz; measured at 2480 MHz.

40. Interferer: 2355 MHz, BW = 10 MHz; measured at 2480 MHz.

41. Bluetooth® reference level for the wanted signal at the Bluetooth® chip port = –79.5 dBm.

Bluetooth® RF specifications
Table 28 Bluetooth® receiver RF specifications (continued)

Parameter	Conditions	Min	Typ	Max	Unit
$\pi/4$-DPSK (2 Mbps)^[36]					
698 MHz–716 MHz	WCDMA	–	–10.0	–	dBm
776 MHz–794 MHz	WCDMA	–	–10.0	–	dBm
824 MHz–849 MHz	GSM850	–	–11.0	–	dBm
824 MHz–849 MHz	WCDMA	–	–11.0	–	dBm
880 MHz–915 MHz	E-GSM	–	–10.0	–	dBm
880 MHz–915 MHz	WCDMA	–	–10.0	–	dBm
1710 MHz–1785 MHz	GSM1800	–	–16.0	–	dBm
1710 MHz–1785 MHz	WCDMA	–	–15.0	–	dBm
1850 MHz–1910 MHz	GSM1900	–	–17.0	–	dBm
1850 MHz–1910 MHz	WCDMA	–	–16.0	–	dBm
1880 MHz–1920 MHz	TD-SCDMA	–	–18.0	–	dBm
1920 MHz–1980 MHz	WCDMA	–	–17.0	–	dBm
2010 MHz–2025 MHz	TD-SCDMA	–	–19.0	–	dBm
2500 MHz–2570 MHz	WCDMA	–	–23.0	–	dBm
2510 MHz ^[37]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2530 MHz ^[37]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2550 MHz ^[37]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2570 MHz ^[37]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2310 MHz ^[38]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2330 MHz ^[38]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2350 MHz ^[38]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2370 MHz ^[38]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2570 MHz–2620 MHz ^[39]	Band 38	–	–33.0	–	dBm
2545 MHz–2575 MHz ^[40]	XGP Band	–	–33.0	–	dBm
8-DPSK (3 Mbps)^[41]					
698 MHz–716 MHz	WCDMA	–	–13.0	–	dBm
776 MHz–794 MHz	WCDMA	–	–13.0	–	dBm
824 MHz–849 MHz	GSM850	–	–13.0	–	dBm
824 MHz–849 MHz	WCDMA	–	–14.0	–	dBm
880 MHz–915 MHz	E-GSM	–	–13.0	–	dBm
880 MHz–915 MHz	WCDMA	–	–13.0	–	dBm
1710 MHz–1785 MHz	GSM1800	–	–18.0	–	dBm

Notes

35.The maximum value represents the actual Bluetooth® specification required for Bluetooth® qualification as defined in the version 4.0 specification.

36.Blutetooth® reference level for the wanted signal at the Bluetooth® Chip port = –84.5 dBm.

37.Interferer: 2560 MHz, BW = 10 MHz; measured at 2480 MHz.

38.Interferer: 2360 MHz, BW = 10 MHz; measured at 2402 MHz.

39.Interferer: 2380 MHz, BW = 10 MHz; measured at 2480 MHz.

40.Interferer: 2355 MHz, BW = 10 MHz; measured at 2480 MHz.

41.Blutetooth® reference level for the wanted signal at the Bluetooth® chip port = –79.5 dBm.

Bluetooth® RF specifications
Table 28 Bluetooth® receiver RF specifications (continued)

Parameter	Conditions	Min	Typ	Max	Unit
1710 MHz–1785 MHz	WCDMA	–	–17.0	–	dBm
1850 MHz–1910 MHz	GSM1900	–	–19.0	–	dBm
1850 MHz–1910 MHz	WCDMA	–	–19.0	–	dBm
1880 MHz–1920 MHz	TD-SCDMA	–	–19.0	–	dBm
1920 MHz–1980 MHz	WCDMA	–	–19.0	–	dBm
2010 MHz–2025 MHz	TD-SCDMA	–	–20.0	–	dBm
2500 MHz–2570 MHz	WCDMA	–	–23.0	–	dBm
2510 MHz ^[37]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2530 MHz ^[37]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2550 MHz ^[37]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2570 MHz ^[37]	LTE band 7 FDD 20 MHz BW	–	–32.0	–	dBm
2310 MHz ^[38]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2330 MHz ^[38]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2350 MHz ^[38]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2370 MHz ^[38]	LTE band 40 TDD 20 MHz BW	–	–37.0	–	dBm
2570–2620 MHz ^[39]	Band 38	–	–33.0	–	dBm
2545–2575 MHz ^[40]	XGP Band	–	–33.0	–	dBm

Spurious emissions

30 MHz–1 GHz	–	–95.0	–	dBm
1 GHz–12.75 GHz	–	–70.0	–	dBm
851 MHz–894 MHz	–	–147.0	–	dBm/Hz
925 MHz–960 MHz	–	–147.0	–	dBm/Hz
1805 MHz–1880 MHz	–	–147.0	–	dBm/Hz
1930 MHz–1990 MHz	–	–147.0	–	dBm/Hz
2110 MHz–2170 MHz	–	–147.0	–	dBm/Hz

Notes

35. The maximum value represents the actual Bluetooth® specification required for Bluetooth® qualification as defined in the version 4.0 specification.

36. Bluetooth® reference level for the wanted signal at the Bluetooth® Chip port = –84.5 dBm.

37. Interferer: 2560 MHz, BW = 10 MHz; measured at 2480 MHz.

38. Interferer: 2360 MHz, BW = 10 MHz; measured at 2402 MHz.

39. Interferer: 2380 MHz, BW = 10 MHz; measured at 2480 MHz.

40. Interferer: 2355 MHz, BW = 10 MHz; measured at 2480 MHz.

41. Bluetooth® reference level for the wanted signal at the Bluetooth® chip port = –79.5 dBm.

Bluetooth® RF specifications
Table 29 Bluetooth® transmitter RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
Note The specifications in this table are measured at the Chip port output unless otherwise specified.					
General					
Frequency range		2402	–	2480	MHz
Basic rate (GFSK) TX power at Bluetooth®		–	13.0	–	dBm
QPSK TX power at Bluetooth®		–	9.0	–	dBm
8PSK TX power at Bluetooth®		–	9.0	–	dBm
Power control step		–	4	–	dB
Note Output power is with TCA and TSSI enabled.					
GFSK In-band spurious emissions					
–20 dBc BW	–	–	0.93	1	MHz
EDR In-band spurious emissions					
1.0 MHz < M – N < 1.5 MHz	M – N = the frequency range for which the spurious emission is measured relative to the transmit center frequency.	–	–38.0	–26.0	dBc
1.5 MHz < M – N < 2.5 MHz		–	–31.0	–20.0	dBm
M – N ≥ 2.5 MHz ^[42]		–	–43.0	–40.0	dBm
Out-of-band spurious emissions					
TX harmonics (HD2, HD3, HD4) • Chip Pout = 13 dBm in BDR and Bluetooth® LE mode • Chip Pout = 10 dBm in BDR and Bluetooth® LE mode	HD2	–	–21	–	dBm
	HD3	–	–18	–	dBm
	HD4	–	–41	–	dBm
GLONASS-band spurious emissions					
FDMA L1 band 1598.0625 MHz–1606.375 MHz	–	–	–111	–	dBm/Hz
FDMA L2 band 1242.9375 MHz–1248.625 MHz	–	–	–160	–	dBm/Hz
CDMA L1 signal 1202.025 MHz	–	–	–161	–	dBm/Hz
CDMA L2 signal 1248.06 MHz	–	–	–160	–	dBm/Hz
CDMA L3 signal 1202.025 MHz	–	–	–161	–	dBm/Hz
GPS band spurious emissions					
CDMA L1 Signal 1575.42 MHz	–	–	–156	–	dBm/Hz
CDMA L2 Signal 1227.60 MHz	–	–	–161	–	dBm/Hz
Out-of-band noise floor ^[43]					
65 MHz–108 MHz	FM RX	–	–160	–	dBm/Hz

Notes

42. The typical number is measured at ±3 MHz offset.

 43. Transmitted power in cellular and FM bands at the Bluetooth® Antenna port. See [Figure 29](#) for location of the port.

Bluetooth® RF specifications
Table 29 Bluetooth® transmitter RF specifications (continued)

Parameter	Conditions	Min	Typ	Max	Unit
776 MHz–794 MHz	CDMA2000	–	–150	–	dBm/Hz
869 MHz–960 MHz	cdmaOne, GSM850	–	–150	–	dBm/Hz
925 MHz–960 MHz	E-GSM	–	–150	–	dBm/Hz
1570 MHz–1580 MHz	GPS	–	–155	–	dBm/Hz
1805 MHz–1880 MHz	GSM1800	–	–147	–	dBm/Hz
1930 MHz–1990 MHz	GSM1900, cdmaOne, WCDMA	–	–147	–	dBm/Hz
2110 MHz–2170 MHz	WCDMA	–	–138	–	dBm/Hz
2500 MHz–2570 MHz	Band 7	–	–134	–	dBm
2300 MHz–2400 MHz	Band 40	–	–133	–	dBm
2570 MHz–2620 MHz	Band 38	–	–135	–	dBm
2545 MHz–2575 MHz	XGP Band	–	–135	–	dBm

Notes

 42. The typical number is measured at ± 3 MHz offset.

 43. Transmitted power in cellular and FM bands at the Bluetooth® Antenna port. See [Figure 29](#) for location of the port.

Table 30 Local oscillator performance

Parameter	Minimum	Typical	Maximum	Unit
LO performance				
Initial carrier frequency tolerance	–	± 25.0	± 75.0	kHz
Frequency drift				
DH1 packet	–	± 8.0	± 25.0	kHz
DH3 packet	–	± 8.0	± 40.0	kHz
DH5 packet	–	± 8.0	± 40.0	kHz
Drift rate	–	5.0	20.0	kHz/50 μ s
Frequency deviation				
00001111 sequence in payload ^[44]	140	155	175	kHz
10101010 sequence in payload ^[45]	115	135	–	kHz
Channel spacing	–	1	–	MHz

Notes

44. This pattern represents an average deviation in payload.

45. Pattern represents the maximum deviation in payload for 99.9% of all frequency deviations.

Bluetooth® RF specifications**Table 31 Bluetooth® LE RF specifications**

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	–	2402	–	2480	MHz
RX sensitivity (dLNA) ^[46]	GFSK, 1 Mbps	–	–100.5	–	dBm
	GFSK, 2 Mbps	–	–97.5	–	dBm
	GFSK, 500 Kbps	–	–106.0	–	dBm
	GFSK, 125 Kbps	–	–110.0	–	dBm
RX sensitivity (sLNA) ^[46]	GFSK, 1 Mbps	–	–101.5	–	dBm
	GFSK, 2 Mbps	–	–98.5	–	dBm
	GFSK, 500 Kbps	–	–107.5	–	dBm
	GFSK, 125 Kbps	–	–110.5	–	dBm
TX power	–	–	13	–	dBm
Mod Char: delta F1 average	GFSK, 1 Mbps	225	255	275.5	kHz
Mod Char: delta F2 max	GFSK, 1 Mbps	185	230	–	kHz
Mod Char: ratio	GFSK, 1 Mbps	0.8	1.0	–	–
TX power	GFSK, 2 Mbps	–	13.0	–	dBm
Mod Char: delta F1 average	GFSK, 2 Mbps	450	500	550	kHz
Mod Char: delta F2 max	GFSK, 2 Mbps	370	450	–	kHz
Mod Char: ratio	GFSK, 2 Mbps	0.8	1.0	–	–
Mod Char: delta F1 average	GFSK, 125 kbps	225	255	275	kHz

Note

46.Dirty TX is off.

WLAN RF specifications

15 WLAN RF specifications

15.1 Introduction

AIROC™ CYW55571 includes an integrated tri-band direct conversion radio that supports the 2.4/5/6 GHz bands. This section describes the RF characteristics of the 2.4/5/6 GHz radios.

Unless otherwise stated, limit values apply for the conditions specified in [Table 33](#), [Table 34](#), [Table 35](#), [Table 36](#), [Table 37](#), and [Table 38](#). Typical values apply for an ambient temperature +25°C.

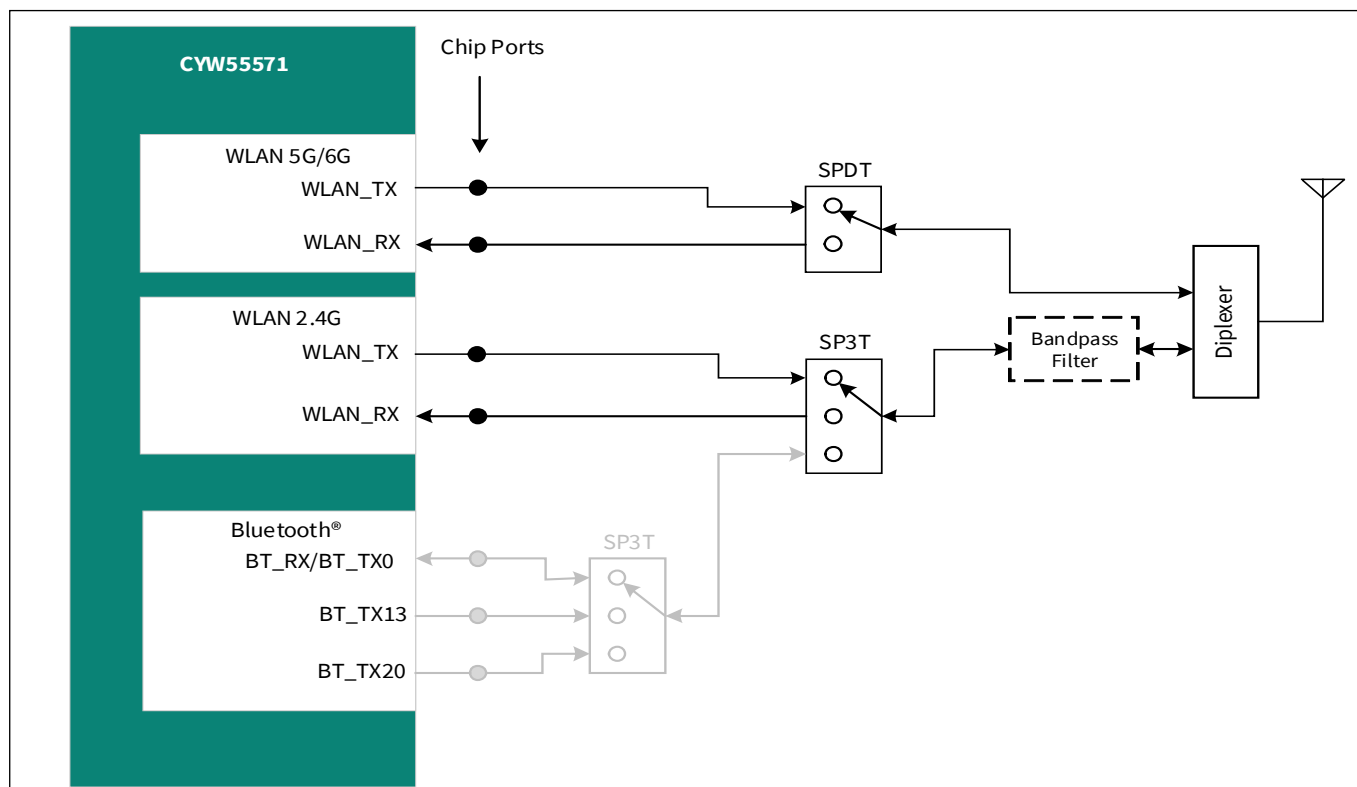


Figure 32 Port locations for WLAN RF testing – shared WLAN/Bluetooth® antenna

WLAN RF specifications

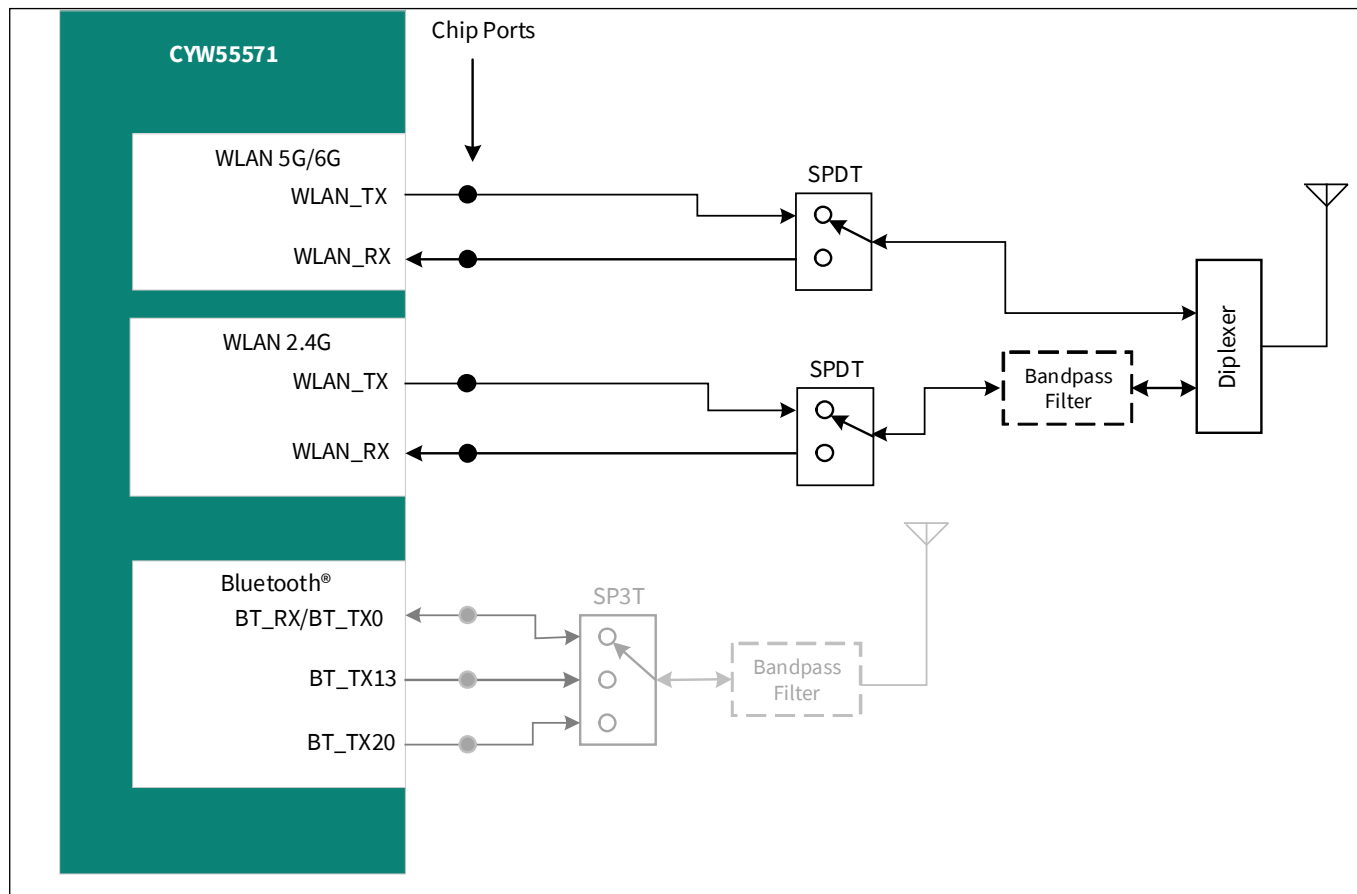


Figure 33 Port locations for WLAN RF testing – dedicated WLAN antenna

15.2 2.4 GHz band general RF specifications

Table 32 2.4 GHz band general RF specifications

Item	Condition	Min	Typ	Max	Unit
TX/RX switch time	Including TX	–	–	5.0	μs
RX/TX switch time	Including TX	–	–	2.0	μs
Power-up and power-down ramp time	DSSS/CCK	–	–	–	–

WLAN RF specifications
15.3 WLAN 2.4 GHz receiver performance specifications

Note The values in [Table 33](#) are specified at the chip port unless otherwise noted.

Table 33 WLAN 2.4 GHz receiver performance specifications

Parameter	Condition/Note	Min	Typ	Max	Unit
Frequency range		2400	–	2500	MHz
Sensitivity					
RX sensitivity IEEE 802.11b (8% PER for 1024 octet PSDU) ^[47]	1 Mbps	–	–101.5	–	dBm
	2 Mbps	–	–98.5	–	dBm
	5.5 Mbps	–	–96.5	–	dBm
	11 Mbps	–	–93.0	–	dBm
RX sensitivity IEEE 802.11g (10% PER for 1000 octet PSDU) ^[47]	6 Mbps	–	–97.5	–	dBm
	9 Mbps	–	–95.5	–	dBm
	12 Mbps	–	–94.5	–	dBm
	18 Mbps	–	–92.0	–	dBm
	24 Mbps	–	–89.0	–	dBm
	36 Mbps	–	–85.5	–	dBm
	48 Mbps	–	–81.5	–	dBm
	54 Mbps	–	–79.5	–	dBm
RX sensitivity IEEE 802.11n 20 MHz channel spacing with High Performance Coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: 800 ns GI, High Performance Coding, and non-STBC. ^[47, 48]	MCS0	–	–97.5	–	dBm
	MCS1	–	–95.5	–	dBm
	MCS2	–	–93.5	–	dBm
	MCS3	–	–90.5	–	dBm
	MCS4	–	–87.0	–	dBm
	MCS5	–	–83.0	–	dBm
	MCS6	–	–81.5	–	dBm
	MCS7	–	–79.5	–	dBm

Notes

- 47.Rx sensitivity data is based on FCBGA part on REF board, for WLPGA parts derate these numbers are better by 0.5-1dB.
- 48.Sensitivity degradations for alternate settings in MCS modes. SGI: 0.8 dB (11ax 1024-QAM rate) and negligible (other rates).
- 49.Desired signal is at a power level 6 dB higher than the IEEE specification for the minimum sensitivity limit.
- 50.Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.
- 51.The typical values shown have a 95% confidence level.

WLAN RF specifications
Table 33 WLAN 2.4 GHz receiver performance specifications (continued)

Parameter	Condition/Note	Min	Typ	Max	Unit
RX sensitivity IEEE 802.11ax 20 MHz channel spacing with High Performance Coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 μ s + 2 $\times$ LTF, High Performance Coding, non-STBC, and 20 MHz BW. ^[47, 48]	MCS0, Nss = 1	–	–97.5	–	dBm
	MCS1, Nss = 1	–	–95.5	–	dBm
	MCS2, Nss = 1	–	–93.0	–	dBm
	MCS3, Nss = 1	–	–90.5	–	dBm
	MCS4, Nss = 1	–	–86.5	–	dBm
	MCS5, Nss = 1	–	–82.5	–	dBm
	MCS6, Nss = 1	–	–81.5	–	dBm
	MCS7, Nss = 1	–	–79.5	–	dBm
	MCS8, Nss = 1	–	–75.5	–	dBm
	MCS9, Nss = 1	–	–73.5	–	dBm
	MCS10, Nss = 1	–	–69.5	–	dBm
	MCS11, Nss = 1	–	–65.5	–	dBm
RX sensitivity IEEE 802.11ax HE-RE PPDU (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 μ s + 2 $\times$ LTF. ^[47, 48]	RU242, MCS0, Nss = 1	–	–99.0	–	dBm
	RU242, MCS1, Nss = 1	–	–95.5	–	dBm
	RU242, MCS2, Nss = 1	–	–92.5	–	dBm
	RU106, MCS0, Nss = 1	–	–99.5	–	dBm
Maximum receiver level @ 2.4 GHz	1, 2 Mbps (8% PER, 1024 octets)	–	–5.0	–	dBm
	5.5, 11 Mbps (8% PER, 1024 octets)	–	–5.0	–	dBm
	6-54 Mbps (10% PER, 1024 octets)	–	–10.0	–	dBm
	MCS0–MCS7 rates (10% PER, 4096 octets)	–	–10.0	–	dBm
	MCS8–MC11 rates (10% PER, 4096 octets)	–	–10.0	–	dBm

ACI/AACI

Adjacent channel rejection – CCK (Difference between interfering and desired signal (20 MHz apart) at 8% PER for 1024 octet PSDU with desired signal level as 6 dB higher than IEEE spec) ^[49]	Desired and interfering signal 30 MHz apart				
	1 Mbps	–74 dBm	–	>54	– dB
	Desired and interfering signal 25 MHz apart				
Adjacent channel rejection – OFDM (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as 3 dB higher than IEEE spec) ^[50]	11 Mbps	–70 dBm	–	>50	– dB
	6 Mbps	–79 dBm	–	40.5	– dB
	54 Mbps	–62 dBm	–	24.0	– dB

Notes

47.Rx sensitivity data is based on FCBGA part on REF board, for WLPGA parts derate these numbers are better by 0.5-1dB.

48.Sensitivity degradations for alternate settings in MCS modes. SGI: 0.8 dB (11ax 1024-QAM rate) and negligible (other rates).

49.Desired signal is at a power level 6 dB higher than the IEEE specification for the minimum sensitivity limit.

50.Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.

51.The typical values shown have a 95% confidence level.

WLAN RF specifications
Table 33 WLAN 2.4 GHz receiver performance specifications (continued)

Parameter	Condition/Note	Min	Typ	Max	Unit
Adjacent channel rejection – MCS0–11 in 20 MHz (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level 3 dB higher than IEEE spec ^[50])	MCS0, Nss=1 –79 dBm	–	42.5	–	dB
	MCS7, Nss=1 –61 dBm	–	20.5	–	dB
	MCS9, Nss=1 –	–	15.5	–	dB
	MCS11, Nss=1 –	–	10.0	–	dB
In-band static CW jammer immunity (fc – 8 MHz < fcw < +8 MHz)	RX PER < 1%, 54 Mbps OFDM, 1024 octet PSDU for: (RxSens + 23 dB < Rxlevel < max. input level)	–	–80.0	–	dBm
Other RF parameters					
Receiver cascaded noise figure	At maximum gain	–	3.0	–	dB
Input in-band IP3	Maximum LNA gain	–	–12.0	–	dBm
	Minimum LNA gain	–	6.0	–	dBm
LPF 3 dB bandwidth	–	–	5.0 to 40	–	MHz
Maximum receiver gain	–	–	67.0	–	dB
Gain control step	–	–	3.0	–	dB
Return loss	Zo = 50 Ω, across the dynamic range	–	10.0	–	dB
RSSI accuracy ^[51]	Range –90 dBm to –30 dBm	–	–3.0 to +3.0	–	dB
	Range above –30 dBm	–	–3.0 to +3.0	–	dB

Notes

- 47.Rx sensitivity data is based on FCBGA part on REF board, for WLPGA parts derate these numbers are better by 0.5-1dB.
- 48.Sensitivity degradations for alternate settings in MCS modes. SGI: 0.8 dB (11ax 1024-QAM rate) and negligible (other rates).
- 49.Desired signal is at a power level 6 dB higher than the IEEE specification for the minimum sensitivity limit.
- 50.Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.
- 51.The typical values shown have a 95% confidence level.

WLAN RF specifications
15.4 WLAN 2.4 GHz transmitter performance specifications

Note: The values in [Table 34](#) are specified at the chip port unless otherwise noted.

Table 34 WLAN 2.4 GHz transmitter performance specifications

Parameter	Condition/Note	EVM limit	Min	Typ	Max	Unit
TX compliance not exceed @ output power						
Max TX power level setting at 25°C and VBAT = 3.3 V with spectral mask and EVM compliance ^[52, 53]	DSSS - 1 Mbps	–9 dB	–	23.0	–	dBm
	DSSS - 11 Mbps	–9 dB	–	23.0	–	dBm
	OFDM - BPSK, R = 3/4	–8 dB	–	22.0	–	dBm
	OFDM - QPSK, R = 3/4	–13 dB	–	22.0	–	dBm
	OFDM - 16QAM, R = 3/4	–19 dB	–	22.0	–	dBm
	OFDM - 64QAM, R = 3/4	–25 dB	–	22.0	–	dBm
	OFDM - 64QAM, R = 5/6 - HE20	–28 dB	–	21.5	–	dBm
	OFDM - 256QAM, R = 3/4 - HE20	–30 dB	–	21.0	–	dBm
	OFDM - 256QAM, R = 5/6 - HE20	–32 dB	–	20.0	–	dBm
	OFDM - 1024QAM, R = 3/4 - HE20	–35 dB	–	19.0	–	dBm
	OFDM - 1024QAM, R = 5/6 - HE20	–35 dB	–	19.0	–	dBm
Carrier suppression	–	–	–	–45.0	–	dBc
TX power control dynamic range	–	–	–	33	–	dB
Gain control step	–	–	–	0.5	–	dB
TX power variation ^[54, 55]	Applies from –10 dBm to 23/22 (DSSS/OFDM) dBm output power range	–	–	±1.5	–	dB

Notes

52. TX complaint power is based on FCBGA part on REF board, for WLBGA parts derate these numbers by 1 dB for 1024-QAM

53. The TX power at the chip output port is controlled by firmware and is approximately 1.5 dB lower from the minimum numbers across process corners, to account for closed loop TX power control and other factors.

54. For range enhancement mode TX power variation will be ±2.0.

55. Tx power variation ±3.0 dB for process, voltage and temperature variation across –40°C to +85°C.

WLAN RF specifications
15.5 WLAN 5 GHz receiver performance specifications

Note: The values in [Table 35](#) are specified at the chip port unless otherwise noted.

Table 35 WLAN 5 GHz receiver performance specifications

Parameter	Condition/Note	Min	Typ	Max	Unit
Sensitivity					
RX sensitivity IEEE 802.11a (10% PER for 1000 octet PSDU) ^[56]	6 Mbps	–	–96.5	–	dBm
	9 Mbps	–	–94.0	–	dBm
	12 Mbps	–	–93.0	–	dBm
	18 Mbps	–	–90.5	–	dBm
	24 Mbps	–	–87.5	–	dBm
	36 Mbps	–	–84.0	–	dBm
	48 Mbps	–	–79.5	–	dBm
	54 Mbps	–	–78.0	–	dBm
RX sensitivity IEEE 802.11n 20 MHz channel spacing with High Performance Coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: 800 ns GI, High Performance Coding, and non-STBC ^[56, 57]	MCS0	–	–97.0	–	dBm
	MCS1	–	–94.5	–	dBm
	MCS2	–	–91.5	–	dBm
	MCS3	–	–89.0	–	dBm
	MCS4	–	–85.5	–	dBm
	MCS5	–	–81.0	–	dBm
	MCS6	–	–79.5	–	dBm
	MCS7	–	–78.0	–	dBm
RX sensitivity IEEE 802.11n 40 MHz channel spacing with High Performance Coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: 800 ns GI, High Performance Coding, and non-STBC ^[56, 57]	MCS0	–	–94.5	–	dBm
	MCS1	–	–91.5	–	dBm
	MCS2	–	–88.5	–	dBm
	MCS3	–	–86.0	–	dBm
	MCS4	–	–82.5	–	dBm
	MCS5	–	–78.5	–	dBm
	MCS6	–	–77.0	–	dBm
	MCS7	–	–75.0	–	dBm

Notes

56. RX sensitivity data is based on FCBGA part on REF board, for WLPGA parts derate the lowest rate numbers by up to 2 dB.

57. Sensitivity degradations for alternate settings in MCS modes. SGI: 1.0 dB (11n/11ac lowest rate and 11ax 1024 QAM rates in 20 MHz) and negligible (other rates/BW).

58. Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.

59. The typical values shown have a 95% confidence level.

WLAN RF specifications
Table 35 WLAN 5 GHz receiver performance specifications (continued)

Parameter	Condition/Note	Min	Typ	Max	Unit
RX sensitivity IEEE 802.11ac 20 MHz channel spacing with High Performance Coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: 800 ns GI, High Performance Coding, and non-STBC [56,57]	MCS0, Nss = 1	–	–97.0	–	dBm
	MCS1, Nss = 1	–	–94.5	–	dBm
	MCS2, Nss = 1	–	–91.5	–	dBm
	MCS3, Nss = 1	–	–89.0	–	dBm
	MCS4, Nss = 1	–	–85.0	–	dBm
	MCS5, Nss = 1	–	–81.0	–	dBm
	MCS6, Nss = 1	–	–79.5	–	dBm
	MCS7, Nss = 1	–	–77.5	–	dBm
	MCS8, Nss = 1	–	–74.0	–	dBm
	MCS9, Nss = 1	–	–72.0	–	dBm
RX sensitivity IEEE 802.11ac 40 MHz channel spacing with High Performance Coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: 800 ns GI, High Performance Coding, and non-STBC [56,57]	MCS0, Nss = 1	–	–94.5	–	dBm
	MCS1, Nss = 1	–	–91.5	–	dBm
	MCS2, Nss = 1	–	–88.5	–	dBm
	MCS3, Nss = 1	–	–86.0	–	dBm
	MCS4, Nss = 1	–	–82.5	–	dBm
	MCS5, Nss = 1	–	–78.5	–	dBm
	MCS6, Nss = 1	–	–77.0	–	dBm
	MCS7, Nss = 1	–	–75.0	–	dBm
	MCS8, Nss = 1	–	–71.0	–	dBm
	MCS9, Nss = 1	–	–69.0	–	dBm
RX sensitivity IEEE 802.11ac 80 MHz channel spacing with High Performance Coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: 800 ns GI, High Performance Coding, and non-STBC [56,57]	MCS0, Nss = 1	–	–91.5	–	dBm
	MCS1, Nss = 1	–	–88.5	–	dBm
	MCS2, Nss = 1	–	–85.5	–	dBm
	MCS3, Nss = 1	–	–83.0	–	dBm
	MCS4, Nss = 1	–	–79.5	–	dBm
	MCS5, Nss = 1	–	–75.5	–	dBm
	MCS6, Nss = 1	–	–74.0	–	dBm
	MCS7, Nss = 1	–	–72.0	–	dBm
	MCS8, Nss = 1	–	–68.5	–	dBm
	MCS9, Nss = 1	–	–66.5	–	dBm

Notes

56. RX sensitivity data is based on FCBGA part on REF board, for WLBGA parts derate the lowest rate numbers by up to 2 dB.

57. Sensitivity degradations for alternate settings in MCS modes. SGI: 1.0 dB (11n/11ac lowest rate and 11ax 1024 QAM rates in 20 MHz) and negligible (other rates/BW).

58. Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.

59. The typical values shown have a 95% confidence level.

WLAN RF specifications
Table 35 WLAN 5 GHz receiver performance specifications (continued)

Parameter	Condition/Note	Min	Typ	Max	Unit
RX sensitivity IEEE 802.11ax 20 MHz channel spacing with High Performance Coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 μ s + 2 $\times$ LTF, High Performance Coding, non-STBC, and 20 MHz BW [56, 57]	MCS0, Nss = 1	–	–97.0	–	dBm
	MCS1, Nss = 1	–	–94.0	–	dBm
	MCS2, Nss = 1	–	–91.5	–	dBm
	MCS3, Nss = 1	–	–88.5	–	dBm
	MCS4, Nss = 1	–	–85.0	–	dBm
	MCS5, Nss = 1	–	–81.0	–	dBm
	MCS6, Nss = 1	–	–79.5	–	dBm
	MCS7, Nss = 1	–	–77.5	–	dBm
	MCS8, Nss = 1	–	–74.0	–	dBm
	MCS9, Nss = 1	–	–71.5	–	dBm
RX sensitivity IEEE 802.11ax 20 MHz channel spacing with High Performance Coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 μ s + 2 $\times$ LTF, High Performance Coding, non-STBC, and 20 MHz BW [56, 57]	MCS10, Nss = 1	–	–67.5		dBm
	MCS11, Nss = 1	–	–63.5	–	dBm

Notes

56. RX sensitivity data is based on FCBGA part on REF board, for WLBGA parts derate the lowest rate numbers by up to 2 dB.
57. Sensitivity degradations for alternate settings in MCS modes. SGI: 1.0 dB (11n/11ac lowest rate and 11ax 1024 QAM rates in 20 MHz) and negligible (other rates/BW).
58. Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.
59. The typical values shown have a 95% confidence level.

WLAN RF specifications
Table 35 WLAN 5 GHz receiver performance specifications (continued)

Parameter	Condition/Note	Min	Typ	Max	Unit
RX sensitivity IEEE 802.11ax 40 MHz channel spacing with High Performance Coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 μ s + 2 $\times$ LTF, High Performance Coding, non-STBC, and 40 MHz BW ^[56, 57]	MCS0, Nss = 1	–	–94.5	–	dBm
	MCS1, Nss = 1	–	–91.5	–	dBm
	MCS2, Nss = 1	–	–88.5	–	dBm
	MCS3, Nss = 1	–	–86.0	–	dBm
	MCS4, Nss = 1	–	–82.5	–	dBm
	MCS5, Nss = 1	–	–78.5	–	dBm
	MCS6, Nss = 1	–	–77.0	–	dBm
	MCS7, Nss = 1	–	–75.5	–	dBm
	MCS8, Nss = 1	–	–71.5	–	dBm
	MCS9, Nss = 1	–	–69.5	–	dBm
	MCS9, Nss = 1	–	–65.5	–	dBm
	MCS11, Nss = 1	–	–61.5	–	dBm
RX sensitivity IEEE 802.11ax 80 MHz channel spacing with High Performance Coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 μ s + 2 $\times$ LTF, High Performance Coding, non-STBC, and 80 MHz BW ^[56, 57]	MCS0, Nss = 1	–	–91.5	–	dBm
	MCS1, Nss = 1	–	–88.5	–	dBm
	MCS2, Nss = 1	–	–85.5	–	dBm
	MCS3, Nss = 1	–	–83.0	–	dBm

Notes

56.RX sensitivity data is based on FCBGA part on REF board, for WLBGA parts derate the lowest rate numbers by up to 2 dB.

57.Sensitivity degradations for alternate settings in MCS modes. SGI: 1.0 dB (11n/11ac lowest rate and 11ax 1024 QAM rates in 20 MHz) and negligible (other rates/BW).

58.Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.

59.The typical values shown have a 95% confidence level.

WLAN RF specifications
Table 35 WLAN 5 GHz receiver performance specifications *(continued)*

Parameter	Condition/Note	Min	Typ	Max	Unit
RX sensitivity IEEE 802.11ax 80 MHz channel spacing with High Performance Coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 μ s + 2 $\times$ LTF, High Performance Coding, non-STBC, and 80 MHz BW [56, 57]	MCS4, Nss = 1	–	–79.5	–	dBm
	MCS5, Nss = 1	–	–75.5	–	dBm
	MCS6, Nss = 1	–	–73.5	–	dBm
	MCS7, Nss = 1	–	–72.0	–	dBm
	MCS8, Nss = 1	–	–68.5	–	dBm
	MCS9, Nss = 1	–	–66.0	–	dBm
	MCS10, Nss = 1	–	–62.0	–	dBm
	MCS11, Nss = 1	–	–58.5	–	dBm
RX sensitivity IEEE 802.11ax HE-RE PPDU (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 μ s + 2 $\times$ LTF [56, 57]	RU242, MCS0, Nss = 1	–	–97.5	–	dBm
	RU242, MCS1, Nss = 1	–	–94.5	–	dBm
	RU242, MCS2, Nss = 1	–	–90.5	–	dBm
	RU106, MCS0, Nss = 1	–	–98.5	–	dBm
Maximum receiver level @ 5 GHz	6–54 Mbps (10% PER, 1024 octets)	–	–5.0	–	dBm/core
	MCS0–MCS7 rates (10% PER, 4096 octets)	–	–5.0	–	dBm/core
	MCS8–MCS11 rates (10% PER, 4096 octets)	–	–8.0	–	dBm/core

Notes

56. RX sensitivity data is based on FCBGA part on REF board, for WLPGA parts derate the lowest rate numbers by up to 2 dB.

57. Sensitivity degradations for alternate settings in MCS modes. SGI: 1.0 dB (11n/11ac lowest rate and 11ax 1024 QAM rates in 20 MHz) and negligible (other rates/BW).

58. Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.

59. The typical values shown have a 95% confidence level.

WLAN RF specifications
Table 35 WLAN 5 GHz receiver performance specifications (continued)

Parameter	Condition/Note		Min	Typ	Max	Unit
ACI / AACI						
Adjacent channel rejection - OFDM (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as 3 dB higher than IEEE spec) ^[58]	6 Mbps	−79 dBm	−	28.5	−	dB
	54 Mbps	−62 dBm	−	12.5	−	dB
Adjacent channel rejection - MCS0–11 in 20 MHz (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level 3 dB higher than IEEE spec) ^[58]	MCS0, Nss=1	−79 dBm	−	29.0	−	dB
	MCS7, Nss=1	−61 dBm	−	12.0	−	dB
	MCS9, Nss=1	−54 dBm	−	6.0	−	dB
	MCS11, Nss=1	−49 dBm	−	0.5	−	dB
Adjacent channel rejection - MCS0–11 in 40 MHz (Difference between interfering and desired signal (40 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level 3 dB higher than IEEE spec) ^[58]	MCS0, Nss = 1	−76 dBm	−	29.0	−	dB
	MCS7, Nss = 1	−58 dBm	−	13.5	−	dB
	MCS9, Nss = 1	−51 dBm	−	9	−	dB
	MCS11, Nss = 1	−46 dBm	−	3.5	−	dB
Adjacent channel rejection - MCS0–11 in 80 MHz (Difference between interfering and desired signal (80 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level 3 dB higher than IEEE spec) ^[58]	MCS0, Nss = 1	−73 dBm	−	29.0	−	dB
	MCS7, Nss = 1	−55 dBm	−	17.0	−	dB
	MCS9, Nss = 1	−48 dBm	−	14.0	−	dB
	MCS11, Nss = 1	−43 dBm	−	6.5	−	dB
Other RF parameters						
Receiver cascaded noise figure	At maximum gain		−	5.0	−	dB
Input In-band IP3	Maximum LNA gain		−	−7.0	−	dBm
	Minimum LNA gain		−	8.0	−	dBm
LPF 3 dB bandwidth	−		−	5.0 to 40	−	MHz
Maximum receiver gain	−		−	63.0	−	dB
Gain control step	−		−	3.0	−	dB
Return loss	Zo = 50 Ω, across the dynamic range		−	10.0	−	dB
RSSI accuracy ^[59]	Range −90 dBm to −30 dBm		−	−3.0 to +3.0	−	dB
	Range above −30 dBm		−	−3.0 to +3.0	−	dB

Notes

56.RX sensitivity data is based on FCBGA part on REF board, for WLPGA parts derate the lowest rate numbers by up to 2 dB.

57.Sensitivity degradations for alternate settings in MCS modes. SGI: 1.0 dB (11n/11ac lowest rate and 11ax 1024 QAM rates in 20 MHz) and negligible (other rates/BW).

58.Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.

59.The typical values shown have a 95% confidence level.

WLAN RF specifications
15.6 WLAN 5 GHz transmitter performance specifications

Note The values in [Table 36](#) are specified at the chip port unless otherwise noted.

Table 36 WLAN 5 GHz transmitter performance specifications

Parameter	Condition	EVM	Min	Typ	Max	Unit
TX compliance not exceed @ output power						
Max TX powerlevel setting at 25°C and VBAT = 3.3 V with spectral mask and EVM compliance ^[60, 61]	OFDM – BPSK, R = 3/4	–8 dB	–	20.5	–	dBm
	OFDM – QPSK, R = 3/4	–13 dB	–	20.5	–	dBm
	OFDM – 16QAM, R = 3/4	–19 dB	–	20.5	–	dBm
	OFDM – 64QAM, R = 3/4	–25 dB	–	20.5	–	dBm
	OFDM – 64QAM, R = 5/6 – HT20	–28 dB	–	20.5	–	dBm
	OFDM – 64QAM, R = 5/6 – HT40	–28 dB	–	20.5	–	dBm
	OFDM – 64QAM, R = 5/6 – VHT80	–28 dB	–	20.5	–	dBm
	OFDM – 64QAM, R = 5/6 – HE80	–28 dB	–	20.0	–	dBm
	OFDM – 256QAM, R = 3/4 – VHT20	–30 dB	–	20.0	–	dBm
	OFDM – 256QAM, R = 5/6 – VHT40	–32 dB	–	19.5	–	dBm
	OFDM – 256QAM, R = 5/6 – VHT80	–32 dB	–	19.0	–	dBm
	OFDM – 256QAM, R = 3/4 – HE20	–30 dB	–	20.0	–	dBm
	OFDM – 256QAM, R = 5/6 – HE20	–32 dB	–	19.0	–	dBm
	OFDM – 256QAM, R = 5/6 – HE40	–32 dB	–	19.0	–	dBm
	OFDM – 256QAM, R = 5/6 – HE80	–32 dB	–	18.5	–	dBm
	OFDM – 1024QAM, R = 3/4 – HE20	–35 dB	–	19.0	–	dBm
	OFDM – 1024QAM, R = 5/6 – HE20	–35 dB	–	18.5	–	dBm
	OFDM – 1024QAM, R = 3/4 – HE40	–35 dB	–	18.0	–	dBm
	OFDM – 1024QAM, R = 5/6 – HE80	–35 dB	–	17.5	–	dBm
Carrier suppression	–	–	–	–45.0	–	dBc
TX power control dynamic range	–	–	–	32.0	–	dB
Gain control step	–	–	–	0.5	–	dB
TX power variation ^[62]	Applies from –10 dBm to 20.0 dBm output power range	–	–	±1.5	–	dB

Notes

60. TX complaint power is based on FCBGA part on REF board, for WLPGA parts derate these numbers by 0.5 dB for 256-QAM and higher.

61. TX power at the chip output port is controlled by firmware and is approximately 1.5 dB lower from the minimum numbers across process corners, to account for closed loop TX power control and other factors.

62. TX power variation ±3.0 dB for process, voltage and temperature variation across –40°C to +85°C.

15.7 WLAN 6 GHz receiver performance specifications

Note: The values in [Table 37](#) are specified at the chip port unless otherwise noted.

Table 37 WLAN 6 GHz receiver performance specifications

Parameter	Condition/note		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
			UNII-5			UNII-6			UNII-7			UNII-8			
Sensitivity															
RX sensitivity IEEE 802.11a (10% PER for 1000 octet PSDU) ^[63]	6 Mbps		–	–96.5	–	–	–95.5	–	–	–94.0	–	–	–90.5	–	dBm
	9 Mbps		–	–94.5	–	–	–93.5	–	–	–91.5	–	–	–88.5	–	dBm
	12 Mbps		–	–93.0	–	–	–92.5	–	–	–90.0	–	–	–87.5	–	dBm
	18 Mbps		–	–90.5	–	–	–89.0	–	–	–87.5	–	–	–84.5	–	dBm
	24 Mbps		–	–87.5	–	–	–86.5	–	–	–85.0	–	–	–82.5	–	dBm
RX sensitivity IEEE 802.11ax 20 MHz channel spacing with High performance coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 μs + 2 × LTF, High Performance Coding, non-STBC, and 20 MHz BW ^[63, 64]	MCS0, Nss = 1		–	–97.0	–	–	–96.0	–	–	–94.0	–	–	–91.5	–	dBm
	MCS1, Nss = 1		–	–94.0	–	–	–93.0	–	–	–91.5	–	–	–88.5	–	dBm
	MCS2, Nss = 1		–	–91.5	–	–	–90.5	–	–	–89.0	–	–	–86.0	–	dBm
	MCS3, Nss = 1		–	–88.5	–	–	–88.0	–	–	–86.0	–	–	–83.0	–	dBm
	MCS4, Nss = 1		–	–85.0	–	–	–84.0	–	–	–82.5	–	–	–80.0	–	dBm
	MCS5, Nss = 1		–	–81.0	–	–	–80.0	–	–	–78.5	–	–	–76.0	–	dBm
	MCS6, Nss = 1		–	–79.5	–	–	–78.5	–	–	–77.0	–	–	–74.0	–	dBm
	MCS7, Nss = 1		–	–77.5	–	–	–76.5	–	–	–75.0	–	–	–72.0	–	dBm

Notes

63. Derate worst case by 4.0 dB (UNII-5/6) and 4.5dB (UNII-7/8) for process, voltage and temperature variation across –40°C to +85°C.

64. Sensitivity degradations for alternate settings in MCS modes. SGI: 1.5 dB (1024QAM rates in 20 MHz) and negligible (for other rates/BW).

65. Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.

66. The typical values shown have a 95% confidence level.

Table 37 WLAN 6 GHz receiver performance specifications *(continued)*

Parameter	Condition/note		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
			UNII-5			UNII-6			UNII-7			UNII-8			
RX sensitivity IEEE 802.11ax 20 MHz channel spacing with high performance Coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 μs + 2 × LTF, High Performance Coding, non-STBC, and 20 MHz BW [63, 64]	MCS8, Nss = 1		–	–74.0	–	–	–73.0	–	–	–71.0	–	–	–68.5	–	dBm
	MCS9, Nss = 1		–	–71.5	–	–	–70.5	–	–	–69.0	–	–	–66.0	–	dBm
	MCS10, Nss = 1		–	–67.0	–	–	–66.5	–	–	–64.5	–	–	–62.0	–	dBm
	MCS11, Nss = 1		–	–63.5	–	–	–62.5	–	–	–61.0	–	–	–58.5	–	dBm
RX sensitivity IEEE 802.11ax 40 MHz channel spacing with High Performance Coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 μs + 2 × LTF, High performance coding, non-STBC, and 40 MHz BW [63, 64]	MCS0, Nss = 1		–	–94.5	–	–	–93.5	–	–	–92.5	–	–	–90.0	–	dBm
	MCS1, Nss = 1		–	–91.5	–	–	–90.5	–	–	–89.0	–	–	–86.0	–	dBm
	MCS2, Nss = 1		–	–88.5	–	–	–87.5	–	–	–86.0	–	–	–83.0	–	dBm
	MCS3, Nss = 1		–	–86.0	–	–	–84.5	–	–	–83.0	–	–	–80.5	–	dBm
	MCS4, Nss = 1		–	–82.5	–	–	–81.5	–	–	–80.0	–	–	–77.5	–	dBm
	MCS5, Nss = 1		–	–78.5	–	–	–77.5	–	–	–76.0	–	–	–73.0	–	dBm
	MCS6, Nss = 1		–	–77.0	–	–	–76.0	–	–	–74.5	–	–	–72.0	–	dBm
	MCS7, Nss = 1		–	–75.0	–	–	–74.5	–	–	–72.5	–	–	–70.0	–	dBm

Notes

63. Derate worst case by 4.0 dB (UNII-5/6) and 4.5dB (UNII-7/8) for process, voltage and temperature variation across –40°C to +85°C.
64. Sensitivity degradations for alternate settings in MCS modes. SGI: 1.5 dB (1024QAM rates in 20 MHz) and negligible (for other rates/BW).
65. Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.
66. The typical values shown have a 95% confidence level.

Table 37 WLAN 6 GHz receiver performance specifications *(continued)*

Parameter	Condition/note	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
		UNII-5			UNII-6			UNII-7			UNII-8			
RX sensitivity IEEE 802.11ax 40 MHz channel spacing with High Performance Coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 μs + 2 × LTF, High Performance Coding, non-STBC, and 40 MHz BW [63, 64]	MCS8, Nss = 1	–	–71.5	–	–	–70.5	–	–	–69.0	–	–	–66.5	–	dBm
	MCS9, Nss = 1	–	–69.5	–	–	–68.5	–	–	–67.0	–	–	–64.5	–	dBm
	MCS10, Nss = 1	–	–65.0	–	–	–64.0	–	–	–63.0	–	–	–60.5	–	dBm
	MCS11, Nss = 1	–	–61.5	–	–	–60.5	–	–	–59.0	–	–	–56.5	–	dBm
RX sensitivity IEEE 802.11ax 80 MHz channel spacing with High Performance Coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 μs + 2 × LTF, High Performance Coding, non-STBC, and 80 MHz BW [63, 64]	MCS0, Nss = 1	–	–91.5	–	–	–91.0	–	–	–89.0	–	–	–86.5	–	dBm
	MCS1, Nss = 1	–	–87.5	–	–	–86.0	–	–	–85.5	–	–	–83.0	–	dBm
	MCS2, Nss = 1	–	–85.0	–	–	–83.0	–	–	–82.5	–	–	–80.0	–	dBm
	MCS3, Nss = 1	–	–83.0	–	–	–82.0	–	–	–80.0	–	–	–77.5	–	dBm
	MCS4, Nss = 1	–	–79.0	–	–	–78.5	–	–	–76.5	–	–	–73.5	–	dBm
	MCS5, Nss = 1	–	–74.0	–	–	–74.0	–	–	–72.5	–	–	–70.0	–	dBm
	MCS6, Nss = 1	–	–73.5	–	–	–73.0	–	–	–71.5	–	–	–68.5	–	dBm
	MCS7, Nss = 1	–	–72.0	–	–	–71.5	–	–	–69.5	–	–	–66.0	–	dBm

Notes

63. Derate worst case by 4.0 dB (UNII-5/6) and 4.5dB (UNII-7/8) for process, voltage and temperature variation across –40°C to +85°C.

64. Sensitivity degradations for alternate settings in MCS modes. SGI: 1.5 dB (1024QAM rates in 20 MHz) and negligible (for other rates/BW).

65. Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.

66. The typical values shown have a 95% confidence level.

Table 37 WLAN 6 GHz receiver performance specifications *(continued)*

Parameter	Condition/note	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
		UNII-5			UNII-6			UNII-7			UNII-8			
RX sensitivity IEEE 802.11ax 80 MHz channel spacing with High Performance Coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = $0.8\text{ }\mu\text{s} + 2 \times \text{LTF}$, High performance coding, non-STBC, and 80 MHz BW [63, 64]	MCS8, Nss = 1	–	–68.0	–	–	–67.5	–	–	–66.0	–	–	–63.0	–	dBm
	MCS9, Nss = 1	–	–66.0	–	–	–65.5	–	–	–64.0	–	–	–60.0	–	dBm
	MCS10, Nss = 1	–	–62.0	–	–	–61.5	–	–	–59.5	–	–	–56.5	–	dBm
	MCS11, Nss = 1	–	–58.0	–	–	–56.5	–	–	–55.5	–	–	–53.0	–	dBm
RX sensitivity IEEE 802.11ax HE-RE PPDU (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = $0.8\text{ }\mu\text{s} + 2 \times \text{LTF}$ [63, 64]	RU242, MCS0, Nss = 1	–	–97.5	–	–	–96.5	–	–	–95.0	–	–	–92.5	–	dBm
	RU242, MCS1, Nss = 1	–	–94.5	–	–	–93.5	–	–	–92.0	–	–	–89.5	–	dBm
	RU242, MCS2, Nss = 1	–	–91.5	–	–	–90.5	–	–	–89.0	–	–	–86.5	–	dBm
	RU106, MCS0, Nss = 1	–	–98.0	–	–	–97.5	–	–	–95.5	–	–	–93.0	–	dBm
Maximum receiver Level @ 6 GHz	6–24 Mbps (10% PER, 1024 octets)	–	–5.0	–	–	–5.0	–	–	–5.0	–	–	–5.0	–	dBm
	MCS0–MCS7 rates (10% PER, 4096 octets)	–	–5.0	–	–	–5.0	–	–	–5.0	–	–	–5.0	–	dBm
	MCS8–MCS11 rates (10% PER, 4096 octets)	–	–8.0	–	–	–8.0	–	–	–8.0	–	–	–8.0	–	dBm

Notes

63. Derate worst case by 4.0 dB (UNII-5/6) and 4.5dB (UNII-7/8) for process, voltage and temperature variation across –40°C to +85°C.
64. Sensitivity degradations for alternate settings in MCS modes. SGI: 1.5 dB (1024QAM rates in 20 MHz) and negligible (for other rates/BW).
65. Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.
66. The typical values shown have a 95% confidence level.

Table 37 WLAN 6 GHz receiver performance specifications *(continued)*

Parameter	Condition/note		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
			UNII-5			UNII-6			UNII-7			UNII-8			
ACI / AAI															
Adjacent channel Rejection - OFDM (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as 3 dB higher than IEEE spec) ^[65]	6 Mbps	−79 dBm	−	28.5	−	−	27.5	−	−	28.5	−	−	26.0	−	dB
	24 Mbps	−76 dBm	−	21.0	−	−	20.0	−	−	21.5	−	−	19.5	−	dB
Adjacent channel Rejection - MCS0–11 in 20 MHz (Difference between inter-fering and desired signal (20 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level 3 dB higher than IEEE spec) ^[65]	MCS0, Nss=1	−79 dBm	−	25.5	−	−	24.5	−	−	25.0	−	−	21.0	−	dB
	MCS7, Nss=1	−61 dBm	−	9.5	−	−	9.0	−	−	10.5	−	−	9.0	−	dB
	MCS9, Nss=1	−54 dBm	−	4.0	−	−	3.5	−	−	5.0	−	−	4.0	−	dB
	MCS11, Nss=1	−49 dBm	−	−1.5	−	−	−2.5	−	−	−0.5	−	−	−2.0	−	dB
Adjacent channel Rejection - MCS0–11 in 40 MHz (Difference between interfering and desired signal (40 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level 3 dB higher than IEEE spec) ^[65]	MCS0, Nss = 1	−76 dBm	−	23.0	−	−	23.5	−	−	21.5	−	−	18.0	−	dB
	MCS7, Nss = 1	−58 dBm	−	10.0	−	−	13.0	−	−	11.0	−	−	11.0	−	dB
	MCS9, Nss = 1	−51 dBm	−	5.5	−	−	8.0	−	−	6.0	−	−	6.0	−	dB
	MCS11, Nss = 1	−46 dBm	−	0.0	−	−	2.0	−	−	1.0	−	−	0.0	−	dB

Notes

63. Derate worst case by 4.0 dB (UNII-5/6) and 4.5dB (UNII-7/8) for process, voltage and temperature variation across -40°C to +85°C.
64. Sensitivity degradations for alternate settings in MCS modes. SGI: 1.5 dB (1024QAM rates in 20 MHz) and negligible (for other rates/BW).
65. Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.
66. The typical values shown have a 95% confidence level.

Table 37 WLAN 6 GHz receiver performance specifications *(continued)*

Parameter	Condition/note		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
			UNII-5			UNII-6			UNII-7			UNII-8			
Adjacent channel Rejection - MCS0–11 in 80 MHz (Difference between interfering and desired signal (80 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level 3 dB higher than IEEE spec) [65]	MCS0, Nss = 1	–73 dBm	–	29.5	–	–	25.5	–	–	25.0	–	–	18.0	–	dB
	MCS7, Nss = 1	–55 dBm	–	14.5	–	–	13.5	–	–	14.5	–	–	13.0	–	dB
	MCS9, Nss = 1	–48 dBm	–	11.5	–	–	10.0	–	–	11.0	–	–	9.5	–	dB
	MCS11, Nss = 1	–43 dBm	–	6.0	–	–	5.0	–	–	5.5	–	–	3.5	–	dB
Other RF parameters															
Receiver cascaded noise figure	At maximum gain		–	5.5	–	–	6.0	–	–	7.0	–	–	8.5	–	dB
Input in-band IP3	Maximum LNA gain		–	–7.0	–	–	–5.0	–	–	–3.0	–	–	0.0	–	dBm
	Minimum LNA gain		–	8.0	–	–	8.0	–	–	9.0	–	–	10.0	–	dBm
LPF 3 dB bandwidth	–		5	–	40	5	–	40	5	–	40	5	–	40	MHz
Maximum receiver gain	–		–	62	–	–	60	–	–	57	–	–	55	–	dB
Gain control step	–		–	3.0	–	–	3.0	–	–	3.0	–	–	3.0	–	dB
Return loss	Zo = 50 Ω, across the dynamic range		–	10.0	–	–	10.0	–	–	7.0	–	–	8.0	–	dB
RSSI accuracy [66]	Range –85 dBm to –30 dBm		–3	–	3	–3	–	3	–3	–	3	–3	–	3	dB
	Range above –30 dBm		–3	–	3	–3	–	3	–3	–	3	–3	–	3	dB

Notes

63. Derate worst case by 4.0 dB (UNII-5/6) and 4.5 dB (UNII-7/8) for process, voltage and temperature variation across –40°C to +85°C.

64. Sensitivity degradations for alternate settings in MCS modes. SGI: 1.5 dB (1024QAM rates in 20 MHz) and negligible (for other rates/BW).

65. Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.

66. The typical values shown have a 95% confidence level.

15.8 WLAN 6 GHz transmitter performance specifications

Note The values in **Table 38** are specified at the chip port unless otherwise noted.

Table 38 WLAN 6 GHz transmitter performance specifications

Parameter	Condition	EVM	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
			UNII-5			UNII-6			UNII-7			UNII-8			
TX compliance not exceed @ output power															
Max TX power level setting at 25°C and VBAT = 3.3 V with spectral mask and EVM compliance ^[67, 68]	OFDM - BPSK, R = 3/4	−8 dB	−	19.0	−	−	19.0	−	−	18.5	−	−	18.5	−	dBm
	OFDM - QPSK, R = 3/4	−13 dB	−	19.0	−	−	19.0	−	−	18.5	−	−	18.5	−	dBm
	OFDM - 16QAM, R = 1/2	−16 dB	−	19.0	−	−	19.0	−	−	18.5	−	−	18.5	−	dBm
	OFDM - 16QAM, R = 3/4 - HE20	−19 dB	−	19.0	−	−	19.0	−	−	18.5	−	−	18.5	−	dBm
	OFDM - 64QAM, R = 5/6 - HE20	−28 dB	−	19.0	−	−	19.0	−	−	18.5	−	−	18.5	−	dBm
	OFDM - 64QAM, R = 5/6 - HE40	−28 dB	−	19.0	−	−	19.0	−	−	18.5	−	−	18.5	−	dBm
	OFDM - 64QAM, R = 5/6 - HE80	−28 dB	−	19.0	−	−	19.0	−	−	18.5	−	−	17.0	−	dBm
	OFDM - 256QAM, R = 3/4 - HE20	−30 dB	−	18.0	−	−	18.0	−	−	17.5	−	−	17.0		dBm
	OFDM - 256QAM, R = 5/6 - HE20	−32 dB	−	18.0	−	−	18.0	−	−	17.5	−	−	16.0	−	dBm
	OFDM - 256QAM, R = 5/6 - HE40	−32 dB	−	18.0	−	−	18.0	−	−	17.5	−	−	16.0	−	dBm
	OFDM - 256QAM, R = 5/6 - HE80	−32 dB	−	17.5	−	−	17.0	−	−	16.5	−	−	15.0	−	dBm
	OFDM - 1024QAM, R = 3/4 - HE20	−35 dB	−	17.5	−	−	17.0	−	−	17.0	−	−	16.0	−	dBm
	OFDM - 1024QAM, R = 5/6 - HE20	−35 dB	−	17.5	−	−	17.5	−	−	17.0	−	−	16.0	−	dBm
	OFDM - 1024QAM, R = 3/4 - HE40	−35 dB	−	18.0	−	−	17.0	−	−	17.0	−	−	15.5	−	dBm
	OFDM - 1024QAM, R = 5/6 - HE80	−35 dB	−	17.0	−	−	16.5	−	−	16.0	−	−	14.0	−	dBm
Carrier suppression	−	−	−	−45.0	−	−	−45.0	−	−	−45.0	−	−	−45.0	−	dBc

Notes

67. Derate worst case (excluding 1024-QAM) by 4.0 dB (UNII-5/6) and 4.5 dB (UNII-7/8) for process, voltage and temperature variation across -40°C to +85°C.

68. TX power at the chip output port is controlled by firmware and is approximately 1.5 dB lower from the minimum numbers mentioned herein, to account for closed loop TX power control variation and other factors.

69. Tx power variation ±3.0 dB for process, voltage and temperature variation across -40°C to +85°C.

Table 38 WLAN 6 GHz transmitter performance specifications *(continued)*

Parameter	Condition	EVM	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
			UNII-5			UNII-6			UNII-7			UNII-8			
TX power control dynamic range	–	–	–	32	–	–	32	–	–	32	–	–	32	–	dB
Gain control step	–	–	–	0.5	–	–	0.5	–	–	0.5	–	–	0.5	–	dB
TX power variation ^[69]	Applies from –10 dBm to 18 dBm output power range	–	–	±1.5	–	–	±1.5	–	–	±1.5	–	–	±1.5	–	dB

Notes

67. Derate worst case (excluding 1024-QAM) by 4.0 dB (UNII-5/6) and 4.5 dB (UNII-7/8) for process, voltage and temperature variation across –40°C to +85°C.

68. TX power at the chip output port is controlled by firmware and is approximately 1.5 dB lower from the minimum numbers mentioned herein, to account for closed loop TX power control variation and other factors.

69. Tx power variation ±3.0 dB for process, voltage and temperature variation across –40°C to +85°C.

WLAN RF specifications**15.9 General spurious emissions specifications**

This section provides the TX and RX spurious emissions specifications for both the WLAN 2.4 GHz and 5 GHz bands. The recommended spectrum analyzer settings for the spurious emissions specifications are provided in [Table 39](#).

Table 39 Recommended spectrum analyzer settings

Parameter	Setting
Resolution bandwidth	1 MHz
Video bandwidth	10 MHz
Sweep	Auto
Span	Variable
Detector	Maximum peak
Trace	Maximum hold
Modulation	Orthogonal frequency-division multiplexing (OFDM)

15.9.1 2.4 GHz band spurious emissions**Table 40 2.4 GHz band, 20 MHz channel spacing TX spurious emissions specifications**
20 MHz channel spacing

Emissions frequency range (MHz)	Channel power (dBm)	Spurious emission (dBm) Core-0
1000–2000	22	–51
2000–2400	22	–50
2500–3000	22	–50
3000–4000	22	–48
4000–5000	22	–15
5000–6000	22	–45
6000–7000	22	–45
7000–8000	22	1.57
8000–10000	22	–13
10000–12000	22	–42
12000–15000	22	–13
15000–20000	22	–39

WLAN RF specifications
15.9.2 5 GHz band spurious emissions
Table 41 5 GHz band, 20 MHz channel spacing TX spurious emissions specifications
20 MHz channel spacing

Emissions frequency range (MHz)	Channel power (dBm)	Spurious emission (dBm) Core-0		
		CH36	CH100	CH165
1000–2000	19.5	–50	–50	–50
2000–3000	19.5	–48	–48	–47
3000–4000	19.5	–46	–47	–46
4000–5000	19.5	–44	–45	–45
5000–6000	19.5	–48	–48	–45
6000–7000	19.5	–38	–37	–43
7000–8000	19.5	–42	–45	–41
8000–10000	19.5	–45	–41	–43
10000–12000	19.5	–2	–14	–6
12000–15000	19.5	–44	–44	–44
15000–20000	19.5	–21	–21	–28

15.9.3 Receiver spurious emissions specifications
Table 42 2G and 5G general receiver spurious emissions

Band	Frequency range	Spurious emission (dBm) Core-0
2G	2.4 GHz < f < 2.5 GHz	–80
	3.6 GHz < f < 3.8 GHz	–81
5G	5.15 GHz < f < 5.85 GHz	–72
	3.8 GHz < f < 4.2 GHz	–61

Internal regulator electrical specifications

16 Internal regulator electrical specifications

Functional operation is not guaranteed outside of the specification limits provided in this section.

16.1 Core buck switching regulator

Table 43 Core buck switching regulator specifications

Specification	Symbol	Note	Min	Typ	Max	Unit
Input supply voltage	V_{BAT}	DC voltage range inclusive of disturbances	3.0	3.3	4.8	V
Switching Frequency	F_{SW}	With calibration (PWM mode only)	3.04	3.2	3.36	MHz
		Programming range	2.8	–	5	
Output current	I_{OUT}	PWM mode Peak rating 800 mA at $T_j \leq 110^\circ\text{C}$ Max DC rating 650 mA at $T_j 125^\circ\text{C}$	–	–	400	mA
Output current limit	I_{OUT_LIMIT}	Peak inductor current	–	1.8	–	A
Output voltage	V_{OUT}	–	–	0.92	–	V
DC accuracy	$V_{OUT_ΔERR}$	Includes line & load regulation	-4	–	4.0	%
		After trim at PWM mode	-2	–	2	
Efficiency ^[70]	E_{FF_PWM}	PWM Peak efficiency at 200 mA. Inductor's DCR Typ = 114 mΩ, ACR Typ = 1 Ω. Fsw = 3.2 MHz	–	86	–	%
	E_{FF_LPPFM}	LPPFM efficiency at 50 mA. Inductor's DCR Typ = 114 mΩ, ACR Typ = 1 Ω.	–	86	–	%
Start-up time	T_{SU}	With VDDIO = 1.8 V as always ON. Measure from rising edge of REG_ON to CSR_pok	–	420	–	μs
External inductor	L	Effective inductance	–	2.2	–	μH
External output capacitor ^[71]	C_O	Effective load capacitance	–	4.7	–	μF
External input capacitor ^[71]	C_{IN}	Effective load capacitance	–	4.7	–	μF

Notes

70.Efficiency numbers are assumed at typical condition (i.e. $V_{BAT} = 3.3\text{ V}$, $V_{DDIO} = 1.8\text{ V}$, $ASR\ V_{OUT} = 1.12\text{ V}$, and $CSR\ V_{OUT} = 0.9\text{ V}$ at room temp = 27°C). Component parts used for $L = 2.2\text{ μH}$, and $C_O = 4.7\text{ μF}$.

71.Min cap value refers to effective cap value after taking into account part-to-part tolerance, DC-bias, temperature and aging. Typ cap value refers to manufacturer nominal part value. Max cap value refers to the total capacitance seen at the output. This includes all decoupling caps connected at the load side (if there is any).

Internal regulator electrical specifications
16.2 Analog switching regulator specifications
Table 44 Analog switching regulator specifications

Specification	Symbol	Notes	Min	Typ	Max	Unit
Input supply voltage	V _{BAT}	DC voltage range inclusive of disturbances	3.0	3.3	4.8	V
Switching Frequency	F _{SW}	With calibration (PWM mode only)	3.04	3.2	3.36	MHz
		Programming range	2.8	–	5	
Output current	I _{OUT}	PWM mode. Peak rating 800 mA at T _j ≤ 110 °C Max DC rating 650 mA at T _j 125 °C	–	–	400	mA
Output current limit	I _{OUT_LIMIT}	Peak inductor current	–	1.8	–	A
Output voltage	V _{OUT}	–	–	1.12	–	V
DC accuracy	V _{OUT_ΔERR}	Includes line & load regulation	-4	–	4.0	%
		After trim at PWM mode	-2	–	2	
Efficiency ^[72]	E _{FF_PWM}	PWM Peak efficiency at 200 mA. Inductor's DCR Typ = 114 mΩ, ACR Typ = 1 Ω. Fsw = 3.2 MHz	–	86	–	%
	E _{FF_LPPFM}	LPPFM efficiency at 50 mA. Inductor's DCR Typ = 114 mΩ, ACR Typ = 1 Ω.	–	86	–	%
Start-up time	T _{SU}	With VDDIO = 1.8 V as always ON. Measure from rising edge of REG_ON to ASR_pok	–	450	–	μs
External inductor	L	Effective inductance	–	2.2	–	μH
External output capacitor ^[73]	C _O	Effective load capacitance	–	4.7	–	μF
External input capacitor ^[73]	C _{IN}	Effective load capacitance	–	4.7	–	μF

Notes

72. Efficiency numbers are assumed at typical condition (i.e. V_{BAT} = 3.3 V, VDDIO = 1.8 V, ASR V_{OUT} = 1.12 V, and CSR V_{OUT} = 0.9 V at room temp = 27°C). Component parts used for L = 2.2 μH, and CO = 4.7 μF.

73. Min cap value refers to effective cap value after taking into account part-to-part tolerance, DC-bias, temperature and aging. Typ cap value refers to manufacturer nominal part value. Max cap value refers to the total capacitance seen at the output. This includes all decoupling caps connected at the load side (if there is any).

Internal regulator electrical specifications
16.3 RF_LDO (VDDOUT_RF3P3)
Table 45 VDDOUT_RF3P3 specifications

Specification	Symbol	Notes	Min	Typ	Max	Unit
Input supply voltage	V_{BAT}	DC voltage range inclusive of disturbances	3.0	3.3	4.8	V
Nominal output voltage	V_{OUT}	–	–	2.87 ^[74]	–	V
Dropout voltage	–	Max load	200	–	–	mV
Output current	I_{OUT}	–	0.3	–	200	mA
Quiescent current	I_{Q_NoLoad}	$I_{OUT} = 100 \mu A$, $V_{OUT} = 3.3 V$	–	40	63	μA
	$I_{Q_MaxLoad}$	$I_{OUT} = 200 mA$, $V_{OUT} = 3.3 V$	–	1.6	1.7	mA
Power-down current	I_{Q_PD}	Typ at ambient Temp 25°C	–	16	–	nA
		Max at ambient Temp 85°C	–	–	13.8	μA
Line regulation	–	V_{BAT} from 3.5–5.5 V; $I_{OUT} = 200 mA$	–	–	3.5	mV/V
Load regulation	–	Load from 1–200 mA; $V_{BAT} = 3.3 V$.	–	–	0.3	mV/mA
Load step error	–	Load from 1–100 mA in 1 μs at $V_{BAT} = 3.3 V$; $C_O = 0.16 \mu F$.	–	–	55	mV
PSRR	–	Freq from 100–100 kHz at max load. Freq at FSW at max load	20.0	–	–	dB
Turn-on time	T_{ON}	Measure from p μ signal to $V_{OUT} = 3.2 V$ with reference ready. $C_O = 2.2 \mu F$	–	–	120	μs
Output current Limit	I_{OUT_LIMIT}	–	–	550	910	mA
In-rush current	I_{INRUSH}	–	–	68	116	mA
Output capacitor ^[75]	C_O	See components section for details	–	2.2	–	μF

Notes

74.LDO output voltage is configured to 2.87 V with a minimum headroom (V_{BAT} -LDO OUPUT) of 120 mV.

75.Min cap value refers to effective cap value after taking into account part-to-part tolerance, DC-bias, temperature and aging. Typ cap value refers to manufacturer nominal part value. Max cap value refers to the total capacitance seen at the output. This includes all decoupling caps connected at the load side (if there is any).

Internal regulator electrical specifications
16.4 BT_LDO (VDDOUT_BT3P3)
Table 46 VDDOUT_BT3P3 specifications

Specification	Symbol	Notes	Min	Typ	Max	Unit
Input supply voltage	V_{BAT}	DC voltage range inclusive of disturbances	3.0	3.3	4.8	V
Nominal output voltage	V_{OUT}	–	–	2.87 ^[76]	–	V
Dropout voltage	–	Max load	200	–	–	mV
Output current	I_{OUT}	–	0.2	–	400	mA
Quiescent current	I_{Q_NoLoad}	$I_{OUT} = 200 \mu A$, $V_{OUT} = 3.3 V$	–	77	124	μA
	$I_{Q_MaxLoad}$	$I_{OUT} = 400 mA$, $V_{OUT} = 3.3 V$	–	3.3	–	mA
Power-down current	I_{Q_PD}	Typ at Ambient Temp 25°C	–	11	–	nA
		Max at Ambient Temp 85°C	–	–	25	μA
Line regulation	–	V_{BAT} from 3.5–5.5 V; $I_{OUT} = 400 mA$	–	–	3.5	mV/V
Load regulation	–	Load from 1–400 mA; $V_{BAT} = 3.3 V$	–	–	0.3	mV/mA
Load step error	–	Load from 1–200.5 mA in 1 μs at $V_{BAT} = 3.3 V$; $C_O = 0.16 \mu F$	–	–	100	mV
PSRR	–	Freq from 100–100 kHz at max load Freq at FSW at max load	20.0	–	–	dB
Turn-on time ^f	T_{ON}	Measure from p μ signal to $V_{OUT} = 3.3 V$ with reference ready. $C_O = 2.2 \mu F$	–	–	150	μs
Output current Limit	I_{OUT_LIMIT}	–	–	1060	1800	mA
In-rush current	I_{INRUSH}	–	–	155	220	mA
Output capacitor ^[77]	C_O	See components section for details	–	2.2	–	μF

Notes

76.LDO output voltage is configured to 2.87 V with a minimum headroom (V_{BAT} -LDO OUPUT) of 120 mV.

77.Min cap value refers to effective cap value after taking into account part-to-part tolerance, DC-bias, temperature and aging. Typ cap value refers to manufacturer nominal part value. Max cap value refers to the total capacitance seen at the output. This includes all decoupling caps connected at the load side (if there is any).

Internal regulator electrical specifications
16.5 3.3 V LDO_PA3P3
Table 47 3.3 V LDO_PA3P3

Specification	Symbol	Notes	Min	Typ	Max	Unit
Input supply voltage	V_{BAT}	Range	2.7	3.3	4.8	V
Nominal output voltage	V_{OUT}	–	–	2.87 ^[78]	–	V
Output voltage accuracy	–	–	–4	–	4	%
Dropout voltage	–	$I_{OUT} = 800 \text{ mA}$	200	–	–	mV
Output current	I_{OUT}	–	0.4	–	800	mA
Power-down current	$I_{Q(PD)}$	Typ @ 25°C	–	1.7	2.8	μA
		Max @ 125°C	–	29	47	
Line regulation	–	$3.5 \text{ V} \leq V_{BAT} \leq 4.8 \text{ V}$, $I_{OUT} = 800 \text{ mA}$, $V_{OUT} = 3.3 \text{ V}$	–	–	3.5	mV/V
Load regulation	–	$1 \text{ mA} \leq I_{OUT} \leq 800 \text{ mA}$, $V_{BAT} = 3.3 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$	–	–	0.3	mV/mA
Load step error	–	Load step from 1 mA to 400 mA in 1 μs, $V_{BAT} = 3.3 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$, $C_{OUT} = 4.7 \text{ μF}$	–	–	85	mV
PSRR	–	$100 \text{ Hz} \leq f_{TEST} \leq 100 \text{ kHz}$	20	–	–	dB
		$I_{OUT} = 800 \text{ mA}$				
Turn-on time ^[79]	T_{ON}	Time from “pu” asserted to $V_{OUT} = 3.2 \text{ V}$, $C_{OUT} = 4.7 \text{ μF}$	–	125	–	μs
Output current limit	$I_{OUT(LIMIT)}$	$V_{IN} = 5 \text{ V}$, $V_{OUT} = 3.3 \text{ V}$, increase I_{OUT} until $V_{OUT} = 3.2 \text{ V}$	–	2.8	3.6	A
In-rush current	I_{INRUSH}	$C_{OUT} = 4.7 \text{ μF}$	–	236	266	mA
Output capacitor	C_{OUT}	See components section for details	–	4.7	–	μF

Notes

78.LDO output voltage is configured to 2.87 V with a minimum headroom (V_{BAT} -LDO OUPUT) of 120 mV.

79.RSee register map for actual inrush delay setting.

Internal regulator electrical specifications
16.6 1 V LDO (VDDOUT_MISC)
Table 48 VDDOUT_MISC specifications

Specification	Symbol	Notes	Min	Typ	Max	Unit
Input supply voltage	V_{IN}	Dropout voltage requirement must be met for performance	–	1.12	–	V
Nominal output voltage	V_{OUT}	–	–	1.005	–	V
Output voltage programmability	–	Range	0.85	–	1.2	V
		Accuracy at any step	–4	–	4	%
Dropout voltage	–	Max load	50	–	–	mV
Output current	I_{OUT}	–	0.1	–	60	mA
Quiescent current	I_{Q_NoLoad}	No load	–	–	7	μA
	$I_{Q_MaxLoad}$	Maximum load	–	–	2	mA
Power-down Current	I_{Q_PD}	$V_{IN} = 1.12$ V Typ at Junction Temp 25°C, Max at Junction Temp 85°C	–	1	14	μA
Bypass Current	I_{Q_byp}	$V_{IN} = 0.8$ V (Chip DS0) Typ at Junction Temp 25°C, Max at Junction Temp 85°C	–	–	1	μA
Line regulation	–	V_{IN} from ($V_{OUT} + V_d$) – 1.3 V; $V_{IOUT} = 60$ mA.	–	–	1	mV/V
Load regulation	–	Load from 1–60 mA; $V_{IN} = 1.22$ V.	–	–	125	mV/A
Load step error	–	Load from 1–60 mA in 100 ns $V_{IN} = 1.22$ V; $C_o = 0.5$ μF effective.	–	–	40	mV
PSRR	–	Freq from 100–100 kHz at ½ max load. Freq at FSW at ½ max load	20.0	–	–	dB
Turn-on time	T_{ON}	Measure from pu signal to $V_{OUT} = 1.0$ V with reference ready. $C_o = 1$ μF	–	40	–	μs
In-rush current	I_{INRUSH}	$C_o = 1$ μF	–	–	60	mA
Output capacitor ^[80]	C_o	See components section for details	–	1	–	μF

Note

80.Min cap value refers to effective cap value after taking into account part-to-part tolerance, DC-bias, temperature and aging. Typ cap value refers to manufacturer nominal part value. Max cap value refers to the total capacitance seen at the output. This includes all decoupling caps connected at the load side (if there is any).

System power consumption

17 System power consumption

17.1 WLAN current consumption – 2.4/5 GHz

The WLAN current consumption measurements are shown in [Table 49](#).

All values in [Table 49](#) are with the Bluetooth® core in reset (that is, Bluetooth® is OFF).

Table 49 WLAN current consumption – 2.4/5 GHz

Mode	Bandwidth (MHz)	Band (GHz)	V _{bat} = 3.3 V mA	V _{io} = 1.8 V μA
Sleep modes				
OFF ^[85]	–	–	0.000207	0.445
Sleep ^[86]	–	–	0.077	8
IEEE power save, DTIM 1 ^[87]	20.0	2.4	0.94	40
IEEE power save, DTIM 3 ^[87]	20.0	2.4	0.40	20
IEEE power save, DTIM 10 ^[87]	20.0	2.4	0.20	11
IEEE power save, DTIM 1 ^[87]	20.0	5.0	0.78	36
IEEE power save, DTIM 3 ^[87]	20.0	5.0	0.34	18
IEEE power save, DTIM 10 ^[87]	20.0	5.0	0.19	11
IEEE power save, DTIM 1 ^[87]	40.0	5.0	0.82	39
IEEE power save, DTIM 3 ^[87]	40.0	5.0	0.36	18
IEEE power save, DTIM 10 ^[87]	40.0	5.0	0.19	11
IEEE power save, DTIM 1 ^[87]	80.0	5.0	0.87	38
IEEE power save, DTIM 3 ^[87]	80.0	5.0	0.38	18
IEEE power save, DTIM 10 ^[87]	80.0	5.0	0.19	11

Notes

81..All current numbers are based on FCBGA part on REF board.

82.Derate IEEE PS VBAT current by up to 0.1 mA for WLBGA parts.

83.TX active current are better by up to 8% for WLBGA parts.

84.Specified with all pins idle (not switching) and not driving any loads.

85.WL_REG_ON, BT_REG_ON both LOW.

86.Idle, not associated, or inter-beacon.

87.Beacon Interval = 102.4 ms. Beacon duration = 1 ms @1 Mbps for 2.4G band and 300 μs @6 Mbps for 5G band.

Average current over three DTIM intervals.

88.Duty cycle is 100%.

89.Measured using Packet engine test mode.

90.Duty cycle is 100%, RX input power –40 dBm. Carrier sense (CS) detect/packet receive.

91.Carrier sense (CCA) when no carrier is present, measured in IFS interval during active RX.

92.Output power per core at chip port = 21.5 dBm.

93.Output power per core at chip port = 20.5 dBm.

94.Output power per core at chip port = 20.0 dBm.

95.Output power per core at chip port = 19.5 dBm.

96.Output power per core at chip port = 19.0 dBm.

97.Output power per core at chip port = 18.5 dBm.

98.Output power per core at chip port = 18.0 dBm.

99.Output power per core at chip port = 17.5 dBm.

100.Output power per core at chip port = 17.0 dBm.

101.Output power per core at chip port = 16.5 dBm.

102.Output power per core at chip port = 16.0 dBm.

103.Output power per core at chip port = 15.5 dBm.

System power consumption
Table 49 WLAN current consumption – 2.4/5 GHz (continued)

Mode	Bandwidth (MHz)	Band (GHz)	V _{bat} = 3.3 V mA	V _{io} = 1.8 V μA
Active modes				
Transmit				
CCK 1 chain [88, 89, 92]	20	2.4	271	3300
6 Mbps [88, 89, 93]	20	2.4	208	2700
MCS7, SGI [88, 89, 94]	20	2.4	240	2800
MCS9, Nss 1, SGI [88, 89, 97]	20	2.4	218	2900
MCS11, Nss 1, SGI [88, 89, 99]	20	2.4	208	2700
6 Mbps [88, 89, 98]	20	5	261	2700
54 Mbps [88, 89, 98]	20	5	304	2600
MCS0, Nss 1 [88, 89, 98]	20	5	261	2900
MCS7, Nss 1, SGI [88, 89, 98]	20	5	304	2800
MCS9, Nss 1, SGI [88, 89, 99]	20	5	297	2900
MCS11, Nss 1, SGI [88, 89, 101]	20	5	283	2700
MCS0, Nss 1 [88, 89, 98]	40	5	318	2800
MCS7, Nss 1, SGI [88, 89, 98]	40	5	320	2800
MCS9, Nss 1, SGI [88, 89, 99]	40	5	311	2800
MCS11, Nss 1, SGI [88, 89, 101]	40	5	297	2700
MCS0, Nss 1 [88, 89, 98]	80	5	329	2800
MCS7, Nss 1, SGI [88, 89, 98]	80	5	333	2700
MCS9, Nss 1, SGI [88, 89, 101]	80	5	307	2800
MCS11, Nss 1, SGI [88, 89, 103]	80	5	297	2700

Notes

- 81..All current numbers are based on FCBGA part on REF board.
- 82.Derate IEEE PS VBAT current by up to 0.1 mA for WLPGA parts.
- 83.TX active current are better by up to 8% for WLPGA parts.
- 84.Specified with all pins idle (not switching) and not driving any loads.
- 85.WL_REG_ON, BT_REG_ON both LOW.
- 86.Idle, not associated, or inter-beacon.
- 87.Beacon Interval = 102.4 ms. Beacon duration = 1 ms @1 Mbps for 2.4G band and 300 μs @6 Mbps for 5G band.
Average current over three DTIM intervals.
- 88.Duty cycle is 100%.
- 89.Measured using Packet engine test mode.
- 90.Duty cycle is 100%, RX input power –40 dBm. Carrier sense (CS) detect/packet receive.
- 91.Carrier sense (CCA) when no carrier is present, measured in IFS interval during active RX.
- 92.Output power per core at chip port = 21.5 dBm.
- 93.Output power per core at chip port = 20.5 dBm.
- 94.Output power per core at chip port = 20.0 dBm.
- 95.Output power per core at chip port = 19.5 dBm.
- 96.Output power per core at chip port = 19.0 dBm.
- 97.Output power per core at chip port = 18.5 dBm.
- 98.Output power per core at chip port = 18.0 dBm.
- 99.Output power per core at chip port = 17.5 dBm.
- 100.Output power per core at chip port = 17.0 dBm.
- 101.Output power per core at chip port = 16.5 dBm.
- 102.Output power per core at chip port = 16.0 dBm.
- 103.Output power per core at chip port = 15.5 dBm.

System power consumption
Table 49 WLAN current consumption – 2.4/5 GHz (continued)

Mode	Bandwidth (MHz)	Band (GHz)	V _{bat} = 3.3 V mA	V _{io} = 1.8 V μA
Receive				
1 Mbps ^[90]	20	2.4	38	1351
6 Mbps ^[90]	20	2.4	40	1340
Receive MCS7, Nss 1 ^[90]	20	2.4	42	1341
Receive MCS9, Nss 1 ^[90]	20	2.4	42	1342
Receive MCS11, Nss 1 ^[90]	20	2.4	43	1341
CRS ^[91]	20	2.4	38	1351
6 Mbps ^[90]	20	5	47	1335
Receive MCS7, Nss 1 ^[90]	20	5	50	1331
Receive MCS9, Nss 1 ^[90]	20	5	50	1331
Receive MCS11, Nss 1 ^[90]	20	5	51	1330
CRS ^[91]	20	5	46	1331
Receive MCS7, Nss 1 ^[90]	40	5	57	1312
Receive MCS9, Nss 1 ^[90]	40	5	57	1312
Receive MCS11, Nss 1 ^[90]	40	5	59	1312
CRS ^[91]	40	5	52	1312
Receive MCS7, Nss 1 ^[90]	80	5	69	1301
Receive MCS9, Nss 1 ^[90]	80	5	70	1301
Receive MCS11, Nss 1 ^[90]	80	5	74	1301
CRS ^[91]	80	5	61	1301

Notes

- 81..All current numbers are based on FCBGA part on REF board.
- 82.Derate IEEE PS VBAT current by up to 0.1 mA for WLPGA parts.
- 83.TX active current are better by up to 8% for WLPGA parts.
- 84.Specified with all pins idle (not switching) and not driving any loads.
- 85.WL_REG_ON, BT_REG_ON both LOW.
- 86.Idle, not associated, or inter-beacon.
- 87.Beacon Interval = 102.4 ms. Beacon duration = 1 ms @1 Mbps for 2.4G band and 300 μs @6 Mbps for 5G band.
Average current over three DTIM intervals.
- 88.Duty cycle is 100%.
- 89.Measured using Packet engine test mode.
- 90.Duty cycle is 100%, RX input power –40 dBm. Carrier sense (CS) detect/packet receive.
- 91.Carrier sense (CCA) when no carrier is present, measured in IFS interval during active RX.
- 92.Output power per core at chip port = 21.5 dBm.
- 93.Output power per core at chip port = 20.5 dBm.
- 94.Output power per core at chip port = 20.0 dBm.
- 95.Output power per core at chip port = 19.5 dBm.
- 96.Output power per core at chip port = 19.0 dBm.
- 97.Output power per core at chip port = 18.5 dBm.
- 98.Output power per core at chip port = 18.0 dBm.
- 99.Output power per core at chip port = 17.5 dBm.
- 100.Output power per core at chip port = 17.0 dBm.
- 101.Output power per core at chip port = 16.5 dBm.
- 102.Output power per core at chip port = 16.0 dBm.
- 103.Output power per core at chip port = 15.5 dBm.

System power consumption
17.2 WLAN current consumption – 6 GHz

The WLAN current consumption measurements are shown in [Table 50](#).

All values in [Table 50](#) are with the Bluetooth® core in reset (that is, Bluetooth® is OFF).

Table 50 WLAN current consumption – 6 GHz

Mode	Bandwidth (MHz)	Band (GHz)	V _{bat} = 3.3 V mA	V _{io} = 1.8 V μA
Sleep modes				
OFF ^[108]	–	–	0.000207	0.445
Sleep ^[109]	–	–	0.077	8
IEEE power save, DTIM 1 ^[110]	20.0	6-UNII5	0.77	36
IEEE power save, DTIM 3 ^[110]	20.0	6-UNII5	0.34	18
IEEE power save, DTIM 10 ^[110]	20.0	6-UNII5	0.18	11
IEEE power save, DTIM 1 ^[110]	40.0	6-UNII5	0.82	42
IEEE power save, DTIM 3 ^[110]	40.0	6-UNII5	0.35	18
IEEE power save, DTIM 10 ^[110]	40.0	6-UNII5	0.18	11
IEEE power save, DTIM 1 ^[110]	80.0	6-UNII5	0.84	40
IEEE power save, DTIM 3 ^[110]	80.0	6-UNII5	0.36	18
IEEE power save, DTIM 10 ^[110]	80.0	6-UNII5	0.19	11
IEEE power save, DTIM 1 ^[110]	20.0	6-UNII6	0.77	42
IEEE power save, DTIM 3 ^[110]	20.0	6-UNII6	0.34	18
IEEE power save, DTIM 10 ^[110]	20.0	6-UNII6	0.18	11

Notes

104.All current numners are based on FCBGA part on REF board.

105.Derate IEEE PS Vbat current by up to 0.1mA for WLBGA parts.

106.TX active current are better by up to 8% for WLBGA parts for UNII-5/6 band and worse by up to 8% for UNII-7/8 band.

107.Specified with all pins idle (not switching) and not driving any loads.

108.WL_REG_ON, BT_REG_ON both LOW.

109.Idle, not associated, or inter-beacon.

110.B.Beacon Interval = 102.4 ms. Beacon duration = 300 μs @6 Mbps. Average current over three DTIM intervals.

111.Duty cycle is 100%.

112.Measured using Packet engine test mode.

113.Duty cycle is 100%, Rx input power –40 dBm. Carrier sense (CS) detect/packet receive.

114.Carrier sense (CCA) when no carrier is present, measured in IFS interval during active RX.

115.Output power per core at chip port = 17.0 dBm.

116.Output power per core at chip port = 16.5 dBm

117.Output power per core at chip port = 16.0 dBm

118.Output power per core at chip port = 15.5 dBm.

119.Output power per core at chip port = 15.0 dBm.

120.Output power per core at chip port = 14.5 dBm.

121.Output power per core at chip port = 14.0 dBm.

122.Output power per core at chip port = 13.5 dBm.

123.Output power per core at chip port = 13.0 dBm

124.Output power per core at chip port = 12.5 dBm.

125.Output power per core at chip port = 12.0 dBm.

126.Output power per core at chip port = 14.5 dBm.

127.Output power per core at chip port = 14.0 dBm.

128.Output power per core at chip port = 13.5 dBm.

System power consumption
Table 50 WLAN current consumption – 6 GHz (continued)

Mode	Bandwidth (MHz)	Band (GHz)	V _{bat} = 3.3 V mA	V _{io} = 1.8 V μA
IEEE power save, DTIM 1 ^[110]	40.0	6-UNII6	0.80	41
IEEE power save, DTIM 3 ^[110]	40.0	6-UNII6	0.35	18
IEEE power save, DTIM 10 ^[110]	40.0	6-UNII6	0.18	11
IEEE power save, DTIM 1 ^[110]	80.0	6-UNII6	0.90	42
IEEE power save, DTIM 3 ^[110]	80.0	6-UNII6	0.36	18
IEEE power save, DTIM 10 ^[110]	80.0	6-UNII6	0.19	11
IEEE power save, DTIM 1 ^[110]	20.0	6-UNII7	0.77	39
IEEE power save, DTIM 3 ^[110]	20.0	6-UNII7	0.34	18
IEEE power save, DTIM 10 ^[110]	20.0	6-UNII7	0.18	11
IEEE power save, DTIM 1 ^[110]	40.0	6-UNII7	0.80	44
IEEE power save, DTIM 3 ^[110]	40.0	6-UNII7	0.35	18
IEEE power save, DTIM 10 ^[110]	40.0	6-UNII7	0.18	11
IEEE power save, DTIM 1 ^[110]	80.0	6-UNII7	0.84	42
IEEE power save, DTIM 3 ^[110]	80.0	6-UNII7	0.36	18
IEEE power save, DTIM 10 ^[110]	80.0	6-UNII7	0.19	11
IEEE power save, DTIM 1 ^[110]	20.0	6-UNII8	0.78	42
IEEE power save, DTIM 3 ^[110]	20.0	6-UNII8	0.34	18
IEEE power save, DTIM 10 ^[110]	20.0	6-UNII8	0.18	11

Notes

104.All current numners are based on FCBGA part on REF board.

105.Derate IEEE PS Vbat current by up to 0.1mA for WLBGA parts.

106.TX active current are better by up to 8% for WLBGA parts for UNII-5/6 band and worse by up to 8% for UNII-7/8 band.

107.Specified with all pins idle (not switching) and not driving any loads.

108.WL_REG_ON, BT_REG_ON both LOW.

109.Idle, not associated, or inter-beacon.

110.B.Beacon Interval = 102.4 ms. Beacon duration = 300 μs @6 Mbps. Average current over three DTIM intervals.

111.Duty cycle is 100%.

112.Measured using Packet engine test mode.

113.Duty cycle is 100%, Rx input power –40 dBm. Carrier sense (CS) detect/packet receive.

114.Carrier sense (CCA) when no carrier is present, measured in IFS interval during active RX.

115.Output power per core at chip port = 17.0 dBm.

116.Output power per core at chip port = 16.5 dBm

117.Output power per core at chip port = 16.0 dBm

118.Output power per core at chip port = 15.5 dBm.

119.Output power per core at chip port = 15.0 dBm.

120.Output power per core at chip port = 14.5 dBm.

121.Output power per core at chip port = 14.0 dBm.

122.Output power per core at chip port = 13.5 dBm.

123.Output power per core at chip port = 13.0 dBm

124.Output power per core at chip port = 12.5 dBm.

125.Output power per core at chip port = 12.0 dBm.

126.Output power per core at chip port = 14.5 dBm.

127.Output power per core at chip port = 14.0 dBm.

128.Output power per core at chip port = 13.5 dBm.

System power consumption
Table 50 WLAN current consumption – 6 GHz (continued)

Mode	Bandwidth (MHz)	Band (GHz)	V _{bat} = 3.3 V mA	V _{io} = 1.8 V μA
IEEE power save, DTIM 1 ^[110]	40.0	6-UNII8	0.80	45
IEEE power save, DTIM 3 ^[110]	40.0	6-UNII8	0.35	18
IEEE power save, DTIM 10 ^[110]	40.0	6-UNII8	0.18	11
IEEE power save, DTIM 1 ^[110]	80.0	6-UNII8	0.85	40
IEEE power save, DTIM 3 ^[110]	80.0	6-UNII8	0.36	18
IEEE power save, DTIM 10 ^[110]	80.0	6-UNII8	0.19	11

Notes

104.All current numners are based on FCBGA part on REF board.

105.Derate IEEE PS Vbat current by up to 0.1mA for WLBGA parts.

106.TX active current are better by up to 8% for WLBGA parts for UNII-5/6 band and worse by up to 8% for UNII-7/8 band.

107.Specified with all pins idle (not switching) and not driving any loads.

108.WL_REG_ON, BT_REG_ON both LOW.

109.Idle, not associated, or inter-beacon.

110.B.Beacon Interval = 102.4 ms. Beacon duration = 300 μs @6 Mbps. Average current over three DTIM intervals.

111.Duty cycle is 100%.

112.Measured using Packet engine test mode.

113.Duty cycle is 100%, Rx input power –40 dBm. Carrier sense (CS) detect/packet receive.

114.Carrier sense (CCA) when no carrier is present, measured in IFS interval during active RX.

115.Output power per core at chip port = 17.0 dBm.

116.Output power per core at chip port = 16.5 dBm

117.Output power per core at chip port = 16.0 dBm

118.Output power per core at chip port = 15.5 dBm.

119.Output power per core at chip port = 15.0 dBm.

120.Output power per core at chip port = 14.5 dBm.

121.Output power per core at chip port = 14.0 dBm.

122.Output power per core at chip port = 13.5 dBm.

123.Output power per core at chip port = 13.0 dBm

124.Output power per core at chip port = 12.5 dBm.

125.Output power per core at chip port = 12.0 dBm.

126.Output power per core at chip port = 14.5 dBm.

127.Output power per core at chip port = 14.0 dBm.

128.Output power per core at chip port = 13.5 dBm.

System power consumption
Table 50 WLAN current consumption – 6 GHz (continued)

Mode	Bandwidth (MHz)	Band (GHz)	V _{bat} = 3.3 V mA	V _{io} = 1.8 V μA
Active modes				
Transmit				
6 Mbps ^[111, 112, 116]	20	6-UNII5	236	2700
24 Mbps ^[111, 112, 116]	20	6-UNII5	264	2700
MCS0, Nss 1 ^[111, 112, 116]	20	6-UNII5	265	2800
MCS7, Nss 1 ^[111, 112, 116]	20	6-UNII5	271	2700
MCS9, Nss 1 ^[111, 112, 117]	20	6-UNII5	272	2700
MCS11, Nss 1 ^[111, 112, 119]	20	6-UNII5	253	2700
MCS0, Nss 1 ^[111, 112, 116]	40	6-UNII5	276	2700
MCS7, Nss 1 ^[111, 112, 116]	40	6-UNII5	280	2700
MCS9, Nss 1 ^[111, 112, 117]	40	6-UNII5	280	2700
MCS11, Nss 1 ^[111, 112, 120]	40	6-UNII5	255	2700
MCS0, Nss 1 ^[111, 112, 116]	80	6-UNII5	287	2700
MCS7, Nss 1 ^[111, 112, 116]	80	6-UNII5	291	2700
MCS9, Nss 1 ^[111, 112, 117]	80	6-UNII5	284	2700
MCS11, Nss 1 ^[111, 112, 120]	80	6-UNII5	266	2700
6 Mbps ^[111, 112, 116]	20	6-UNII6	244	2700
24 Mbps ^[111, 112, 116]	20	6-UNII6	276	2700

Notes

- 104.All current numners are based on FCBGA part on REF board.
- 105.Derate IEEE PS Vbat current by up to 0.1mA for WLBGA parts.
- 106.TX active current are better by up to 8% for WLBGA parts for UNII-5/6 band and worse by up to 8% for UNII-7/8 band.
- 107.Specified with all pins idle (not switching) and not driving any loads.
- 108.WL_REG_ON, BT_REG_ON both LOW.
- 109.Idle, not associated, or inter-beacon.
- 110.B.Beacon Interval = 102.4 ms. Beacon duration = 300 μs @6 Mbps. Average current over three DTIM intervals.
- 111.Duty cycle is 100%.
- 112.Measured using Packet engine test mode.
- 113.Duty cycle is 100%, Rx input power –40 dBm. Carrier sense (CS) detect/packet receive.
- 114.Carrier sense (CCA) when no carrier is present, measured in IFS interval during active RX.
- 115.Output power per core at chip port = 17.0 dBm.
- 116.Output power per core at chip port = 16.5 dBm
- 117.Output power per core at chip port = 16.0 dBm
- 118.Output power per core at chip port = 15.5 dBm.
- 119.Output power per core at chip port = 15.0 dBm.
- 120.Output power per core at chip port = 14.5 dBm.
- 121.Output power per core at chip port = 14.0 dBm.
- 122.Output power per core at chip port = 13.5 dBm.
- 123.Output power per core at chip port = 13.0 dBm
- 124.Output power per core at chip port = 12.5 dBm.
- 125.Output power per core at chip port = 12.0 dBm.
- 126.Output power per core at chip port = 14.5 dBm.
- 127.Output power per core at chip port = 14.0 dBm.
- 128.Output power per core at chip port = 13.5 dBm.

System power consumption
Table 50 WLAN current consumption – 6 GHz (continued)

Mode	Bandwidth (MHz)	Band (GHz)	V _{bat} = 3.3 V mA	V _{io} = 1.8 V μA
MCS0, Nss 1 ^[111, 112, 116]	20	6-UNII6	277	2800
MCS7, Nss 1 ^[111, 112, 116]	20	6-UNII6	283	2700
MCS9, Nss 1 ^[111, 112, 118]	20	6-UNII6	277	2700
MCS11, Nss 1 ^[111, 112, 119]	20	6-UNII6	263	2700
MCS0, Nss 1 ^[111, 112, 116]	40	6-UNII6	287	2700
MCS7, Nss 1 ^[111, 112, 116]	40	6-UNII6	290	2700
MCS9, Nss 1 ^[111, 112, 118]	40	6-UNII6	283	2700
MCS11, Nss 1 ^[111, 112, 120]	40	6-UNII6	264	2700
MCS0, Nss 1 ^[111, 112, 116]	80	6-UNII6	298	2700
MCS7, Nss 1 ^[111, 112, 116]	80	6-UNII6	302	2700
MCS9, Nss 1 ^[111, 112, 119]	80	6-UNII6	282	2700
MCS11, Nss 1 ^[111, 112, 120]	80	6-UNII6	275	2700
6 Mbps ^[111, 112, 117]	20	6-UNII7	244	2700
24 Mbps ^[111, 112, 117]	20	6-UNII7	273	2700
MCS0, Nss 1 ^[111, 112, 117]	20	6-UNII7	275	2800
MCS7, Nss 1 ^[111, 112, 117]	20	6-UNII7	281	2700
MCS9, Nss 1 ^[111, 112, 118]	20	6-UNII7	275	2700
MCS11, Nss 1 ^[111, 112, 120]	20	6-UNII7	264	2700

Notes

104.All current numners are based on FCBGA part on REF board.

105.Derate IEEE PS Vbat current by up to 0.1mA for WLBGA parts.

106.TX active current are better by up to 8% for WLBGA parts for UNII-5/6 band and worse by up to 8% for UNII-7/8 band.

107.Specified with all pins idle (not switching) and not driving any loads.

108.WL_REG_ON, BT_REG_ON both LOW.

109.Idle, not associated, or inter-beacon.

110.B.Beacon Interval = 102.4 ms. Beacon duration = 300 μs @6 Mbps. Average current over three DTIM intervals.

111.Duty cycle is 100%.

112.Measured using Packet engine test mode.

113.Duty cycle is 100%, Rx input power –40 dBm. Carrier sense (CS) detect/packet receive.

114.Carrier sense (CCA) when no carrier is present, measured in IFS interval during active RX.

115.Output power per core at chip port = 17.0 dBm.

116.Output power per core at chip port = 16.5 dBm

117.Output power per core at chip port = 16.0 dBm

118.Output power per core at chip port = 15.5 dBm.

119.Output power per core at chip port = 15.0 dBm.

120.Output power per core at chip port = 14.5 dBm.

121.Output power per core at chip port = 14.0 dBm.

122.Output power per core at chip port = 13.5 dBm.

123.Output power per core at chip port = 13.0 dBm

124.Output power per core at chip port = 12.5 dBm.

125.Output power per core at chip port = 12.0 dBm.

126.Output power per core at chip port = 14.5 dBm.

127.Output power per core at chip port = 14.0 dBm.

128.Output power per core at chip port = 13.5 dBm.

System power consumption
Table 50 WLAN current consumption – 6 GHz (continued)

Mode	Bandwidth (MHz)	Band (GHz)	V _{bat} = 3.3 V mA	V _{io} = 1.8 V μA
MCS0, Nss 1 ^[111, 112, 117]	40	6-UNII7	283	2700
MCS7, Nss 1 ^[111, 112, 117]	40	6-UNII7	288	2700
MCS9, Nss 1 ^[111, 112, 118]	40	6-UNII7	282	2700
MCS11, Nss 1 ^[111, 112, 120]	40	6-UNII7	270	2700
MCS0, Nss 1 ^[111, 112, 117]	80	6-UNII7	293	2700
MCS7, Nss 1 ^[111, 112, 117]	80	6-UNII7	298	2700
MCS9, Nss 1 ^[111, 112, 120]	80	6-UNII7	280	2700
MCS11, Nss 1 ^[111, 112, 122]	80	6-UNII7	270	2700
6 Mbps ^[111, 112, 117]	20	6-UNII8	249	2700
24 Mbps ^[111, 112, 117]	20	6-UNII8	277	2700
MCS0, Nss 1 ^[111, 112, 117]	20	6-UNII8	278	2800
MCS7, Nss 1 ^[111, 112, 117]	20	6-UNII8	284	2700
MCS9, Nss 1 ^[111, 112, 121]	20	6-UNII8	262	2700
MCS11, Nss 1 ^[111, 112, 123]	20	6-UNII8	253	2700
MCS0, Nss 1 ^[111, 112, 117]	40	6-UNII8	287	2700
MCS7, Nss 1 ^[111, 112, 117]	40	6-UNII8	291	2700
MCS9, Nss 1 ^[111, 112, 121]	40	6-UNII8	268	2700
MCS11, Nss 1 ^[111, 112, 123]	40	6-UNII8	259	2700

Notes

104.All current numners are based on FCBGA part on REF board.

105.Derate IEEE PS Vbat current by up to 0.1mA for WLBGA parts.

106.TX active current are better by up to 8% for WLBGA parts for UNII-5/6 band and worse by up to 8% for UNII-7/8 band.

107.Specified with all pins idle (not switching) and not driving any loads.

108.WL_REG_ON, BT_REG_ON both LOW.

109.Idle, not associated, or inter-beacon.

110.B.Beacon Interval = 102.4 ms. Beacon duration = 300 μs @6 Mbps. Average current over three DTIM intervals.

111.Duty cycle is 100%.

112.Measured using Packet engine test mode.

113.Duty cycle is 100%, Rx input power –40 dBm. Carrier sense (CS) detect/packet receive.

114.Carrier sense (CCA) when no carrier is present, measured in IFS interval during active RX.

115.Output power per core at chip port = 17.0 dBm.

116.Output power per core at chip port = 16.5 dBm

117.Output power per core at chip port = 16.0 dBm

118.Output power per core at chip port = 15.5 dBm.

119.Output power per core at chip port = 15.0 dBm.

120.Output power per core at chip port = 14.5 dBm.

121.Output power per core at chip port = 14.0 dBm.

122.Output power per core at chip port = 13.5 dBm.

123.Output power per core at chip port = 13.0 dBm

124.Output power per core at chip port = 12.5 dBm.

125.Output power per core at chip port = 12.0 dBm.

126.Output power per core at chip port = 14.5 dBm.

127.Output power per core at chip port = 14.0 dBm.

128.Output power per core at chip port = 13.5 dBm.

System power consumption
Table 50 WLAN current consumption – 6 GHz (continued)

Mode	Bandwidth (MHz)	Band (GHz)	V _{bat} = 3.3 V mA	V _{io} = 1.8 V μA
MCS0, Nss 1 ^[111, 112, 117]	80	6-UNII8	298	2700
MCS7, Nss 1 ^[111, 112, 119]	80	6-UNII8	291	2700
MCS9, Nss 1 ^[111, 112, 123]	80	6-UNII8	275	2700
MCS11, Nss 1 ^[111, 112, 125]	80	6-UNII8	263	2700
Receive				
6 Mbps ^[113]	20	6-UNII5	47	1341
24 Mbps ^[113]	20	6-UNII5	47	1340
Receive MCS0, Nss 1 ^[113]	20	6-UNII5	49	1336
Receive MCS7, Nss 1 ^[113]	20	6-UNII5	49	1337
Receive MCS9, Nss 1 ^[113]	20	6-UNII5	50	1337
Receive MCS11, Nss 1 ^[113]	20	6-UNII5	50	1336
CRS ^[114]	20	6-UNII5	44	1340
Receive MCS0, Nss 1 ^[113]	40	6-UNII5	57	1316
Receive MCS7, Nss 1 ^[113]	40	6-UNII5	57	1317
Receive MCS9, Nss 1 ^[113]	40	6-UNII5	58	1317
Receive MCS11, Nss 1 ^[113]	40	6-UNII5	59	1319
CRS ^[114]	40	6-UNII5	50	1317
Receive MCS0, Nss 1 ^[113]	80	6-UNII5	66	1303

Notes

104.All current numners are based on FCBGA part on REF board.

105.Derate IEEE PS Vbat current by up to 0.1mA for WLBGA parts.

106.TX active current are better by up to 8% for WLBGA parts for UNII-5/6 band and worse by up to 8% for UNII-7/8 band.

107.Specified with all pins idle (not switching) and not driving any loads.

108.WL_REG_ON, BT_REG_ON both LOW.

109.Idle, not associated, or inter-beacon.

110.B.Beacon Interval = 102.4 ms. Beacon duration = 300 μs @6 Mbps. Average current over three DTIM intervals.

111.Duty cycle is 100%.

112.Measured using Packet engine test mode.

113.Duty cycle is 100%, Rx input power –40 dBm. Carrier sense (CS) detect/packet receive.

114.Carrier sense (CCA) when no carrier is present, measured in IFS interval during active RX.

115.Output power per core at chip port = 17.0 dBm.

116.Output power per core at chip port = 16.5 dBm

117.Output power per core at chip port = 16.0 dBm

118.Output power per core at chip port = 15.5 dBm.

119.Output power per core at chip port = 15.0 dBm.

120.Output power per core at chip port = 14.5 dBm.

121.Output power per core at chip port = 14.0 dBm.

122.Output power per core at chip port = 13.5 dBm.

123.Output power per core at chip port = 13.0 dBm

124.Output power per core at chip port = 12.5 dBm.

125.Output power per core at chip port = 12.0 dBm.

126.Output power per core at chip port = 14.5 dBm.

127.Output power per core at chip port = 14.0 dBm.

128.Output power per core at chip port = 13.5 dBm.

System power consumption
Table 50 WLAN current consumption – 6 GHz (continued)

Mode	Bandwidth (MHz)	Band (GHz)	V _{bat} = 3.3 V mA	V _{io} = 1.8 V μA
Receive MCS7, Nss 1 ^[113]	80	6-UNII5	69	1303
Receive MCS9, Nss 1 ^[113]	80	6-UNII5	71	1303
Receive MCS11, Nss 1 ^[113]	80	6-UNII5	72	1302
CRS ^[114]	80	6-UNII5	58	1340
6 Mbps ^[113]	20	6-UNII6	47	1341
24 Mbps ^[113]	20	6-UNII6	48	1340
Receive MCS0, Nss 1 ^[113]	20	6-UNII6	50	1336
Receive MCS7, Nss 1 ^[113]	20	6-UNII6	50	1337
Receive MCS9, Nss 1 ^[113]	20	6-UNII6	50	1337
Receive MCS11, Nss 1 ^[113]	20	6-UNII6	50	1336
CRS ^[114]	20	6-UNII6	44	1340
Receive MCS0, Nss 1 ^[113]	40	6-UNII6	57	1316
Receive MCS7, Nss 1 ^[113]	40	6-UNII6	58	1317
Receive MCS9, Nss 1 ^[113]	40	6-UNII6	58	1317
Receive MCS11, Nss 1 ^[113]	40	6-UNII6	59	1319
CRS ^[114]	40	6-UNII6	51	1316
Receive MCS0, Nss 1 ^[113]	80	6-UNII6	67	1303
Receive MCS7, Nss 1 ^[113]	80	6-UNII6	70	1303

Notes

104.All current numners are based on FCBGA part on REF board.

105.Derate IEEE PS Vbat current by up to 0.1mA for WLBGA parts.

106.TX active current are better by up to 8% for WLBGA parts for UNII-5/6 band and worse by up to 8% for UNII-7/8 band.

107.Specified with all pins idle (not switching) and not driving any loads.

108.WL_REG_ON, BT_REG_ON both LOW.

109.Idle, not associated, or inter-beacon.

110.B.Beacon Interval = 102.4 ms. Beacon duration = 300 μs @6 Mbps. Average current over three DTIM intervals.

111.Duty cycle is 100%.

112.Measured using Packet engine test mode.

113.Duty cycle is 100%, Rx input power –40 dBm. Carrier sense (CS) detect/packet receive.

114.Carrier sense (CCA) when no carrier is present, measured in IFS interval during active RX.

115.Output power per core at chip port = 17.0 dBm.

116.Output power per core at chip port = 16.5 dBm

117.Output power per core at chip port = 16.0 dBm

118.Output power per core at chip port = 15.5 dBm.

119.Output power per core at chip port = 15.0 dBm.

120.Output power per core at chip port = 14.5 dBm.

121.Output power per core at chip port = 14.0 dBm.

122.Output power per core at chip port = 13.5 dBm.

123.Output power per core at chip port = 13.0 dBm

124.Output power per core at chip port = 12.5 dBm.

125.Output power per core at chip port = 12.0 dBm.

126.Output power per core at chip port = 14.5 dBm.

127.Output power per core at chip port = 14.0 dBm.

128.Output power per core at chip port = 13.5 dBm.

System power consumption
Table 50 WLAN current consumption – 6 GHz (continued)

Mode	Bandwidth (MHz)	Band (GHz)	V _{bat} = 3.3 V mA	V _{io} = 1.8 V μA
Receive MCS9, Nss 1 ^[113]	80	6-UNII6	71	1303
Receive MCS11, Nss 1 ^[113]	80	6-UNII6	73	1302
CRS ^[114]	80	6-UNII6	59	1303
6 Mbps ^[113]	20	6-UNII7	47	1341
24 Mbps ^[113]	20	6-UNII7	48	1340
Receive MCS0, Nss 1 ^[113]	20	6-UNII7	50	1336
Receive MCS7, Nss 1 ^[113]	20	6-UNII7	50	1337
Receive MCS9, Nss 1 ^[113]	20	6-UNII7	50	1337
Receive MCS11, Nss 1 ^[113]	20	6-UNII7	51	1336
CRS ^[114]	20	6-UNII7	44	1340
Receive MCS0, Nss 1 ^[113]	40	6-UNII7	57	1316
Receive MCS7, Nss 1 ^[113]	40	6-UNII7	58	1317
Receive MCS9, Nss 1 ^[113]	40	6-UNII7	59	1317
Receive MCS11, Nss 1 ^[113]	40	6-UNII7	59	1319
CRS ^[114]	40	6-UNII7	51	1316
Receive MCS0, Nss 1 ^[113]	80	6-UNII7	67	1303
Receive MCS7, Nss 1 ^[113]	80	6-UNII7	70	1303
Receive MCS9, Nss 1 ^[113]	80	6-UNII7	71	1303

Notes

104.All current numners are based on FCBGA part on REF board.

105.Derate IEEE PS Vbat current by up to 0.1mA for WLBGA parts.

106.TX active current are better by up to 8% for WLBGA parts for UNII-5/6 band and worse by up to 8% for UNII-7/8 band.

107.Specified with all pins idle (not switching) and not driving any loads.

108.WL_REG_ON, BT_REG_ON both LOW.

109.Idle, not associated, or inter-beacon.

110.B.Beacon Interval = 102.4 ms. Beacon duration = 300 μs @6 Mbps. Average current over three DTIM intervals.

111.Duty cycle is 100%.

112.Measured using Packet engine test mode.

113.Duty cycle is 100%, Rx input power –40 dBm. Carrier sense (CS) detect/packet receive.

114.Carrier sense (CCA) when no carrier is present, measured in IFS interval during active RX.

115.Output power per core at chip port = 17.0 dBm.

116.Output power per core at chip port = 16.5 dBm

117.Output power per core at chip port = 16.0 dBm

118.Output power per core at chip port = 15.5 dBm.

119.Output power per core at chip port = 15.0 dBm.

120.Output power per core at chip port = 14.5 dBm.

121.Output power per core at chip port = 14.0 dBm.

122.Output power per core at chip port = 13.5 dBm.

123.Output power per core at chip port = 13.0 dBm

124.Output power per core at chip port = 12.5 dBm.

125.Output power per core at chip port = 12.0 dBm.

126.Output power per core at chip port = 14.5 dBm.

127.Output power per core at chip port = 14.0 dBm.

128.Output power per core at chip port = 13.5 dBm.

System power consumption
Table 50 WLAN current consumption – 6 GHz (continued)

Mode	Bandwidth (MHz)	Band (GHz)	V _{bat} = 3.3 V mA	V _{io} = 1.8 V μA
Receive MCS11, Nss 1 ^[113]	80	6-UNII7	73	1302
CRS ^[114]	80	6-UNII7	59	1303
6 Mbps ^[113]	20	6-UNII8	48	1341
24 Mbps ^[113]	20	6-UNII8	48	1340
Receive MCS0, Nss 1 ^[113]	20	6-UNII8	50	1336
Receive MCS7, Nss 1 ^[113]	20	6-UNII8	50	1337
Receive MCS9, Nss 1 ^[113]	20	6-UNII8	51	1337
Receive MCS11, Nss 1 ^[113]	20	6-UNII8	51	1336
CRS ^[114]	20	6-UNII8	45	1340
Receive MCS0, Nss 1 ^[113]	40	6-UNII8	58	1316
Receive MCS7, Nss 1 ^[113]	40	6-UNII8	58	1317
Receive MCS9, Nss 1 ^[113]	40	6-UNII8	59	1317
Receive MCS11, Nss 1 ^[113]	40	6-UNII8	60	1319
CRS ^[114]	40	6-UNII8	51	1316
Receive MCS0, Nss 1 ^[113]	80	6-UNII8	67	1303
Receive MCS7, Nss 1 ^[113]	80	6-UNII8	70	1303
Receive MCS9, Nss 1 ^[113]	80	6-UNII8	72	1303

Notes

104. All current numbers are based on FCBGA part on REF board.
105. Derate IEEE PS Vbat current by up to 0.1mA for WLPGA parts.
106. TX active current are better by up to 8% for WLPGA parts for UNII-5/6 band and worse by up to 8% for UNII-7/8 band.
107. Specified with all pins idle (not switching) and not driving any loads.
108. WL_REG_ON, BT_REG_ON both LOW.
109. Idle, not associated, or inter-beacon.
110. B. Beacon Interval = 102.4 ms. Beacon duration = 300 μs @6 Mbps. Average current over three DTIM intervals.
111. Duty cycle is 100%.
112. Measured using Packet engine test mode.
113. Duty cycle is 100%, Rx input power –40 dBm. Carrier sense (CS) detect/packet receive.
114. Carrier sense (CCA) when no carrier is present, measured in IFS interval during active RX.
115. Output power per core at chip port = 17.0 dBm.
116. Output power per core at chip port = 16.5 dBm
117. Output power per core at chip port = 16.0 dBm
118. Output power per core at chip port = 15.5 dBm.
119. Output power per core at chip port = 15.0 dBm.
120. Output power per core at chip port = 14.5 dBm.
121. Output power per core at chip port = 14.0 dBm.
122. Output power per core at chip port = 13.5 dBm.
123. Output power per core at chip port = 13.0 dBm
124. Output power per core at chip port = 12.5 dBm.
125. Output power per core at chip port = 12.0 dBm.
126. Output power per core at chip port = 14.5 dBm.
127. Output power per core at chip port = 14.0 dBm.
128. Output power per core at chip port = 13.5 dBm.

System power consumption
Table 50 WLAN current consumption – 6 GHz (continued)

Mode	Bandwidth (MHz)	Band (GHz)	V _{bat} = 3.3 V mA	V _{io} = 1.8 V μA
Receive MCS11, Nss 1 ^[113]	80	6-UNII8	74	1302
CRS ^[114]	80	6-UNII8	59	1303

Notes

104. All current numbers are based on FCBGA part on REF board.
105. Derate IEEE PS Vbat current by up to 0.1mA for WLBGA parts.
106. TX active current are better by up to 8% for WLBGA parts for UNII-5/6 band and worse by up to 8% for UNII-7/8 band.
107. Specified with all pins idle (not switching) and not driving any loads.
108. WL_REG_ON, BT_REG_ON both LOW.
109. Idle, not associated, or inter-beacon.
110. B. Beacon Interval = 102.4 ms. Beacon duration = 300 μs @6 Mbps. Average current over three DTIM intervals.
111. Duty cycle is 100%.
112. Measured using Packet engine test mode.
113. Duty cycle is 100%, Rx input power –40 dBm. Carrier sense (CS) detect/packet receive.
114. Carrier sense (CCA) when no carrier is present, measured in IFS interval during active RX.
115. Output power per core at chip port = 17.0 dBm.
116. Output power per core at chip port = 16.5 dBm
117. Output power per core at chip port = 16.0 dBm
118. Output power per core at chip port = 15.5 dBm.
119. Output power per core at chip port = 15.0 dBm.
120. Output power per core at chip port = 14.5 dBm.
121. Output power per core at chip port = 14.0 dBm.
122. Output power per core at chip port = 13.5 dBm.
123. Output power per core at chip port = 13.0 dBm
124. Output power per core at chip port = 12.5 dBm.
125. Output power per core at chip port = 12.0 dBm.
126. Output power per core at chip port = 14.5 dBm.
127. Output power per core at chip port = 14.0 dBm.
128. Output power per core at chip port = 13.5 dBm.

System power consumption
17.3 Bluetooth® current consumption

The Bluetooth® and Bluetooth® LE current consumption measurements are shown in [Table 51](#).

Notes:

- The WLAN core is in reset (WL_REG_ON = low) for all measurements provided in [Table 51](#).
- The Bluetooth® current consumption numbers are measured based on GFSK TX output power = 13 dBm.

Table 51 Bluetooth® and Bluetooth® LE current consumption

Operating mode	VBAT (VBAT = 3.3 V) typical	VDDIO (VDDIO = 1.8 V) typical	Unit
Sleep	41	8	µA
Standard 1.28 s inquiry scan	139	12	µA
500 ms sniff master	122	14	µA
DM1/DH1 master TXRX	13.21	0.3	mA
DM1/DH1 slave TXRX	13.12	0.3	mA
DM3/DH3 master TXRX	15.55	0.326	mA
DM3/DH3 slave TXRX	15.23	0.325	mA
DM5/DH5 master TXRX	15.8	0.331	mA
DM5/DH5 slave TXRX	15.53	0.331	mA
3DH5/3DH1 master TXRX	15.73	0.433	mA
3DH5/3DH1 slave TXRX	15.61	0.433	mA
SCO HV3 master	7.42	0.264	mA
Bluetooth® LE scan	147	12	µA
Bluetooth® LE nonconnectable 1 s ADV (3 channels)	90	11	µA
Bluetooth® LE nonconnectable 1.28 s ADV (3 channels)	79	10	µA
Bluetooth® LE connectable 1.28 s ADV (3 channels)	83	10	µA
Bluetooth® LE connectable 1.28 s ADV (3 channels) 0 dBm (low-power TX path)	76	10	µA
Bluetooth® LE 300 ms connected slave	169	20	µA
Bluetooth® LE 300 ms connected slave 0 dBm (low-power TX path)	164	19	µA
Bluetooth® LE 1 s connected slave	83	11	µA

System power consumption
Notes

- The WLAN core is in reset (WL_REG_ON = LOW) for all measurements provided in [Table 52](#).
- The Bluetooth® current consumption numbers are measured based on GFSK TX output power = 20 dBm.

Table 52 Bluetooth® and Bluetooth® LE current consumption (TX 20 dbm)

Operating mode	DVT measured current numbers Averaged over 3-TT parts		Unit
	VBAT (VBAT = 3.3 V) typical	VDDIO (VDDIO = 1.8 V) typical	
Sleep	40.239	8.857	μA
Standard 1.28 s inquiry scan	137.222	12.542	μA
500 ms sniff master	165.702	14	μA
DM1/DH1 master TXRX	53.623	0.302	mA
DM1/DH1 slave TXRX	53.665	0.302	mA
DM3/DH3 master TXRX	70.83	0.333	mA
DM3/DH3 slave TXRX	70.816	0.333	mA
DM5/DH5 master TXRX	74.094	0.339	mA
DM5/DH5 slave TXRX	73.988	0.338	mA
3DH5/3DH1 master TXRX	82.169	0.439	mA
3DH5/3DH1 slave TXRX	82.096	0.439	mA
SCO HV3 master	20.812	0.249	mA
Bluetooth® LE scan	147.074	12.861	μA
Bluetooth® LE nonconnectable 1 s ADC (3 channels)	147.502	11.009	μA
Bluetooth® LE nonconnectable 1.28 s ADC (3 channels)	124.34	10.514	μA
Bluetooth® LE connected 1.28 s ADC (3 channels)	130.49	10.66	μA
Bluetooth® LE 300 ms connected slave	167.85	19.101	μA
Bluetooth® LE 1 s connected slave	83.809	11.047	μA

18 Interface timing and AC characteristics

18.1 SDIO timing

18.1.1 SDIO default mode timing

SDIO default mode timing is shown by the combination of [Figure 34](#) and [Table 53](#).

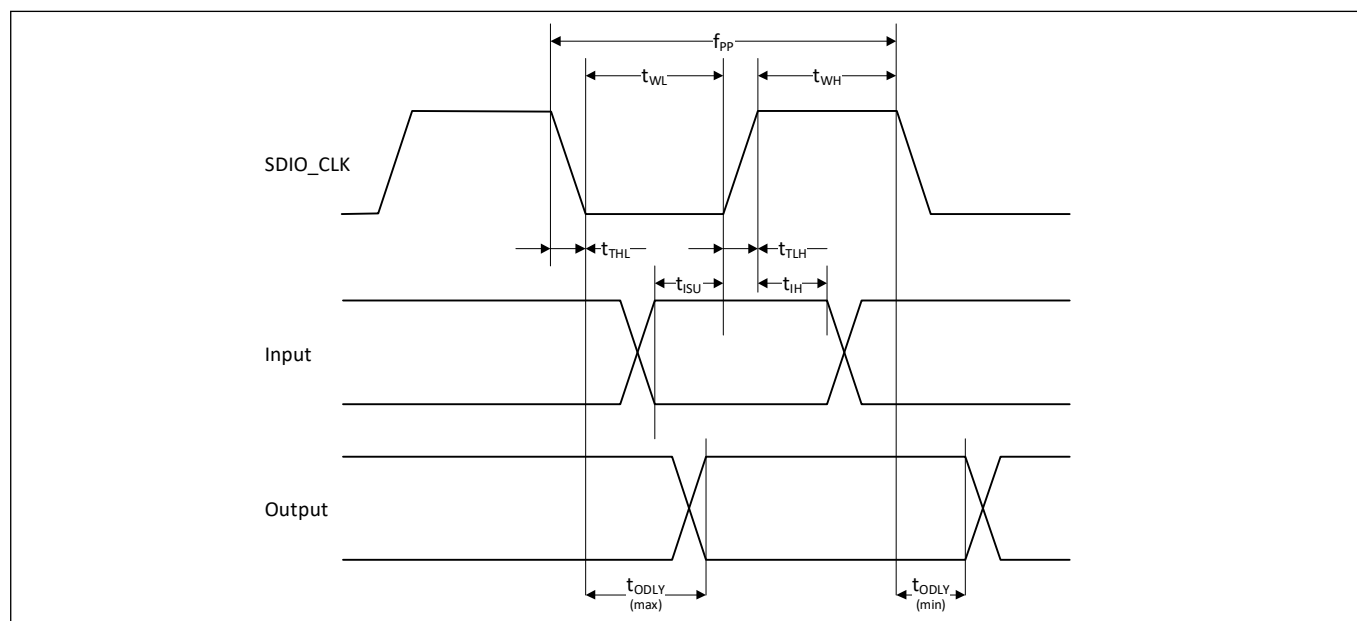


Figure 34 SDIO bus timing (Default mode)

Table 53 SDIO bus timing^[144] parameters (Default mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL^[145])					
Frequency – Data Transfer mode	f_{PP}	0	–	25.0	MHz
Frequency – Identification mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	10.0	–	–	ns
Clock high time	t_{WH}	10.0	–	–	ns
Clock rise time	t_{TLH}	–	–	10.0	ns
Clock low time	t_{THL}	–	–	10.0	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5.0	–	–	ns
Input hold time	t_{IH}	5.0	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	t_{ODLY}	0	–	14.0	ns
Output delay time – Identification mode	t_{ODLY}	0	–	50.0	ns

Notes

132. Timing is based on $CL \leq 40$ pF load on CMD and data.

133. Min (Vih) = $0.7 \times VDDIO$ and max (Vil) = $0.2 \times VDDIO$.

18.1.2 SDIO High-speed (HS) Mode timing

SDIO high-speed mode timing is shown by the combination of **Figure 35** and **Table 54**.

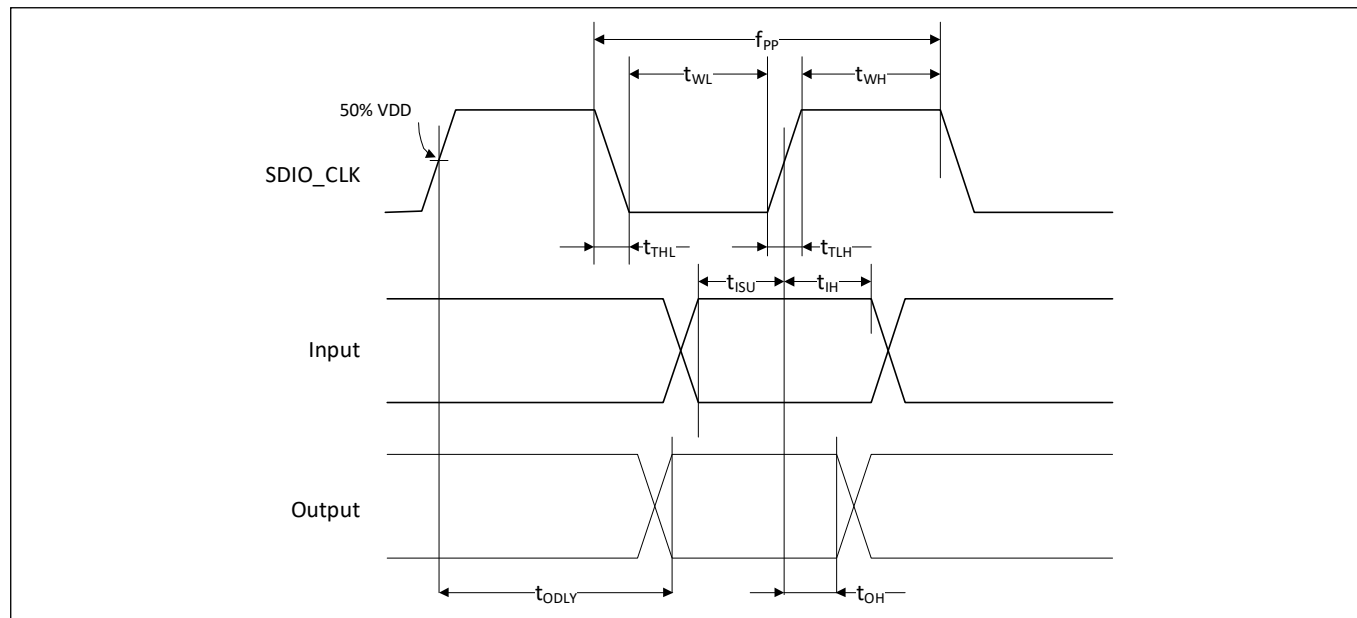


Figure 35 SDIO bus timing (HS mode)

Table 54 SDIO bus timing^[134] parameters (HS mode)

Parameter	Symbol	Min	Typ	Max	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL^[135])					
Frequency – Data Transfer Mode	f_{PP}	0	–	50	MHz
Frequency – Identification Mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	7.0	–	–	ns
Clock high time	t_{WH}	7.0	–	–	ns
Clock rise time	t_{TLH}	–	–	3.0	ns
Clock low time	t_{THL}	–	–	3.0	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	t_{ISU}	6.0	–	–	ns
Input hold Time	t_{IH}	2.0	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	t_{ODLY}	–	–	14.0	ns
Output hold time	t_{OH}	2.5.0	–	–	ns
Total system capacitance (each line)	CL	–	–	40.0	pF

Notes

134. Timing is based on $CL \leq 40$ pF load on CMD and data.

135. Min (Vih) = $0.7 \times VDDIO$ and max (Vil) = $0.2 \times VDDIO$.

18.1.3 SDIO bus timing specifications in SDR modes

18.1.3.1 Clock timing

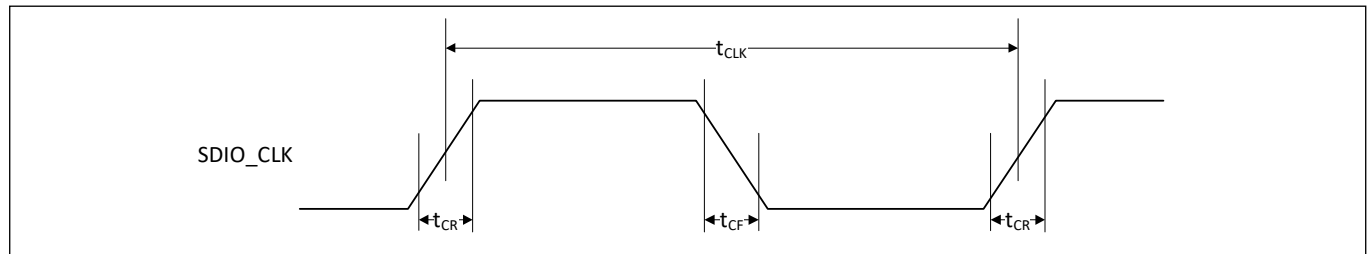


Figure 36 SDIO clock timing (SDR modes)

Table 55 SDIO bus clock timing parameters (SDR modes)

Parameter	Symbol	Min	Max	Unit	Comments
–	t_{CLK}	40.0	–	ns	SDR12 mode
		20.0	–	ns	SDR25 mode
		10.0	–	ns	SDR50 mode
		4.8	–	ns	SDR104 mode
–	t_{CR}, t_{CF}	–	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 2.00$ ns (max) @ 100 MHz, $C_{CARD} = 10$ pF $t_{CR}, t_{CF} < 0.96$ ns (max) @ 208 MHz, $C_{CARD} = 10$ pF
Clock duty	–	30.0	70.0	%	–

Interface timing and AC characteristics

18.1.3.2 Device input timing

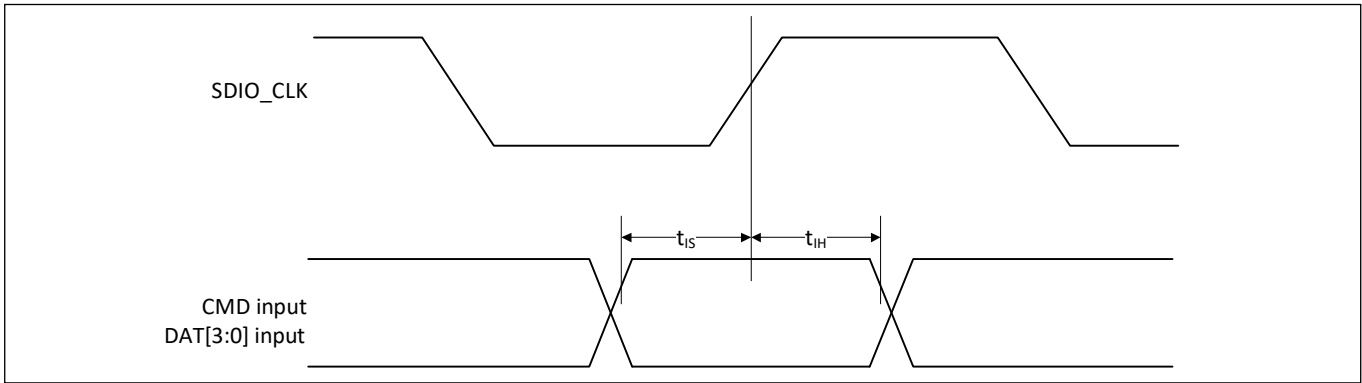
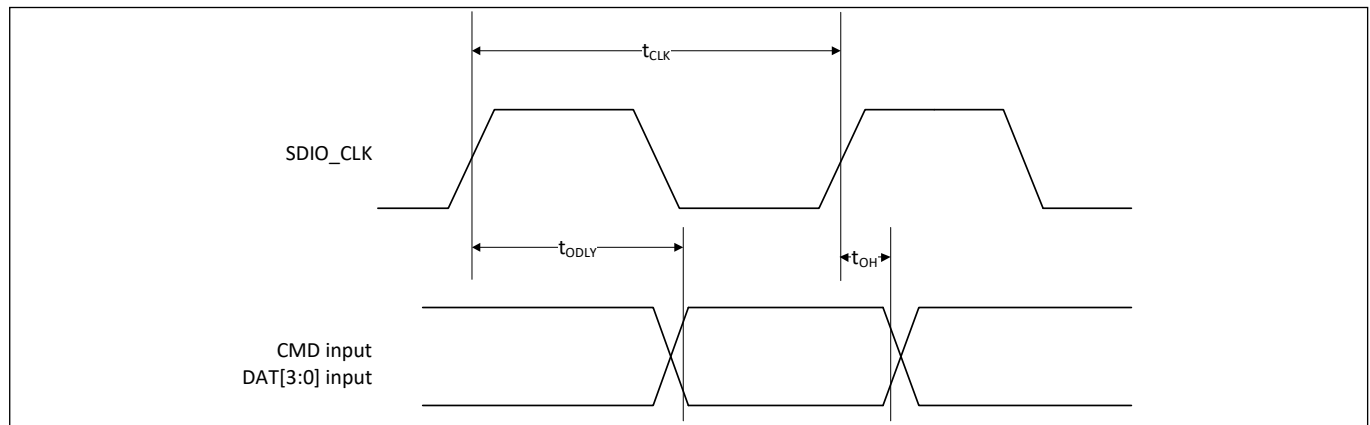


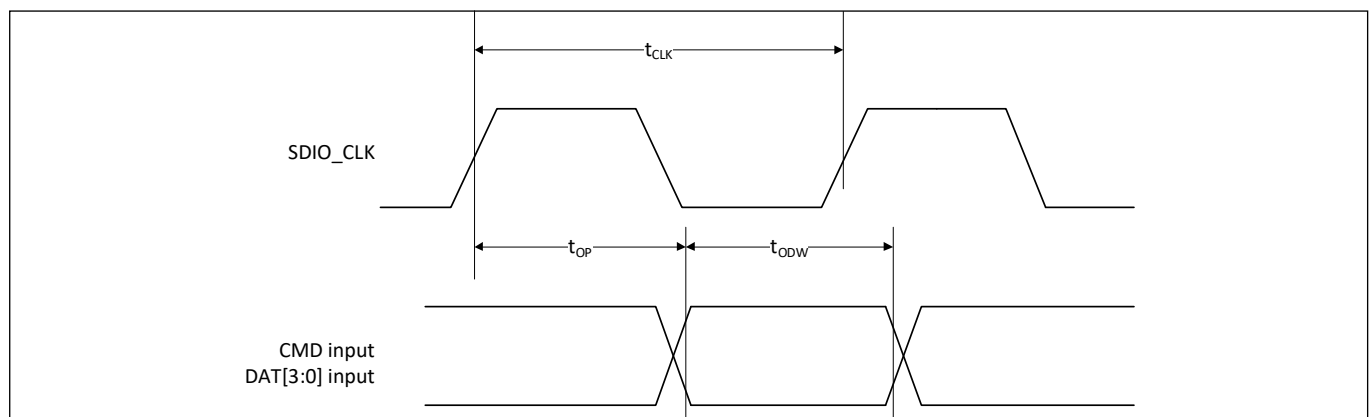
Figure 37 SDIO bus input timing (SDR modes)

Table 56 SDIO bus input timing parameters (SDR modes)

Symbol	Min	Max	Unit	Comments
SDR104 mode				
t_{IS}	1.4	–	ns	$C_{CARD} = 10 \text{ pF}$, $V_{CT} = 0.975 \text{ V}$
t_{IH}	0.80	–	ns	$C_{CARD} = 5 \text{ pF}$, $V_{CT} = 0.975 \text{ V}$
SDR50 mode				
t_{IS}	3.00	–	ns	$C_{CARD} = 10 \text{ pF}$, $V_{CT} = 0.975 \text{ V}$
t_{IH}	0.80	–	ns	$C_{CARD} = 5 \text{ pF}$, $V_{CT} = 0.975 \text{ V}$

Interface timing and AC characteristics
18.1.3.3 Device output timing

Figure 38 SDIO bus output timing (SDR modes up to 100 MHz)
Table 57 SDIO bus output timing parameters (SDR modes up to 100 MHz)

Symbol	Min	Max	Unit	Comments
t_{ODLY}	–	7.5	ns	$t_{CLK} \geq 10$ ns, $C_L = 30$ pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	$t_{CLK} \geq 20$ ns, $C_L = 40$ pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) $C_L = 15$ pF


Figure 39 SDIO bus output timing (SDR modes 100 MHz to 208 MHz)
Table 58 SDIO Bus Output Timing parameters (SDR Modes 100 MHz to 208 MHz)

Symbol	Min	Max	Unit	Comments
t_{OP}	0	2.0	UI	Card output phase
Δt_{OP}	–350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	–	UI	$t_{ODW} = 2.88$ ns @ 208 MHz

- $\Delta t_{OP} = +1550$ ps for junction temperature of $\Delta t_{OP} = 90$ degrees during operation
- $\Delta t_{OP} = -350$ ps for junction temperature of $\Delta t_{OP} = -20$ degrees during operation
- $\Delta t_{OP} = +2600$ ps for junction temperature of $\Delta t_{OP} = -20$ to $+125$ degrees during operation

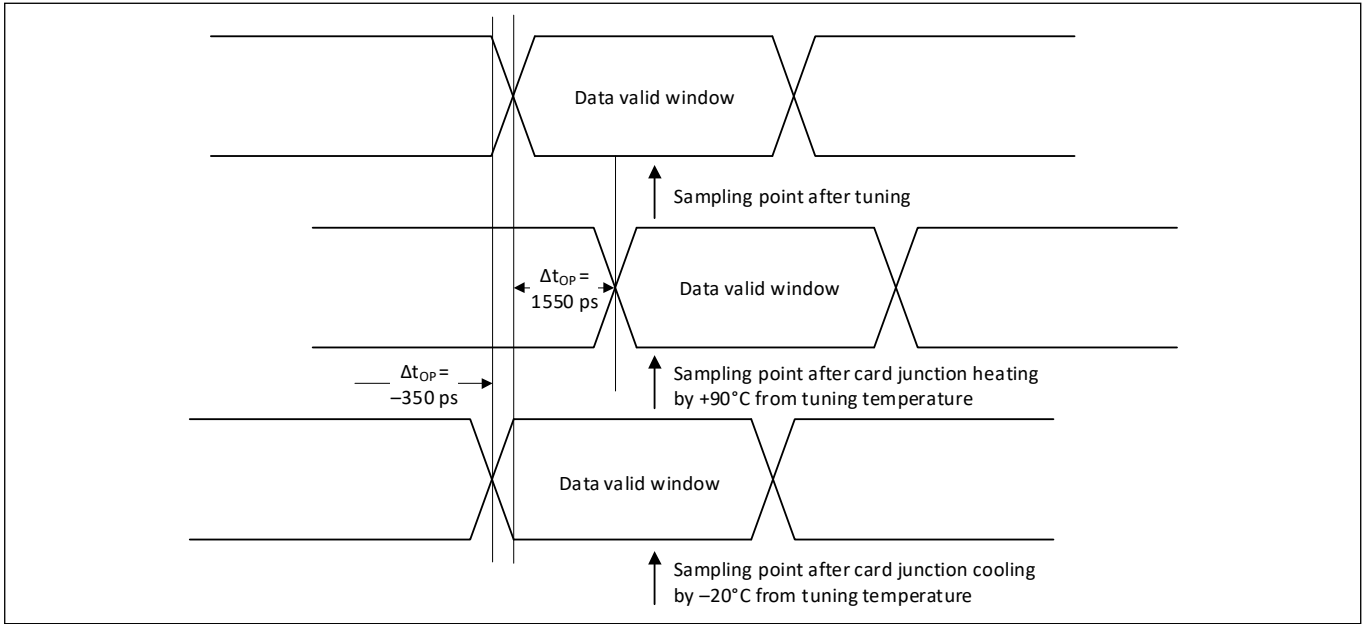


Figure 40 Δt_{OP} consideration for variable data window (SDR 104 mode)

18.1.4 SDIO bus timing specifications in DDR50 mode

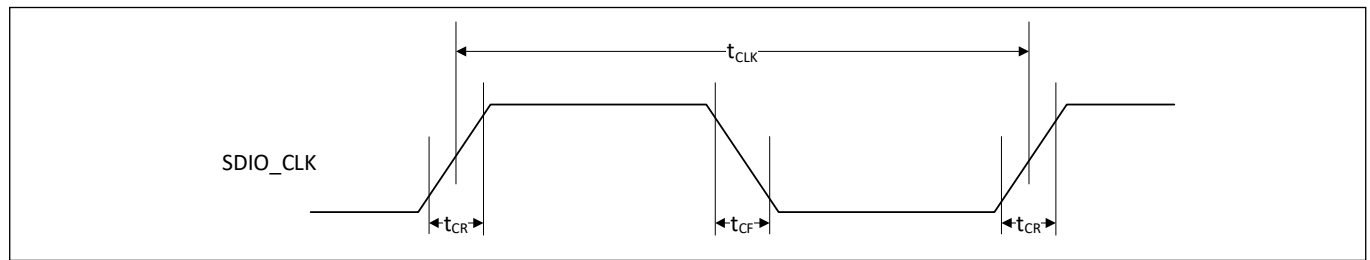


Figure 41 SDIO clock timing (DDR50 mode)

Table 59 SDIO bus clock timing parameters (DDR50 mode)

Parameter	Symbol	Min	Max	Unit	Comments
–	t_{CLK}	20.0	–	ns	DDR50 mode
–	t_{CR}, t_{CF}	–	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00$ ns (max) @ 50 MHz, $C_{CARD} = 10$ pF
Clock duty	–	45.0	55.0	%	–

18.1.4.1 Data timing, DDR50 mode

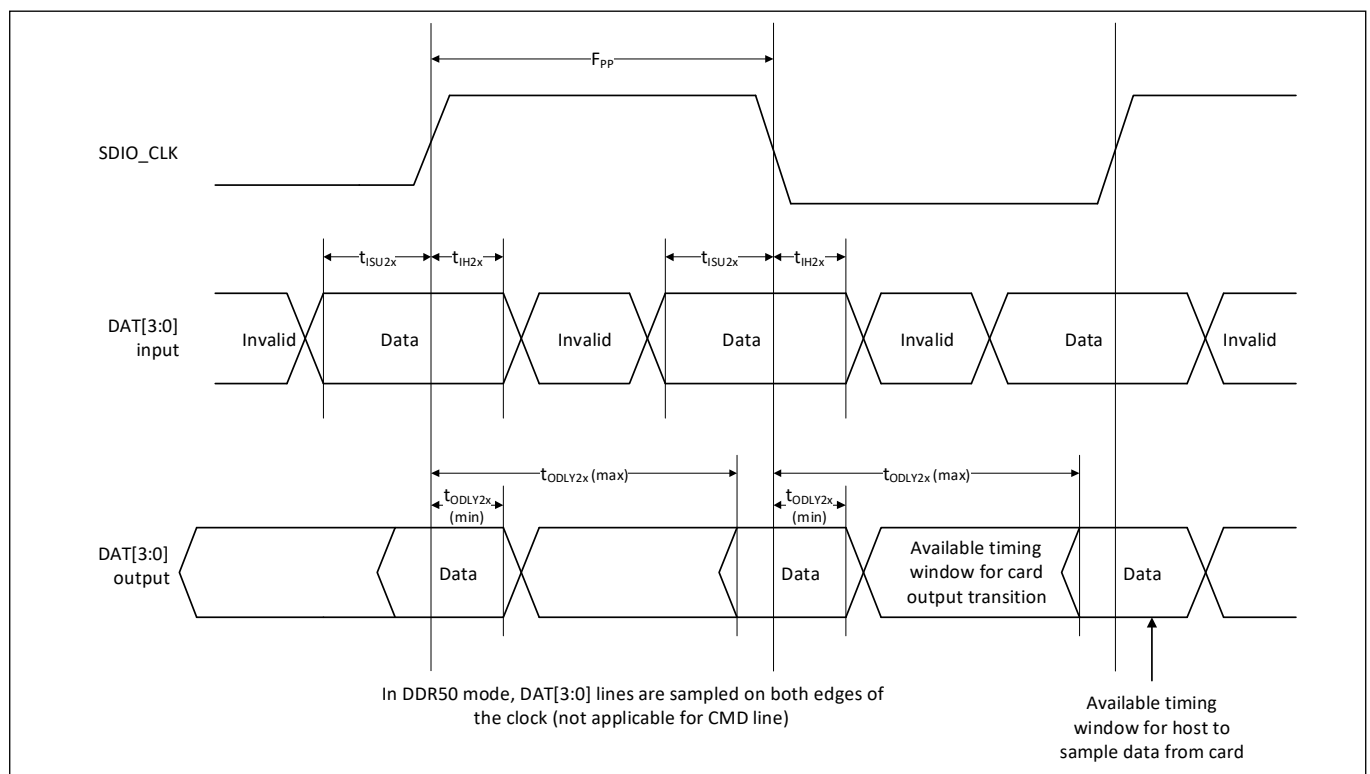


Figure 42 SDIO data timing (DDR50 mode)

Interface timing and AC characteristics
Table 60 SDIO bus timing parameters (DDR50 mode)

Parameter	Symbol	Min	Max	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6.0	–	ns	$C_{CARD} < 10 \text{ pF}$ (1 Card)
Input hold time	t_{IH}	0.8	–	ns	$C_{CARD} < 10 \text{ pF}$ (1 Card)
Output CMD					
Output delay time	t_{ODLY}	–	13.7	ns	$C_{CARD} < 30 \text{ pF}$ (1 Card)
Output hold time	t_{OH}	1.5	–	ns	$C_{CARD} < 15 \text{ pF}$ (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3.0	–	ns	$C_{CARD} < 10 \text{ pF}$ (1 Card)
Input hold time	t_{IH2x}	0.8	–	ns	$C_{CARD} < 10 \text{ pF}$ (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	–	7.5	ns	$C_{CARD} < 25 \text{ pF}$ (1 Card)
Output hold time	t_{ODLY2x}	1.5	–	ns	$C_{CARD} < 15 \text{ pF}$ (1 Card)

18.2 PCI express interface parameters
Table 61 PCI express interface parameters

Parameter	Symbol	Comments	Min	Typ	Max	Unit
General						
Baud rate	BPS	–	–	5	–	Gbaud
Reference clock peak-to-peak differential amplitude ^[136]	$V_{IH}^{[137]}$	Differential Input High Voltage	150	–	–	mV
	$V_{IL}^{[137]}$	Differential Input Low Voltage	–	–	–150	mV
	$V_{cross}^{[138, 139, 140]}$	Absolute crossing point Voltage	250	–	550	mV
Receiver						
Differential termination	ZRX-DIFF-DC	Differential termination	80.0	100	120	Ω
DC impedance	ZRX-DC	DC common-mode impedance	40.0	50.0	60	Ω
Powered down termination (POS)	ZRX-HIGH-IMP-DC-POS	Power-down or RESET high impedance	100k	–	–	Ω
Powered down termination (NEG)	ZRX-HIGH-IMP-DC-NEG	Power-down or RESET high impedance	1k	–	–	Ω
Input voltage	VRX-DIFFp-p	AC coupled, differential p-p	175	–	–	mV

Notes

136.The reference clock inputs comply with the requirements of PCI Express CEM v2.0.

137.Measurements taken from differential waveform.

138.Measurements taken from single ended waveform.

139.Measurements at crossing point where the instantaneous voltage value of the rising edge REFCLK+ equals the falling edge of REFCLK–.

140.Refers to the total variations from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for the requirements.

Interface timing and AC characteristics
Table 61 **PCI express interface parameters** *(continued)*

Parameter	Symbol	Comments	Min	Typ	Max	Unit
Jitter tolerance	TRX-EYE	Minimum receiver eye width	0.4	–	–	UI
Differential return loss	RLRX-DIFF	Differential return loss	10.0	–	–	dB
Common-mode return loss	RLRX-CM	Common-mode return loss	6	–	–	dB
Unexpected electrical idle enter detect threshold integration time	TRX-IDEL-DET-DIFF-ENTERTIME	An unexpected electrical idle must be recognized no longer than this time to signal an unexpected idle condition.	–	–	10.0	ms
Signal detect threshold	VRX-IDLE-DET-DIFFp-p	Electrical idle detect threshold	65.0	–	175	mV

Transmitter

Output voltage	VTX-DIFFp-p	Differential p-p, programmable in 16 steps	0.8	–	1200	mV
Output voltage rise time	VTX-RISE	20% to 80%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	–	–	UI
Output voltage fall time	VTX-FALL	80% to 20%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	–	–	UI
RX detection voltage swing	VTX-RCV-DETECT	The amount of voltage change allowed during receiver detection.	–	–	600	mV
TX AC peak common-mode voltage (5 GT/s)	VTX-CM-AC-PP	TX AC common mode voltage (5 GT/s)	–	–	100	mV
TX AC peak common-mode voltage (2.5 GT/s)	VTX-CM-AC-P	TX AC common mode voltage (2.5 GT/s)	–	–	20.0	mV
Absolute delta of DC common-model voltage during L0 and electrical idle	VTX-CM-DC-ACTIVE-IDLE-DELTA	Absolute delta of DC common-model voltage during L0 and electrical idle.	0	–	100	mV
Absolute delta of DC common-model voltage between D+ and D–	VTX-CM-DC-LINE-DELTA	DC offset between D+ and D–	0	–	25.0	mV

Notes

136.The reference clock inputs comply with the requirements of PCI Express CEM v2.0.

137.Measurements taken from differential waveform.

138.Measurements taken from single ended waveform.

139.Measurements at crossing point where the instantaneous voltage value of the rising edge REFCLK+ equals the falling edge of REFCLK–.

140.Refers to the total variations from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for the requirements.

Interface timing and AC characteristics
Table 61 PCI express interface parameters (continued)

Parameter	Symbol	Comments	Min	Typ	Max	Unit
Electrical idle differential peak output voltage	VTX-IDLE-DIFF-AC-p	Peak-to-peak voltage	0	–	20.0	mV
TX short circuit current	ITX-SHORT	Current limit when TX output is shorted to ground.	–	–	90.0	mA
DC differential TX termination	ZTX-DIFF-DC	Low impedance defined during signaling (parameter is captured for 5.0 GHz by RLTX-DIFF)	80.0	–	120	Ω
Differential return loss	RLTX-DIFF	Differential return loss	10 (min) for 0.05: 1.25 GHz	–	–	dB
Common-mode return loss	RLTX-CM	Common-mode return loss	6.0	–	–	dB
TX eye width	TTX-EYE	Minimum TX eye width	0.75	–	–	UI

Notes

136.The reference clock inputs comply with the requirements of PCI Express CEM v2.0.

137.Measurements taken from differential waveform.

138.Measurements taken from single ended waveform.

139.Measurements at crossing point where the instantaneous voltage value of the rising edge REFCLK+ equals the falling edge of REFCLK–.

140.Refers to the total variations from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for the requirements.

18.3 JTAG timing

Table 62 JTAG timing characteristics

Signal name	Period	Output maximum	Output minimum	Setup	Hold
TCK	125 ns	–	–	–	–
TDI	–	–	–	20 ns	0 ns
TMS	–	–	–	20 ns	0 ns
TDO	–	100 ns	0 ns	–	–
JTAG_TRST	250 ns	–	–	–	–

19 Power-up sequence and timing

19.1 Sequencing of reset and regulator control signals

CYW55571 has two signals that allow the host to control power consumption by enabling or disabling the Bluetooth®, WLAN, and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see [Figure 43](#), [Figure 44](#), [Figure 45](#), and [Figure 46](#)). The timing values indicated are minimum required values; longer delays are also acceptable.

19.1.1 Description of control signals

- **WL_REG_ON:** Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal CYW55571 regulators. When this pin is HIGH, the regulators are enabled and the WLAN section is out of reset. When this pin is LOW the WLAN section is in reset. If both the BT_REG_ON and WL_REG_ON pins are LOW, the regulators are disabled.
- **BT_REG_ON:** Used by the PMU (OR-gated with WL_REG_ON) to power up the internal CYW55571 regulators. If both the BT_REG_ON and WL_REG_ON pins are LOW, the regulators are disabled. When this pin is LOW and WL_REG_ON is HIGH, the Bluetooth® section is in reset.

Notes

- CYW55571 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after VDDC and VDDIO have both passed the POR threshold. Wait at least 51.5 ms after VDDC and VDDIO are available before initiating PCIe accesses.
- VBAT and VDDIO should not rise 10%–90% faster than 40 μ s.

19.1.2 Control signal timing diagrams

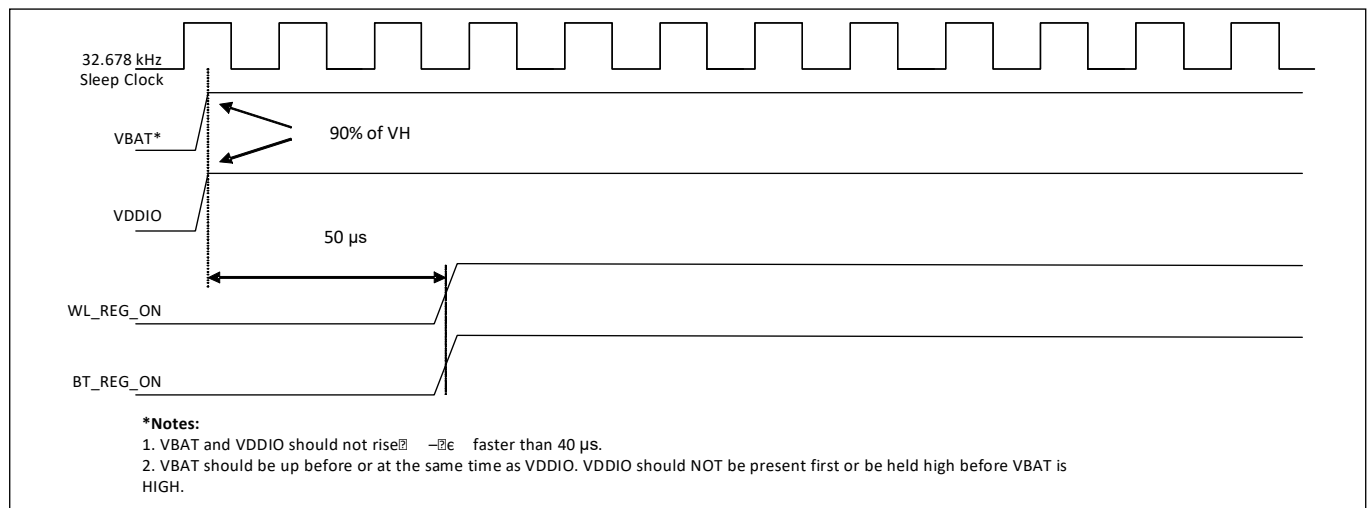


Figure 43 WLAN = ON, Bluetooth® = ON

Power-up sequence and timing

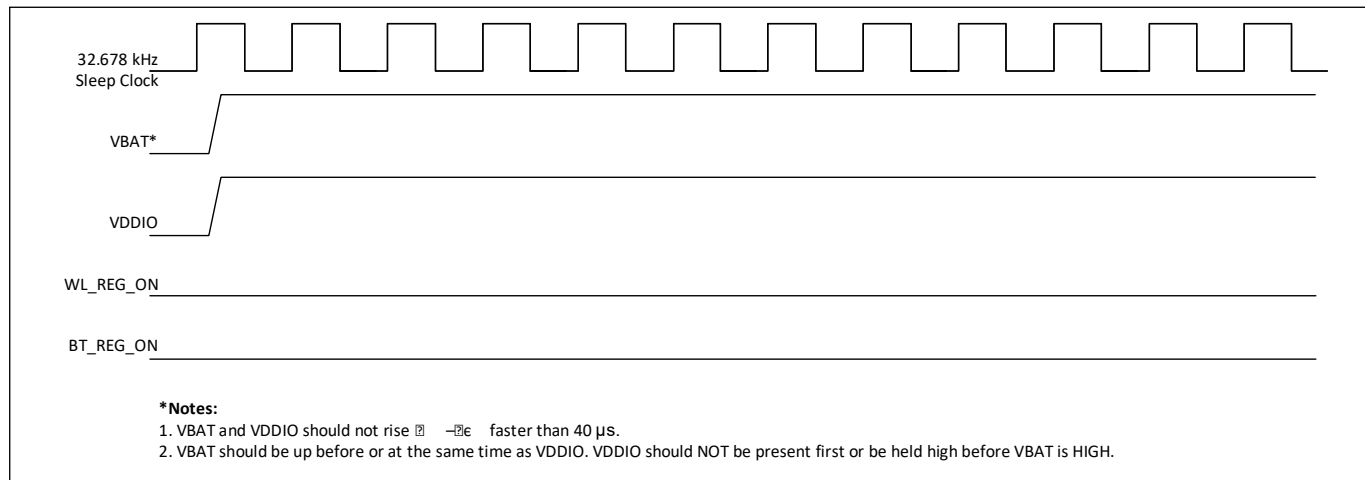


Figure 44 WLAN = OFF, Bluetooth® = OFF

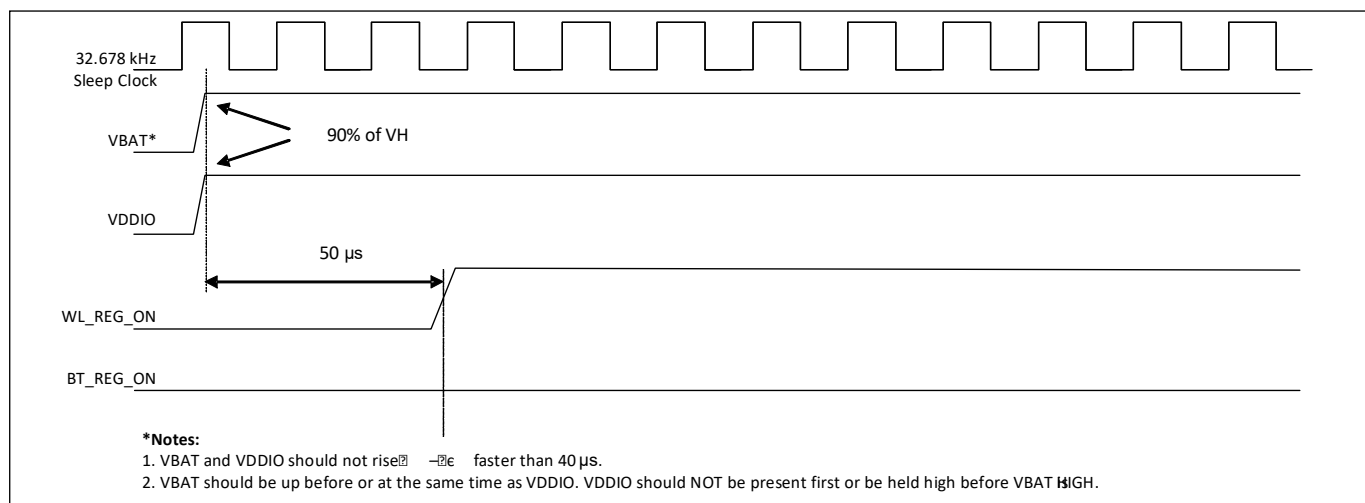


Figure 45 WLAN = ON, Bluetooth® = OFF

Power-up sequence and timing

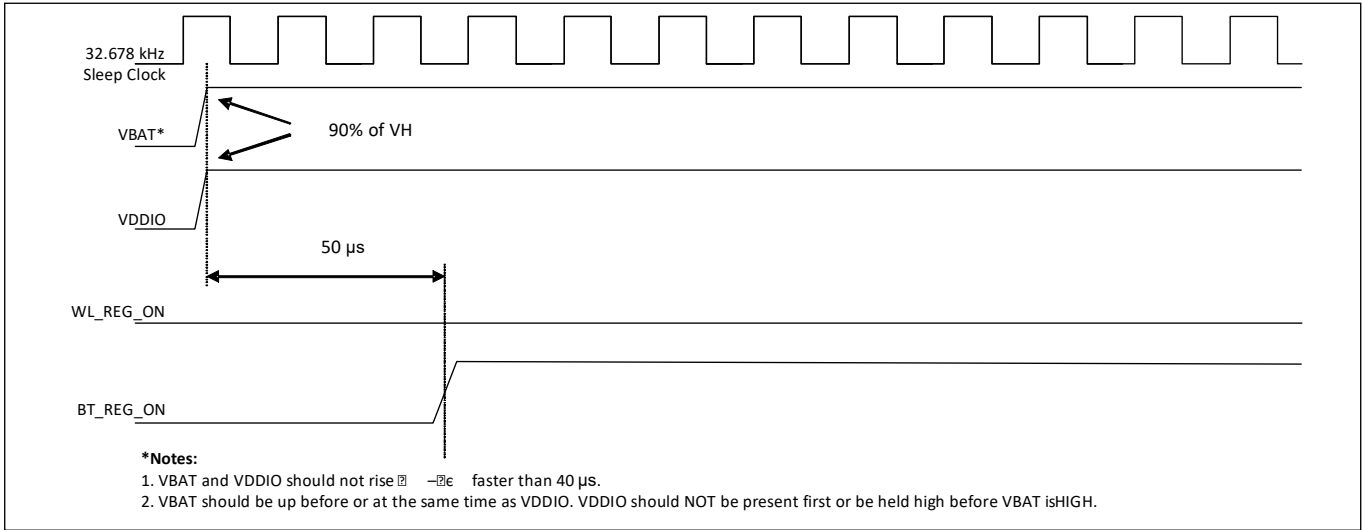


Figure 46 WLAN = OFF, Bluetooth® = ON

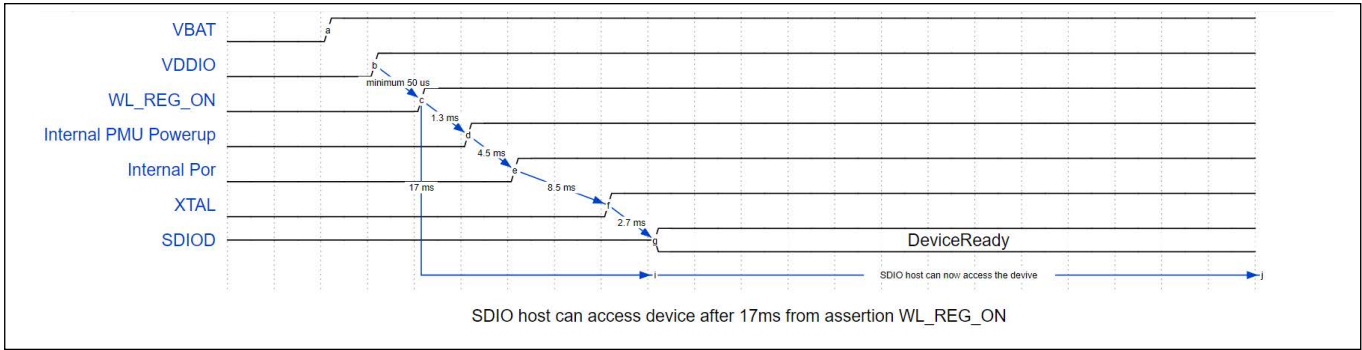


Figure 47 WLAN boot-up sequence for SDIO host

Figure 48 shows the WLAN boot-up sequence from power-up to firmware download.

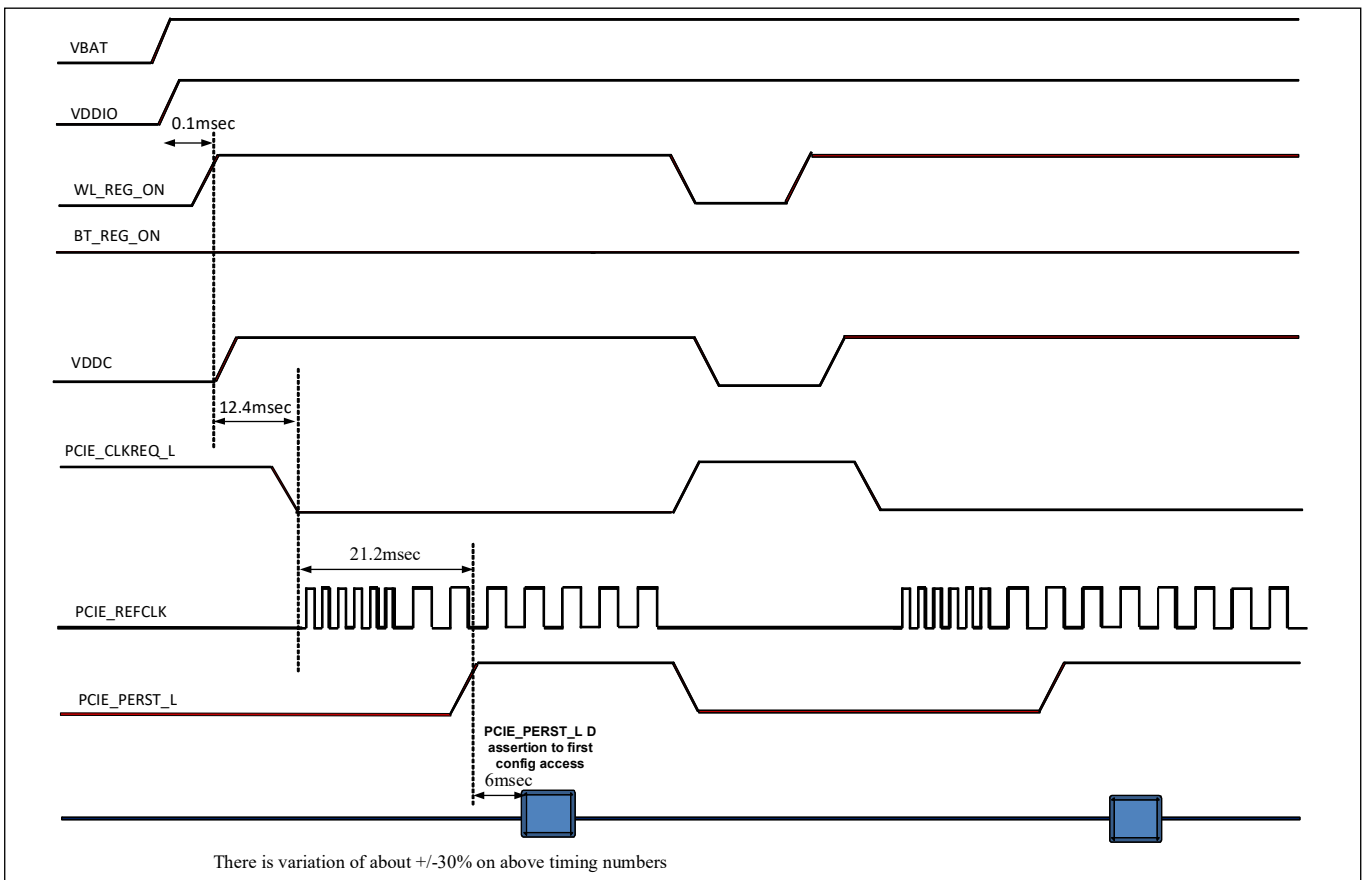


Figure 48 WLAN power-Up sequence for PCIe host

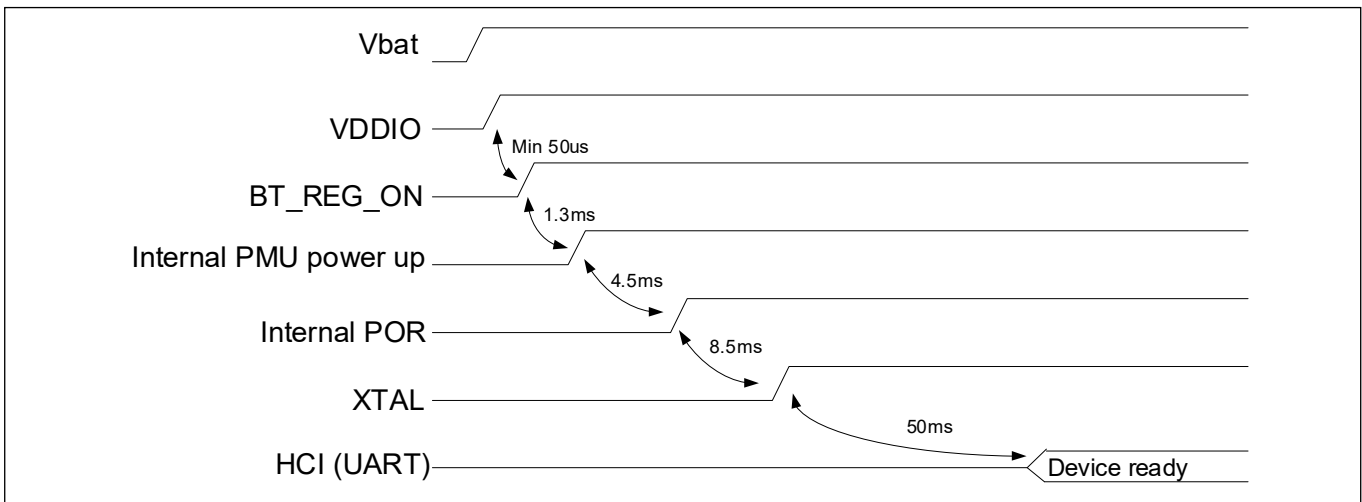


Figure 49 Bluetooth® boot-up for HCI

Package information

20 Package information

20.1 Package thermal characteristics

The information in [Table 63](#) and [Table 64](#) is based on the following conditions:

- Absolute junction temperature 125°C limit is maintained through active thermal monitoring, throttling, and turning off one of the TX chains or both.

Table 63 FCFBGA package thermal characteristics

Characteristic	FCFBGA
θ_{JA} (°C/W) (value in still air)	27.3
θ_{JB} (°C/W)	14.1
θ_{JC} (°C/W)	14.8
Ψ_{JT} (°C/W)	2.3
Ψ_{JB} (°C/W)	14.7
Maximum junction temperature T_j (°C)	123.22
Maximum power dissipation (W)	1.4

Table 64 WLBGA package thermal characteristics

Characteristic	WLBGA
θ_{JA} (°C/W) (value in still air)	15.5
θ_{JB} (°C/W)	14.1
θ_{JC} (°C/W)	14.8
Ψ_{JT} (°C/W)	2.3
Ψ_{JB} (°C/W)	14.7
Maximum junction temperature T_j (°C)	111
Maximum power Dissipation (W)	1.655

Table 65 WLCSP package thermal characteristics

Characteristic	WLCSP
θ_{JA} (°C/W)	20.1
θ_{JB} (°C/W)	15.1
θ_{JC} (°C/W)	15.8
Ψ_{JT} (°C/W)	2.3
Ψ_{JB} (°C/W)	14.7
Maximum junction temperature T_j (°C)	118.27
Maximum power dissipation (W)	1.655

20.2 Junction temperature estimation and Ψ_{JT} versus Θ_{JC}

The package thermal characterization parameter Ψ_{JT} (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) than using the junction-to-case thermal resistance parameter Θ_{JC} (Θ_{JC}). The reason for this is that Θ_{JC} is based on the assumption that all the power is dissipated through the top surface of the package case. In actual applications, however, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account the power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is:

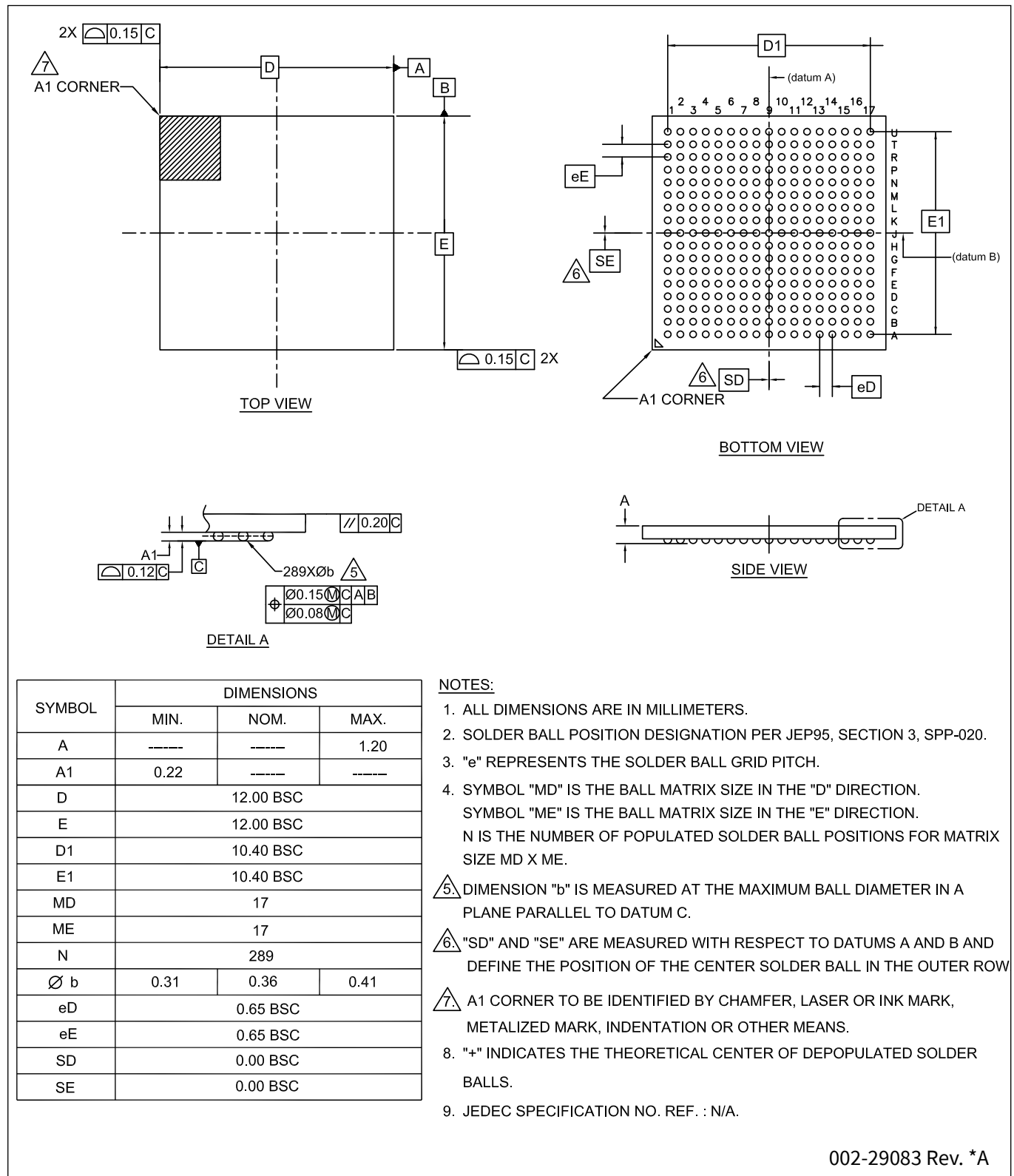
$$T_J = T_T + P \times \Psi_{JT}$$

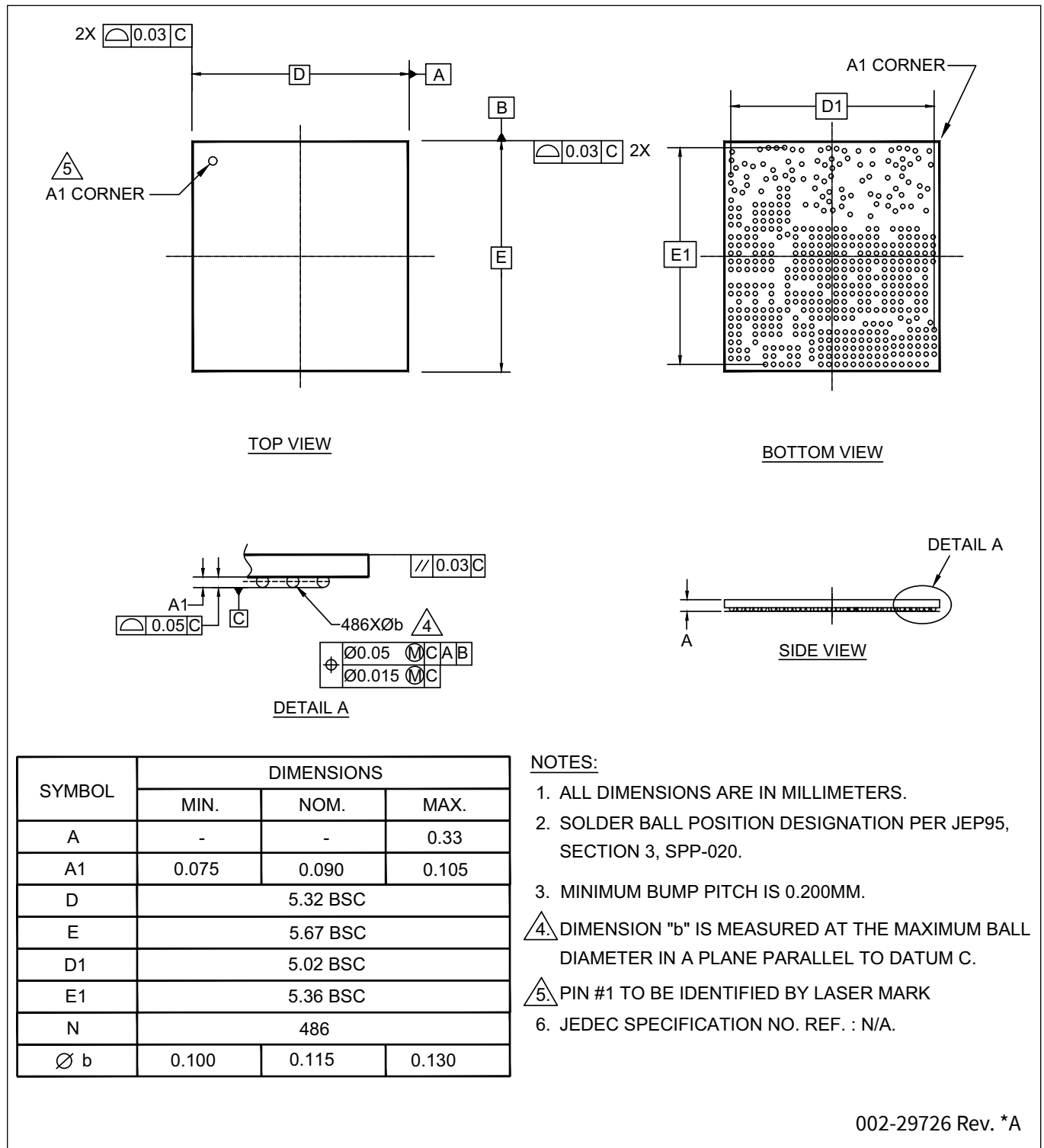
Where:

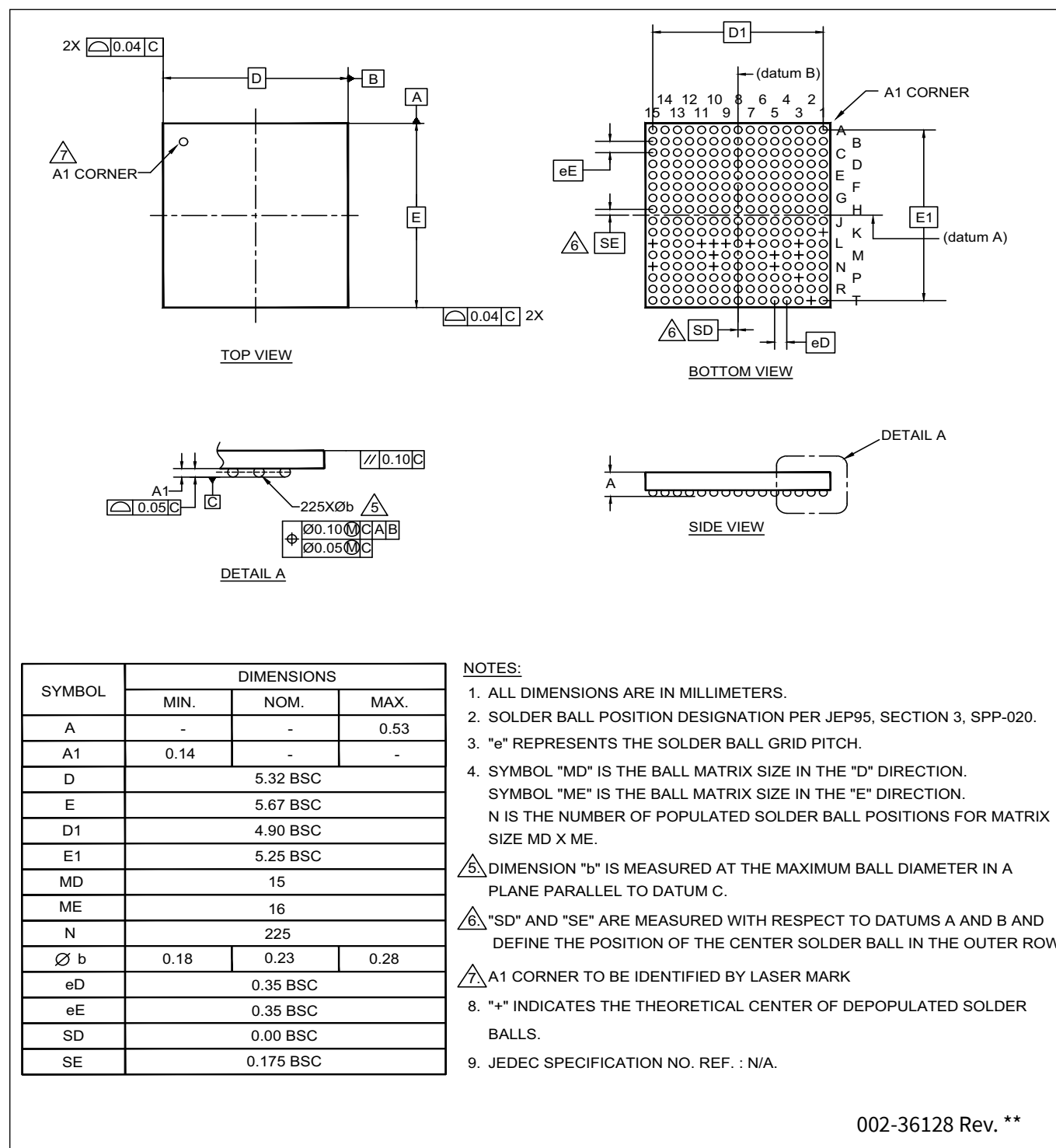
- T_J = Junction temperature at steady-state condition (°C)
- T_T = Package case top center temperature at steady-state condition (°C)
- P = Device power dissipation (Watts)
- Ψ_{JT} = Package thermal characteristics; no airflow (°C/W)

20.3 Environmental characteristics

For environmental characteristics data, see [Table 25](#).

Package information
20.4 Package diagrams

Figure 50 289-ball FCFBGA (12 × 12 × 1.20 mm) FR0BJ/FZA289 package outline (PG-TF2BGA-289)

Package information

Figure 51 486-ball WLCSP (5.32 × 5.67 × 0.33 mm) FL0DA package outline (SG-XFWLB-486)

Package information


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Figure 52 225-ball WLBGA (5.32 × 5.67 × 0.53 mm) FN0BE package outline

Package information

20.5 Tape, Reel, and Packing specification

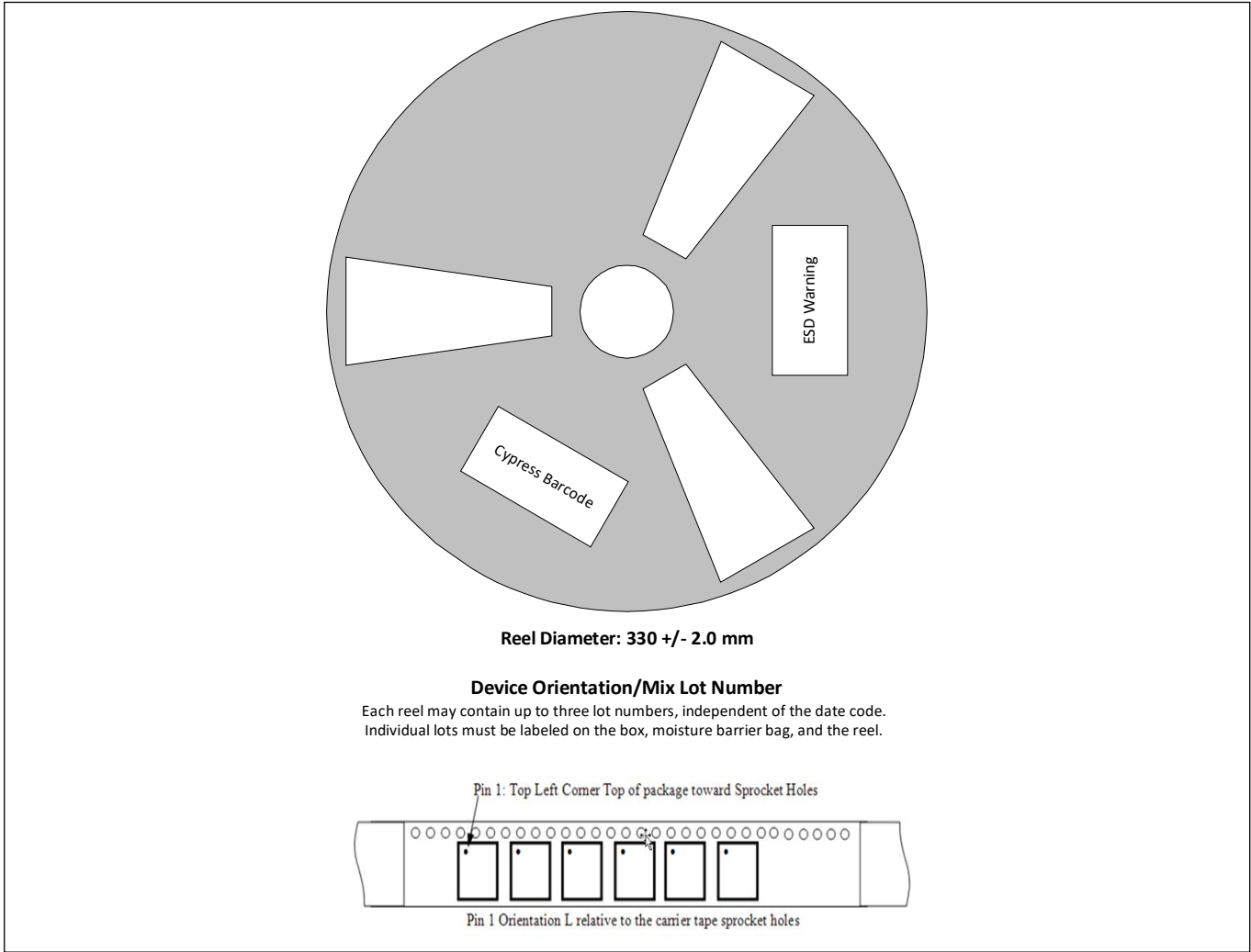


Figure 53 Reel, labeling, and packaging

21 Ordering information

Table 66 Ordering Information

Product	Package	Description	Operating ambient temperature
CYW55571MIWBGT	486-ball WLCSP (5.3 mm × 5.7 mm, 0.2 mm pitch)	Tri-band WLAN 2.4/5/6 GHz 802.11ax 1 × 1 Bluetooth® 5.3 tape and reel	–40°C to +85°C
CYW55571MIFFBGT	289-ball FCFBGA (12 mm × 12 mm, 0.65 mm pitch)	Tri-band WLAN 2.4/5/6 GHz 802.11ax 1 × 1 Bluetooth® 5.3 tape and reel	
CYW55571MIUBGT	225-ball WLBGA (5.32 mm × 5.67 mm, 0.35 mm pitch)	Tri-band WLAN 2.4/5/6GHz 802.11ax 1 × 1, Bluetooth® 5.3 tape and reel	

22 Additional information

22.1 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined upon first use. For a more complete list of acronyms and other terms used in Infineon documents, go to [Infineon at a glance](#).

Table 67 Acronyms used in this document

Term	Description
AES	Advanced Encryption Standard
AES-CTR	Advanced Encryption Standard-Counter Mode
ALU	Arithmetic logic unit
APB	advanced peripheral bus
APU	audio processing unit
CBC-MAC	Cipher Block Chaining Message Authentication Code
CCK	Complementary Code Keying
CCM	Counter with Cipher block chaining Message authentication code
CSC	Cypress Serial Control
CTS	Clear to Send
DMA	direct memory access
DSSS	Direct Sequence Spread Spectrum
DTE	Data Termination Equipment
EIR	Extended inquiry response
EPR	Encryption pause resume
ESR	Equivalent Series Resistance
eSCO	Extended synchronous connections
FEM	Front-End Module
FFT	Fast Fourier Transform
HCI	Host Control Interface
IRQ	interrupt request
JTAG	Joint Test Action Group
LCU	link control unit
LDO	low drop-out
LST	Link supervision timeout
LTE	Long Term Evolution
MIB	Management Information Base
MIC	Message Integrity Check
MSB	most significant bit
OFDM	orthogonal frequency division multiplexing
PDM	pulse density modulation
PLL	phase locked loop
POR	power-on reset
RTS	Request to Send
RX/TX	receive, transmit

Additional information

Table 67 **Acronyms used in this document** *(continued)*

Term	Description
SPI	serial peripheral interface
SP3T	Single Pole 3 Throw
SSP	Secure simple pairing
SSR	Sniff subrating
SWD	serial wire debug
TXOP	Transmit Opportunity
UART	universal asynchronous receiver/transmitter
WD	watchdog
WPA	Wi-Fi Protected Access
QoS	Quality of Service

23 References

The references in this section may be used in conjunction with this document.

Note Infineon provides customer access to technical documentation and software through its Customer Support Portal (CSP) and Downloads & Support site (see [IoT resources](#)).

For Infineon documents, replace the “xx” in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Table 68 **References**

Document (or Item) name	Number	Source
Bluetooth® MWS Coexistence 2-wire Transport Interface specification	–	Bluetooth®

23.1 IoT resources

Infineon provides a wealth of data at [Embedded security for the Internet of Things \(IoT\)](#) to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Infineon provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the [Infineon Developer Community](#).

Revision history
Revision history

Document revision	Date	Description of changes
*B	2023-03-23	Changed status from Preliminary to Final.
*C	2023-06-09	Migrated to Infineon template.
*D	2023-09-12	Updated Security related changes (TKIP WEP removal). Updated Bluetooth® TX 20 in Table 52 . Updated General features in Features - 4, 6 layer PCB design detail.
*E	2024-05-10	Updated the Table 31 , Table 33 , Table 34 , Table 35 , Table 36 , Table 37 , Table 38 , Table 49 and Table 50 . Updated the internal pull down resistor to 50 kΩ in Table 2 . Updated “One-time programmable memory (OTP)” on page 39. Update unit “v” in Table 23 . Removed footnotes from Table 30 through Table 32 . Updated the typical value and footnote for nominal output in Table 44 through Table 46 . Updated “Description of control signals” on page 119. Removed the Part number “CYW5571MIFFBG” from “Ordering information” on page 186. Added IFX package code for Figure 50 and Figure 51 .
*F	2025-10-31	Updated Table 49 and Table 50 . Updated Disclaimer.

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