# CIPOS™ Maxi IM818

## IM818-SCC

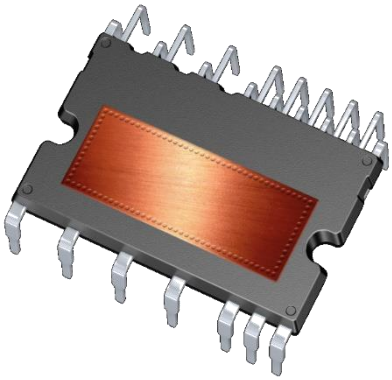
## Description

The CIPOS™ Maxi IM818 product group offers the chance for integrating various power and control components to increase reliability, optimize PCB size and system costs. It is designed to control three phase AC motors and permanent magnet motors in variable speed drives applications such as low power motor drives (GPI, Servo drives), pumps, fan drives and active filter for HVAC (Heating, Ventilation, and Air Conditioning). The product concept is specially adapted to power applications, which need good thermal performance and electrical isolation as well as EMI save control and overload protection.
Three phase inverter with 1200V TRENCHSTOP™ IGBTs and Emitter Controlled diodes are combined with an optimized 6-channel SOI gate driver for excellent electrical performance.

## Features

- Fully isolated Dual In-Line molded module
- 1200V TRENCHSTOP™ IGBT4
- Rugged 1200V SOI gate driver technology with stability against transient and negative voltage
- Allowable negative VS potential up to -11 V for signal transmission at VBS = 15 V
- Integrated bootstrap functionality
- Over current shutdown
- Built-in NTC thermistor for temperature monitor
- Under-voltage lockout at all channels
- Low side emitter pins accessible for phase current monitoring (open emitter)
- Anti cross-conduction
- All of 6 switches turn off during protection
- Programmable fault clear timing and enable input
- Lead-free terminal plating; RoHS compliant



## Potential applications

Fan drives and active filter for HVAC, pumps, and low power motor drives (GPI, Servo Drives)

## Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

**Table 1 Product Information**

| Product Name | Package Type | Standard Pack | | Remark |
|---|---|---|---|---|
| | | Form | MOQ | |
| IM818-SCC | DIP 36x23D | 14 pcs / tube | 280 | |

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# 1 Internal Electrical Schematic

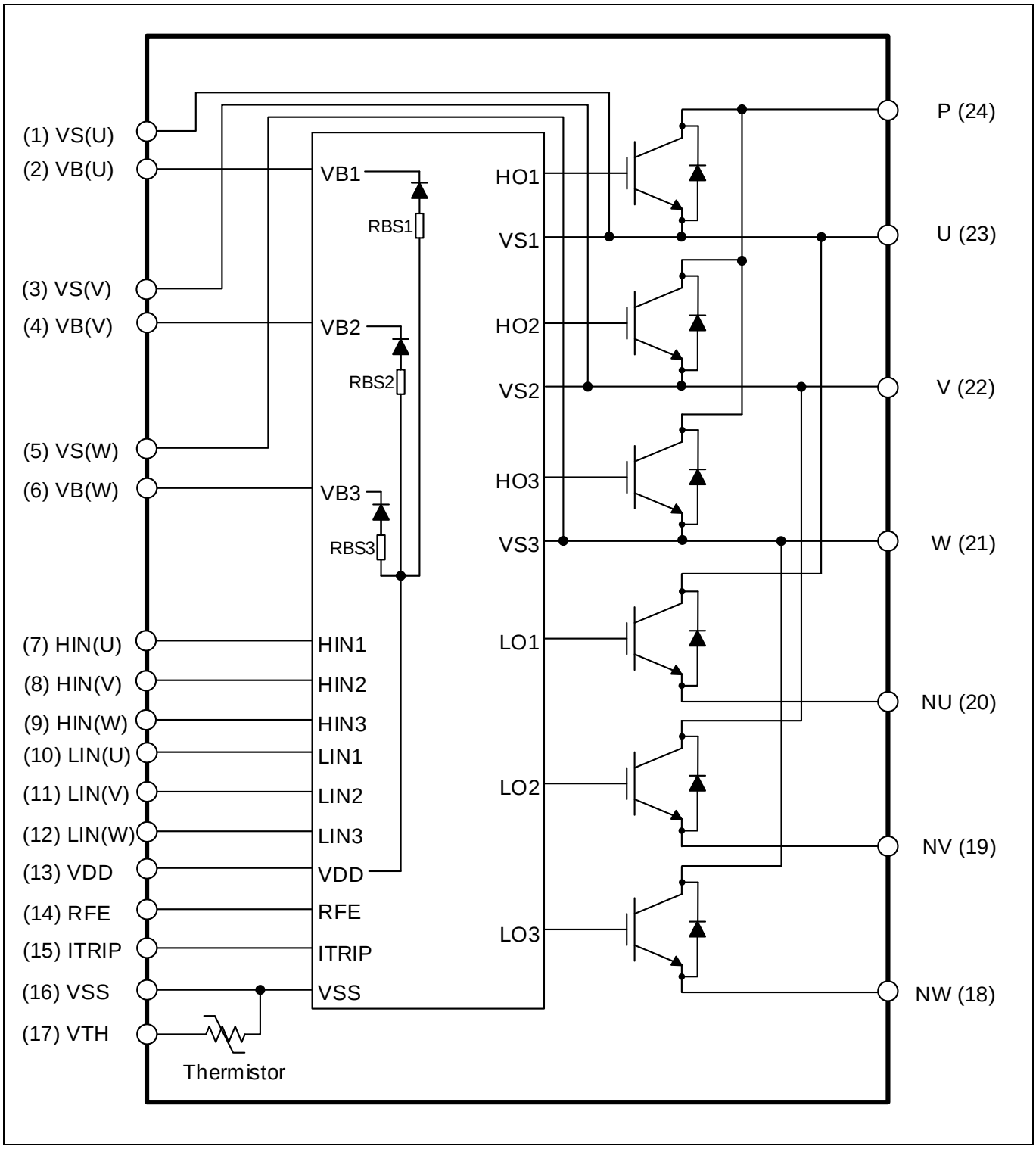



**Figure 1 Internal electrical schematic**

# 2 Pin Configuration

## 2.1 Pin Assignment

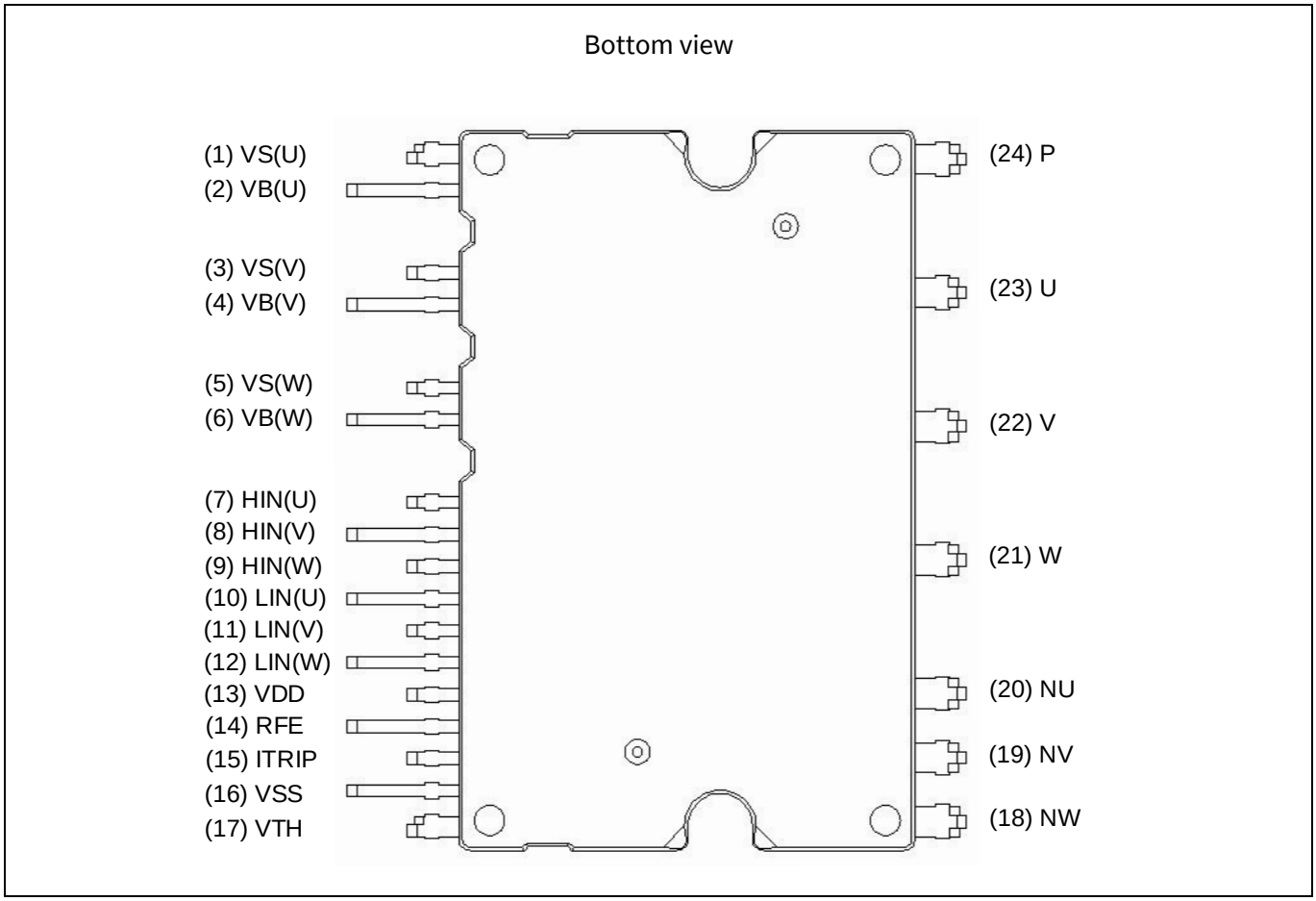



**Figure 2 Module pinout**

**Table 2 Pin Assignment**

| Pin Number | Pin name | Pin Description |
|---|---|---|
| 1 | VS(U) | U-phase high side floating IC supply offset voltage |
| 2 | VB(U) | U-phase high side floating IC supply voltage |
| 3 | VS(V) | V-phase high side floating IC supply offset voltage |
| 4 | VB(V) | V-phase high side floating IC supply voltage |
| 5 | VS(W) | W-phase high side floating IC supply offset voltage |
| 6 | VB(W) | W-phase high side floating IC supply voltage |
| 7 | HIN(U) | U-phase high side gate driver input |
| 8 | HIN(V) | V-phase high side gate driver input |
| 9 | HIN(W) | W-phase high side gate driver input |
| 10 | LIN(U) | U-phase low side gate driver input |
| 11 | LIN(V) | V-phase low side gate driver input |
| 12 | LIN(W) | W-phase low side gate driver input |
| 13 | VDD | Low side control supply |

**Pin Configuration**

| Pin Number | Pin name | Pin Description |
|---|---|---|
| 14 | RFE | Programmable fault clear time, fault output, enable input |
| 15 | ITRIP | Over current shutdown input |
| 16 | VSS | Low side control negative supply |
| 17 | VTH | Thermistor |
| 18 | NW | W-phase low side emitter |
| 19 | NV | V-phase low side emitter |
| 20 | NU | U-phase low side emitter |
| 21 | W | Motor W-phase output |
| 22 | V | Motor V-phase output |
| 23 | U | Motor U-phase output |
| 24 | P | Positive bus input voltage |

## 2.2 Pin Description

**HIN (U, V, W) and LIN (U, V, W) (Low side and high side control pins, Pin 7 - 12)**

These pins are positive logic and they are responsible for the control of the integrated IGBTs. The schmitt-trigger input thresholds of them are such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. Pull-down resistor of about 5 kΩ is internally provided to pre-bias inputs during supply start-up. Input schmitt-trigger and noise filter provide beneficial noise rejection to short input pulses.

The noise filter suppresses control pulses which are below the filter time $t_{FIL,IN}$. The filter acts according to Figure 4.

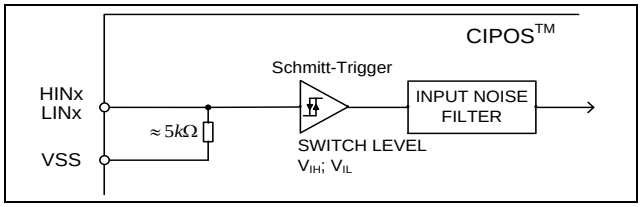



**Figure 3 Input pin structure**

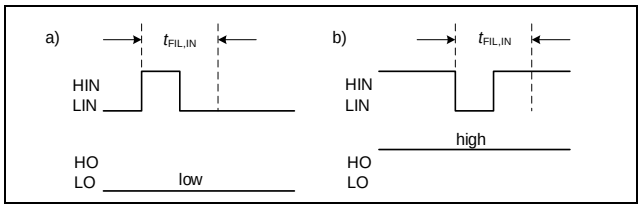



**Figure 4 Input filter timing diagram**

It is not recommended for proper work to provide input pulse-width lower than 1 µs.

The integrated gate driver provides additionally a shoot through prevention capability which avoids the simultaneous on-state of two gate drivers of the same leg (i.e. HO1 and LO1, HO2 and LO2, HO3 and LO3). When two inputs of a same leg are activated, only former activated one is activated so that the leg is kept steadily in a safe state.

A minimum deadtime insertion of typically 360 ns is also provided by driver IC, in order to reduce cross-conduction of the external power switches.

**RFE (Fault / Fault clear time / Enable, Pin 14)**

The RFE pin conbines three functions in one pin: programmable fault clear time by RC-network, fault-out and enable input.

The programmable fault-clear time can be adjusted by RC network, which is external pull-up resistor and capacitor. For example, typical value is about 1ms at 1 MΩ and 2 nF.

The fault-out indicates a module failure in case of under voltage at pin VDD or in case of triggered over current detection at ITRIP.

The microcontroller can pull this pin low to disable the IPM functionality. This is enable function.

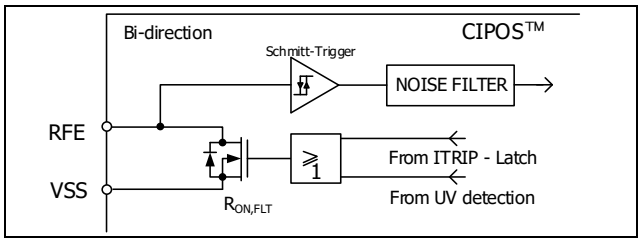



**Figure 5 Internal circuit at pin RFE**

### VTH (Thermistor, Pin 17)

The VTH pin provides direct access to the NTC, which is referenced to VSS. An external pull-up resistor connected to +5 V ensures that the resulting voltage can be directly connected to the microcontroller.

### ITRIP (Over current detection function, Pin 15)

IM818 provides an over current detection function by connecting the ITRIP input with the IGBT collector current feedback. The ITRIP comparator threshold (typ. 0.5 V) is referenced to VSS ground. An input noise filter ($t_{ITRIPMIN}$ = typ. 500 ns) prevents the driver to detect false over-current events.

Over current detection generates a shutdown of all outputs of the gate driver after the shutdown propagation delay of typically 1 µs.

Fault-clear time is set to typical 1.1 ms at $R_{RCIN}$ = 1 MΩ and $C_{RCIN}$ = 2 nF.

### VDD, VSS (Low side control supply and reference, Pin 13, 16)

VDD is the control supply and it provides power both to input logic and to output power stage. Input logic is referenced to VSS ground.

The under-voltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of $V_{DDUV+}$ = 12.2 V is present.

The IC shuts down all the gate drivers power outputs, when the VDD supply voltage is below $V_{DDUV-}$ = 11.2 V. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

### VB (U, V, W) and VS (U, V, W) (High side supplies, Pin 1 - 6)

VB to VS is the high side supply voltage. The high side circuit can float with respect to VSS following the external high side power device emitter voltage.

Due to the low power consumption, the floating driver stage is supplied by integrated bootstrap circuit.

The under-voltage detection operates with a rising supply threshold of typical $V_{BSUV+}$ = 11.2 V and a falling threshold of $V_{BSUV-}$ = 10.2 V.

VS (U, V, W) provide a high robustness against negative voltage in respect of VSS of -50 V transiently. This ensures very stable designs even under rough conditions.

### NW, NV, NU (Low side emitter, Pin 18 - 20)

The low side emitters are available for current measurements of each phase leg. It is recommended to keep the connection to pin VSS as short as possible in order to avoid unnecessary inductive voltage drops.

### W, V, U (High side emitter and low side collector, Pin 21 - 23)

These pins are motor U, V, W input pins.

### P (Positive bus input voltage, Pin 24)

The high side IGBTs are connected to the bus voltage. It is noted that the bus voltage does not exceed 900 V.

# 3 Absolute Maximum Ratings

($V_{DD}$ = 15 V and $T_J$ = 25°C, if not stated otherwise)

## 3.1 Module Section

| Description | Symbol | Condition | Value | Unit |
|---|---|---|---|---|
| Storage temperature range | $T_{STG}$ | | -40 ~ 125 | °C |
| Operating case temperature | $T_C$ | Refer to Figure 6 | -40 ~ 125 | °C |
| Operating junction temperature | $T_J$ | | -40 ~ 150 | °C |
| Isolation test voltage | $V_{ISO}$ | 1 min, RMS, f = 60 Hz | 2500 | V |

## 3.2 Inverter Section

| Description | Symbol | Condition | Value | Unit |
|---|---|---|---|---|
| Max. blocking voltage | $V_{CES}/V_{RRM}$ | | 1200 | V |
| DC link supply voltage of P-N | $V_{PN}$ | Applied between P-N | 900 | V |
| DC link supply voltage (surge) of P-N | $V_{PN(surge)}$ | Applied between P-N | 1000 | V |
| DC collector current | $I_C$ | $T_C$ = 25°C, $T_J$ < 150°C | ±8 | A |
| | | $T_C$ = 80°C, $T_J$ < 150°C | ±5 | |
| Peak collector current | $I_{CP}$ | $T_C$ = 25°C, $t_p$ < 1 ms | ±10 | A |
| Power dissipation per IGBT | $P_{tot}$ | | 49.6 | W |
| Short circuit withstand time[1] | $t_{SC}$ | $V_{DC}$ ≤ 800 V, $T_J$ = 150°C | 10 | µs |

## 3.3 Control Section

| Description | Symbol | Condition | Value | Unit |
|---|---|---|---|---|
| High side offset voltage | VS | | 1200 | V |
| Repetitive peak reverse voltage of bootstrap diode | $V_{RRM}$ | | 1200 | V |
| Module control supply voltage | $V_{DD}$ | | -1 ~ 20 | V |
| High side floating supply voltage ($V_B$ reference to $V_S$) | $V_{BS}$ | | -1 ~ 20 | V |
| Input voltage (LIN, HIN, ITRIP, RFE) | $V_{IN}$ | | -1 ~ $V_{DD}$ + 0.3 | V |

[1] Allowed number of short circuits: <1000; time between short circuits: >1s.

# 4 Thermal Characteirstics

| Description | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Single IGBT thermal resistance, junction-case | $R_{thJC}$ | High side V-phase IGBT | - | - | 2.52 | K/W |
| Single diode thermal resistance, junction-case | $R_{thJC,D}$ | High side V-phase diode | - | - | 3.60 | K/W |

# 5 Recommended Operation Conditions

All voltages are absolute voltages referenced to $V_{SS}$ -potential unless otherwise specified.

| Description | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| DC link supply voltage of P-N | $V_{PN}$ | 350 | 600 | 800 | V |
| Low side supply voltage | $V_{DD}$ | 13.5 | 15 | 18.5 | V |
| High side floating supply voltage ($V_B$ vs. $V_S$) | $V_{BS}$ | 12.5 | - | 18.5 | V |
| Logic input voltages LIN, HIN, ITRIP, RFE | $V_{IN}$ | 0 | - | 5 | V |
| PWM carrier frequency | $F_{PWM}$ | - | - | 20 | kHz |
| External dead time between HIN & LIN | DT | 0.5 | - | - | µs |
| Voltage between VSS - N (including surge) | $V_{COMP}$ | -5 | - | 5 | V |
| Minimum input pulse width | $PW_{IN(ON)}$<br>$PW_{IN(OFF)}$ | 1 | - | - | µs |
| Control supply variation | $\Delta V_{BS,}$<br>$\Delta V_{DD}$ | -1<br>-1 | -<br>- | 1<br>1 | V/µs |

# 6 Static Parameters

($V_{DD}$ = 15V and $T_J$ = 25°C, if not stated otherwise)

## 6.1 Inverter Section

| Description | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Collector-Emitter saturation voltage | $V_{CE(sat)}$ | $I_C$ = 5 A<br>$T_J$ = 25°C<br>150°C | -<br>- | 2.0<br>2.5 | 2.3<br>- | V |
| Collector-Emitter leakage current | $I_{CES}$ | $V_{CE}$ = 1200 V | - | - | 1 | mA |
| Diode forward voltage | $V_F$ | $I_F$ = 5 A<br>$T_J$ = 25°C<br>150°C | -<br>- | 1.9<br>1.9 | 2.4<br>- | V |

## 6.2 Control Section

| Description | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Logic "1" input voltage (LIN, HIN) | $V_{IH}$ | | - | 1.9 | 2.3 | V |
| Logic "0" input voltage (LIN, HIN) | $V_{IL}$ | | 0.7 | 0.9 | - | V |
| ITRIP positive going threshold | $V_{IT,TH+}$ | | 475 | 500 | 525 | mV |
| ITRIP input hysteresis | $V_{IT,HYS}$ | | - | 55 | - | mV |
| $V_{DD}$ and $V_{BS}$ supply under voltage positive going threshold | $V_{DDUV+}$<br>$V_{BSUV+}$ | | 11.5<br>10.5 | 12.2<br>11.2 | 13.0<br>12.0 | V |
| $V_{DD}$ / $V_{BS}$ supply under voltage negative going threshold | $V_{DDUV-}$<br>$V_{BSUV-}$ | | 10.5<br>9.5 | 11.2<br>10.2 | 12.0<br>11.0 | V |
| $V_{DD}$ / $V_{BS}$ supply under voltage lockout hysteresis | $V_{DDUVH}$<br>$V_{BSUVH}$ | | - | 1 | - | V |
| Quiescent $V_{Bx}$ supply current ($V_{Bx}$ only) | $I_{QBS}$ | $H_{IN}$ = 0 V | - | 175 | - | µA |
| Quiescent $V_{DD}$ supply current ($V_{DD}$ only) | $I_{QDD}$ | $L_{IN}$ = 0 V, $H_{INX}$ = 5 V | - | 1 | - | mA |
| Input bias current for LIN, HIN | $I_{IN+}$ | $V_{IN}$ = 5 V | - | 1 | - | mA |
| Input bias current for ITRIP | $I_{ITRIP+}$ | $V_{ITRIP}$ = 5 V | - | 30 | 100 | µA |
| Input bias current for RFE | $I_{RFE}$ | $V_{RFE}$ = 5 V,<br>$V_{ITRIP}$ = 0 V | - | - | 5 | µA |
| RFE output voltage | $V_{RFE}$ | $I_{RFE}$ = 10 mA,<br>$V_{ITRIP}$ = 1 V | - | 0.4 | - | V |
| $V_{RFE}$ positive going threshold | $V_{RFE,TH+}$ | | - | 1.9 | 2.3 | V |
| $V_{RFE}$ negative going threshold | $V_{RFE,TH-}$ | | 0.7 | 0.9 | - | V |
| Bootstrap diode forward voltage | $V_{F_BSD}$ | $I_F$ = 0.3 mA | - | 0.9 | - | V |
| Bootstrap diode resistance | $R_{BSD}$ | Between $V_F$ = 4 V and $V_F$ = 5 V | - | 120 | - | Ω |

# 7 Dynamic Parameters

($V_{DD}$ = 15V and $T_J$ = 25°C, if not stated otherwise)

## 7.1 Inverter Section

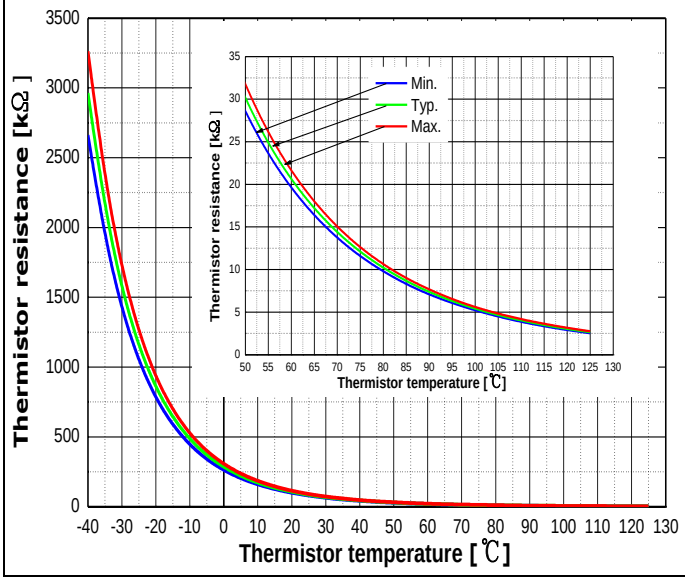
| Description | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Turn-on propagation delay time | $t_{on}$ | $V_{LIN, HIN}$ = 5 V, $I_C$ = 5 A, $V_{DC}$ = 600 V | - | 790 | - | ns |
| Turn-on rise time | $t_r$ | | - | 25 | - | ns |
| Turn-on switching time | $t_{c(on)}$ | | - | 170 | - | ns |
| Reverse recovery time | $t_{rr}$ | | - | 420 | - | ns |
| Turn-off propagation delay time | $t_{off}$ | $V_{LIN, HIN}$ = 0 V, $I_C$ = 5 A, $V_{DC}$ = 600 V | - | 990 | - | ns |
| Turn-off fall time | $t_f$ | | - | 150 | - | ns |
| Turn-off switching time | $t_{c(off)}$ | | - | 230 | - | ns |
| Short circuit propagation delay time | $t_{SCP}$ | From $V_{IT,TH+}$ to 10% $I_{SC}$ | - | 1100 | - | ns |
| IGBT turn-on energy (includes reverse recovery of diode) | $E_{on}$ | $V_{DC}$ = 600 V, $I_C$ = 5 A<br>$T_J$ = 25°C<br>150°C | -<br>- | 0.4<br>0.6 | -<br>- | mJ |
| IGBT turn-off energy | $E_{off}$ | $V_{DC}$ = 600 V, $I_C$ = 5 A<br>$T_J$ = 25°C<br>150°C | -<br>- | 0.3<br>0.5 | -<br>- | mJ |
| Diode recovery energy | $E_{rec}$ | $V_{DC}$ = 600 V, $I_C$ = 5 A<br>$T_J$ = 25°C<br>150°C | -<br>- | 0.2<br>0.3 | -<br>- | mJ |

## 7.2 Control Section

| Description | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Input filter time ITRIP | $t_{ITRIPmin}$ | $V_{ITRIP}$ = 1 V | - | 500 | - | ns |
| Input filter time at LIN, HIN for turn on and off | $t_{FIL,IN}$ | $V_{LIN, HIN}$ = 0 or 5 V | - | 350 | - | ns |
| Fault clear time after ITRIP-fault | $t_{FLT,CLR}$ | $V_{ITRIP}$ = 1 V, $V_{pull-up}$ = 5 V ($R_{RFE}$ = 1 MΩ, $C_{RFE}$ = 2 nF) | | 1.1 | - | ms |
| ITRIP to Fault propagation delay | $t_{FLT}$ | $V_{LIN, HIN}$ = 0 or 5 V, $V_{ITRIP}$ = 1 V | - | 650 | 900 | ns |
| Internal deadtime | $DT_{IC}$ | $V_{IN}$ = 0 or $V_{IN}$ = 5 V | 300 | - | - | ns |
| Matching propagation delay time (On & Off) all channels | $M_T$ | External dead time > 500 ns | - | | 130 | ns |

# 8 Thermistor Characteristics

| Description | Condition | Symbol | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Resistor | $T_{NTC}$ = 25°C | $R_{NTC}$ | - | 85 | - | kΩ |
| B-constant of NTC (Negative Temperature Coefficient) | | B (25/100) | - | 4092 | - | K |




| T [°C] | Rmin. [kΩ] | Rtyp. [kΩ] | Rmax. [kΩ] |
|---|---|---|---|
| 50 | 28.400 | 29.972 | 31.545 |
| 60 | 19.517 | 20.515 | 21.514 |
| 70 | 13.670 | 14.315 | 14.960 |
| 80 | 9.745 | 10.169 | 10.593 |
| 90 | 7.062 | 7.345 | 7.628 |
| 100 | 5.199 | 5.388 | 5.576 |
| 110 | 3.856 | 4.009 | 4.163 |
| 120 | 2.900 | 3.024 | 3.149 |
| 125 | 2.527 | 2.639 | 2.751 |

**Figure 6 Thermistor resistance – temperature curve and table**

**(For more information, please refer to the application note 'AN2019-16 CIPOS Mini IM818 application note')**

# 9 Mechanical Characteristics and Ratings

| Description | Condition | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| Comparative Tracking Index (CTI) | | 600 | - | - | |
| Mounting torque | M3 screw and washer | 0.49 | - | 0.78 | Nm |
| Backside Curvature | Refer to Figure 8 | 0 | - | 150 | µm |
| Weight | | - | 7.1 | - | g |

# 10 Qualification Information

| | | |
|---|---|---|
| **UL Certification** | File number E314539 | |
| **Moisture sensitivity level (SOP package only)** | - | |
| **RoHS Compliant** | Yes (Lead-free terminal plating) | |
| **ESD (Electrostatic Discharge)** | HBM (Human body model) Class as per JESD22-A114 | 2 (>2000V to < 4000V) |
| | CDM (Charged Device model) Class as per JESD22-C101 | C3 (>=1000V) |

# 11 Diagrams and Tables

## 11.1 $T_C$ Measurement Point

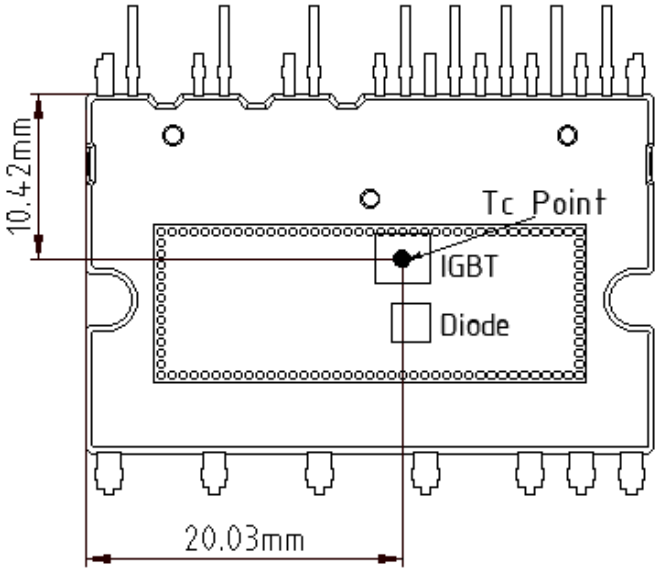



**Figure 7 $T_C$ measurement point[1]**

## 11.2 Backside Curvature Measurement Point

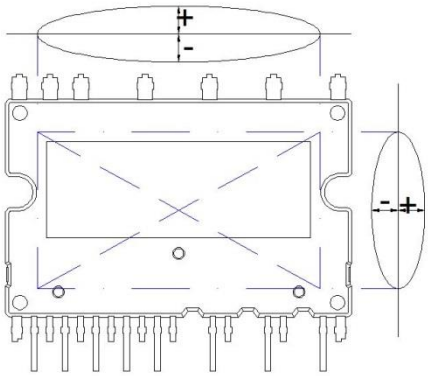



**Figure 8 Backside curvature measurement position**

[1]Any measurement except for the specified point in figure 7 is not relevant for the temperature verification and brings wrong or different information.

## 11.3 Switching Time Definition

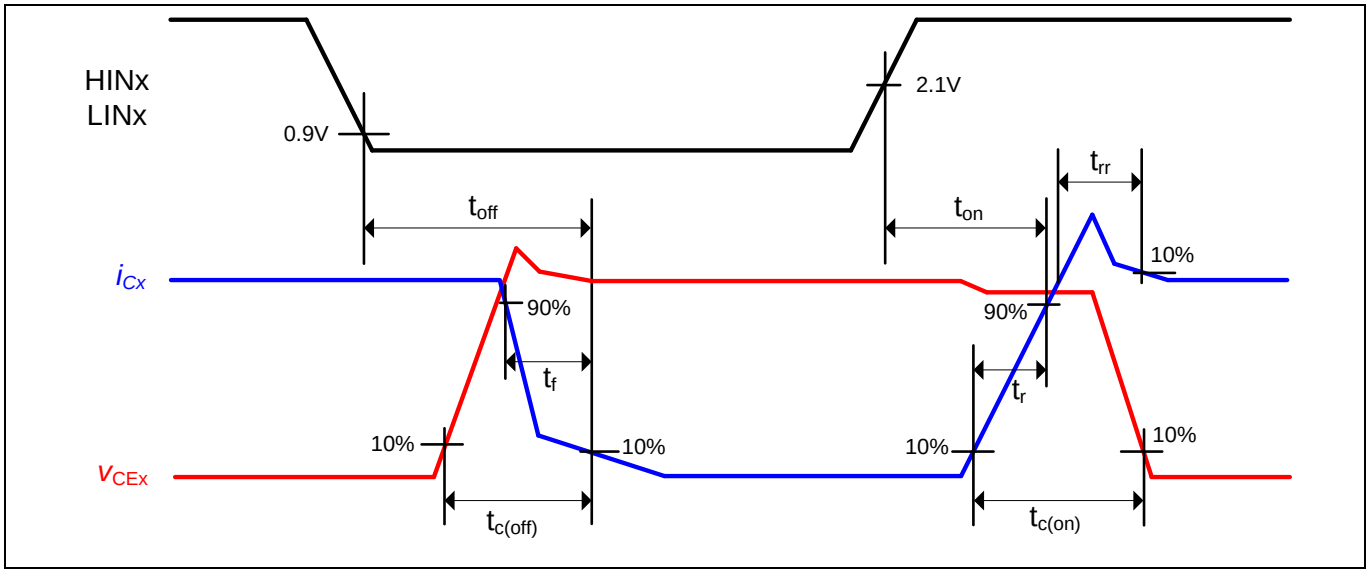



**Figure 9 Switching times definition**

# 12 Application Guide

## 12.1 Typical Application Schematic

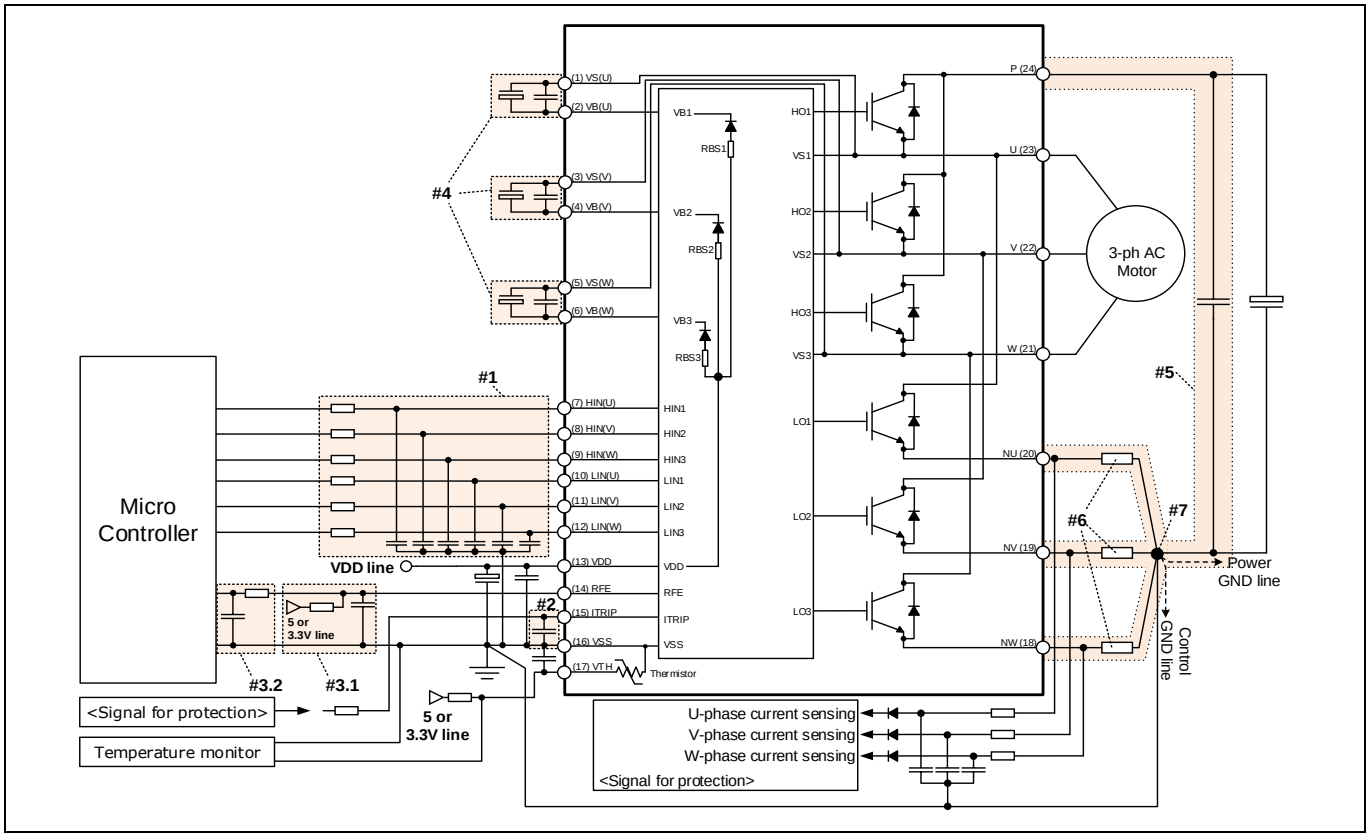



**Figure 10 Typical application circuit**

1. Input circuit
   - To reduce input signal noise by high speed switching, the $R_{IN}$ and $C_{IN}$ filter circuit should be mounted. (100 Ω, 1 nF)
   - $C_{IN}$ should be placed as close to $V_{SS}$ pin as possible.
2. Itrip circuit
   - To prevent protection function errors, $C_{ITRIP}$ should be placed as close to Itrip and $V_{SS}$ pins as possible.
3. RFE circuit

   3.1 Pull-up resistor ($R_{RFE}$) and pull-down capacitor ($C_{RFE}$)
   - RFE output is an open drain output. This signal line should be pulled up to the positive side of the 5 V / 3.3 V control power supply voltage ($V_{CTR}$) with a proper resistor $R_{FE}$.
   - The fault-clear time is adjusted by RC network of $R_{RFE}$ and $C_{RFE}$ and pull-up voltage.
     - $t_{FLTCLR} = -R_{RFE} \cdot C_{RFE} \cdot \ln(1 - V_{RFE,TH+}/V_{CTR})$ + internal fault-clear time 160 µs
     - $t_{FLTCLR} = -1\ M\Omega \times 2\ nF \times \ln(1 - 1.9 / 5\ V) + 160\mu s \cong 1.1ms$ at $R_{RFE} = 1\ M\Omega$, $C_{RFE} = 2\ nF$ and $V_{CTR} = 5\ V$
     - A pull-up resistor is limited to max. 2 MΩ
     - In case of $V_{CTR}$ is higher than 5 V, the $R_{RFE}$ needs to be at least 200 kΩ to limit the IC power dissipation

   3.2 RC filter
   - It is recommended that RC filter be placed as close to the controller as possible.
4. VB-VS circuit
   - Capacitor for high side floating supply voltage should be placed as close to VB and VS pins as possible.
5. Snubber capacitor
   - The wiring between IM818 and snubber capacitor including shunt resistor should be as short as possible.
6. Shunt resistor
   - The shunt resistor of SMD type should be used for reducing its stray inductance.
7. Ground pattern
   - Ground pattern should be separated at only one point of shunt resistor as short as possible.

## 12.2 Performance Charts

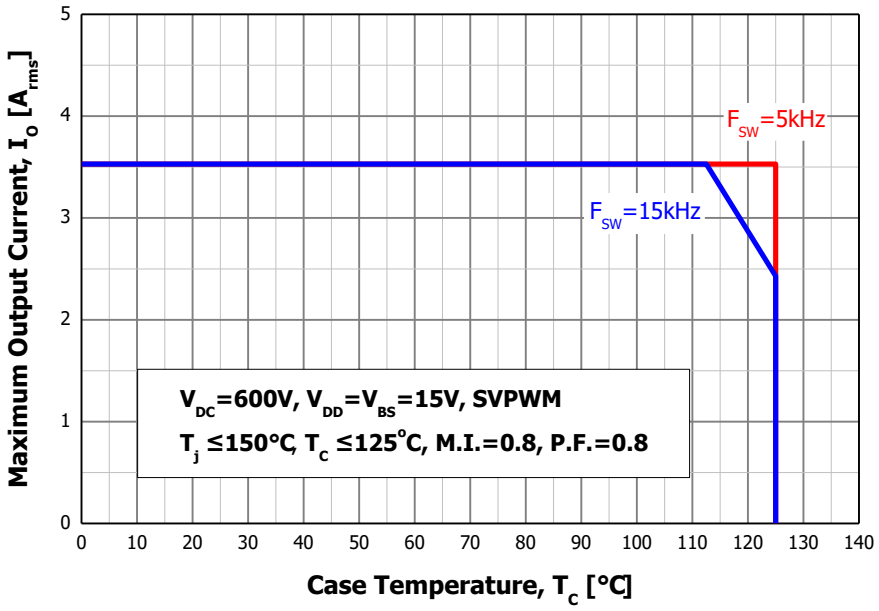
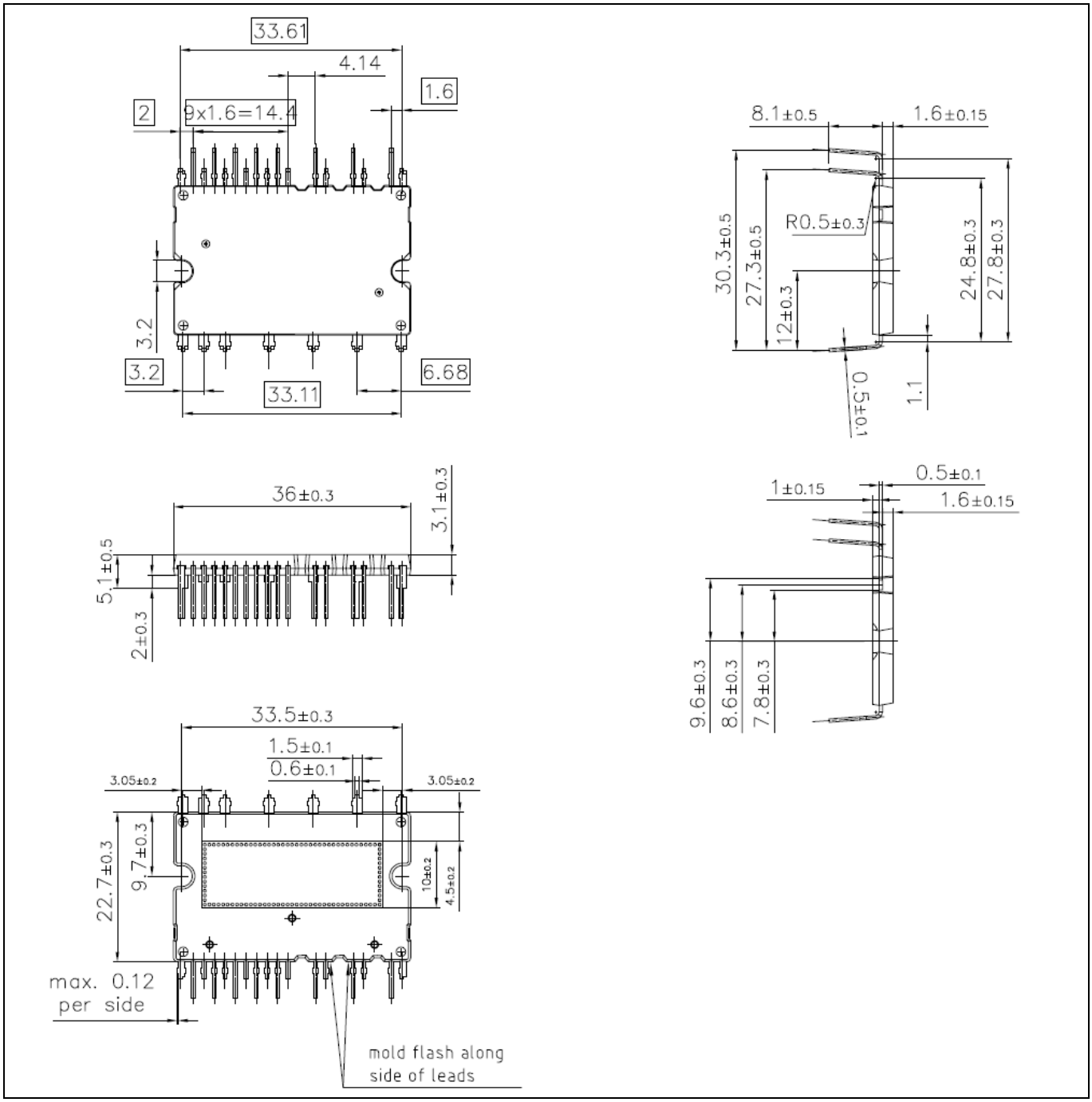



**Figure 11 Maximum operating current SOA[1]**

[1]This maximum operating current SOA is just one of example based on typical characteristics for this product. It can be changed by each user's actual operating conditions.

# 13 Package Outline



# Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| 2.0 | 2018-06-25 | Initial release |
| 2.1 | 2018-08-20 | Minor change - Figure7, section 4(thermal resistance), section 10(qualification information), section 13(package outline) |
| 2.2 | 2019-06-07 | Corrected typo section 7.1(HINx,LINx=0V)<br>Minor change – Table 1 and reference document (AN) number in figure 6 |
| 2.3 | 2020-03-13 | Corrected typo section 7.1($I_C$ = 5 A) |
| 2.4 | 2022-02-23 | Update notes (3.1) in section 12.1 |
| 2.5 | 2024-06-24 | Minor change - Corrected typo section 5 (Maximum value of DC link supply voltage of P-N) |

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