

ESD121-B1-W0201

Protection device

TVS (transient voltage suppressor)

Bi-directional, 7 V, 0.25 pF, 0201, RoHS and halogen free compliant

Feature list

- ESD/ transient protection of high speed data lines according to:
 - IEC61000-4-2 (ESD): ± 18 kV (air/ contact discharge)
 - IEC61000-4-4 (EFT): ± 1.5 kV/ ± 30 A (5/50 ns)
 - IEC61000-4-5 (Surge): ± 2 A (8/20 μ s)
- Bi-directional working voltage up to: $V_{WM} = \pm 7$ V
- Line capacitance: $C_L = 0.25$ pF (typical) at $f = 1$ MHz
- Clamping voltage: $V_{CL} = 24$ V (typical) at $I_{TLP} = 16$ A with $R_{DYN} = 0.91 \Omega$ (typical)
- Very low leakage current: $I_L = 1$ nA (typical)
- Small form factor SMD size 0201, low profile (0.58 mm x 0.28 mm x 0.15 mm) [\[2\]](#)
- Bi-directional, symmetric I/V characteristic for optimized design and assembly, recommendations for PCB assembly see [\[3\]](#)



Potential applications

- Capacitance sensitive data transmission lines in portable devices

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Device information

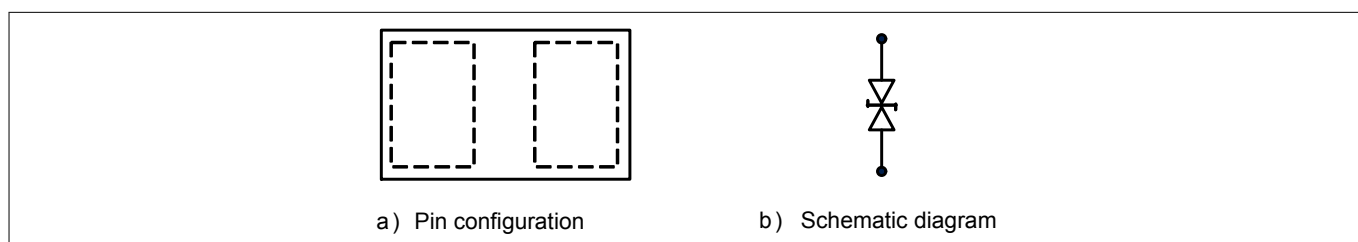


Figure 1 Pin configuration and schematic diagram

Table 1 Part information

Type	Package	Configuration	Marking code
ESD121-B1-W0201	WLL-2-3	1 line, bi-directional	WY ¹⁾

¹ The marking code is on pad side.

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Maximum ratings

1 Maximum ratings

Note: $T_A = 25\text{ °C}$, unless otherwise specified.

Table 2 Maximum ratings

Parameter	Symbol	Values	Unit
Working voltage	V_{WM}	± 7	V
ESD discharge ²⁾	V_{ESD} (contact)	± 18	kV
	V_{ESD} (air)	± 18	
Peak pulse power ³⁾	P_{PK}	24	W
Peak pulse current ³⁾	I_{PP}	± 2	A
Operating temperature	T_{OP}	-55 to 125	°C
Storage temperature	T_{stg}	-65 to 150	°C

Attention: *Stresses above the maximum values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the component.*

² V_{ESD} according to IEC61000-4-2 ($R = 330\ \Omega$, $C = 150\text{ pF}$ discharge network)

³ Stress pulse: 8/20 μ s current waveform according to IEC61000-4-5

Electrical characteristics

2 Electrical characteristics

Note: $T_A = 25\text{ °C}$, unless otherwise specified. Device is electrically symmetrical.

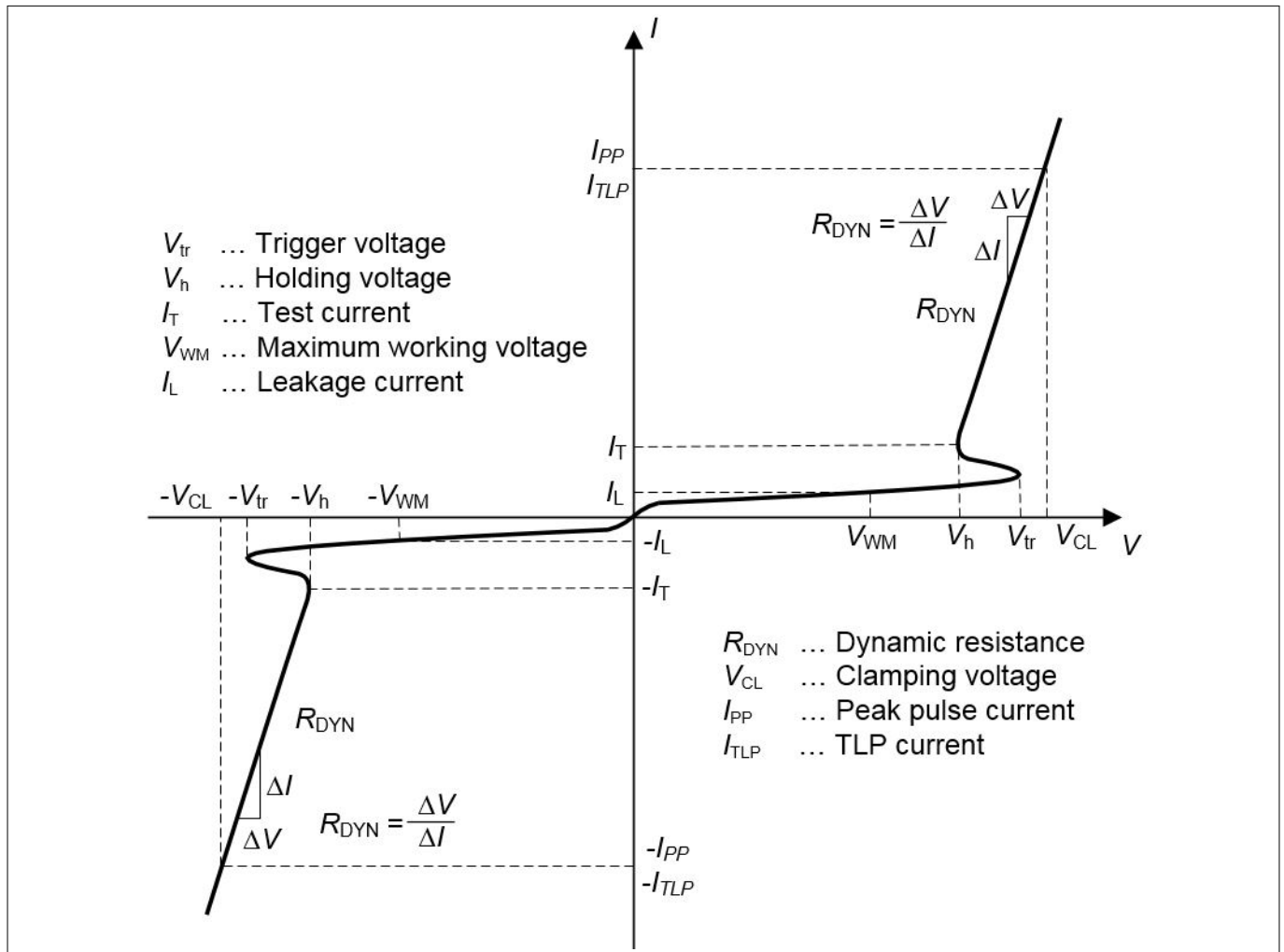


Figure 2 Definition of electrical characteristics

Electrical characteristics

Table 3 DC characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Trigger voltage ⁴⁾	V_{tr}	–	12	–	V	–
Holding voltage	V_h	8	9.5	12	V	$I_T = 1 \text{ mA}$
Leakage current	I_L	–	1	100	nA	$V = V_{WM} = 7 \text{ V}$

Table 4 RF characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	0.25	0.5	pF	$V = 0 \text{ V}, f = 1 \text{ MHz}$
		–	0.2	–		$V = 0 \text{ V}, f = 1 \text{ GHz}$
Series inductance ⁴⁾	L_S	–	<0.1	–	nH	

Table 5 ESD and Surge characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Clamping voltage ⁵⁾	V_{CL}		13	–	V	$I_{TLP} = 4 \text{ A}, t_p = 100 \text{ ns}$
		–	17	–		$I_{TLP} = 8 \text{ A}, t_p = 100 \text{ ns}$
		–	24	–		$I_{TLP} = 16 \text{ A}, t_p = 100 \text{ ns}$
		–	10	–		$I_{PP} = 1 \text{ A}, t_p = 8/20 \text{ } \mu\text{s}$
Clamping voltage ⁶⁾		–	10	–		
Dynamic resistance ⁵⁾	R_{DYN}	–	0.9	–	Ω	$t_p = 100 \text{ ns}$

⁴⁾ Verified by design

⁵⁾ Please refer to application note AN210 [\[1\]](#). TLP parameter: $Z_0 = 50 \text{ } \Omega$, $t_p = 100 \text{ ns}$, $t_r = 0.6 \text{ ns}$

⁶⁾ Stress pulse: 8/20 μs current waveform according to IEC61000-4-5

Typical characteristic diagrams

3 Typical characteristic diagrams

Note: $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified

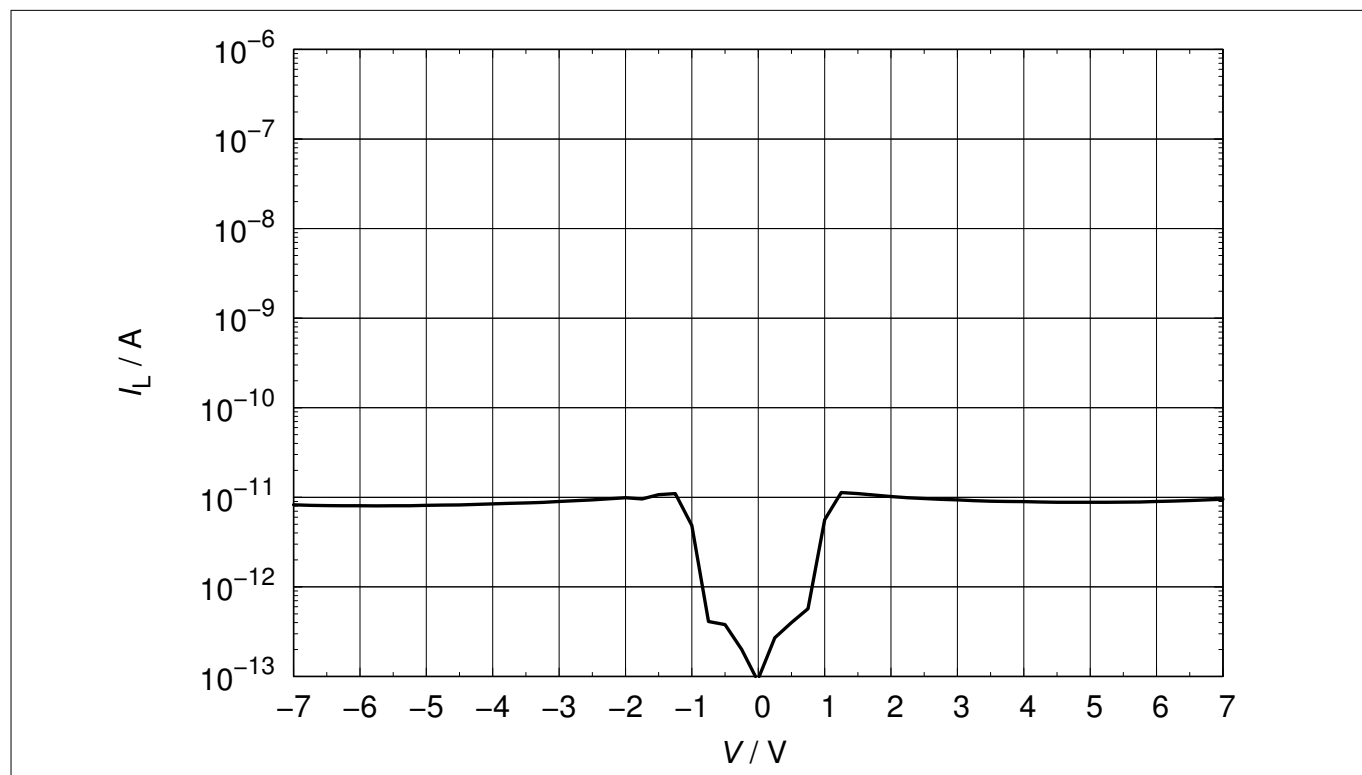


Figure 3 Leakage current: $I_L = f(V)$

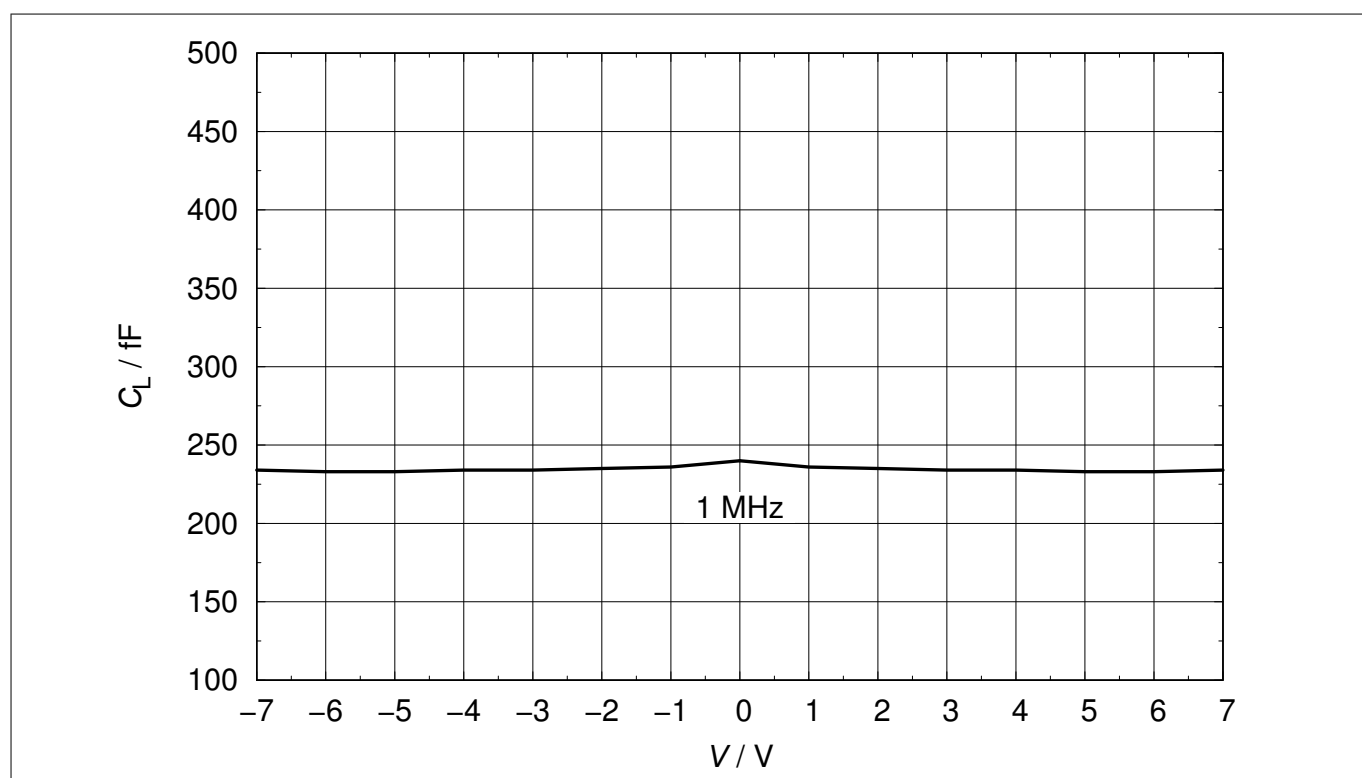


Figure 4 Line capacitance: $C_L = f(V)$

Typical characteristic diagrams

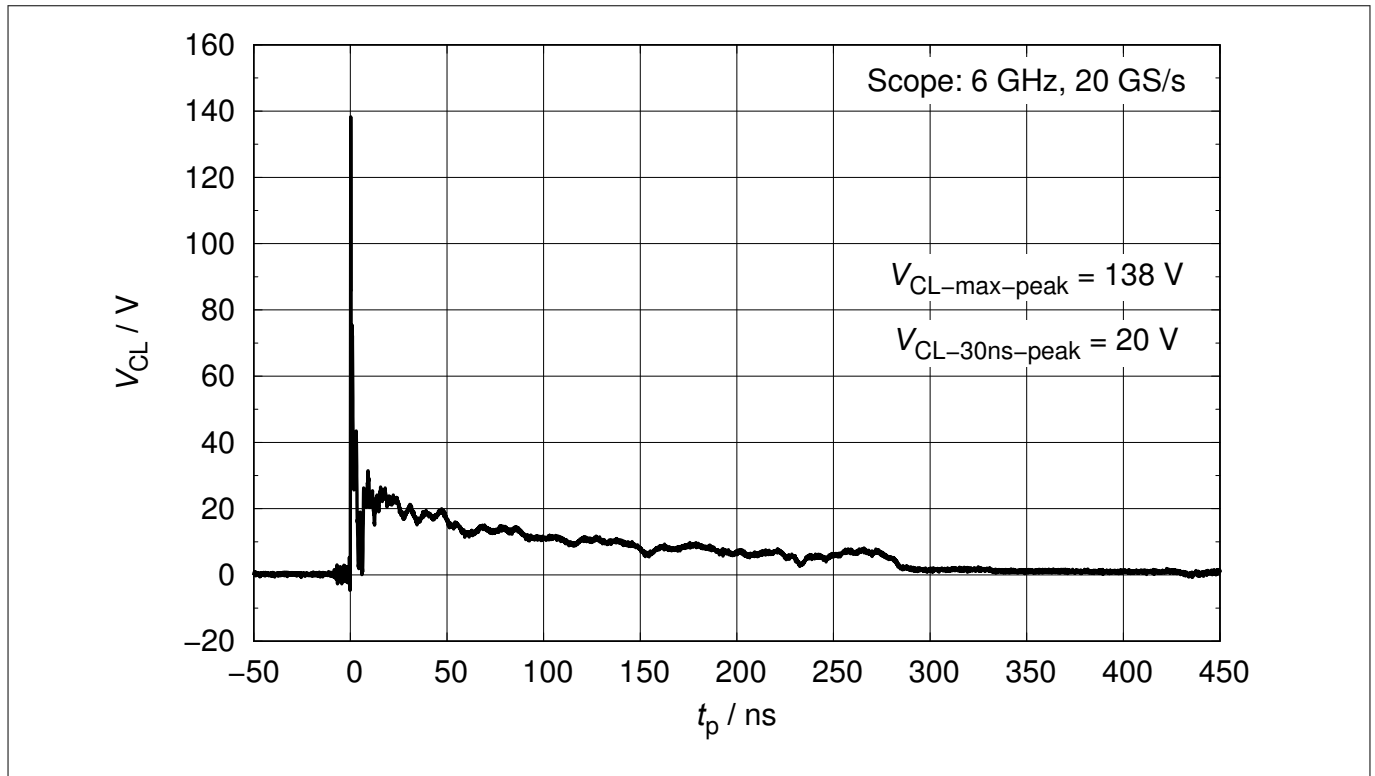


Figure 5 Clamping voltage (ESD): $V_{CL} = f(t)$, 8 kV positive pulse according to IEC61000-4-2

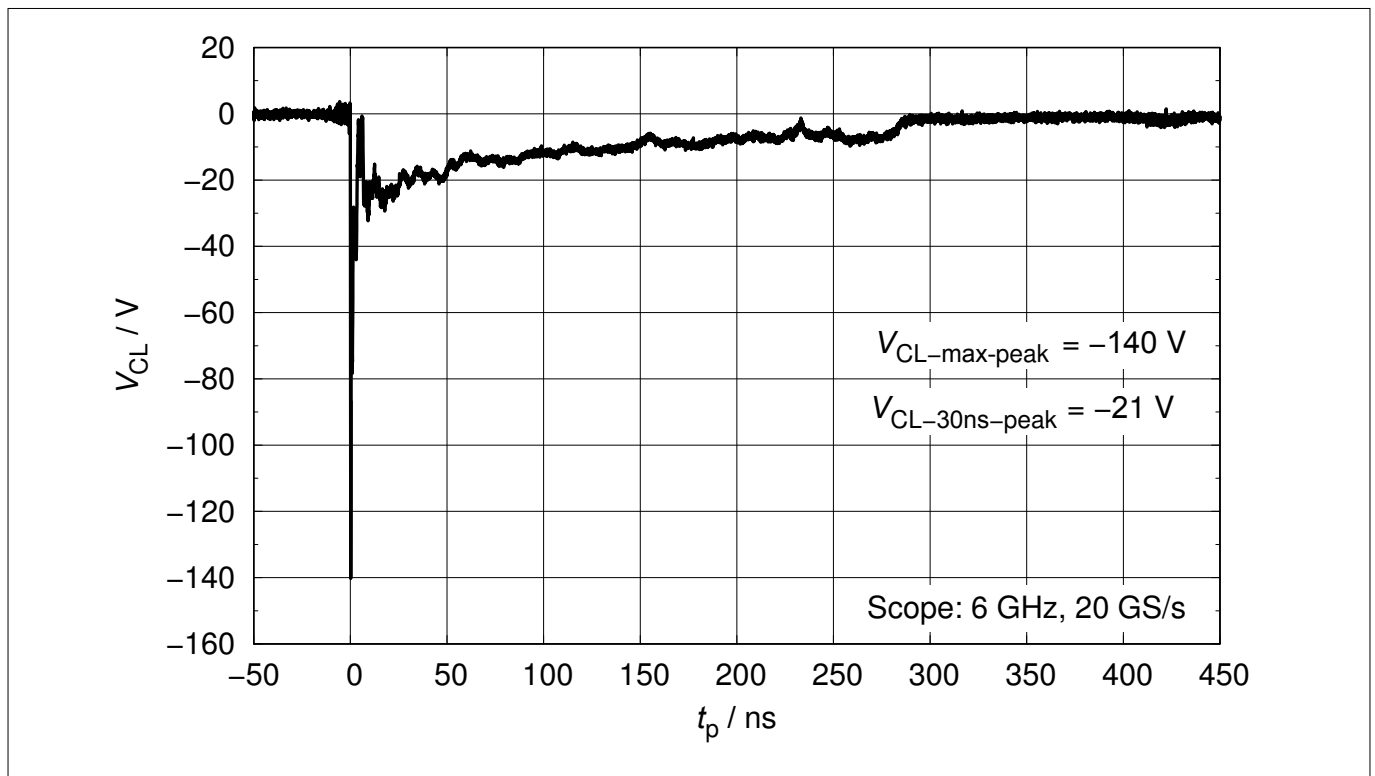


Figure 6 Clamping voltage (ESD): $V_{CL} = f(t)$, 8 kV negative pulse according to IEC61000-4-2

Typical characteristic diagrams

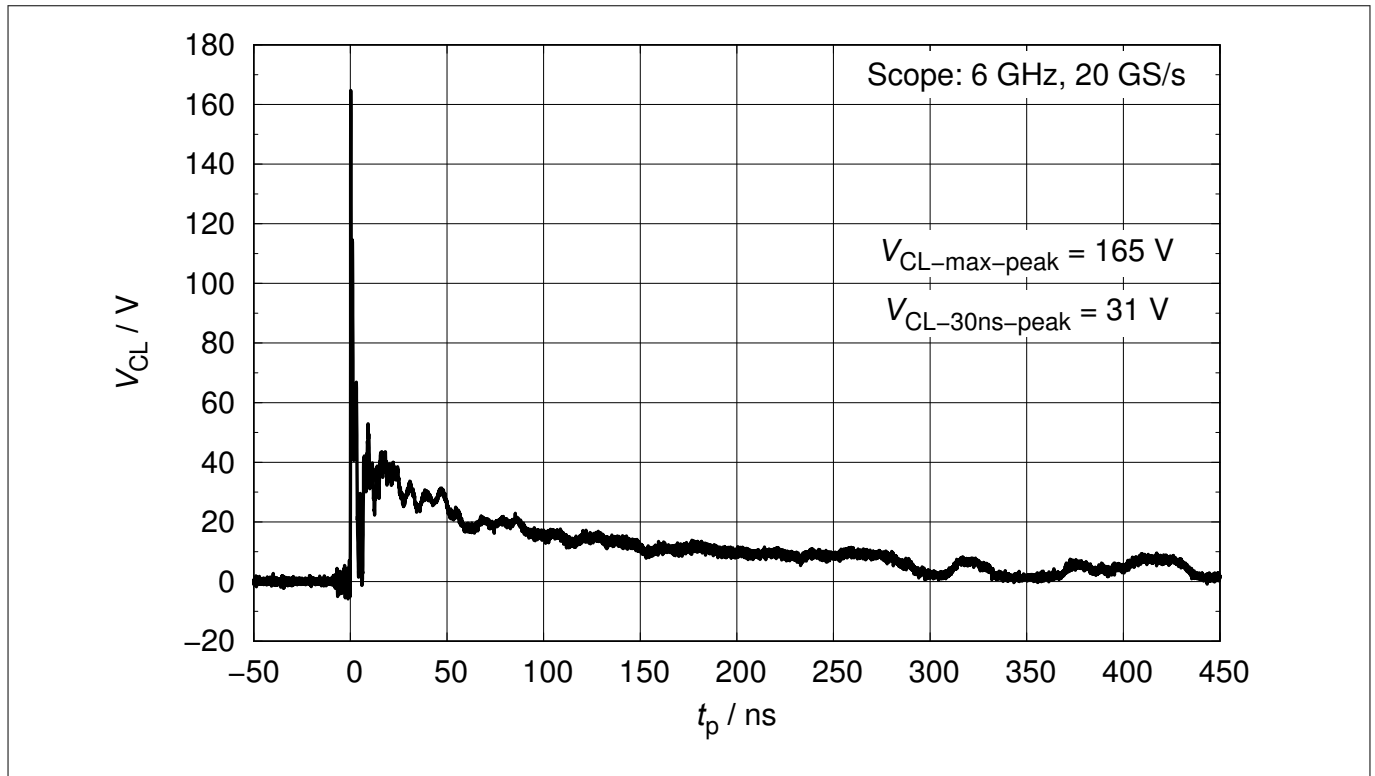


Figure 7 Clamping voltage (ESD): $V_{CL} = f(t)$, 15 kV positive pulse according to IEC61000-4-2

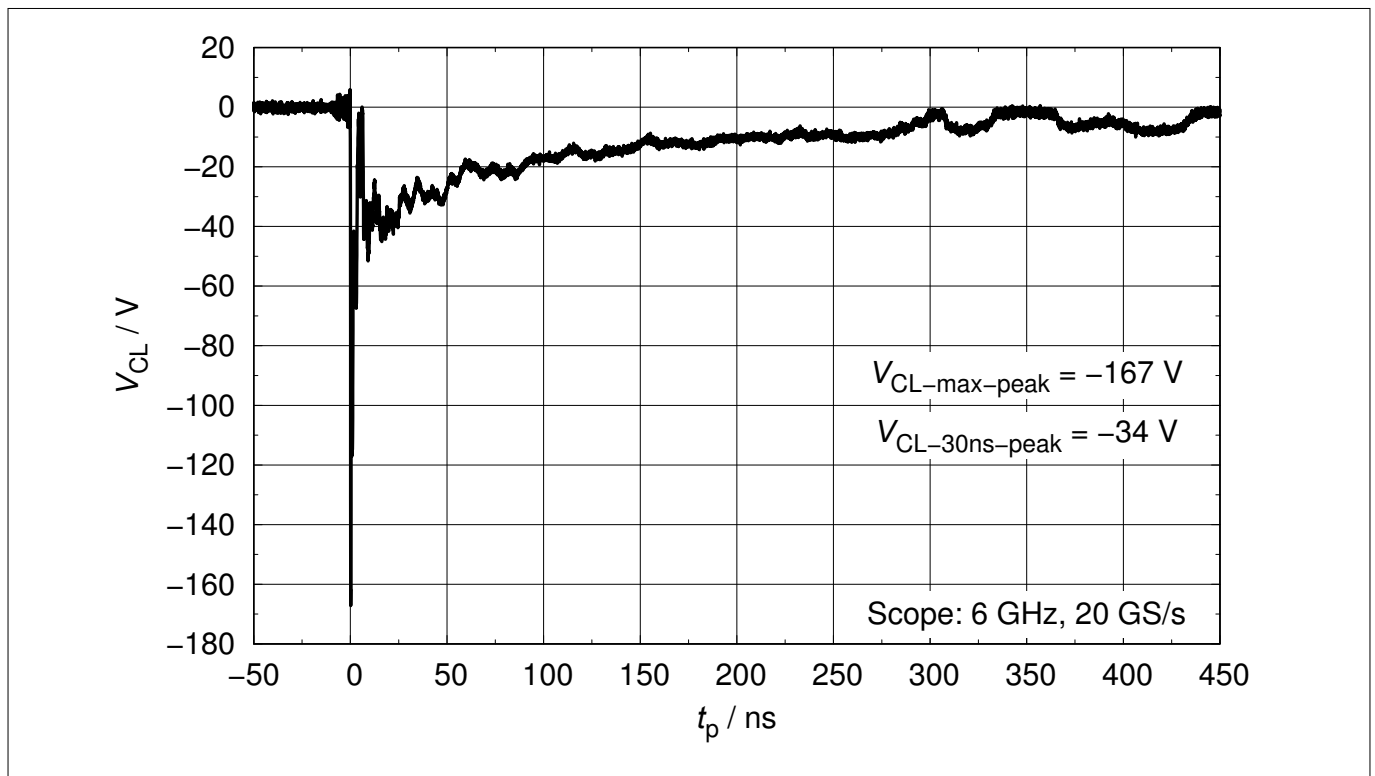


Figure 8 Clamping voltage (ESD): $V_{CL} = f(t)$, 15 kV negative pulse according to IEC61000-4-2

Typical characteristic diagrams

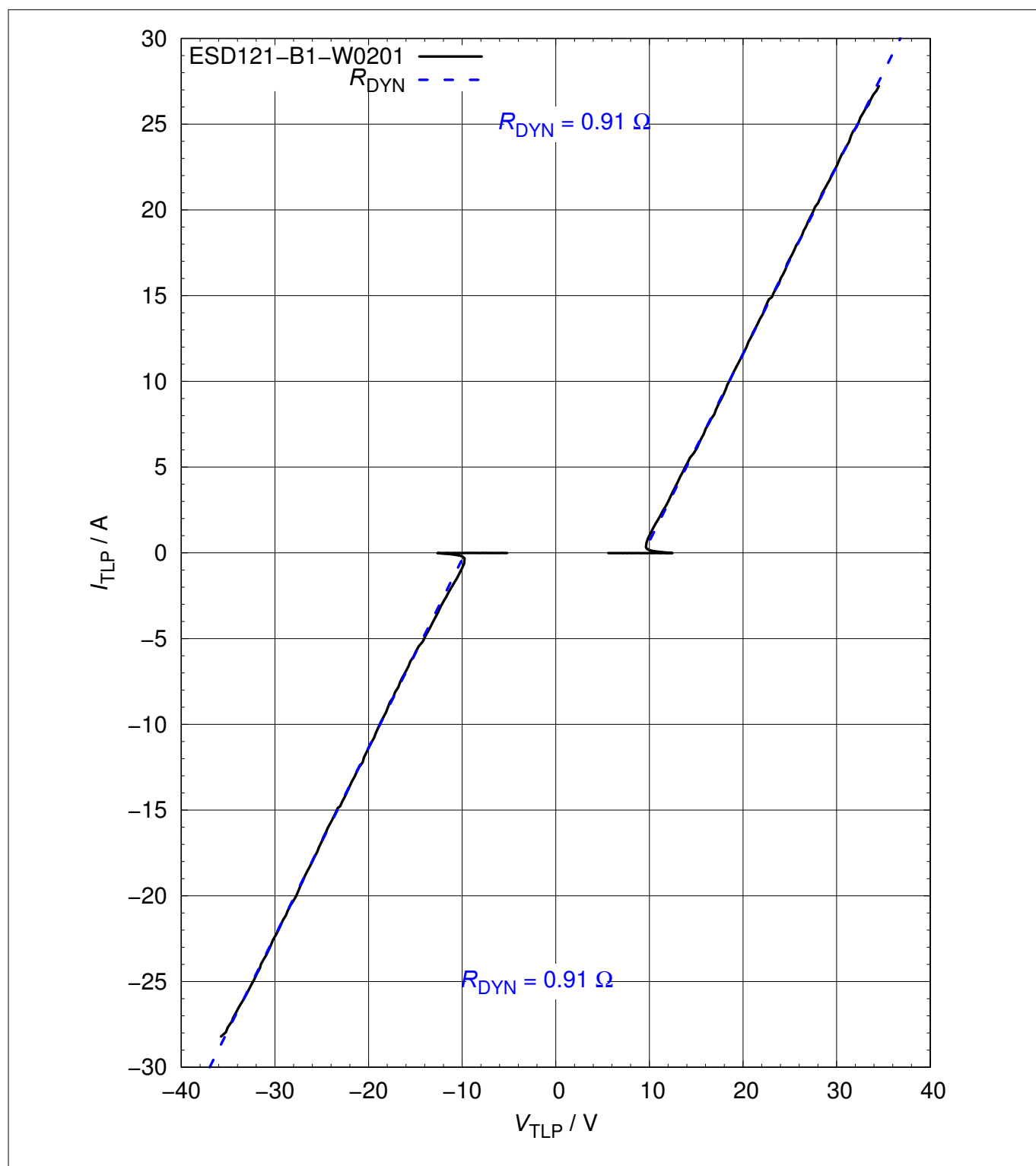


Figure 9 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$

Typical characteristic diagrams

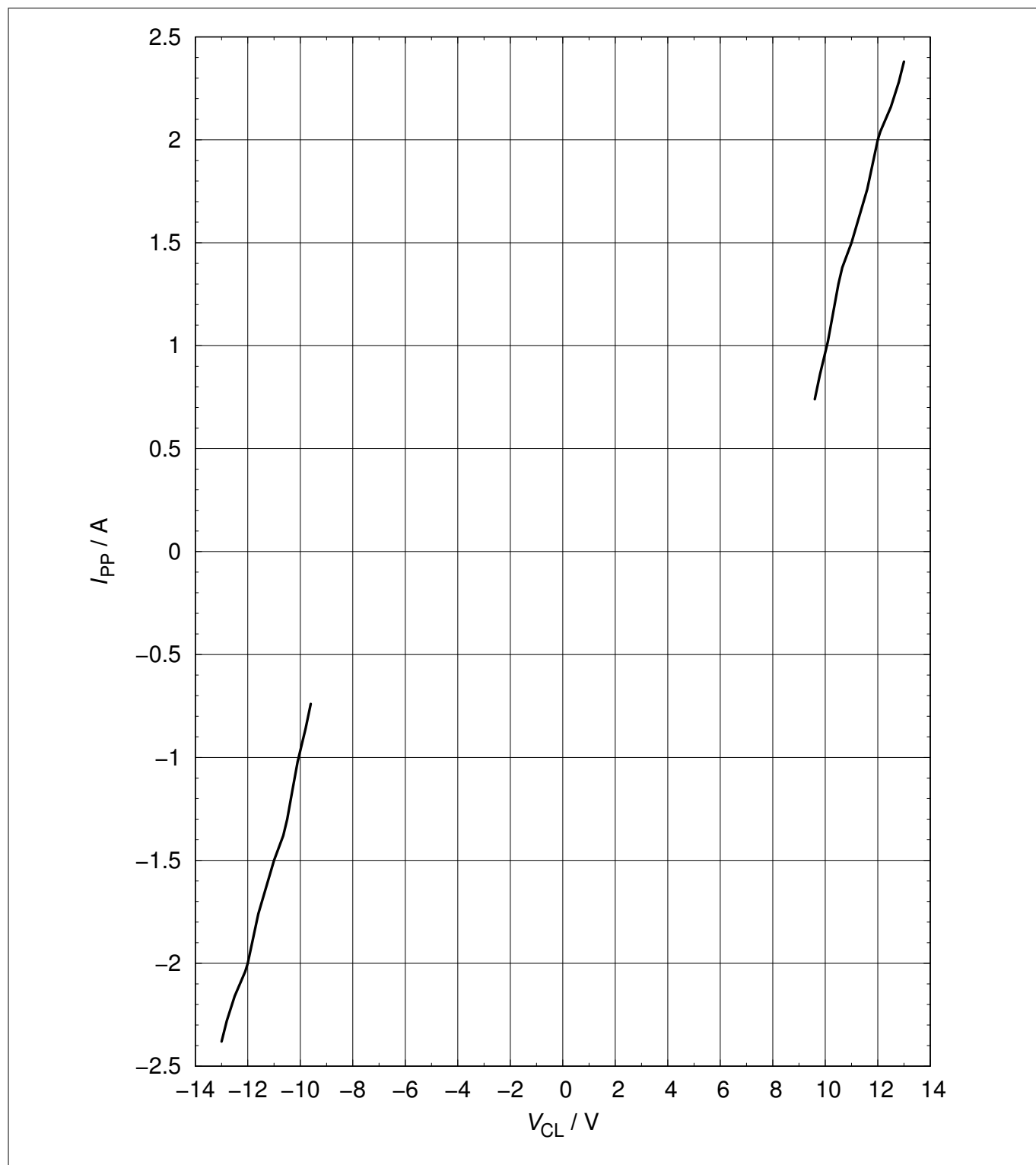


Figure 10 Clamping voltage (Surge): $I_{PP} = f(V_{CL})$

Typical characteristic diagrams

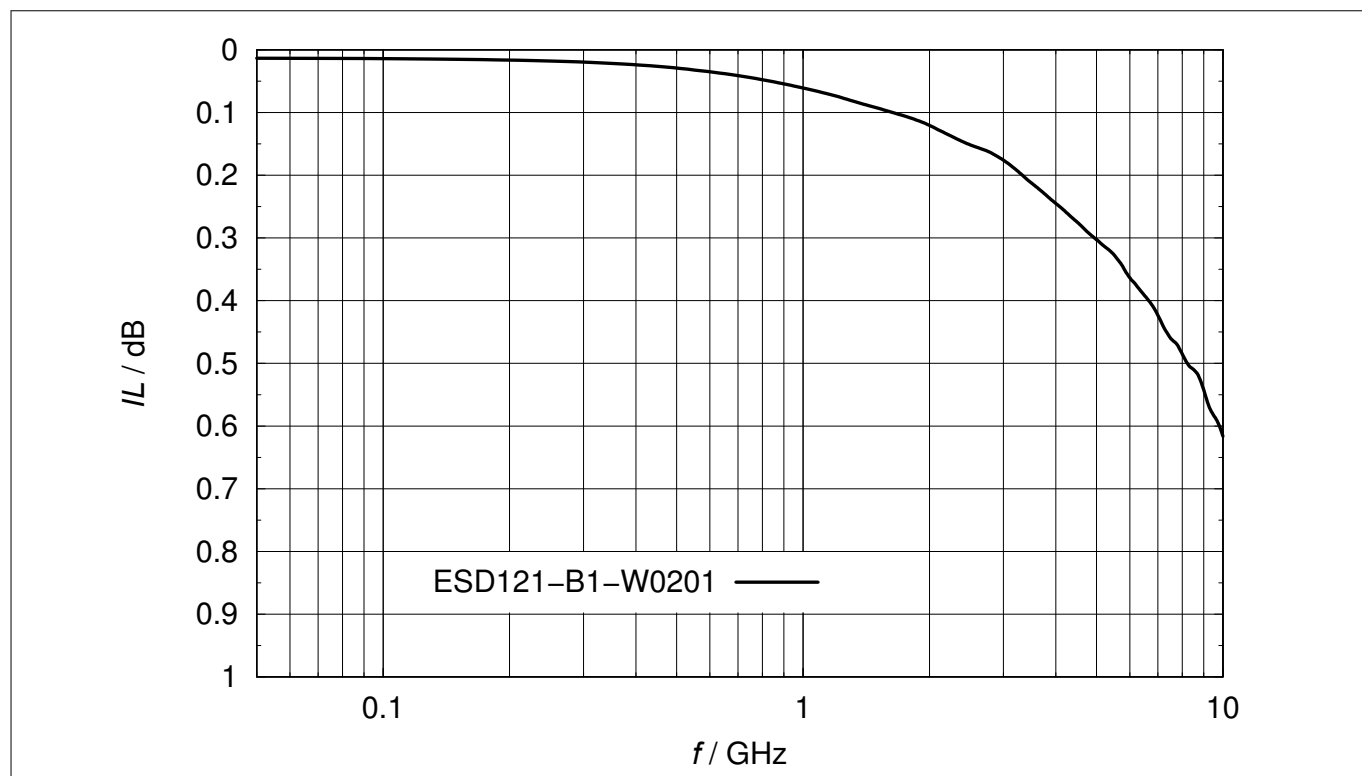


Figure 11 Insertion loss in a 50 Ω system: $IL = f(f)$

Package information

4 Package information

4.1 WLL-2-3 package

Note: Dimensions in mm

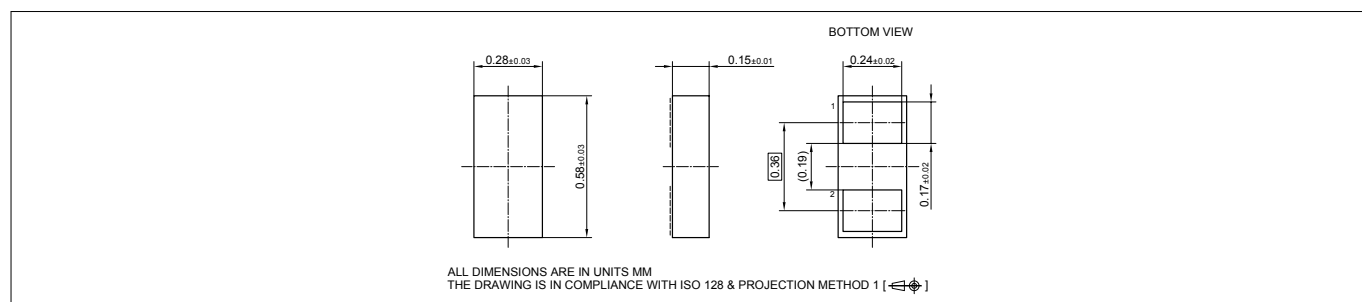


Figure 12 **Package outline**

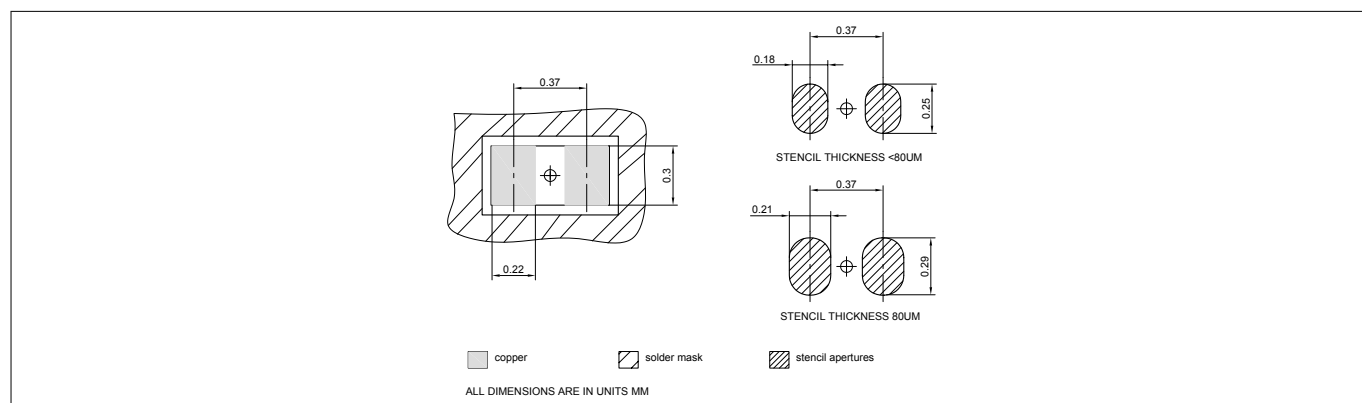


Figure 13 **Footprint**

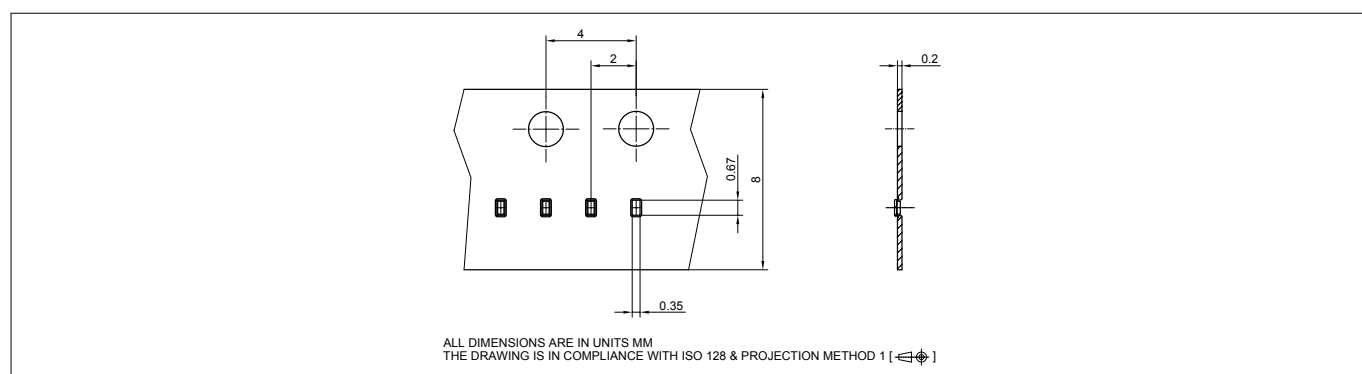


Figure 14 **Packing**

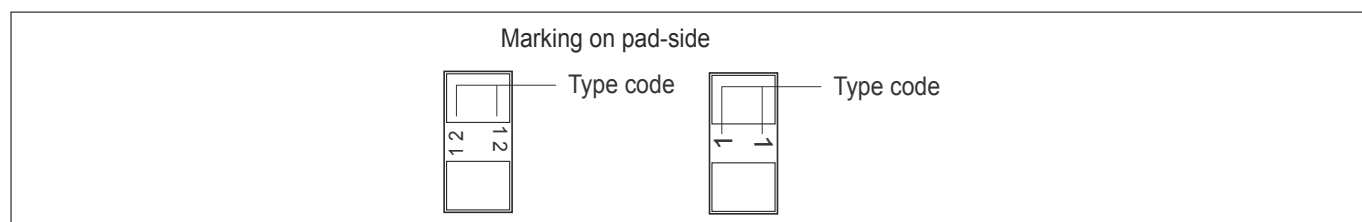


Figure 15 **Marking example (marking code see [Device information](#))**

References

5 References

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection Design at System level Using VF-TLP Characterization Methodology
- [2] Infineon AG - Recommendations for Printed Circuit Board Assembly of Infineon WLL Packages
http://www.infineon.com/Packageinformation_WLL
- [3] Infineon AG - **Application Note AN392**: TVS Diodes in Chip Scale Package reduce size and save cost

Revision history

Document version	Date of release	Description of changes
1.0	2019-07-12	Final datasheet version
1.1	2019-07-29	Upper spec limit of Vh parameter updated

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