

ICC80QSG QR flyback controller for battery charger applications of up to 120 W

About this document

Scope and purpose

The [ICC80QSG](#) is a controller for flyback topologies operating in quasi-resonant mode (QRM) and valley switching discontinuous conduction mode (DCM). It is well suited for applications such as general-purpose power supplies and battery chargers. This document comprehensively covers all the design steps of the power supply component of a battery charger using this device, particularly highlighting the input rectifier configuration, a crucial aspect for cost-effective design. Additionally, the guide also highlights the loop compensation, which is essential when the load is not resistive, but rather a battery. The specific characteristic of the actual battery charging will only be covered as it affects the power conversion stage.

Intended audience

This document is intended for power supply design engineers and field application engineers.

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1 Power supplies for battery chargers

1.1 Introduction

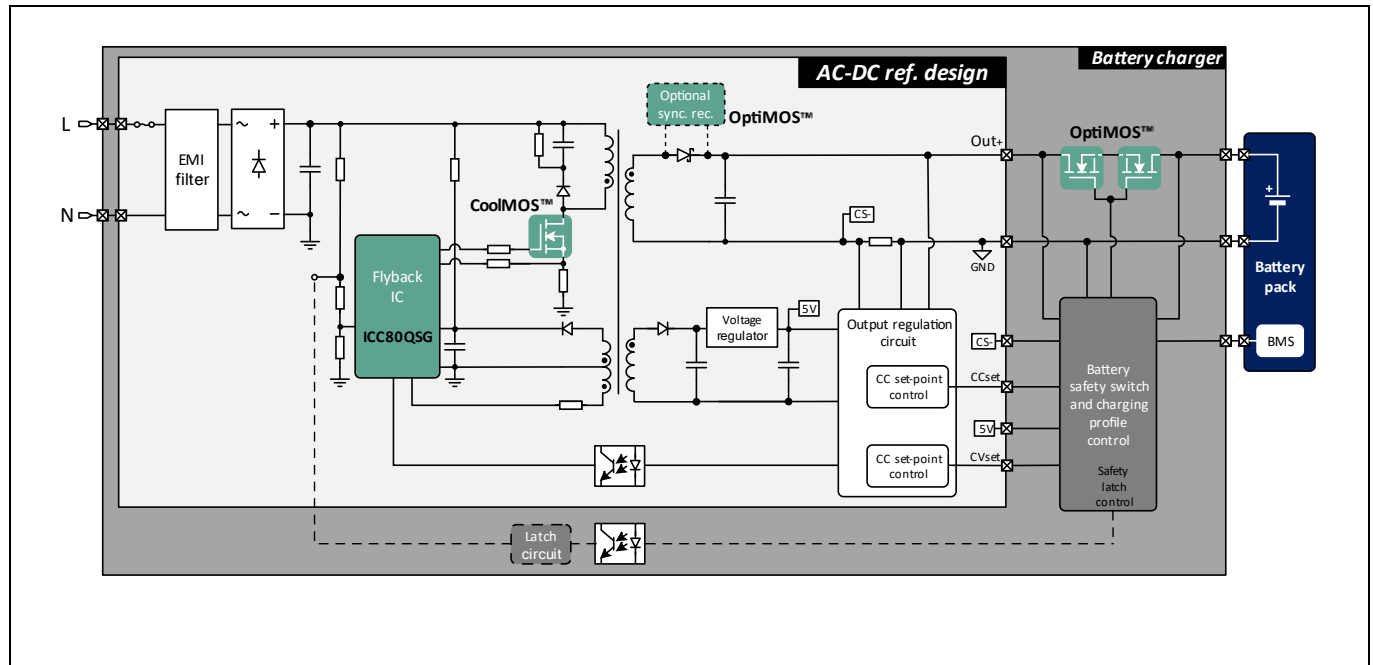


Figure 1 Simplified schematic of AC powered battery charger

Due to the enormous popularity of battery-driven devices, such as power tools, there is a huge demand for battery chargers. The basic structure of such a charger does not differ much from other power supply circuits; the main difference can be found on the secondary side. While most standard power supplies are designed to provide a constant output voltage, a battery charger typically has a 'rectangular' output characteristic, where the output current is constant below a certain maximum output voltage. When the battery is fully charged, the charger transitions from the constant current (CC) into constant voltage (CV) mode. The same is true when no battery is connected, then the converter runs in CV mode as well.

The detailed I-V characteristic, such as charge current and maximum voltage, depend on battery chemistry and will not be discussed in this application note.

Apart from the control of the charging profile, several safety and protection features, such as battery inrush current limit or wrong polarity protection for example, need to be present on the secondary side.

This application note focuses on the AC-DC conversion part of the battery charger and the feedback circuit, i.e., the light gray region of [Figure 1](#). Details of the charging profile of a certain battery type will not be discussed here and need to be taken from the datasheet of the battery.

The most popular and cost-effective AC-DC converter topology for power levels up to ~150 W is the flyback topology. In this application note the ICC80QSG is used to control the latter. ICC80QSG is a quasi-resonant controller operating in a critical conduction mode (CrCM) at full load and minimum input voltage. QR control helps to minimize switching noise and increases efficiency by turning on the main power MOSFET at the lowest possible drain-source voltage during transformer demagnetization.

The device will operate in CrCM even with increasing input voltage and decreasing load, as long as the on-time is above a certain level. If on-time becomes too short, the controller goes into DCM with valley switching in higher numbered valleys. For a detailed description of this behavior, see the [datasheet](#) of the device.

2 Specifications and requirements of the AC-DC converter

Apart from special requirements specific to the target design, there are several fundamental parameters that are key for the design of almost any AC-DC converter. These key parameters include:

- **Minimum input voltage (V_{INmin})** affects the value of the bulk capacitor as well as the current flowing in the primary side, such as EMI filter chokes, rectifier, transformer primary, and MOSFET current.
- **Maximum input voltage (V_{INmax})** determines the required breakdown voltages of the semiconductors on the primary as well as the rated voltage of the filters and bulk capacitors.
- **Minimum line frequency (f_{Lmin})** is important for selecting the bulk capacitor value.
- **Maximum output voltage (V_{OUTmax})** affects maximum duty-cycle ' d_{max} ' and transformer turns-ratio ' n '.
- **Minimum output voltage (V_{OUTmin})**, together with V_{OUTmax} , defines the design requirements for internal supplies of the converter.
- **Maximum output current I_{OUT}**

In addition to the above-mentioned six hard requirements, you need to choose the following additional parameters selected from a broader range of possible values:

- **Target efficiency (η)** determines the expected input power and thus currents on the primary side.
- **Minimum switching frequency (f_s)** determines transformer size and EMI filtering effort.
- **MOSFET breakdown voltage ($V_{(BR)DSS}$)** serves as a starting parameter in the design flow.
While many designs begin by selecting a starting value for the maximum duty cycle (d_{max}) in the range of 0.4 to 0.6, and then iteratively adjust its value until the MOSFET drain-voltage stress is within an acceptable range, we will take a different approach. Instead, we will start by selecting a MOSFET breakdown voltage ($V_{(BR)DSS}$) and then determine the transformer turns ratio (n) and maximum duty cycle (d_{max}) based on this parameter.
- **Minimum bus voltage (V_{CBmin})** is another key design parameter which is determined by V_{INmin} and the value of the input electrolytic capacitor. The lower V_{CBmin} , the higher the peak currents on the primary side of the flyback.

The exact values for these parameters that are suitable for the design will be determined and explained as the design process progresses. It is important to note that the design of a switched mode power supply (SMPS) is often an iterative process and some of these four parameters may need to be adjusted as the designing step progresses. For instance, the design may need a smaller transformer, which is enabled by increasing the switching frequency.

Battery chargers need to have a wide output voltage range that typically varies by a factor of three or more. At the same time, in a universal input design, the input range would vary by about the same amount.

Designing for a wide input and output voltage range simultaneously can be challenging and may lead to increased complexity and cost. One possible solution to address this issue is to create separate designs for specific input voltage ranges, such as 90-130 V_{RMS} and 190-264 V_{RMS}, to cover the various line voltages in different regions. However, this approach essentially doubles the design effort and complexity cost.

An alternative approach for designing the power supply could be to use an input voltage doubler configuration, as described in [Appendix A: Rectification and bulk capacitor](#). Although the doubler input stage needs two electrolytic capacitors instead of one, these capacitors need to withstand only half the maximum voltage and therefore size and cost do not increase significantly. At the same time, the flyback stage does not change with the different input voltages and as will be shown, the transformer can be smaller, and system efficiency higher than for a universal input design.

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Specifications and requirements of the AC-DC converter

This application note will compare the universal input solution with one that uses an input voltage doubler and highlight the pros and cons of each.

3 Universal input design

In the following sections the design of an AC-DC supply will be exemplified using the target specification in [Table 1](#).

Table 1 Target design data

Parameter	Symbol	Value	Unit
Minimum input voltage	V_{INmin}	90	V_{RMS}
Maximum input voltage	V_{INmax}	265	V_{RMS}
Minimum line frequency	f_{Lmin}	47	Hz
Maximum output voltage	V_{OUTmax}	21	V
Minimum output voltage	V_{OUTmin}	9	V
Maximum output current	I_{OUT}	4	A
Target efficiency	η	90	%
Minimum switching frequency	f_{Smin}	45	kHz
MOSFET breakdown voltage	$V_{(BR)DSS}$	700	V
Minimum bus voltage	V_{CBmin}	90	V_{DC}

The input power of the converter is given by,

$$P_{INmax} = \frac{I_{OUTmax} \cdot V_{OUTmax}}{\eta} = \frac{4A \cdot 21V}{0.9} = \frac{84W}{0.9} = 93.3W$$

Equation 1

3.1 EMI filter, rectifier, and bulk capacitor

This section only shows how to determine the current stress of the EMI filter components and the rectifier, without focusing on achieving conducted EMI compliance.

3.1.1 Bulk capacitor C_B

As explained in [Appendix A: Rectification and bulk capacitor](#), the input current of a bridge rectifier followed by a bulk capacitor is anything else than sinusoidal. Therefore, it is not possible to determine the RMS input current directly from the input power and line voltage; several approximations need to be applied. A detailed derivation and explanation of the following equations can be found in Appendix A.

$$C_B > 93.3W \cdot \left(\frac{\arcsin\left(\frac{90V}{\sqrt{2} \cdot 90V}\right)}{\pi} + \frac{1}{2} \right) / (47Hz \cdot (2 \cdot (90V)^2 - (90V)^2)) = 183.9 \mu F$$

Equation 2

The first design step is to calculate the required minimum bulk capacitance that gives the specified minimum bus voltage V_{CBmin} , using [Equation 136](#).

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The next bigger standard value is **220 μF**. If a slightly lower value for V_{CBmin} is acceptable, a 180μF capacitor might be sufficient. However, it is essential to consider that the electrolytic capacitors typically have a tolerance of up to 20% . Therefore, a 220μF capacitor is recommended to ensure a safe design margin.

The next step is to determine the time intervals t_1 and t_2 , which indicates the start and end times of line input current starting with [Equation 3](#).

$$t_2 = \frac{\arcsin\left(\frac{2 \cdot 93.3 \text{ W}}{2 \cdot 90^2 \text{ V}^2 \cdot 220 \text{ μF} \cdot 295.31 \text{ Hz}}\right)}{2 \cdot 295.31 \text{ Hz}} + \frac{1}{4 \cdot 47 \text{ Hz}} = 5.62 \text{ ms}$$

Equation 3

With a known t_2 value, determine t_1 by solving [Equation 134](#) by means of standard numerical methods, leading to $t_1 = 2.92 \text{ ms}$.

In each line half-wave, the input current starts to flow at 2.92 ms after zero crossing and stops at 5.62 ms. This results in a conduction angle (from [Equation 131](#)) of 45.7°, equivalent to a 'duty-cycle' $d_{IN} = 25.4\%$ of the period of input voltage.

Knowing t_1 , it is possible to determine V_{CBmin} at the minimum input frequency:

$$V_{CBmin} = 127.3 \text{ V} \cdot \sin(295.31 \text{ s}^{-1} \cdot 2.92 \text{ ms}) = 96.6 \text{ V}$$

Equation 4

This is higher than the target value of 90 V since the capacitor value is higher than calculated. If the calculations are repeated with a capacitor of maximum negative tolerance (176 μF in this case), the results will reveal that it is just right. Finally, use [Equation 129](#) and [Equation 132](#) to determine peak- and RMS input currents respectively.

$$I_{INpk} = 220 \text{ μF} \cdot 127.3 \text{ V} \cdot 295.3 \text{ s}^{-1} \cdot |\cos(295.31 \text{ s}^{-1} \cdot 2.92 \text{ ms})| + \frac{93.3 \text{ W}}{127.3 \text{ V} \cdot |\sin(295.31 \text{ s}^{-1} \cdot 2.92 \text{ ms})|} = 6.35 \text{ A}$$

Equation 5

$$I_{INrms} = 6.35 \text{ A} \cdot \sqrt{\frac{0.254}{3}} = 1.85 \text{ A}$$

Equation 6

The calculated values of 6.35 A peak and 1.85 A RMS are significantly higher than the expected for a pure sinusoidal input current of 1.47 A peak and 1.04 A RMS, respectively.

To specify the capacitor C_B completely, the ripple current I_{CBrip} flowing through it must be known. Although calculating I_{CBrip} appears to be complex at first, it can be determined based on the following facts:

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Universal input design

- Each of the currents delivered by the rectifier and drawn by the flyback can be decomposed into a pure DC- and AC-component.
- The RMS value of such a composite current is $I_{ACDcrms} = \sqrt{I_{ACrms}^2 + I_{DCrms}^2}$
- In steady state, the average current through a capacitor, which is the DC component, is zero.
- Hence, the ripple current through C_B is the geometric sum of the AC currents of the rectifier bridge and the flyback stage.

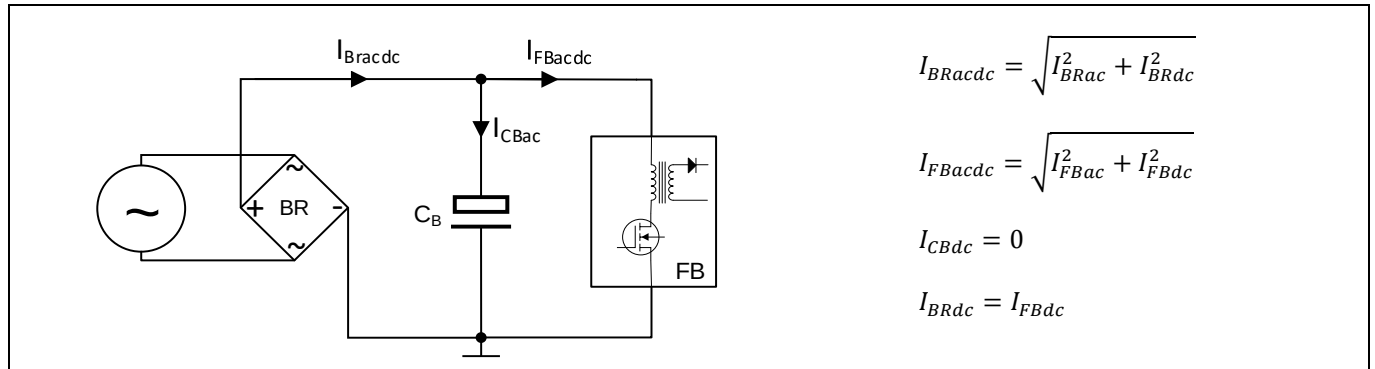


Figure 2 RMS currents in the input stage

Now the procedure should be clear. First, determine the respective RMS currents of bridge and flyback together with their DC components. Having these four values, the two pure AC values and finally the ripple current through C_B can be calculated.

Let us start the calculation with the bridge. The values for the peak and RMS currents are already known from [Equation 5](#) and [Equation 6](#) respectively, with $I_{BRpk} = 6.35 \text{ A}$ and $I_{BRrms} = 1.85 \text{ A}$, as well as the conduction angle. As before, it is assumed that the bridge current as triangular, with an average value of:

$$I_{BRdc} = I_{BRavg} = \frac{I_{BRpk}}{2} \cdot d_{IN} = \frac{6.35 \text{ A}}{2} \cdot 0.254 = \mathbf{0.81 \text{ A}}$$

Equation 7

As already mentioned, this is also the DC-component of the flyback input current, since there is no DC current in the capacitor. The AC-component, I_{BRac} , can be easily determined:

$$I_{BRac} = \sqrt{I_{BRacdc}^2 - I_{FBdc}^2} = \sqrt{(1.85 \text{ A})^2 - (0.81 \text{ A})^2} = \mathbf{1.66 \text{ A}}$$

Equation 8

Finally, the RMS input current of the flyback stage is required, which will be derived in a later section. The result from [Equation 23](#) is $I_{Q1rms} = I_{FBacdc} = \mathbf{1.4 \text{ A}}$. Then:

$$I_{FBac} = \sqrt{I_{FBacdc}^2 - I_{FBdc}^2} = \sqrt{(1.4 \text{ A})^2 - (0.81 \text{ A})^2} = \mathbf{1.14 \text{ A}}$$

Equation 9

These two pure AC currents finally make up the capacitor ripple current I_{CBrip} :

$$I_{CBrip} = \sqrt{I_{FBac}^2 + I_{BRac}^2} = \sqrt{(1.66 \text{ A})^2 + (1.14 \text{ A})^2} = \mathbf{2.0 \text{ A}}$$

Equation 10

As the capacitor ripple current is substantially large (Equation 10), it may be challenging to find capacitors that can handle such high ripple currents. Very likely you will have to use two capacitors of 100 μF and 120 μF in parallel.

3.1.2 Rectifier losses

As detailed in [Appendix C: Estimating diode forward loss](#), diode losses can be approximated by modelling the V-I characteristic of the diode with a constant voltage V_{Dfwd} in series with a resistor R_{Ddyn} . The methods of determining these two values are also explained in the appendix.

When modeling the bridge rectifier loss, it is essential to consider that each of the rectifier diodes only conducts half-waves, i.e., the conduction angle of each diode is only half of the previously calculated value: 22.9°, equivalent to a 0.127 duty cycle.

As mentioned above, the diode current is assumed to have a triangular shape. For a triangular shape, the average diode current I_{Davg} becomes:

$$I_{Davg} = \frac{I_{Dpk}}{2} \cdot \frac{d_{IN}}{2} = \frac{6.35 \text{ A}}{2} \cdot 0.127 = \mathbf{0.4 \text{ A}}$$

Equation 11

While the RMS value is given by,

$$I_{Drms} = 6.35 \text{ A} \cdot \sqrt{0.127/3} = \mathbf{1.31 \text{ A}}$$

Equation 12

At this point, it is necessary to select a bridge rectifier or alternatively four diodes and determine V_{Dfwd} and R_{Ddyn} from its datasheet. For example, consider a 1000 V and 4 A bridge rectifier. The V-I characteristic shown in the datasheet has a logarithmic Y-axis, but there is no need to convert it to a linear scale. For a diode forward current of 0.1 A, the forward voltage is about 0.76V, increasing to 0.92 V at a forward current of 4 A. Therefore, the differential resistance can be approximated by $R_D = (0.92 \text{ V} - 0.76 \text{ V}) / (4 \text{ A} - 0.1 \text{ A}) = \mathbf{0.041 \Omega}$ and $V_F = \mathbf{0.76 \text{ V}}$. This leads to an estimated loss of:

$$P_{BRloss} = 4 \cdot (0.76 \text{ V} \cdot 0.4 \text{ A} + 0.041 \Omega \cdot (1.31 \text{ A})^2) = \mathbf{1.51 \text{ W}}$$

Equation 13

It needs to be emphasized that the peak, RMS, and average values of the input current are approximations that neglect certain factors, such as the effect of common mode choke resistance and diode characteristics.

Universal input design

Although both the parameters help making the true input current a bit ‘smoother’, the approximation still provides a reasonably accurate estimate of the losses in the input stage.

3.1.3 EMI filter

The EMI filter chokes must be selected to handle the calculated peak currents without saturation. If saturation would occur, the inductance would decrease, and the filter performance would be compromised. At the same time, the resistive losses $I_{FILTrms}^2 \cdot R_{FILTdc}$ in the filter choke will be roughly four times of those which would be present with pure sinusoidal input.

Table 2 Summary of bridge rectifier input stage calculations

Parameter	Symbol	Value	Unit	Comment
Input power	P_{IN}	93.3	W	–
Input RMS current	I_{INrms}	1.85	A	Determines power loss of EMI chokes
Input peak current	I_{INpk}	6.35	A	EMI choke must not saturate at I_{INpk}
Bridge rectifier loss	P_{Lbr}	1.51	W	–
Bulk capacitor value	C_B	220	μF	–
Bulk capacitor voltage rating	V_{CB}	400	V	–
Bulk capacitor ripple current	I_{CBrip}	2.0	A	–

3.2 Flyback primary side

3.2.1 Transformer turns ratio, reflected voltage, and duty cycle

The transformer winding ratio (n) and the duty cycle (d) are interdependent, as evident from the steady-state volt-second balance of the transformer:

$$V_{IN} \cdot t_{ON} = n \cdot (V_{OUT} + V_D) \cdot t_{OFF} \Leftrightarrow \frac{1}{n} \cdot \frac{d}{1-d} = \frac{V_{OUT} + V_D}{V_{IN}}$$

Equation 14

In [Equation 14](#), V_D is the forward voltage of the output rectifier and the term “ $n \cdot (V_{OUT} + V_D)$ ” is the output voltage reflected to the input or simply “reflected voltage” V_R .

[Equation 14](#) reveals that the turn ratio ‘ n ’ must increase as the duty cycle ‘ d ’ increases, since the right-hand side of the equation is constant for a given V_{IN} . However, the larger ‘ n ’ results in a higher ‘ V_R ’, which is the voltage across the primary side of the transformer during the off-time of the MOSFET. As shown in [Figure 3](#) (left), this voltage V_R adds to the input voltage, thus increasing the maximum V_{DS} across the MOSFET during its off state.

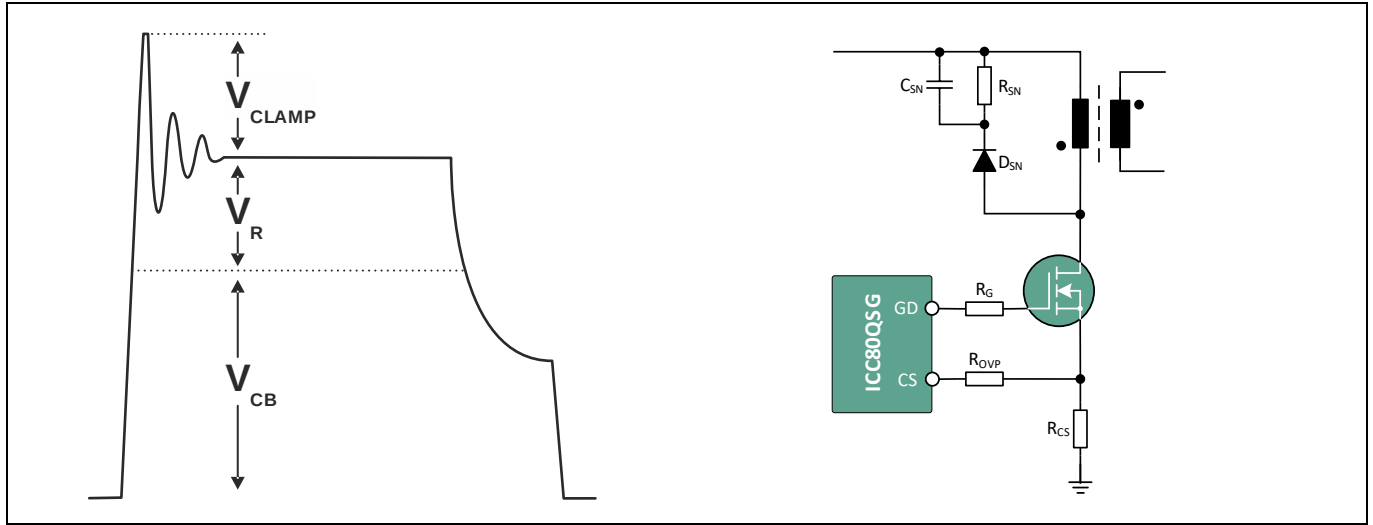


Figure 3 Simplified drain waveform of QR-Flyback (left) and drain clamping network (right)

In the case of QR-switching, a higher V_R leads to deeper valleys, resulting in a reduced turn-on loss of the MOSFET. Furthermore, with higher d_{max} and n , the MOSFETs RMS current will be lower, which in turn reduces the conduction losses.

In most designs, a compromise between the above two effects, higher V_{DSmax} versus lower losses needs to be met and the design might start with an estimation of the maximum tolerable V_R (i.e. $n \cdot V_{DSmax}$) is given by:

$$V_{DSmax} = V_{CBmax} + V_R + V_{CLAMP} = V_{INmax} \cdot \sqrt{2} + n \cdot (V_{OUT} + V_D) + V_{CLAMP}$$

Equation 15

It is generally a good practice to have a certain margin between V_{DSmax} and the MOSFET breakdown voltage $V_{(BR)DSS}$, and most often a 10% margin is used. The voltage V_{CLAMP} of the snubber network is typically chosen around 50% of V_R . That sets an upper boundary for 'n' in case a maximum $V_{(BR)DSS}$ of 700 V is selected, for example:

$$n \lesssim \frac{0.9 \cdot V_{(BR)DSS} - V_{INmax} \cdot \sqrt{2}}{1.5 \cdot (V_{OUT} + V_D)} = \frac{630 \text{ V} - 374.8 \text{ V}}{1.5 \cdot (21 \text{ V} + 0.7 \text{ V})} = 7.84$$

Equation 16

It can be challenging to achieve the desired turns ratio n with reasonable turns number. Probably, you may have to revisit this point and chose a different 'n' value. However, start with a 'n' value closer to the value mentioned in Equation-13, **n = 7.8**. Then calculate the reflected voltage V_R as:

Universal input design

$$V_R = n \cdot (V_{OUT} + V_D) = 7.8 \cdot 21.7 \text{ V} = 169.3 \text{ V}$$

Equation 17

Next, calculate the related maximum duty-cycle d_{max} that will occur at maximum load and minimum input voltage:

$$d_{max} = \frac{V_R}{V_{CBmin} + V_R} = \frac{169.3 \text{ V}}{(96.6 \text{ V} + 169.3 \text{ V})} = 0.637$$

Equation 18

Now, a minimum switching frequency f_{SWmin} needs to be assumed that will occur at minimum input voltage and maximum load. There is no straightforward way to determine an optimum switching frequency. In general, the transformer will be smaller at higher f_{SW} , but the switching losses as well as losses in core material and windings will increase. Especially for QR control, it is important to consider that f_{SW} will generally increase with lower output voltage and lower load. The ICC80QSG will increase the frequency until about $0.1 \cdot t_{ONmax}$ is reached, i.e., about ten times, before it changes to DCM and turns on in the second valley. Details of the on-time mapping can be found in the [datasheet \[1\]](#).

To keep a reasonably low maximum switching frequency before the valley change, f_{SWmin} is typically selected in the range of 40 to 50 kHz for most designs, although it is not strictly limited to this range. For this design, a value of 45 kHz has been chosen for f_{SWmin} . With this value, the on-time for full output power, t_{ONfp} , can be calculated.

$$t_{ONfp} = \frac{d_{max}}{f_{SWmin}} = \frac{0.628}{45 \text{ kHz}} = 14.15 \text{ } \mu\text{s}$$

Equation 19

The input current of the flyback is triangular, and its mean value must be equal to P_{IN}/V_{CB} . This allows to determine the maximum primary peak current I_{Q1pk} , which will occur at full power and minimum input voltage:

$$I_{Q1pk} = \frac{2 \cdot P_{INmax}}{V_{CBmin} \cdot d_{max}} = \frac{2 \cdot 93.3 \text{ W}}{96.6 \text{ V} \cdot 0.637} = 3.04 \text{ A}$$

Equation 20

3.2.2 Transformer design

Knowing the peak primary current, the primary main winding inductance L_p can be defined and calculated as:

$$L_p = \frac{V_{CBmin} \cdot t_{ONfp}}{I_{Q1pk}} = \frac{96.6 \text{ V} \cdot 14.15 \text{ } \mu\text{s}}{3.04 \text{ A}} = 450.3 \text{ } \mu\text{H}$$

Equation 21

Since the transformer is a customized device with relatively high tolerance, the calculated value (L_p) can be directly used. However, in a QR flyback converter, the actual frequency will be, due to the resonant period, somewhat lower than the desired one. To account for this, it is recommended to reduce the calculated inductance by about 5% and use the resulting value, $L_p = 430 \text{ } \mu\text{H}$.

For the transferred power, a PQ 32/30 core with a magnetic cross section A_e of 154 mm^2 seems to be well suited. The selected material, N97 by TDK, has a saturation flux density B_s (100 °C) of 410 mT, as specified in the datasheet. The value at 100 °C has to be used because, depending on the thermal environment, the transformer very likely needs to operate properly at such temperatures. Now, the value of 'N_p' can be determined:

$$N_p \geq \frac{L_p \cdot I_{Q1pk}}{A_e \cdot B_s \cdot D_F} = \frac{430 \text{ } \mu\text{H} \cdot 3.04 \text{ A}}{154 \cdot 10^{-6} \text{ m}^2 \cdot 0.41 \text{ T} \cdot 0.9} = 23.0$$

Equation 22

In [Equation 22](#), the term "D_F" is a derating factor ranging from 0.85 to 0.95 to ensure the maximum flux density is well below B_s (100 °C) for normal operating conditions. As a starting point, select a value in the middle of the range, i.e., $D_F = 0.9$.

Now, select the value of $N_p \geq 23.0$ and determine N_s accordingly to achieve a ratio of 7.8. A reasonable integer ratio that comes close to 7.8 is $23/3 = 7.66$, which is only about 1.8 % smaller than the target value.

Select **N_p = 23** and **N_s = 3**

3.2.2.1 RMS currents

The currents in the transformer windings as well as in the MOSFET and the secondary side rectifier have triangular shape and RMS values can be calculated easily.

The primary side peak currents were previously determined in [Equation 20](#). The RMS currents of transformer primary side and MOSFET can now be calculated as follows:

$$I_{PRIrms} = I_{Q1rms} = I_{Q1pk} \cdot \sqrt{\frac{d_{max}}{3}} = 3.04 \text{ A} \cdot \sqrt{\frac{0.637}{3}} = 1.4 \text{ A}$$

Equation 23

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Universal input design

On the secondary side, the transformer and diode currents are:

$$I_{SECrms} = I_{D2rms} = I_{Q1pk} \cdot n \cdot \sqrt{\frac{(1-d_{max})}{3}} = 23.7 \text{ A} \cdot \sqrt{\frac{0.363}{3}} = \mathbf{8.24 \text{ A}}$$

Equation 24

There is no simple recipe for proper selection of wire diameter. As a starting point, assume a current density of about 5 A/mm². At higher switching frequencies above 50 kHz, not the whole copper area will be conducting due to the skin effect and more significantly, the proximity effect. To mitigate the copper losses, it is necessary to use paralleled strands of thinner wires or even litz wire.

With the above-mentioned RMS currents, a copper area of about $1.4 \text{ A} / 5 \text{ A} \cdot \text{mm}^{-2} = \mathbf{0.28 \text{ mm}^2}$ will be needed for the primary and $8.24 \text{ A} / 5 \text{ A} \cdot \text{mm}^{-2} = \mathbf{1.65 \text{ mm}^2}$ for the secondary winding, i.e., diameters of 0.6 mm and 1.45 mm, respectively. Especially, the diameter of the secondary wire leads to skin and proximity effects at relative low frequencies. Apart from that, its stiffness makes it difficult to handle. For the actual transformer construction, six paralleled wires with an individual area of 0.28 mm² has been used.

To reduce transformer leakage inductance for low MOSFET voltage spike $V_{SPIKE-FET}$, transformer design with interleaved construction (Figure 4) is highly recommended.

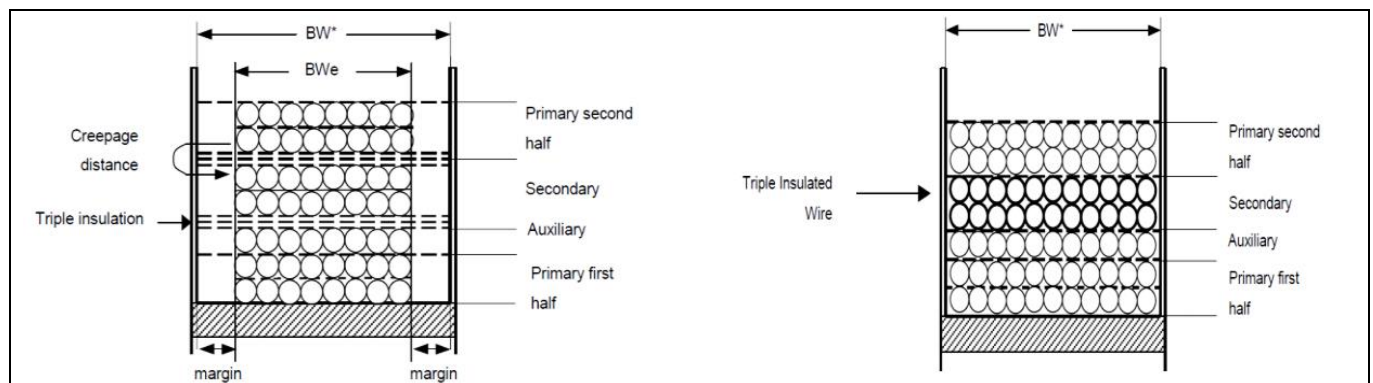


Figure 4 Transformer design with sandwich construction

3.2.2.2 Summary Transformer

Table 3 Transformer specification

Parameter	Value	Unit	Comment
Bobbin winding cross section AW	47	mm ²	–
Peak flux density	370	mT	90% of B _s (100°C)
Inductance	430	μH	–
Primary number of turns N _P	23	–	–
Secondary number of turns N _S	3	–	–
V _{CC} winding number of turns N _{VCC}	3	–	Forward direction
Primary side RMS current	1.4	A	–
Secondary side RMS current	8.24	A	–
Primary winding wire diameter	0.6	mm	–
Secondary winding wire diameter	6 x 0.6	mm	–

Universal input design

Parameter	Value	Unit	Comment
Bobbin winding cross section AW	47	mm ²	–
V _{CC} winding wire diameter	0.1	mm	–

3.2.3 MOSFET selection and snubber design

The design so far assumes a MOSFET maximum drain voltage $V_{(BR)DSS}$ of 700V. Now, determine the proper $R_{DS(ON)}$ for a given or desired power loss.

The power losses of the MOSFET can be divided into conduction losses and the switching losses. An easy first-pass guideline is to assume that total loss is equally distributed to 50 percent conduction loss and 50 percent switching loss.

$$P_{Q1loss(tot)} = P_{Q1loss(con)} + P_{Q1loss(sw)} \cong 2 \cdot P_{Q1loss(con)}$$

Equation 25

In case total power loss $P_{Q1loss(tot)}$ is given, the maximum acceptable $R_{DS(on)}$ can be determined using the following equation:

$$R_{DS(ON)}(100^{\circ}C) \leq \frac{P_{Q1loss(tot)}}{2 \cdot I_{Q1rms}^2}$$

Equation 26

[Equation 23](#) gives the maximum $R_{DS(ON)}$ value at elevated temperatures in the range of 80°C to 100°C, rather than the typical value at 25 °C found in the datasheet. This is because the MOSFETs temperature will increase during operation, causing the $R_{DS(ON)}$ rises as well. As a rule of thumb, it is assumed that the 100 °C $R_{DS(ON)}$ is approximately double the value at 25 °C.

If a maximum permissible MOSFET loss is assumed to be of 2 W, then the $R_{DS(ON)}(100^{\circ}C)$ should be less than:

$$R_{DS(ON)}(100^{\circ}C) \leq \frac{2 \text{ W}}{2 \cdot (1.41 \text{ A})^2} = 0.51 \, \Omega$$

Equation 27

The IPA70R360P7S, with an $R_{DS(ON)}(25^{\circ}C)$ of 0.36 Ω , comes close to this requirement and will be a good choice.

Now, IPA70R360P7S comes in a TO220 package having a $R_{\theta JA}$ of 80 K/W, resulting in a temperature increase of about 160 °C, which is totally unacceptable. Assuming maximum ambient of 45 °C and a tolerable maximum T_J of 120 °C, then the thermal resistance of an heatsink will be calculated as follows:

$$R_{\theta HS} \leq \frac{120^{\circ}C - 45^{\circ}C}{2 \text{ W}} = 37.5 \, \frac{K}{W}$$

Equation 28

Since the selected $R_{DS(ON)}$ might be a slightly high, choose a heatsink with smaller thermal resistance such as like 30 K/W.

Universal input design

The CoolMOS™ P7 MOSFET series from Infineon is well-suited to ICC80QSG applications due to its balance of high performance and reasonable cost. Through optimizing key parameters (C_{oss} , E_{oss} , Q_g , C_{iss} , and $V_{GS(th)}$), integrating a Zener diode for ESD protection and other measures, this product family fully addresses market concerns in performance, ease of use, and price/performance ratio. The 700 V, 800 V, and 950 V CoolMOS™ P7 MOSFET series have been specifically designed for flyback and PFC topologies.

3.2.3.1 Drain clamping network

The voltage across the drain-source of the power MOSFET is ideally a square wave with a plateau determined by the AC input voltage and the reflected output voltage.

During the turn-off transition of the power MOSFET, the current flow through the transformer's primary side stops. While most of the energy stored in the magnetic field is transferred to the secondary side, the energy trapped in the leakage inductance causes a voltage spike at the drain of the MOSFET. This, combined with the stray capacitance of the circuit, generates high-frequency, and high-amplitude oscillation. The resulting high-frequency voltage spike is seen rising above the plateau mentioned earlier and needs to be considered when determining the V_{DS} rating of the power MOSFET.

There are numerous methods to dampen the oscillation and reduce the voltage spike magnitude. In this document, the RCD clamping circuit is explained, which is shown in [Figure 3](#).

The energy trapped in the leakage inductance is transferred into the capacitor C_{Sn} via diode D_{Sn} , and finally dissipated in resistor R_{Sn} .

Actually, the dissipated energy is higher than that of the energy stored in the leakage inductance by a factor $\frac{(V_R + V_{Clamp})}{V_{Clamp}}$. This factor results from the circumstance that the voltage across the leakage inductance V_{Clamp} and the reflected voltage V_R are in series and both conduct the demagnetization current of the leakage inductance.

$$P_{Snub} = \frac{L_{LK} \cdot I_{Q1pk}^2 \cdot f_{SW}}{2} \cdot \frac{V_R + V_{Clamp}}{V_{Clamp}}$$

Equation 29

If the sandwich transformer construction as proposed in [Figure 4](#) is used, the leakage inductance can be reduced to as low as 1% of L_p . Initially, it was assumed that V_{Clamp} is 50% of V_R . Then, the snubber loss P_{Snub} becomes:

$$P_{Snub} \cong \frac{4.5 \mu H \cdot (3.04 A)^2 \cdot 45 kHz}{2} \cdot \frac{1.5 \cdot V_R}{0.5 \cdot V_R} = 2.81 W$$

Equation 30

The actual power dissipation will be somewhat lower than the calculated value since part of the energy is transferred to the output capacitance of the MOSFET and parasitic capacitances of the system.

The value of the resistor R_{Sn} is based on P_{Snub} that needs to be dissipated by R_{Sn} . Assuming a reasonably constant voltage across the clamp network, its value can be determined by:

$$R_{Sn} \cong \frac{(V_R + V_{Clamp})^2}{P_{Snub}} = \frac{(1.5 \cdot 169.3 \text{ V})^2}{2.81 \text{ W}} = \mathbf{23.0 \text{ k}\Omega}$$

Equation 31

To calculate the value of the capacitor, the maximum allowed ripple voltage V_{Rip} must be specified. Let's assume it to be 30 percent in this calculation:

$$C_{Sn} = \frac{V_R + V_{Clamp}}{V_{Rip} \cdot R_{Sn} \cdot f_{SW}} = \frac{1}{0.3 \cdot 23.0 \text{ k}\Omega \cdot 45 \text{ kHz}} = \mathbf{3.2 \text{ nF}}$$

Equation 32

Due to parasitic capacitances mentioned earlier, the actual power dissipation will be smaller, which means the optimum resistance will be higher and the capacitance smaller than the values calculated above.

Nevertheless, equations [Equation 30](#) to [Equation 32](#) offer good starting points for an optimization.

3.2.4 Current sense resistor

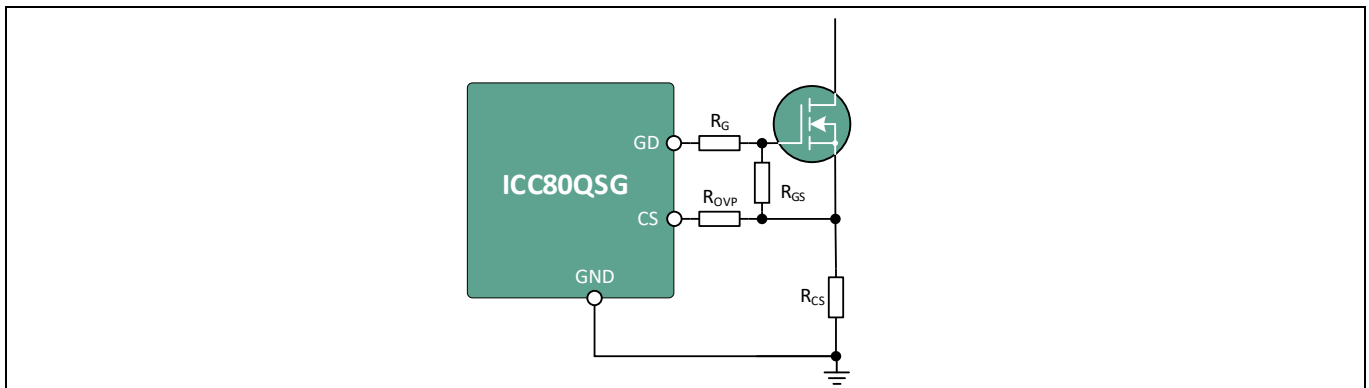


Figure 5 Overvoltage (OVP) and overcurrent (OCP) protection resistors

Select the OCP level such that in the worst case the required peak current I_{Q1pk} will not trigger the protection. The worst case is when the detection level V_{OCP1} is at the lower end of its specification. That means that the maximum value for R_{CS} is:

$$R_{CSmax} = \frac{V_{OCP1min}}{I_{Q1pk}} = \frac{0.57 \text{ V}}{3.04 \text{ A}} = \mathbf{0.188 \text{ }\Omega}$$

Equation 33

Although the power dissipation of the sense resistor is relatively small (~ 360 mW), such a low value is often realized by paralleling two or more resistors.

Even if the OVP feature described in [Section 6.7](#) is not used, it is advised to connect a resistor from the CS pin to the source of the MOSFET. The size of the resistor should be a few 100 ohms smaller than the resistor calculated for OVP. This helps to limit the occurring voltage spikes on this pin.

The resistor R_{GS} is to ensure that the MOSFET remains in an off-state when AC input is applied, with the IC not being activated yet. A value of $R_{GS} = \mathbf{10 \text{ k}\Omega}$ is a reasonable choice.

Universal input design

The resistor R_G is placed in series with the power MOSFETs' gate pin to damp the gate-rise oscillation, and to control switching speed to a certain degree. With the high-speed switching characteristics of CoolMOS™ P7 MOSFET, which reduce the switching losses, it is recommended to start with a gate resistor R_G of **20 to 50 Ω** . For a faster switching, MOSFETs with higher gate charge than CoolMOS™ P7 will need a lower resistance R_G .

The gate-drive peak voltage, $V_{GD,pk}$, is typically 11 V with a sufficient V_{CC} voltage supply. To achieve a good balance of switching loss and EMI, the gate voltage rising and falling slope can be modified by using external components around the MOSFET, including the gate resistance. More information can be found in the [CoolMOS™ P7 MOSFET](#) application note.

3.3 Flyback secondary side

3.3.1 Secondary side diode selection

To select a proper rectifier diode, it is necessary to calculate the maximum reverse voltage V_{D2max} :

$$V_{D2max} = V_{OUT} + \frac{V_{CBmax}}{n} + V_{DSSpike}$$

Equation 34

The additional term $V_{DSSpike}$ results from the fact that the turn-off of the diode provokes oscillations of the parasitic capacitances and inductances of the circuit. Although an RC network across the diode can, and sometimes must, be used to damp these voltage spikes, it is wise to assume that $V_{DSSpike}$ is 50% of the sum of the other two voltages.

$$V_{D2max} = 1.5 \cdot \left(V_{OUT} + \frac{V_{CBmax}}{n} \right) = 1.5 \cdot \left(21 \text{ V} + \frac{374.8 \text{ V}}{7.8} \right) = \mathbf{103.6 \text{ V}}$$

Equation 35

The peak secondary winding current, which is at the same time the peak diode current, as well as the RMS current have been calculated in [Equation 24](#). Hence, $I_{D2pk} = \mathbf{23.67 \text{ A}}$ and $I_{D2rms} = \mathbf{8.24 \text{ A}}$ and finally $I_{D2avg} = I_{OUT} = \mathbf{4 \text{ A}}$.

Based on the calculated voltages and current, select the 100 V Schottky diode with the forward current capability ranging between 16 to 20 A. Although the calculated maximum voltage is 103.6 V, a 100 V Schottky diode is still suitable due to the 50% safety margin included in [Equation 35](#). Moreover, the forward voltage of a 100 V Schottky diode is lower than that of an ultrafast PN diode, but higher than that of a low-voltage Schottky diode.

A 150 V diode would have an even higher forward voltage at the given current, which would increase losses further. Selecting a higher current rating for the Schottky diode helps to reduce the forward voltage and losses at the actual operating point.

Assuming the selection of **MBRL20100CT**, a 100 V / 20 A low V_F Schottky diode, the datasheet estimates $V_F \approx \mathbf{0.35 \text{ V}}$ and $R_D \approx \mathbf{50 \text{ m}\Omega}$. This results in an approximate power loss of:

$$P_{D2} = V_F \cdot I_{Davg} + R_D \cdot I_{Drms}^2 = 0.35 \text{ V} \cdot 4 \text{ A} + 50 \text{ m}\Omega \cdot (8.24 \text{ A})^2 = \mathbf{4.8 \text{ W}}$$

Equation 36

The calculated values once again demonstrate that the rectifiers are among the primary contributors to losses. Implementing a synchronous rectification stage would significantly improve the efficiency and thermal

Universal input design

performance of the charger. Given the calculated power dissipation, a heat sink will be necessary to ensure reliable operation of the diode.

3.3.2 Rectifier diode snubber network

To reduce voltage stress and EMI emissions, add an RC network (snubber) across the diode to dampen parasitic oscillations. The snubber resistor value can be determined through an empirical process involving the following steps:

- With an oscilloscope, measure the reverse voltage across the rectifier diode and determine the frequency f_0 of the parasitic oscillation (ringing) when the reverse voltage has built up.
- Next, add a capacitor C_{SN} of about three times C_D , the reverse capacitance of the diode, in parallel with the diode. This should be roughly half f_0 . In this case, if the value of C_D is not provided in the diode's datasheet, then empirically determine the value of the capacitor C_{SN} that halves f_0 .
- The theoretical optimum for the snubber resistor is then $R_{SN} = \frac{2}{2 \cdot \pi \cdot f_0 \cdot C_{SN}}$

The above calculated value will give the best damping of the ringing, but it also results in the highest power dissipation. If the losses caused by the snubber are unacceptable high, a compromise can be reached by using a slightly higher resistance than calculated, resulting in worse damping but lower losses.

3.3.3 Secondary side filter capacitor

Essentially, the following two parameters define the filter capacitor:

- Maximum output voltage
- Ripple current

It is essential to ensure that the rated voltage of the capacitor needs to be higher than the maximum possible output voltage, taking in account of potential failures in the regulation loop and resulting overvoltage. In a later chapter, you will learn how to set the output overvoltage protection (OVP) level to, for example, 30 V. Therefore, a 35 V electrolytic capacitor would be perfect for the application.

In most switch mode power supplies, the value of the output filter capacitor is determined by the high-frequency ripple current it can handle. Typically, the capacitance value required to handle the ripple current is sufficient to fulfill all the other requirements such as peak power requirements.

The maximum ripple current through the capacitor occurs with maximum output power is calculated as follows:

$$I_{C2rms} = \sqrt{I_{D2rms}^2 - I_{OUT}^2} = \sqrt{(8.24 \text{ A})^2 - (4 \text{ A})^2} = 7.2 \text{ A}$$

Equation 37

It is challenging to find a single capacitor that can handle the required ripple current, and it will be necessary to place several capacitors in parallel. For example, the Rubycon ZLH series or the series of other suppliers that can be considered. With a rated voltage of 35 V, use four 560 μF capacitors, providing a ripple current capability of 7.84 A.

4 Design with input voltage doubler configuration

As an example, we design an input voltage doubler stage with the following parameters.

Table 4 Example design target data for input voltage doubler

Parameter	Symbol	Value	Unit
Minimum input voltage	V_{INmin}	90	V_{RMS}
Maximum input voltage	V_{INmax}	135	V_{RMS}
Minimum line frequency	f_{Lmin}	47	Hz
Minimum bus voltage	V_{CBmin}	210	V

Note: Any other parameter not mentioned here will be the same as before.

4.1 EMI filter, rectifier, and bulk capacitor

4.1.1 Bulk capacitors

First, determine the approximate values that are needed for C_1 and C_2 to achieve the desired minimum bus voltage, using [Equation 141](#).

$$C_1 = C_2 \approx \frac{93.3 \text{ W} \cdot \left(\frac{\sin\left(\frac{210 \text{ V}}{2 \cdot 127.3 \text{ V}}\right)}{\pi} + \frac{3}{2} \right)}{2 \cdot 47 \text{ Hz} \cdot (127.3^2 - 105^2) \text{ V}^2} = 347.0 \text{ } \mu\text{F}$$

Equation 38

As explained in [Appendix A: Rectification and bulk capacitor](#), use the next smaller standard value, i.e., **330 μF** in this case. Now, use this value and [Equation 138](#) to determine t_4 ($t_4 = 24.5 \text{ ms}$) and t_1 respectively ($t_1 = 3.2 \text{ ms}$), and then use [Equation 139](#) to find the minimum bus voltage V_{BUSmin} .

$$V_{CBmin} \cong 127.3 \text{ V} \cdot \sin(2 \cdot \pi \cdot 47 \text{ Hz} \cdot 24.5 \text{ ms}) + \left(127.3^2 \text{ V}^2 - \frac{93.3 \text{ W}}{330 \text{ } \mu\text{F}} \cdot (24.5 \text{ ms} - 15.9 \text{ ms}) \right) = 221.2 \text{ V}$$

Equation 39

The calculated minimum bus voltage turns out to be slightly higher than intended for the design. A quick calculation reveals that with 220 μF , the next smaller capacitor value from the E6 series, would result in V_{CBmin} of 204.2 V, which is lower than the intended. Consider the possible -20% tolerance of electrolytic capacitors, it becomes clear that a 330 μF capacitor is a right choice.

You may still want to consider whether a lower V_{CBmin} is acceptable. The only way to find this out is to start the design of the flyback stage and evaluate the implications of lowering the V_{CBmin} . As you will see, a lower minimum bus voltage goes with higher peak and RMS MOSFET current i.e., you potentially need to use a lower $R_{DS(on)}$ MOSFET for a certain loss budget. However, that is already a matter of design optimization and therefore let us stay with 330 μF .

ICC80QSG QR flyback controller for battery charger applications of up to 120 W



Design with input voltage doubler configuration

The remaining key design parameters are now calculated in a similar manner to the bridge rectifier case, without much additional explanation.

Peak bus voltage with minimum and maximum input voltages are as follows:

$$V_{CBpk} \cong 127.3 \text{ V} + \sqrt{(127.3 \text{ V})^2 - \frac{93.3 \text{ W}}{330 \mu\text{F} \cdot 2 \cdot 47 \text{ Hz}}} = \mathbf{242.13 \text{ V}}$$

Equation 40

$$V_{CBmaxpk} \cong 190.9 \text{ V} + \sqrt{(190.9 \text{ V})^2 - \frac{93.3 \text{ W}}{330 \mu\text{F} \cdot 2 \cdot 47 \text{ Hz}}} = \mathbf{373.75 \text{ V}}$$

Equation 41

Peak input current:

$$I_{INpk} = 330 \mu\text{F} \cdot 127.3 \text{ V} \cdot 295.3 \frac{1}{\text{s}} \cdot \left| \cos \left(295.3 \frac{1}{\text{s}} \cdot 24.5 \text{ ms} \right) \right| + \frac{93.3 \text{ W}}{2 \cdot 127.3 \text{ V} \cdot \left| \sin \left(295.3 \frac{1}{\text{s}} \cdot 24.5 \text{ ms} \right) \right|} = \mathbf{7.63 \text{ A}}$$

Equation 42

Input conduction duty cycle (equivalent to conduction angle):

$$dc_{IN} = 2 \cdot \left(\frac{T}{4} - t_1 \right) \cdot f_{Line} = 2 \cdot (5.3 \text{ ms} - 3.2 \text{ ms}) \cdot 47 \text{ Hz} = \mathbf{19.6\%}$$

Equation 43

RMS input current:

$$I_{INrms} = I_{INDou,pk} \cdot \sqrt{\frac{dc_{INDou}}{3}} = 7.62 \cdot \sqrt{\frac{0.196}{3}} = \mathbf{1.95 \text{ A}}$$

Equation 44

RMS current flows through D₁/D₂:

$$I_{D1rms} = I_{D2rms} = I_{INpk} \cdot \sqrt{\frac{dc_{IN}}{2} \cdot \frac{1}{3}} = 7.62 \cdot \sqrt{\frac{0.196}{6}} = \mathbf{1.38 \text{ A}}$$

Equation 45

ICC80QSG QR flyback controller for battery charger applications of up to 120 W



Design with input voltage doubler configuration

DC component of the above current:

$$I_{D1dc} = I_{D2dc} = \frac{93.3 \text{ W}}{221.2 \text{ V}} = \mathbf{0.422 \text{ A}}$$

Equation 46

Pure AC component of diode current:

$$I_{D1acrms} = I_{D2acrms} = \sqrt{I_{C1rms}^2 - I_{C1dc}^2} = \sqrt{(1.38 \text{ A})^2 - (0.422 \text{ A})^2} = \mathbf{1.31 \text{ A}}$$

Equation 47

As in the bridge rectifier case, for the AC component drawn out from C₁ and C₂ the RMS input current of the flyback stage is required, which will be calculated in a later section. The result from Equation 60 is I_{FLYrms} = 0.74 A. Then:

$$I_{FLYacrms} = \sqrt{I_{FLYrms}^2 - I_{FLYdcrms}^2} = \sqrt{(0.74 \text{ A})^2 - (0.422 \text{ A})^2} = \mathbf{0.608 \text{ A}}$$

Equation 48

These two pure AC currents finally make up the capacitor ripple current I_{CBrip}.

$$I_{CBrip} = \sqrt{I_{FLYrms}^2 + I_{INacrms}^2} = \sqrt{(1.31 \text{ A})^2 + (0.608 \text{ A})^2} = \mathbf{1.44 \text{ A}}$$

Equation 49

This ripple current is considerably smaller than in the bridge rectifier case and there will be a larger selection of capacitors readily available that can handle it.

4.1.2 Rectifier diode selection and losses

As above, we assume that the diode current has a triangular shape. For a triangular shape the average diode current I_{Davg} becomes,

$$I_{Dxavg} = \frac{I_{Dxpk}}{2} \cdot \frac{d_{IN}}{2} = \frac{7.63 \text{ A} \cdot 0.196}{4} = \mathbf{0.374 \text{ A}}$$

Equation 50

While the RMS value is **1.38 A** (Equation 45).

If the selected bridge is same 1000 V bridge as before, then the estimated losses are as follows:

$$P_{BRloss} = 2 \cdot (0.76 \text{ V} \cdot 0.374 \text{ A} + 0.041 \Omega \cdot (1.38 \text{ A})^2) = \mathbf{0.725 \text{ W}}$$

Equation 51

4.1.3 EMI Filter

The EMI filter chokes must be selected such that they can handle the above calculated peak currents without saturation. If saturation would occur, the inductance would decrease, and the filter performance would be compromised. At the same time, the resistive losses $I_{FILTrms}^2 \cdot R_{FILTdc}$ in the filter choke will be roughly four times of those which would be present with pure sinusoidal input.

4.2 Flyback primary side

4.2.1 Transformer turns ratio, reflected voltage and duty cycle

The transformer turns ratio is calculated by determining an upper boundary based on the maximum breakdown voltage of the MOSFET, with a suitable safety margin applied.

$$n \lesssim \frac{0.9 \cdot V_{(BR)DSS} - V_{INmax} \cdot \sqrt{2}}{1.5 \cdot (V_{OUT} + V_D)} = \frac{630 \text{ V} - 373.75 \text{ V}}{1.5 \cdot (21 \text{ V} + 0.7 \text{ V})} = \mathbf{7.87}$$

Equation 52

Not surprisingly this is the same as with bridge rectifier input and therefore select the same turns ratio as before: **n = 7.8**. Consequently, the reflected voltage V_R is the same as before:

$$V_R = n \cdot (V_{OUT} + V_D) = 7.8 \cdot 21.7 \text{ V} = \mathbf{169.3 \text{ V}}$$

Equation 53

But, since the minimum input voltage to the flyback stage has changed, maximum duty-cycle d_{max} is different:

$$d_{max} = \frac{V_R}{V_{CBdounmin} + V_R} = \frac{169.3 \text{ V}}{(221.2 \text{ V} + 169.3 \text{ V})} = \mathbf{0.433}$$

Equation 54

With the same f_{SWmin} of 45 kHz, the t_{ONfp} is calculated to be:

$$t_{ONfp} = \frac{d_{max}}{f_{SWmin}} = \frac{0.433}{45 \text{ kHz}} = \mathbf{9.63 \mu s}$$

Equation 55

Finally, the MOSFET peak current I_{Q1pk} at full power and minimum input voltage is almost halved:

$$I_{Q1pk} = \frac{2 \cdot P_{INmax}}{V_{CBdounmin} \cdot d_{max}} = \frac{2 \cdot 93.3 \text{ W}}{221.2 \text{ V} \cdot 0.433} = \mathbf{1.95 \text{ A}}$$

Equation 56

4.2.2 Transformer design

The selected value of L_p is calculated as follows:

$$L_p = \frac{V_{CBmin} \cdot t_{ONmax}}{I_{Q1pk}} = \frac{221.2 \text{ V} \cdot 9.63 \mu\text{s}}{1.95 \text{ A}} = \mathbf{1.09 \text{ mH}}$$

Equation 57

Using the same core as before (PQ3230) the minimum number of primary turns becomes:

$$N_p \geq \frac{L_p \cdot I_{Q1pk}}{A_e \cdot B_s \cdot D_F} = \frac{1.09 \text{ mH} \cdot 1.95 \text{ A}}{154 \cdot 10^{-6} \text{ m}^2 \cdot 0.41 \text{ T} \cdot 0.9} = \mathbf{37.3}$$

Equation 58

It is found that $N_p = 39$ turns and $N_s = 5$ turns lead to the desired turns ratio of $n = 7.8$.

$$N_s = \frac{N_p}{n} = \frac{39}{7.8} = \mathbf{5}$$

Equation 59

4.2.2.1 RMS currents

The RMS currents of transformer primary side and MOSFET are:

$$I_{PRIrms} = I_{Q1rms} = I_{Q1pk} \cdot \sqrt{\frac{d_{max}}{3}} = 1.95 \text{ A} \cdot \sqrt{\frac{0.433}{3}} = \mathbf{0.74 \text{ A}}$$

Equation 60

On the secondary side, the transformer and diode currents are:

$$I_{SECrms} = I_{D2rms} = I_{Q1pk} \cdot n \cdot \sqrt{\frac{(1-d_{max})}{3}} = 15.21 \text{ A} \cdot \sqrt{\frac{0.567}{3}} = \mathbf{6.6 \text{ A}}$$

Equation 61

With the above-mentioned RMS currents, a copper area of about $0.748 \text{ A} / 5 \text{ A} \cdot \text{mm}^{-2} = \mathbf{0.15 \text{ mm}^2}$ will be needed for the primary and $6.6 \text{ A} / 5 \text{ A} \cdot \text{mm}^{-2} = \mathbf{1.36 \text{ mm}^2}$ for the secondary winding, i.e., diameters of 0.45 mm and 1.32 mm, respectively. Especially, the diameter of the secondary wire leads to skin and proximity effects even at relatively low frequencies. Apart from that, its stiffness makes it difficult to handle. Therefore, it is recommended to split primary and secondary into parallel strand of thinner wires.

4.2.2.2 Transformer specification summary

Table 5 Transformer specification

Core magnetic cross section A_e	154.2	mm ²	PQ 32/30
Bobbin winding cross section AW	47	mm ²	–
Peak flux density	370	mT	90% of $B_s(100^\circ\text{C})$
Inductance	1.09	mH	–
Primary number of turns N_p	39	–	–
Secondary number of turns N_s	5	–	–
V_{CC} winding number of turns N_{VCC}	3	–	Forward direction
ZCD winding number of turns N_{ZCD}	3	–	Flyback direction
Primary side RMS current	0.763	A	–
Secondary side RMS current	6.71	A	–
Primary winding wire diameter	0.45	mm	–
Secondary winding wire diameter	6 x 0.5	mm	–
V_{CC} winding wire diameter	0.1	mm	–

4.2.3 MOSFET selection and snubber design

Assuming an identical loss budget as for the universal input design, the required $R_{DS(ON)}$ is approximately:

$$R_{DS(ON)}(100^\circ\text{C}) \leq \frac{P_{Q1loss(tot)}}{2 \cdot I_{Q1rms}^2} = \frac{2 \text{ W}}{2 \cdot (0.74 \text{ A})^2} = \mathbf{1.83 \Omega}$$

Equation 62

While the IPA70R900P7S might seem like an obvious choice for the MOSFET, a better option would be to consider an alternative

For instance, selecting **IPN70R450P7S** would reduce losses by half, eliminating the need for a heatsink. This easily compensates the higher cost for lower $R_{DS(ON)}$ MOSFETs.

4.2.3.1 Drain clamping network

The snubber loss P_{Snub} becomes:

$$P_{Snub} \cong \frac{10.9 \mu\text{H} \cdot (1.95 \text{ A})^2 \cdot 45 \text{ kHz}}{2} \cdot \frac{1.5 \cdot V_R}{0.5 \cdot V_R} = \mathbf{2.6 \text{ W}}$$

Equation 63

Snubber losses are almost identical to the previous design since the higher primary side inductance almost cancels the effect of the lower primary current. Therefore, the same values for R_{Sn} and C_{Sn} can be used.

4.2.4 Current sense resistor

The maximum value for R_{CS} is:

$$R_{CSmax} = \frac{V_{OCP1min}}{I_{Q1pk}} = \frac{0.57 \text{ V}}{1.95 \text{ A}} = \mathbf{0.292 \text{ } \Omega}$$

Equation 64

4.3 Secondary side filter capacitor

The capacitor ripple current is:

$$I_{C2rms} = \sqrt{I_{D2rms}^2 - I_{OUT}^2} = \sqrt{(6.6 \text{ A})^2 - (4.0 \text{ A})^2} = \mathbf{5.25 \text{ A}}$$

Equation 65

As previously discussed, place several capacitors in parallel. Use the same three 560 μF / 35 V Rubycon ZLH series as before and get a ripple current capability of 5.88 A.

4.4 Secondary-side diode selection

To select a proper rectifier diode, calculate the maximum reverse voltage V_{D2max} :

$$V_{D2max} = V_{OUT} + \frac{V_{CBmax}}{n} + V_{DSspike}$$

Equation 66

The additional term $V_{DSspike}$ results from the diode's turn-off, which triggers oscillations of the circuit's parasitic capacitances and inductances. Although these can, and sometimes must, be damped by an RC network across the diode, it is wise to assume that $V_{DSspike}$ is 50% of the sum of the other two voltages.

$$V_{D2max} = 1.5 \cdot \left(V_{OUT} + \frac{V_{CBmax}}{n} \right) = 1.5 \cdot \left(21 \text{ V} + \frac{374.8 \text{ V}}{7.8} \right) = \mathbf{101.76 \text{ V}}$$

Equation 67

The peak secondary winding current, which is at the same time the peak diode current, as well as the RMS current have been calculated in. Hence, $I_{D2pk} = \mathbf{15.21 \text{ A}}$ and $I_{D2rms} = \mathbf{6.6 \text{ A}}$ and finally $I_{D2avg} = I_{OUT} = \mathbf{4 \text{ A}}$.

Based on the calculated voltages and current, select the 100 V Schottky diode with the forward current capability ranging between 16 to 20 A. The forward voltage of a 100 V Schottky diode is lower than that of an ultrafast PN diode, but higher than that of a low-voltage Schottky diode. Therefore, selecting a higher current rating helps to reduce forward voltage at the actual operating point, thereby minimizing losses.

Let us assume you selected **MBRL20100CT**, a 100 V / 20 A low V_F Schottky diode. From the device datasheet, you can estimate $V_F \approx \mathbf{0.35 \text{ V}}$ and $R_D \approx \mathbf{50 \text{ m}\Omega}$.

ICC80QSG QR flyback controller for battery charger applications of up to 120 W



Design with input voltage doubler configuration

Then, estimate the diode loss as follows:

$$P_{D2} = V_F \cdot I_{Davg} + R_D \cdot I_{Drms}^2 = 0.35 \text{ V} \cdot 4 \text{ A} + 50 \text{ m}\Omega \cdot (6.6 \text{ A})^2 = \mathbf{3.65 \text{ W}}$$

Equation 68

The calculated values once again demonstrate that the rectifiers are among the primary contributors to losses. Implementing a synchronous rectification stage would significantly improve the efficiency and thermal performance of the charger. Given the calculated power dissipation, a heat sink will be necessary to ensure reliable operation of the diode.

5 Comparison of universal input vs. voltage doubler solution

Table 6 shows a comparison of key parameters between the two solutions with different rectifier configurations.

Table 6 Key design parameters of different solutions

Parameter	Symbol	Value Doubler Input	Value Universal Input	Unit	Comment
Input RMS voltage	V_{IN}	90		V	—
Input power	P_{IN}	93.33		W	—
Input RMS current	I_{INrms}	1.95	1.85	A	—
Input peak current	I_{INpk}	7.63	6.35	A	—
Bulk capacitor value	C_B	2 x 330	220	μF	—
Bulk capacitor voltage rating	V_{CB}	200	400	V	—
Bulk capacitor ripple current	I_{CBrip}	1.44	2.0	A	—
Rectifier loss	$P_{RECTloss}$	0.725	1.51	W	—
MOSFET peak current	I_{Q1pk}	1.95	3.04	A	—
MOSFET RMS current	I_{Q1rms}	0.74	1.4	A	—
MOSFET resistance	V_{DSmax}	700		V	—
MOSFET resistance	$R_{DS(ON)}$	450	360	$m\Omega$	—
Heatsink for MOSFET	—	n.a.	30	K/W	—
Transformer size	—	PQ32/20		—	—
Secondary peak current	I_{DSpk}	15.21	23.67	A	—
Secondary RMS current	I_{DSrms}	6.6	8.24	A	—
Secondary diode loss	P_{DSloss}	3.65	4.80	W	MBRL20100CT
Secondary filter capacitors	—	3 x 560	4 x 560	μF	Rubycon ZLH
Secondary caps RMS ripple current	I_{RIP}	5.25	7.2	A	—

Not surprising, with the voltage doubler input, the input peak and RMS currents are about 20% and 5%, respectively, higher than those of the bridge rectifier input. This will result in slightly larger EMI filter chokes to prevent saturation and compensate for the higher ohmic losses. The potentially higher losses of the EMI filter will be at least partially compensated by the lower losses of the rectifier diodes, which are only half that of the bridge.

Although the two capacitors of the voltage doubler seem to be a disadvantage, their ripple current is much lower and a huge selection of capacitors that can handle this current is available. In contrast, the ripple current of the bridge rectifier is so high that, that splitting it into two caps seems almost unavoidable.

The main advantage of the voltage doubler approach comes from the flyback stage, where the higher input voltage results in lower currents. Unlike the universal input, this enables the use of a lower $R_{DS(on)}$ MOSFET, without the need for a heatsink.

Furthermore, the voltage doubler approach reduces the currents on both the primary side and secondary sides. The secondary side rectifier diode experiences a lower RMS current and consequently lower losses, enabling the use of a smaller and less expensive heat sink. The ripple current of the filter capacitors is reduced

Comparison of universal input vs. voltage doubler solution

considerably, and there are only three capacitors in parallel required to handle the ripple current, further reducing costs.

Overall, the voltage doubler is the most effective approach to handle worldwide input voltage requirements while enabling reduced component stress, with the exception of moderately increased input peak and RMS currents.

6 ICC80QSG

6.1 Auxiliary winding for V_{CC}

In applications with a wide output voltage range, such as battery chargers or LED lighting, generating the supply voltage for the control IC can be a challenge. The usual method is to use a separate transformer winding to provide the controller V_{CC} . If this is a flyback winding, then the voltage of this winding will be proportional to the output voltage and vary with the same factor as the latter. That means, if the output voltage changes by a factor of three, so will the controller supply voltage. Most controllers cannot handle such wide voltage variations and even the ICC80QSG, with its recommended V_{CC} range from 8 V to 24 V, would be operating at the limits of its specified range. Higher output voltage range would make an additional V_{CC} regulator necessary.

If the input voltage is single range or if the input voltage doubler is used to achieve wide range input, then using the transformer winding in the forward mode can solve the above issue. In that mode, the V_{CC} winding will be proportional to the input voltage instead. No matter whether the input is from 85 V to 135 V or from 175 V to 265 V, the variation of V_{CC} will be always less than a factor of 1.6. That means, if minimum V_{CC} is designed to be 13 V, then the maximum will be below 21 V, well within the recommended operating range.

6.1.1 V_{CC} winding in flyback mode

Although the V_{CC} of ICC80QSG can go as low as 8 V, it is recommended to design for a higher minimum V_{CCmin} of 12 V to ensure good gate drive for any type of MOSFET. The minimum number of turns will then be defined by the minimum output voltage:

$$N_{V_{CCmin}} = \frac{V_{CCmin} + V_D}{V_{OUTmin} + V_D} \cdot N_S = \frac{12.7 \text{ V}}{9.7 \text{ V}} \cdot 5 = 6.55$$

Equation 69

To ensure that the maximum V_{CC} will not be higher than 24 V with maximum output voltage:

$$N_{V_{CCmax}} = \frac{V_{CCmax} + V_D}{V_{OUTmax} + V_D} \cdot N_S = \frac{24.7 \text{ V}}{21.7 \text{ V}} \cdot 5 = 5.7$$

Equation 70

Here, the contradiction is immediately apparent: $N_{V_{CCmin}}$ must be higher than $N_{V_{CCmax}}$. One possible solution is to accept a V_{CCmin} of only 9 V and use $N_{V_{CC}} = 5$. But this approach risks the marginal gate drive and it needs to be carefully verified to ensure its acceptability with the chosen MOSFET.

The better solution would be to use $N_{V_{CC}} = 6$ and accept a minimum V_{CC} of about 11 V, which should be fine with the majority of MOSFET on the market. However, it is essential to add a voltage regulator that limits V_{CCmax} to 24 V or lower. If the regulator is used, it is possible to use $N_{V_{CC}} = 7$ and have a comfortable V_{CCmin} of about 13 V.

In case if the linear regulator is chosen, it is necessary to check power loss and potential hot spot on the PCB.

6.1.2 V_{CC} winding in forward mode

The solution that is recommended to be used for battery charger applications is the V_{CC} winding in the forward mode. The calculation of the necessary turns number is similar to the flyback case, just with the input voltage as reference. The minimum number of turns is as follows:

$$N_{V_{CCmin}} = \frac{(V_{CCmin} + V_D)}{V_{CBminlo}} \cdot N_P = \frac{12.7 \text{ V}}{221.2 \text{ V}} \cdot 39 = 2.24$$

Equation 71

And similarly, the maximum turns number in forward mode:

$$N_{V_{CCmax}} = \frac{(V_{CCmax} + V_D)}{V_{CBmaxhi}} \cdot N_P = \frac{24.7 \text{ V}}{374.8 \text{ V}} \cdot 39 = 2.57$$

Equation 72

Initially, with this winding direction, N_{V_{CCmax}} is greater than N_{V_{CCmin}}, as it should be. However, there is no solution with an integer number of turns. In this case, one possible solution is to choose N_{V_{CC}} = 3 and add a linear regulator.

Fortunately, there are possibilities to improve the situation.

- First, use N_{V_{CC}} = 2 and accept a minimum V_{CC} of about 11 V. As mentioned before, this should be fine with most MOSFETs on the market. The main advantage compared to the flyback solution is that no additional regulator will be needed as the maximum V_{CC} will be 18.5 V with N_{V_{CC}} = 2.
- Second, increase the overall number of turns of the transformer. For example, with N_P = 47 and N_S = 6 you would find N_{V_{CCmin}} = 2.7 and N_{V_{CCmax}} = 3.1. Consequently, N_{V_{CC}} = 3 would be a good choice in this case. But this solution is only possible if the transformer has enough free winding space, which is not the case with the chosen transformer core and bobbin.

There is another reason for preferring the forward mode for V_{CC} supply, even in the case if a linear regulator is required. In most regions of the world, line over- and undervoltage are rare and, more important, typically will not last for a long time. As a result, the power supply will operate with the nominal input voltage for the majority of the time, and the linear regulator does not dissipate a lot of power, if any. This is different from the flyback solution, where the maximum output voltage, and with that the V_{CCmax}, can and will occur for extended periods.

When using a V_{CC} winding in forward direction, a second winding in flyback direction is needed to provide the proper polarity for the ZCD signal. The number of turns for this winding is not very critical, as the voltage at ZCD pin is clamped, and later we will determine a series resistor R_{ZCD} that keeps the current within given limits.

Let us assume N_{V_{CC}} = N_{ZCD} = 3 for the following sections.

6.2 Start-up of ICC80QSG

This section shows how to determine the minimum capacitance C_{V_{CC}} needed to enable proper start of the application and the value and power rating of the start-up resistors. In the second part of this section, you will see how to build an active startup circuit that reduces start-up time as well as losses in the startup circuit.

When an AC power is first applied to the system, C_{V_{CC}}, the capacitor connected to pin V_{CC}, must be charged to the turn-on threshold V_{V_{CC}on} of the controller. Until this level has not been reached, the IC's typical current

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consumption is only 30 μA . The capacitor can either be charged by a high ohmic resistor from the rectified mains (resistive start-up) or with an active circuit consisting of a 600 V depletion MOSFET and a few passive components controlled through pin TD (active start-up), see [Figure 6](#).

The resistive start-up has lower component count and cost, but higher losses and standby consumption since the charging current is flowing continuously even when the IC supply comes from transformer winding. It is typically used within a narrow input range or in situations where standby losses are not critical.

It has to be emphasized that due to the low start-up current of the IC itself the losses in the start-up resistors are considerably smaller than with most other controllers.

6.2.1 Resistive start-up

For a resistive start-up, first determine the minimum value C_{VCC} from I_{CC} , the current consumption of the controller, t_{START} , the time until the auxiliary supply is working, and V_{DROP} , the allowed V_{CC} drop before the controller goes into shutdown. The I_{CC} and V_{DROP} ¹ can be found in the datasheet while t_{START} is not known a priori and needs to be estimated.

A reasonable value to start with is $t_{START} = 50 \text{ ms}$. Later, while testing and debugging the application, measure the real start-up time and possibly adjust the value of C_{VCC} .

$$C_{VCCmin} = \frac{I_{CC} \cdot t_{START}}{V_{DROP}} = \frac{2 \text{ mA} \cdot 50 \text{ ms}}{5 \text{ V}} = 20 \mu\text{F}$$

Equation 73

Select the next higher standard value: $C_{VCC} = 22 \mu\text{F}$ with a rated voltage of 35 V.

If the capacitor C_{VCC} is too small, the system continuously restarts. Each time the system is restarted, the output capacitor is charged a bit more until the system can fully start up and operate properly. A large C_{VCC} leads to a prolonged start-up time. Therefore, it is advisable to use a capacitor close to the necessary minimum value. Now, select the maximum permissible start-up time. Let us assume 500 ms is required. To charge the 22 μF within 500 ms to V_{VCCcon} the required current is calculated as follows:

$$I_{START} = \frac{C_{VCC} \cdot V_{VCCcon}}{t_{charge}} + I_{VCCstart} = \frac{22 \mu\text{F} \cdot 13.1 \text{ V}}{0.5 \text{ s}} + 30 \mu\text{A} = 606 \mu\text{A}$$

Equation 74

The required resistance is:

$$R_{START} = \frac{V_{CBmin} - V_{VCCcon}}{I_{START}} = \frac{210 \text{ V} - 13.1 \text{ V}}{606 \mu\text{A}} = 325 \text{ k}\Omega$$

Equation 75

Because the start-up resistor needs to withstand up to 370 V, it is recommended to split the resistor into (at least) three resistors of (ideally) the same value. This distributes power loss as well and reduces hot spots on the PCB. The highest power loss will occur with the highest input voltage:

¹ $V_{DROP} = V_{VCCcon,min} - V_{VCCmin,max}$

$$P_{LOSSrstart} = \frac{(V_{INmaxpk} - V_{VCCon})^2}{R_{START}} = \frac{(263 \text{ V} \cdot \sqrt{2} - 13.1 \text{ V})^2}{325 \text{ k}\Omega} = 0.4 \text{ W}$$

Equation 76

These losses are always present, especially under no-load condition. They can certainly be reduced by increasing the start-up time to the maximum acceptable value. If the losses are still too high, then active startup is recommended.

6.2.2 Active start-up circuit

The start-up circuit can be designed as illustrated in [Figure 6](#) on the right.

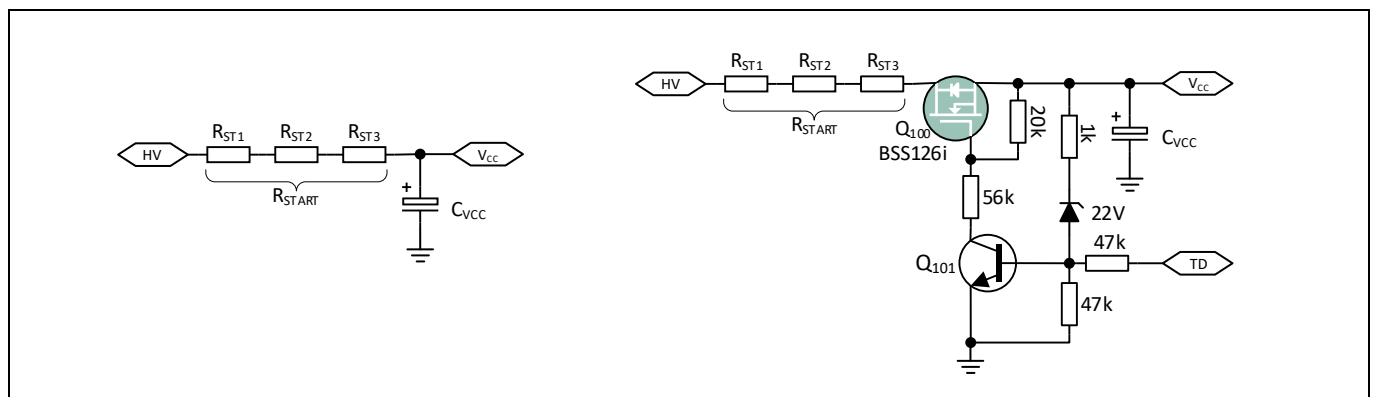


Figure 6 *Passive (left) and Active start-up (right) circuits*

In series to the resistor R_{START} is a depletion (i.e., normally-on) MOSFET Q_{100} , that is controlled by pin TD of the ICC80QSG via Q_{101} and associated components.

As long as the threshold V_{VCCon} has not been reached, the voltage at pin TD has a low level and Q_{101} is off, while the depletion MOSFET is on. In this state C_{VCC} is charged through R_{START} and the on-resistance of Q_{100} . As soon as the threshold has been reached and the IC becomes active, TD goes to approx. 1.4 V and Q_{101} is turned on, turning off Q_{100} . This way the current through R_{START} is essentially zero as long as the IC is active. In case V_{CC} becomes too high during start up, i.e., when the IC cannot start for whatever reason, the resistor and Zener diode from V_{CC} to the base of Q_{101} turn Q_{100} off, even when TD is in a low state.

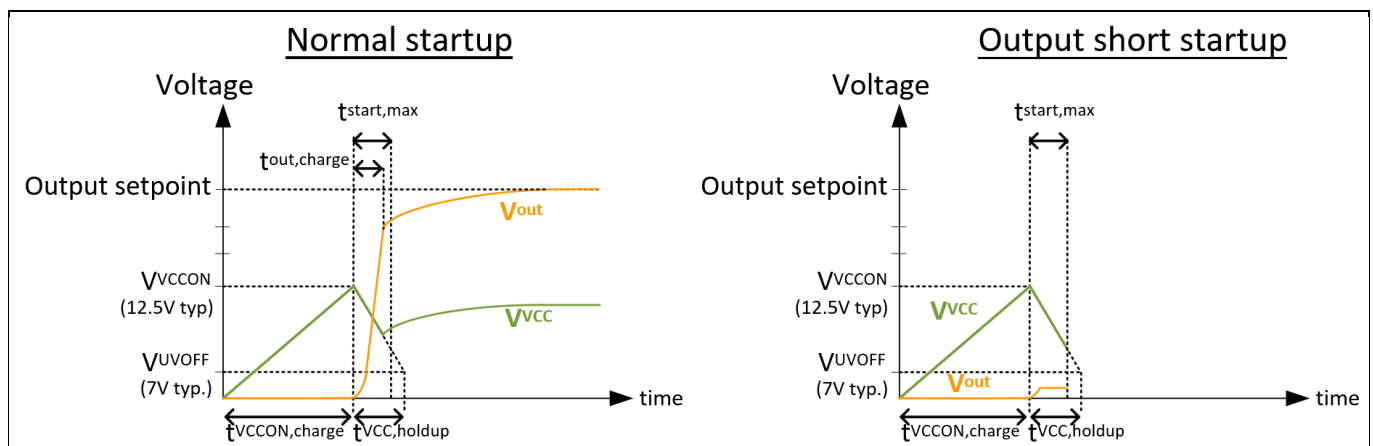


Figure 7 *Start-up behavior*

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The value of C_{VCC} is determined exactly in the same way as for resistive start-up, but R_{START} can have a lower value, thus allow much faster loading. The minimum value for R_{START} in this case should be 15 to 20 times the $R_{DS(on)}$ of Q_{101} in order to limit its power dissipation.

In case of an output short condition, the V_{CC} is not supplied over the auxiliary winding, since all the power flows to the shorted output. This behavior is displayed in [Figure 7](#) (right).

It is recommended to design the V_{CC} auxiliary turns ratio to reduce V_{CC} below 7 V (UVLO) to ensure the system shuts down during output conditions where the voltage reduces below its specified operating range. This ensures the main power MOSFET is not being switched on while operating in its saturated operating region.

6.3 TD configuration

The TD pin resistance to ground R_{TD} measurement in the pre-start-up phase has to be fine-tuned manually for a given system, to adjust the turn-on delay (TD) upon zero-crossing detection, for quasi-resonant valley switching.

The minimum R_{TD} value for proper configuration of the controller in the pre-start phase is 27 k Ω and the maximum is 68 k Ω . If there is any circuit more than just a resistor connected between TD pin and ground, such as the active start-up circuit, the following generic equation for R_{TD} calculation is applied:

$$R_{TD} = \frac{V_{TD}}{I_{TDsrc}}$$

Equation 77

Where V_{TD} is the TD pin voltage with reference to ground and I_{TDsrc} is the current flowing out of TD pin when the internal pull-up resistor of $R_{TD,RUN}$ or $R_{TD,flyback}$ is enabled in the pre-start-up phase.

If a calculation based on the equation for R_{TD} approximation results a value close to 27 k Ω or 68 k Ω , [Equation 77](#) should be used to verify whether the actual R_{TD} is still within the specified limits.

6.4 Input voltage detection and protection

The rectified and smoothed input voltage is sensed at the VIN pin through a resistor divider consisting of R_{VINhi} and R_{VINlo} as shown in [Figure 8](#). This input voltage sensing function enables brown-in (BI) and brown-out (BO) protection as well as input overvoltage protection (I-OVP).

ICC80QSG detects the AC or DC amplitude based on the ADC sampling of the VIN pin voltage. For the power limiting function and BI/BO protections, the controller measures the average VIN pin voltage based on the average of the highest VIN pin voltage sample and the lowest VIN pin voltage sample within an observation cycle. The observation time in RUN state is around 10.6 ms and 12.7 ms, based on the last synced AC line frequency of 50 Hz and 60 Hz, respectively.²

At higher power transfer, the primary bus voltage ripple is higher, and $V_{VIN,avg}$ becomes lower. As a result, a relatively higher AC input brownout protection level can be triggered at higher power transfer, to better protect the primary components from overheating and saturation in case of input under-voltage condition occurs.

² In case of non-line-syncing, the observation time is around 10.6 ms. For example, non-line-syncing can happen when the system is started up with a DC input.

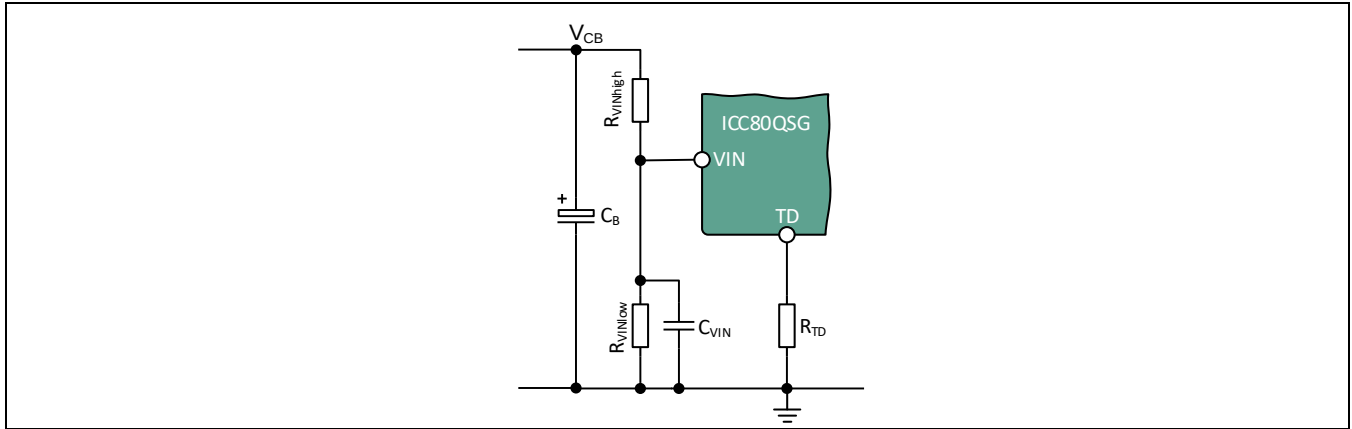


Figure 8 HV pin, $R_{VINhigh}$, R_{VINlow} , C_{VIN} , D_{HV1} and D_{HV2} connections

To determine the input voltage divider ratio, first decide on the brown-in voltage. At brown-in, there is virtually no load connected to C_B , and V_{CB} will be close to the peak value of the input voltage with input bridge rectification and double the peak input voltage with a voltage doubler input. For example, assume there is a doubler input and it is desired to set brown-in at 85 V_{AC}. The corresponding capacitor voltage is then $V_{CBbi} = 2 \cdot \sqrt{2} \cdot 85 \text{ V} \approx 240 \text{ V}$.

Next, select a value for R_{VINlow} in the range of tens of k Ω (for example, 30 k Ω). Then, the $R_{VINhigh}$ is calculated as follows:

$$R_{VINhigh} = \left(\frac{V_{CBbi}}{V_{BI}} - 1 \right) \cdot R_{VINlow} = \left(\frac{240 \text{ V}}{0.647 \text{ V}} - 1 \right) \cdot 30 \text{ k}\Omega \approx 11.1 \text{ M}\Omega$$

Equation 78

The calculated resistance is distributed over at least three resistors to reduce the voltage and power stress of each of them.

The ICC80QSG has a 16 mV hysteresis between the BI- and BO-levels, i.e., $V_{BO} = 0.631 \text{ V}$. Now, calculate the brown-out level V_{CBbo} :

$$V_{CBbo} = \left(\frac{R_{VINhigh}}{R_{VINlow}} + 1 \right) \cdot V_{BO} = \left(\frac{11.1 \text{ M}\Omega}{30 \text{ k}\Omega} + 1 \right) \cdot 0.631 \text{ V} \approx 234 \text{ V}$$

Equation 79

The hysteresis is only about 6 V in this case, and it may happen that the average V_{CB} falls below this level when the converter starts with full load. If this occurs, then the V_{CB} ripple increases considerably, and the average V_{CB} voltage drops immediately below the BO level.

If the hysteresis is too small, it can be increased by adding an additional resistor $R_{VINoffs}$ between pins VIN and TD pins, as shown in [Figure 9](#). Since the ICC80QSG is inactive until the BI level at VIN is not reached, the sum of $R_{VINoffs}$ and R_{TD} is in parallel to R_{VINlow} at startup. In this configuration the BI level will be:

$$V_{CBbi} = \left(\frac{R_{VINhigh}}{R_{VINoffs} + R_{TD}} + \frac{R_{VINhigh}}{R_{VINlow}} + 1 \right) \cdot V_{BI}$$

Equation 80

While the BO level is now:

$$V_{CBbo} = \left(\frac{R_{VINhigh}}{R_{VINlow}} + 1 \right) \cdot V_{BO} + \frac{R_{VINhigh}}{R_{VINoffs}} \cdot (V_{BO} - V_{OFFS})$$

$$\text{with } V_{OFFS} = \frac{V_{INT}}{1 + \frac{R_{TDrun}}{R_{TD}} + \frac{R_{TDrun}}{R_{VINoffs}}} + \frac{V_{BO}}{1 + \frac{R_{VINoffs}}{R_{TD}} + \frac{R_{VINoffs}}{R_{TDrun}}}$$

Equation 81

There is no simple formula to calculate the values for $R_{VINhigh}$, R_{VINlow} , and $R_{VINoffs}$ but an iterative solution.

First, select a proper value for R_{TD} according to Section 6.3. If it is not already determined, assume an R_{TD} of 47 kΩ as a starting point. Its influence on V_{OFFS} is not that strong that a different value will later affect the BI and BO levels. Next, assume an $R_{VINoffs}$ of 1 MΩ, which is much higher than R_{TD} .

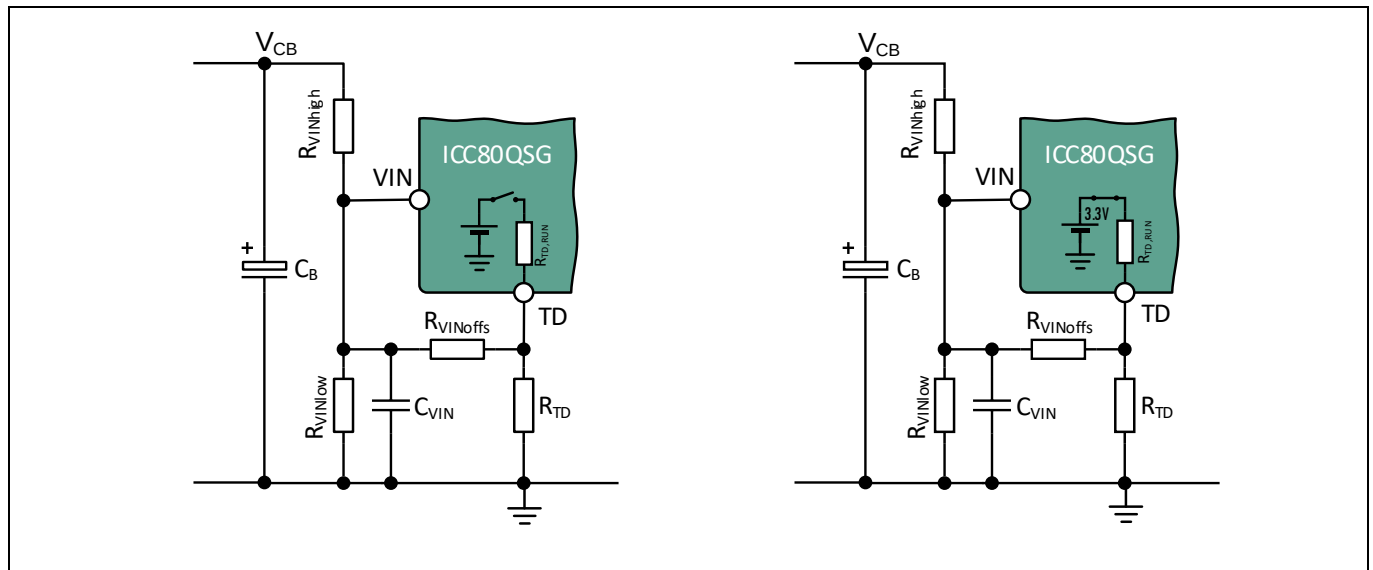


Figure 9 Adding hysteresis to Bi/BO. Left device inactive (BI), right device active (BO)

The value of $R_{VINhigh}$ when $R_{VINoffs}$ is used:

$$R_{VINhigh} = \left(\frac{V_{CBbi}}{V_{BI}} - 1 \right) \cdot \frac{(R_{VINoffs} + R_{TD}) \cdot R_{VINlow}}{R_{VINoffs} + R_{VINlow} + R_{TD}} = \left(\frac{240 V}{0.647 V} - 1 \right) \cdot \frac{(1 M\Omega + 47 k\Omega) \cdot 30 k\Omega}{1 M\Omega + 47 k\Omega + 30 k\Omega} = \mathbf{10.8 M\Omega}$$

Equation 82

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Calculate V_{OFFS} , using $V_{INT} = 3.3 \text{ V}$ and $R_{TDRUN} = 10 \text{ k}\Omega$:

$$V_{OFFS} = \frac{3.3 \text{ V}}{1 + \frac{10 \text{ k}\Omega}{47 \text{ k}\Omega} + \frac{10 \text{ k}\Omega}{1 \text{ M}\Omega}} + \frac{0.631 \text{ V}}{1 + \frac{1 \text{ M}\Omega}{47 \text{ k}\Omega} + \frac{1 \text{ M}\Omega}{10 \text{ k}\Omega}} = 2.7 \text{ V}$$

Equation 83

And finally use [Equation 81](#) to determine the BO level:

$$V_{CBbo} = \left(\frac{10.8 \text{ M}\Omega}{30 \text{ k}\Omega} + 1 \right) \cdot 0.631 \text{ V} + \frac{10.8 \text{ M}\Omega}{1 \text{ M}\Omega} \cdot (0.631 \text{ V} - 2.7 \text{ V}) = 215 \text{ V}$$

Equation 84

The hysteresis has increased to 25 V by adding $R_{VINOFFS}$. If this value is not acceptable, either increase $R_{VINOFFS}$ to decrease the hysteresis, or vice versa, and then start over from [Equation 82](#).

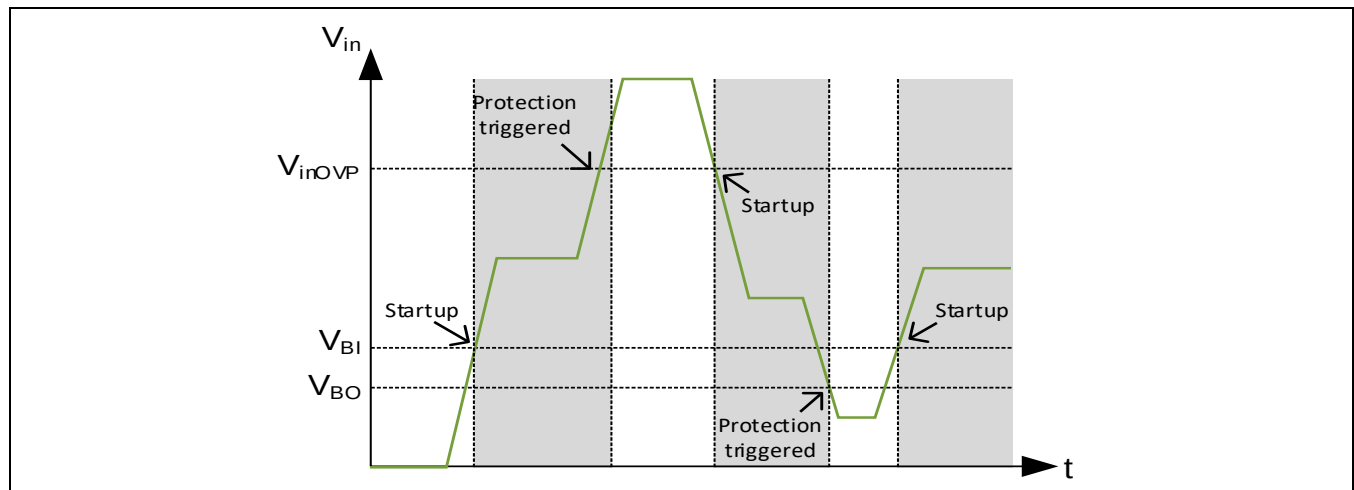


Figure 10 Input voltage levels for start-up and protection

6.5 Fast restart

The VIN pin offers an additional fast restart feature. Unlike the normal start-up, which takes 200 ms after a protection is triggered, the fast restart checks the start-up conditions every 25 ms, as long as a V_{CC} is available.

This feature might be useful to turn the IC off for very low standby applications with additional auxiliary power supply. In this case, the response time to start-up is largely decreased from the worst-case 200 ms + start-up time to just 25 ms + start-up time.

6.6 On-time adjustment

The maximum power transfer at low input voltages is limited by the ICC80QSG by limiting the maximum on-time. The latter can be adjusted with the resistor connecting the ZCD pin with the auxiliary winding. The maximum on-time occurs at the minimum input voltage and is reduced when a higher input voltage is detected through pin VIN. For details, please consult the ICC80QSG datasheet.

The on-time has a linear relationship with I_{ZCDclp} , the peak-to-peak current flowing to ZCD pin, with a factor of 16.66 ms/A.

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In Section 4.2.1, the maximum on-time needed to transmit the full power at lowest input voltage is determined to be $t_{onfp} = 9.63 \mu s$. To cover possible tolerances and provide a sufficient margin to support transients, a margin of at least 25% for the maximum on-time is recommended, i.e., a minimum of $12 \mu s$ should be used.

This is accomplished by a peak to peak current of $12 \mu s / 16.66 ms/A = 0.735 mA$.

To determine the value of the current limiting resistor R_{ZCD} , calculate the peak-to-peak voltage of the auxiliary winding.

$$V_{ZCDPPmin} = \left(\frac{V_{OUT} + V_D}{N_{SEC}} + \frac{U_{CBmin}}{N_P} \right) \cdot N_{ZCD} = \left(\frac{21.7 V}{5} + \frac{210 V}{39} \right) \cdot 3 = 29.2 V$$

$$V_{ZCDPPmax} = \left(\frac{V_{OUT} + V_D}{N_{SEC}} + \frac{U_{CBmax}}{N_P} \right) \cdot N_{ZCD} = \left(\frac{21.7 V}{5} + \frac{375 V}{39} \right) \cdot 3 = 41.8 V$$

Equation 85

Then R_{ZCD} is given by,

$$R_{ZCDmax} = \frac{V_{AUXPPmin}}{I_{ZCD}} = \frac{29.2 V}{0.735 mA} = 39.7 k\Omega$$

Equation 86

Select the next smaller standard value for R_{ZCD} , which is **39 kΩ**.

To stay below a maximum value of $I_{ZCDmax} = 1.8 mA$, the R_{ZCD} must be at least:

$$R_{ZCDmin} = \frac{V_{AUXPPmax}}{I_{ZCDmax}} = \frac{41.8 V}{1.8 mA} = 23.2 k\Omega$$

Equation 87

Given these two conditions, the ZCD resistor may be selected without restriction between 24 kΩ and 39 kΩ.

6.6.1 Trade-off between power limitation and operating point

The on-time of ICC80QSG is influenced by the current out of the ZCD pin and the R_{ZCD} resistor selected as described above. The R_{ZCD} value also affects the operating point of the system. To be clearer, the value of R_{ZCD} will have an effect on what valley number the converter uses to turn on the main power MOSFET.

As the value of resistor R_{ZCD} reduces, the ICC80QSG moves to a higher valley number earlier. Bench analysis has shown that the best trade-off between power limitation and performance is achieved with a smaller R_{ZCD} than initially calculated.

Note that the value chosen for R_{ZCD} impacts the secondary-side OVP value. Increasing the current out of the ZCD pin of the ICC80QSG reduces the magnitude of the voltage where the OVP is triggered.

6.7 Output OVP-related design

In case of a failure in the feedback loop, the output voltage of the charger might rise and become destructive. ICC80QSG monitors the ZCD current during demagnetization of the transformer since that is a measure for the output voltage. This current is mirrored with a factor of $n_{ZCDovp} = 0.484$ to the CS pin. A series resistor between shunt resistor and CS pin is used to translate this current out of CS pin into a voltage offset that initiates a restart when 0.61 V at 'CS' is reached. For more details, see the ICC80QSG device datasheet.

Assuming an output OVP level of 30 V, the ZCD current at the border to overvoltage condition is:

$$I_{ZCDovp} = \frac{\frac{N_{ZCD}}{N_{SEC}} \cdot V_{OUTovp}}{R_{ZCD}} = \frac{\frac{3}{5} \cdot 30 \text{ V}}{39 \text{ k}\Omega} = 461 \text{ }\mu\text{A}$$

Equation 88

The current out of the CS pin:

$$I_{CSovp} = I_{ZCDovp} \cdot n_{ZCDovp} = 461 \text{ }\mu\text{A} \cdot 0.484 = 223 \text{ }\mu\text{A}$$

Equation 89

Finally, determine the value of the resistor R_{CSovp} between the shunt and pin 'CS':

$$R_{CSovp} = \frac{V_{OCP1}}{I_{CSovp}} = \frac{0.61 \text{ V}}{223 \text{ }\mu\text{A}} = 2.73 \text{ k}\Omega$$

Equation 90

Start optimization of OVP with $R_{CSovp} = 2.7 \text{ k}\Omega$. This should be one of the last components to be optimized, as the output voltage, the ZCD resistor, and the winding ratio are determining the value, the OVP can be easily triggered inadvertently.

It is recommended to keep the value low until all the other parameters are set. Only then will the adjustment of the secondary-side OVP generate a satisfying result.

Even when not intending to use the second OVP feature, it is still advised to connect this resistor. The size of the resistor should be around 100 Ohms smaller than the calculated value of the resistor. This helps to limit the occurring voltage spikes on this pin.

7 Feedback circuit

There are several charging methods in use, but in general, battery charging needs adjustable constant voltage and constant current, depending on the charging state and battery chemistry.

Typically, this is accomplished with the circuitry shown in [Figure 11](#).

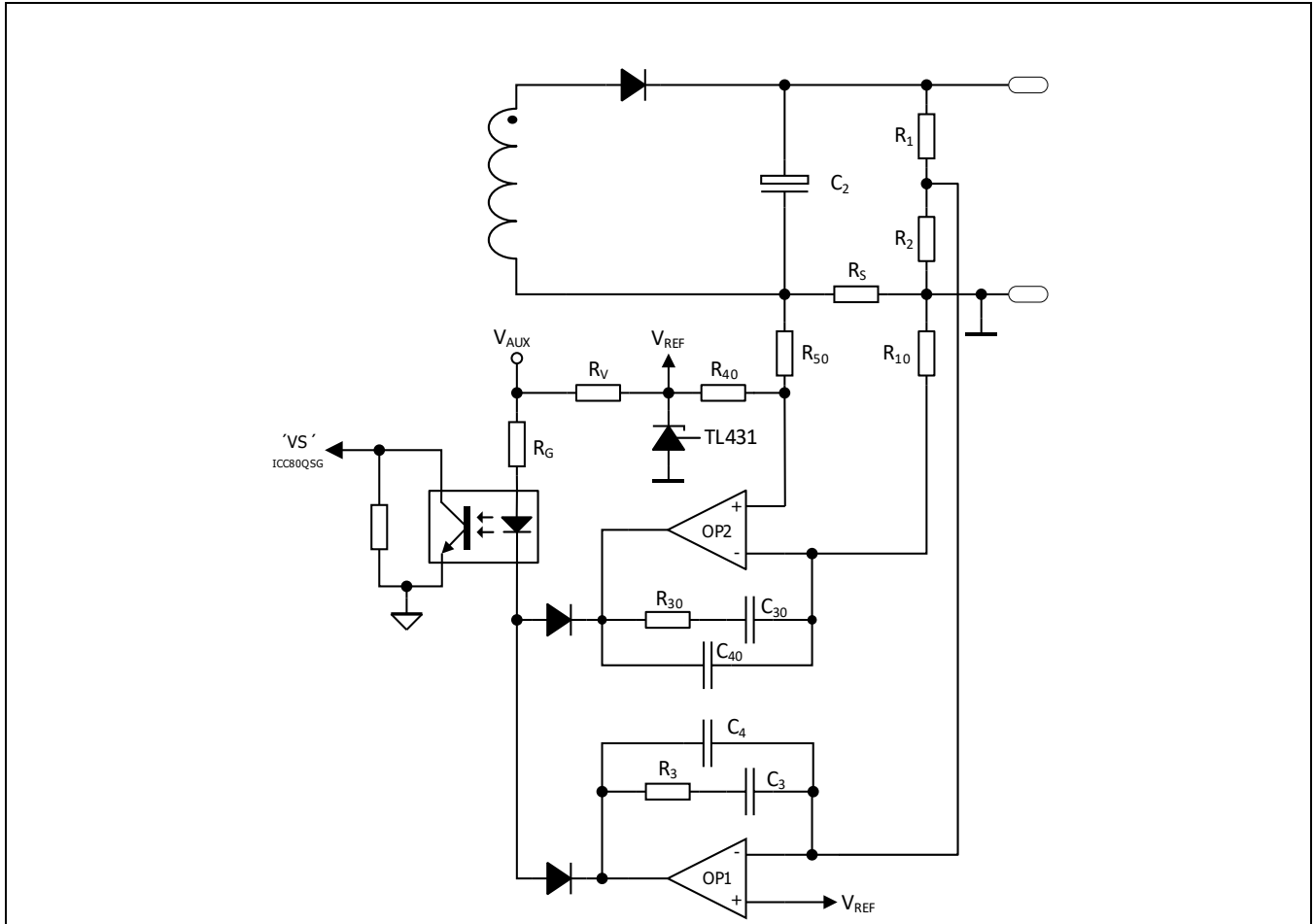


Figure 11 Basic feedback circuit for constant current (CC) and constant voltage (CV) regulation

It is assumed that there is a stable auxiliary voltage, V_{AUX} , is available that supplies the operational amplifiers as well as the voltage reference, TL431.

The voltage regulation loop is quite standard. The scaled-down output voltage is compared to V_{REF} by OP1. In this case, if the regulated output voltage is higher than the setpoint selected by the divider ratio R_1/R_2 , the output of OP1 goes low and drives current through the optocoupler. This results in a higher current drawn out of pin 'VS' which results in shorter on-times and reduced output voltage. Steady-state output voltage V_{Out} will be as follows:

$$V_{Out} = \left(1 + \frac{R_1}{R_2}\right) \cdot V_{REF}$$

Equation 91

Feedback circuit

The current loop regulates the voltage across shunt R_S and compares it to a scaled down V_{REF} by means of OP2. If the current through R_S is increasing, the voltage at the node R_S-R_{50} is getting more and more negative. Similarly, the voltage at input '+', which has a small positive offset $V_{REF}/(1+R_{40}/R_{50})$ at zero output current, is going down and eventually reaches zero volt as current increases. Then the output of OP2 is going low and the output current is reduced in a similar way as in the voltage loop. Steady-state output current I_{Out} will be as follows:

$$I_{Out} = \frac{R_{40}}{R_S \cdot R_{50}} \cdot V_{REF}$$

Equation 92

Here, R_S is typically selected such that the voltage drop is in the order of some 100 mV. A low voltage drop across R_S reduces power losses as well as accuracy.

If both, output current and output voltage are lower than the values determined by Equation 37 and Equation 91 respectively, the outputs of OP1 and OP2 will both be high and there will be no current flowing through the optocoupler. In this case the on-time of ICC80QSG is maximum and the output voltage will rise until either setpoint Equation 37 or Equation 91 is met. In steady state, always only one of the two loops is active, depending on load resistance and setpoints.

The frequency compensation of the feedback loops is accomplished by means of C_2 and R_4 in case of the voltage loop and C_{20} and R_{40} in case of current loop i.e. a type 2a configuration.

7.1 Loop response

The open-loop small-signal transfer function of the converter can be split into five distinct functions, as shown in Figure 12. Most of these transfer functions are easily determined since they have a flat frequency response, at least in the frequency band of interest. The two more complex transfer functions are $H_{FB}(s)$ and $H_{EA}(s)$ of the flyback stage and the error amplifier, respectively.

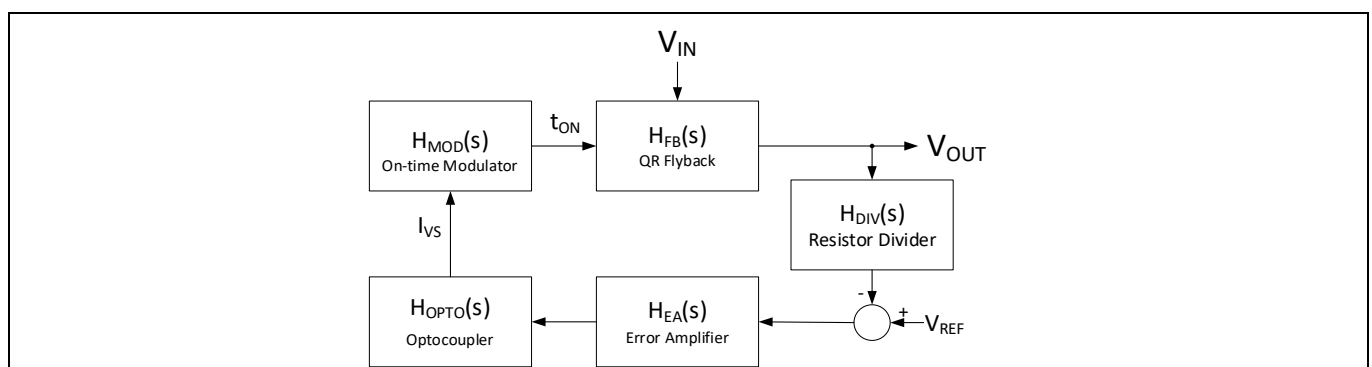


Figure 12 Elements of regulation loop transfer function

The transfer functions of each block, starting with the flyback stage, are derived in the following sections.

7.1.1 Transfer Function of the Flyback Stage

As mentioned previously, the flyback stage is an on-time controlled, QR one and its transfer function mode has the general form (e.g. [5]):

Feedback circuit

$$H_{FB}(s) = H_{0,FB} \cdot \frac{1 + \frac{s}{\omega_{Z,FB}}}{1 + \frac{s}{\omega_{P,FB}}} \left[\frac{V}{s} \right]$$

Equation 93

With a static gain $H_{0,FB}$, a zero at $s = -\omega_{Z,FB}$ and a pole at $s = -\omega_{P,FB}$. Actually, this is not the complete transfer function since there exists a second pole and a right half-plane zero at higher frequencies. Since the latter frequencies are an order of magnitude above the typical crossover frequencies, you may ignore them for the sake of simplicity.

In its simplest form, the pole and zero of interest are determined by the output impedance R_{OUT} of the flyback converter, the output capacitor C_2 , ESR of C_2 and the load resistance R_L .

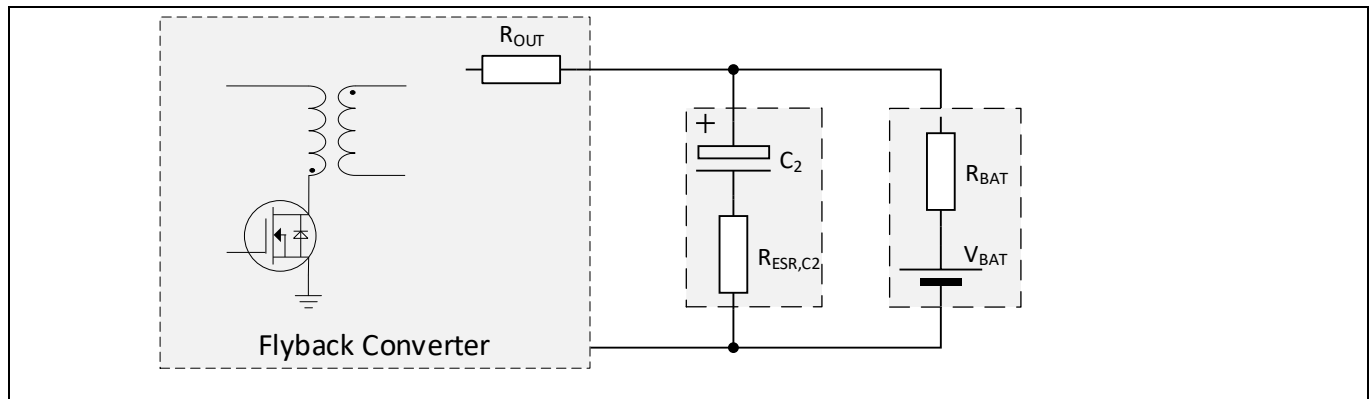


Figure 13 Elements determining the pole and zero frequencies of $H_{FB}^{CV}(s)$

In case of a battery charger obviously the load is a battery, which cannot be simply modeled by a resistor. The minimum model of a battery is a voltage source V_{BAT} in series with a (differential) resistance R_{BAT} . Because the voltage source of this model is a short-circuit for AC, only R_{BAT} is important for the frequency response.

With the help of [Figure 13](#), it is clear that the zero and pole are determined by the two following equations:

$$\omega_{Z,FB} = \frac{1}{R_{ESR,C_2} \cdot C_2} \text{ and } \omega_{P,FB} = \frac{1}{(R_{OUT} \parallel R_{BAT}) \cdot C_2} = \frac{R_{OUT} + R_{BAT}}{R_{OUT} \cdot R_{BAT} \cdot C_2}$$

Equation 94

Actually, there are two transfer functions of the flyback, depending on whether the output voltage is regulated or the output current. The good news is that they only differ in the DC-gain, i.e., there is $aH_{0,FB}^{CV}$ and a $H_{0,FB}^{CC}$, while the poles and zeroes are not affected

7.1.1.1 Calculation of Flyback Transfer Function

Before determining the value of the converter's open-loop output impedance R_{OUT} , first determine the static gain $H_{0,FB}$. The expression for R_{OUT} can be easily derived from the equation for the latter. Starting with the fact that the flyback stores a well-defined amount of energy and transfers it to the output in each switching cycle, we can multiply this energy with the actual switching frequency f_{SW} , to obtain a steady-state equation for the output power:

Feedback circuit

$$V_{OUT} \cdot I_{OUT} = \frac{V_{IN}^2 \cdot t_{ON}^2 \cdot f_{SW} \cdot \eta}{2 \cdot L_P}$$

Equation 95

Where,

V_{IN} : DC input voltage of the flyback stage

t_{ON} : Current on-time of switch

f_{SW} : Switching frequency.

η : Efficiency of flyback stage

L_P : Primary side inductance

The switching frequency that you can determine from the fact that the QR flyback is operating in boundary mode at high-load levels:

$$f_{SW} = \frac{1}{t_{ON} + t_{OFF}} = \frac{1}{t_{ON} \cdot \left(1 + \frac{V_{IN}}{n \cdot (V_{OUT} + V_D)}\right)}$$

Equation 96

Inserting [Equation 96](#) into [Equation 95](#), you get the below equation for V_{OUT} :

$$V_{OUT} = \frac{V_{IN}^2 \cdot t_{ON} \cdot \eta}{2 \cdot L_P \cdot I_{OUT} \cdot \left(1 + \frac{V_{IN}}{n \cdot (V_{OUT} + V_D)}\right)}$$

Equation 97

Now, for simplification, assume that $V_{OUT} \gg V_D^3$ and neglect the latter. Solving [Equation 97](#) with $V_D \neq 0$ would result in a lengthy expression that adds complications without significantly increasing the accuracy. With the described simplification, the solution of [Equation 97](#) is:

$$V_{OUT} = \frac{V_{IN}^2 \cdot \eta \cdot t_{ON}}{2 \cdot I_{OUT} \cdot L_P} - \frac{V_{IN}}{n}$$

Equation 98

The 'only' remaining step is to express I_{OUT} by means of V_{BAT} and R_{BAT} and use that expression instead of I_{OUT} in [Equation 98](#).

But before doing that, calculate the output impedance R_{OUT} , since [Equation 98](#) is the best starting point for that.

³ A necessary condition to achieve a decent efficiency

Feedback circuit

$$R_{OUT} = -\frac{dV_{OUT}}{dI_{OUT}} = \frac{V_{IN}^2 \cdot \eta \cdot t_{ON}}{2 \cdot I_{OUT}^2 \cdot L_P}$$

Equation 99

This expression can be further simplified. Consider the equivalent load resistor R_L , which is the resistor that would draw the same current I_{OUT} as the battery does at a certain output voltage V_{OUT} ⁴.

$$R_L \stackrel{\text{def}}{=} \frac{V_{OUT}}{I_{OUT}} = \frac{V_{IN}^2 \cdot \eta \cdot t_{ON}}{2 \cdot I_{OUT}^2 \cdot L_P} - \frac{V_{IN}}{n \cdot I_{OUT}}$$

Equation 100

Using [Equation 100](#), R_{OUT} can be rewritten as:

$$R_{OUT} = R_L + \frac{V_{IN}}{n \cdot I_{OUT}} = R_L \cdot \left(1 + \frac{V_{IN}}{n \cdot V_{OUT}}\right) \simeq \frac{R_L}{d}$$

Equation 101

Now, with this handy expression for R_{OUT} , back to $H_{0,FB}$.

To get an expression that involves the physical load parameters, replace I_{OUT} in [Equation 98](#) by $(V_{OUT}-V_{BAT})/R_{BAT}$ and solve the resulting equation for V_{OUT} . The solution is as follows:

$$V_{OUT} = \frac{1}{2} \cdot \left(\sqrt{\frac{2 \cdot R_{BAT} \cdot V_{IN}^2 \cdot t_{ON} \cdot \eta}{L_P}} + \left(V_{BAT} + \frac{V_{IN}}{n} \right)^2 - \frac{V_{IN}}{n} + V_{BAT} \right)$$

Equation 102

The relationship between V_{OUT} and t_{ON} is non-linear, and linearization is necessary to obtain the small signal response of the flyback stage. Linearization involves taking the first derivative of $V_{OUT}(t_{ON})$ at the actual operating point t_{ONop} .

$$H_{0,FB}^{CV} = \left. \frac{dV_{OUT}(t_{ON})}{dt_{ON}} \right|_{t_{ON}=t_{ONop}} = \frac{R_{BAT} \cdot V_{IN}^2 \cdot \eta}{2 \cdot L_P \cdot \sqrt{\frac{2 \cdot R_{BAT} \cdot V_{IN}^2 \cdot t_{ONop} \cdot \eta}{L_P} + \left(\frac{V_{IN}}{n} + V_{BAT} \right)^2}}$$

Equation 103

At this point, it is essential to check whether the above equations are reasonable. To do so, use the parameter of the flyback with input voltage doubler designed earlier. The selected and calculated parameters are: $V_{IN} = 221.2$ V, $\eta = 0.9$, $L_P = 1.09$ mH, $n = 39/5$, $t_{ONop} = 9.63$ μ s, $C_2 = 1680$ μ F, and $R_{ESRC1} = 7$ m Ω . Since a battery in that design was not considered, assume $R_{BAT} = R_L = 5.25$ Ω and $V_{BAT} = 0$ V, and [Equation 103](#) must provide the correct result with this load.

⁴ Note that R_L is not a traditional resistive load, but rather a mathematical construct whose value varies with the operating point.

Feedback circuit

The result is $V_{OUT} = 20.78 \text{ V}$, slightly smaller than the 21 V output targeted with above selected values. The reason why the calculated gain is about 1% smaller than the target lies in the assumption $V_D = 0$ in [Equation 97](#). But this result is accurate to determine the loop gain. The lengthy and complicated expressions with $V_D \neq 0 \text{ V}$ are definitely not worth the effort.

The small signal gain is then:

$$H_{0,FB}^{CV} = \frac{5.25 \, \Omega \cdot (221.2 \text{ V})^2 \cdot 0.9}{2 \cdot 1.09 \text{ mH} \cdot \sqrt{\frac{2 \cdot 5.25 \, \Omega \cdot (221.2 \text{ V})^2 \cdot 9.63 \, \mu\text{s} \cdot 0.9}{1.09 \text{ mH}} + \left(\frac{221.2 \text{ V}}{7.8} + 0 \text{ V}\right)^2}} = 1.517 \frac{\text{MV}}{\text{s}} = \mathbf{123.6 \text{ dB}}$$

Equation 104

The left half-plane zero:

$$\omega_{Z,FB} = \frac{1}{1680 \, \mu\text{F} \cdot 7 \text{ m}\Omega} = \mathbf{85 \cdot 10^3 \text{ s}^{-1}} \text{ (equivalent } 13.54 \text{ kHz)}$$

Equation 105

The open-loop output impedance:

$$R_{OUT} = R_L \cdot \left(1 + \frac{V_{IN}}{n \cdot V_{OUT}}\right) = 5.25 \, \Omega \cdot \left(1 + \frac{221.2 \text{ V}}{7.8 \cdot 21 \text{ V}}\right) = \mathbf{12.3 \, \Omega}$$

Equation 106

And finally, the pole:

$$\omega_{P,FB} = \frac{12.3 \, \Omega + 5.25 \, \Omega}{12.3 \, \Omega \cdot 5.25 \, \Omega \cdot 1680 \, \mu\text{F}} = \mathbf{162.4 \text{ s}^{-1}} \text{ (equivalent } 25.85 \text{ Hz)}$$

Equation 107

The frequency $\omega_{Z,FB}$ is relatively high and will have minimum to no influence on the loop compensation. Next, use software like MathCAD or Maxima (freeware) to enter [Equation 93](#) with the above calculated values and create a Bode plot of $H_{FB(s)}$. Actually, that's not really necessary because you can sketch the asymptotic behavior easily by hand with the above information. At frequencies up to 25.85 Hz, the gain is 123.6 dB and starts to drop from there with a slope of -20 dB per decade. At 13.54 kHz, it goes back to a horizontal slope. The phase goes from 0° at very low frequencies to -45° at $\omega_{P,FB}$ and $\omega_{Z,FB}$ approaching almost -90° between these two.

The described asymptotic behavior is shown [Figure 14](#) in blue, together with the calculated gain and phase in red. Later you will see that the easily found asymptotic curve is actually all you need to design the loop compensation.

Feedback circuit

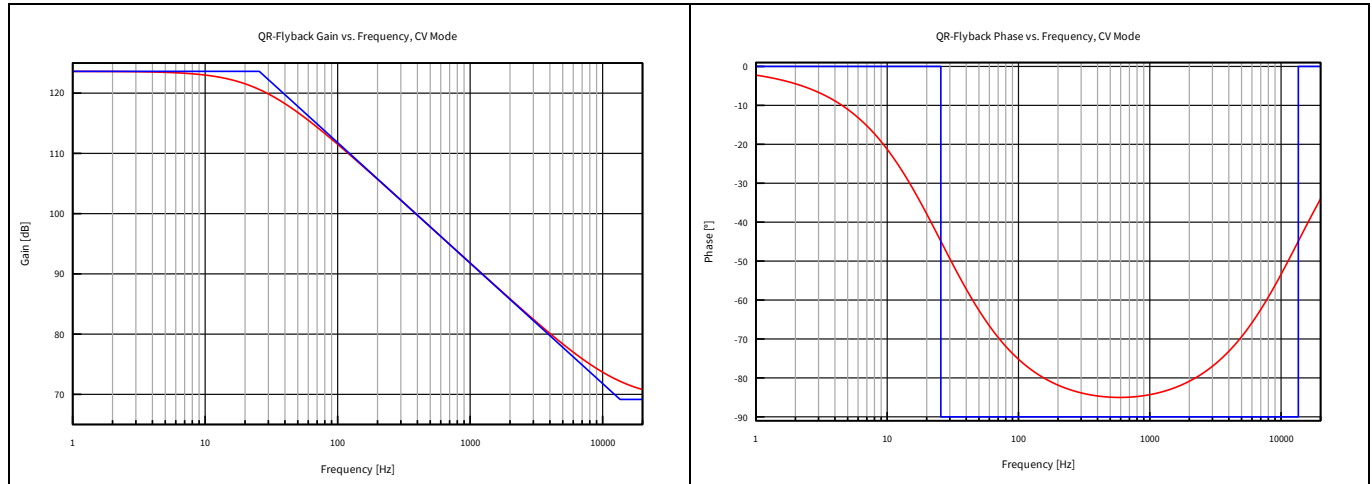


Figure 14 Calculated gain (left) and phase (right) of the flyback's transfer function; Calculated response (red), asymptotic behavior (blue)

Now let us investigate the behavior of the transfer function with variable resistance R_{BAT} and voltage V_{BAT} . In [Equation 94](#) and [Equation 103](#), the zero does not depend on these two parameters, and the pole is only influenced by R_{BAT} and finally the DC-gain by both.

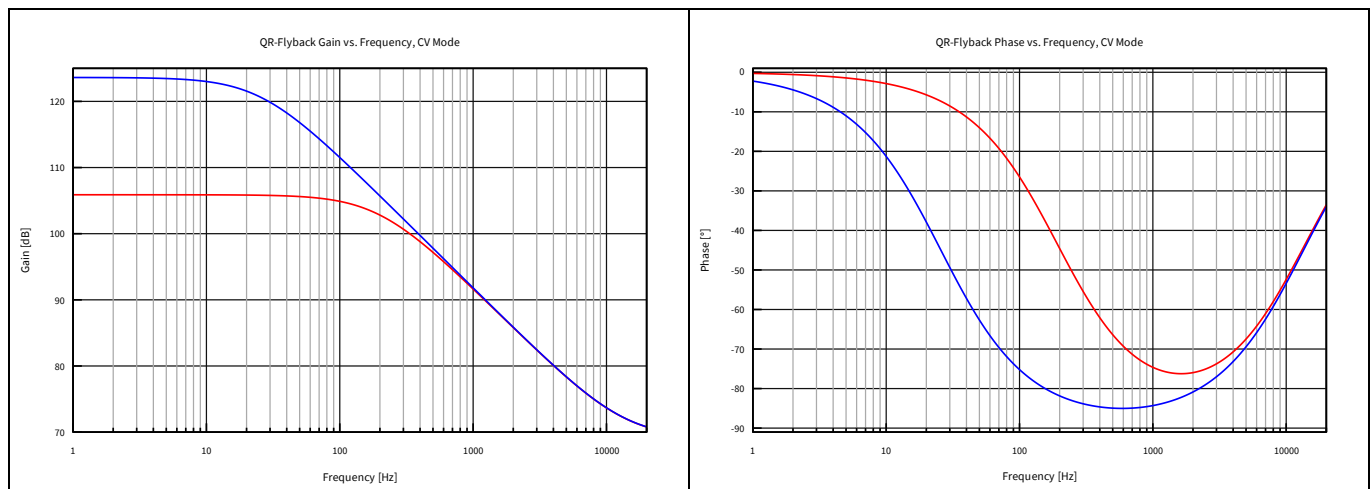


Figure 15 Calculated gain (left) and phase (right) of the flyback's transfer function for different values of R_{BAT} and V_{BAT} . Red: $V_{BAT} = 19\text{ V}$, $R_{BAT} = 0.25\ \Omega$, Blue: $V_{BAT} = 0\text{ V}$, $R_{BAT} = 5.25\ \Omega$.

A closer inspection shows that the gain $H_{(0,FB)}$ increases almost linearly with R_{BAT} , while $\omega_{(P,FB)}$ decreases essentially with $1/R_{BAT}$. This is well visible in the plots of [Figure 15](#), where R_{BAT} has been chosen with $5.25\ \Omega$ and $0.25\ \Omega$, respectively, and V_{BAT} accordingly to get the desired output voltage and power. With this change of the load resistance by a factor of 21, the gain drops from about 123 dB to about 100 dB, i.e., by a factor of 15, while the pole rises from about 26 Hz to 400 Hz, i.e., by a factor of 20. As you see, the rising pole frequency almost perfectly compensates the gain drop and the response at 1 kHz and above is virtually unchanged. The impact of this on loop compensation will be discussed later.

In a similar way to the constant voltage loop, the gain $H_{0,FB}^{CC}$ for a constant current loop can be derived. Not very surprising, it turns out to be the transfer function of the voltage loop divided by R_{BAT} :

Feedback circuit

$$H_{0,FB}^{CC} = \left. \frac{d I_{OUT}(t_{ON})}{d t_{ON}} \right|_{t_{ON}=t_{ONop}} = \frac{V_{IN}^2 \cdot \eta}{2 \cdot L_P \cdot \sqrt{\frac{2 \cdot R_{BAT} \cdot V_{IN}^2 \cdot t_{ONop} \cdot \eta}{L_P} + \left(\frac{V_{IN}}{n} + V_{BAT}\right)^2}}$$

Equation 108

This seemingly small difference will make a big difference for the compensation of the current loop. This is because now the dependency of the DC-gain on R_{BAT} becomes comparatively small while the variation of the position of the pole with R_{BAT} is unchanged.

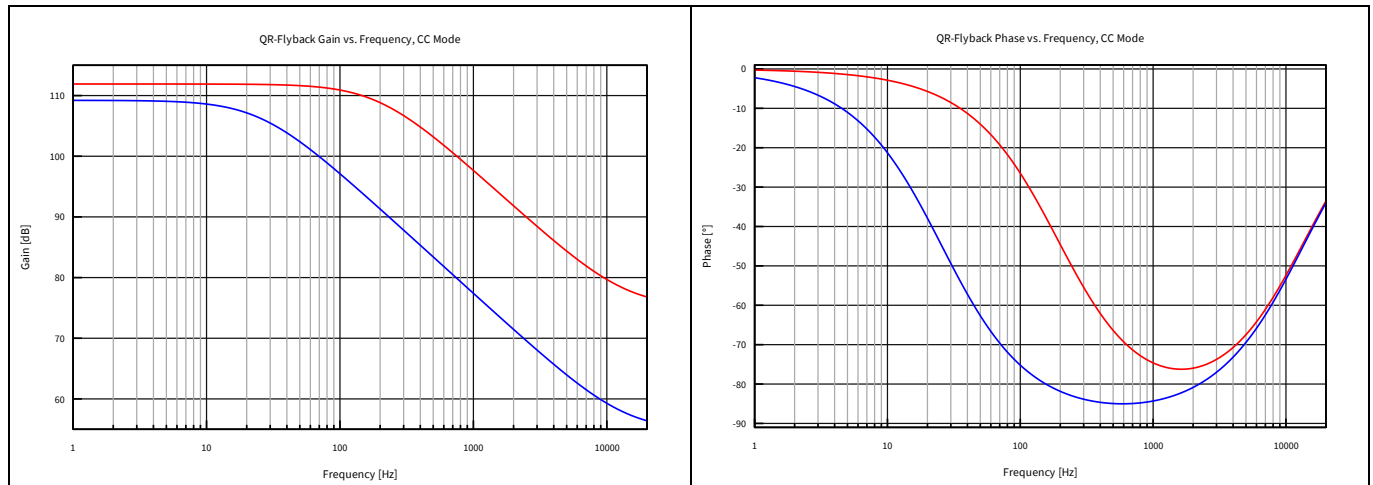


Figure 16 Calculated gain (left) and phase (right) of the flyback's transfer function in current regulation mode. Red: $V_{BAT} = 19\text{ V}$, $R_{BAT} = 0.5\ \Omega$, Blue: $V_{BAT} = 0\text{ V}$, $R_{BAT} = 5.25\ \Omega$.

The implication for the transfer function in current regulation is well visible in the plots of Figure 16. In contrast to the voltage regulation mode, the gain **increases** a few dB when R_{BAT} is lowered from $5.25\ \Omega$ to $0.5\ \Omega$, while the frequency of the pole increases by a factor of ~ 20 as before in voltage regulation mode. As a consequence, the gain at 1 kHz differs by about 26 dB for the two loads. When designing the compensation for the current loop, it is important to pay attention to this behavior and have a reasonable value for R_{BAT} . Actually, the combination $V_{BAT} = 19\text{ V}$ and $R_{BAT} = 0.5\ \Omega$ has been chosen consciously. According to the reference [6], the resistance of a single cell of size $65\text{ mm} \times 18\text{ mm}$ (18650 battery), 1.1 Ah , LiFePO₄ capable of 4 A fast charge is $75\text{ m}\Omega$. In our application, six cells would be used in series, resulting in a total resistance of $0.45\ \Omega$.

7.1.1.2 Simulation of Flyback Transfer Function

Another viable, but sometimes tricky, option to determine the flyback transfer function is through simulation. Any SPICE variant can be used to simulate the frequency response, but care must be taken due to the different variants of SPICE that differ in small but important details. The details of simulation models for switched-mode converters and the differences between simulators are beyond the scope of this application note. For guidance on setting up simulations, see the following references [3],[4].

ICC80QSG QR flyback controller for battery charger applications of up to 120 W

Feedback circuit

While it is possible to use transient analysis to determine the small-signal transfer function, it takes far too long since thousands of switching cycles have to be simulated for every single data point.

The above-mentioned references develop and use linearized models for the switching cell that allows the transfer function to be simulated with AC-analysis. This is an extremely fast process and allows quick inspection of the influence of component variations.

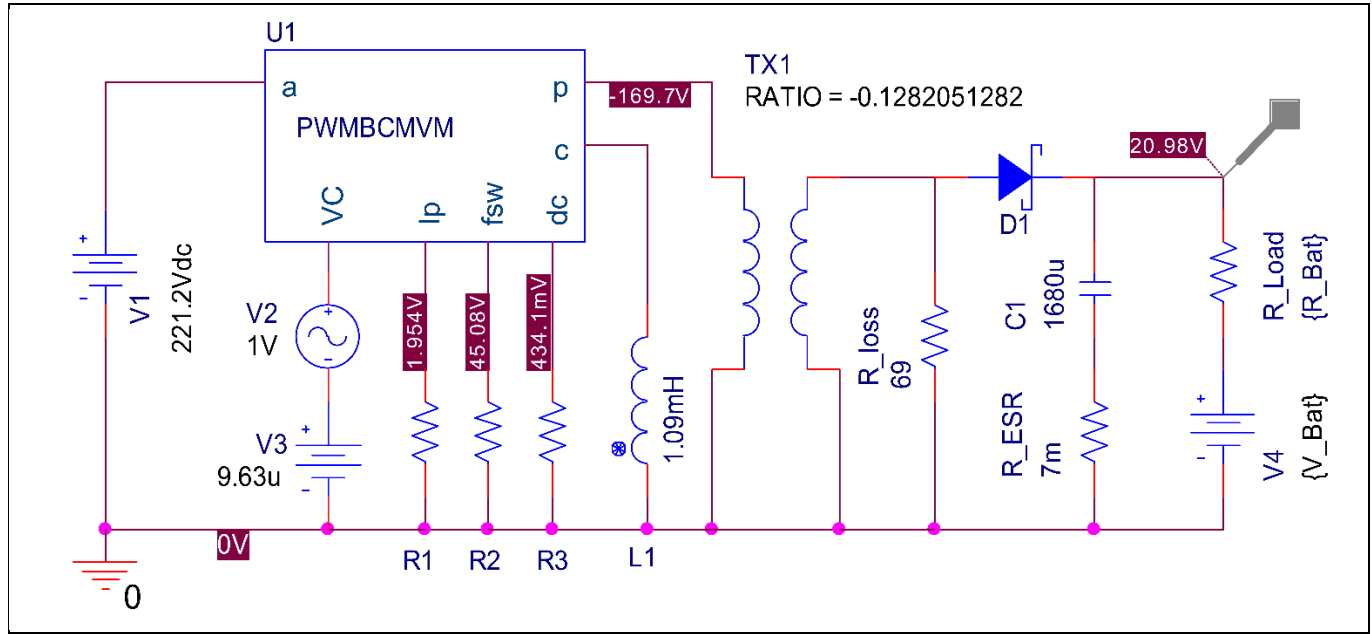


Figure 17 Schematic for simulation of averaged model of QR-Flyback

Figure 17 was generated with PSpice using the 'PWMBCMVM' model [3]. As the name implies, this is a model for a Boundary Conduction Mode (BCM) flyback in Voltage Mode (VM). It is an averaged model of the PWM switch which accepts a control voltage at pin 'VC' (actually this voltage is a measure for the on-time), input voltage at pin 'a', reflected voltage V_R at pin 'p' and finally the transformer primary side inductance L_P as a parameter. From these values, the model generates all relevant quantities.

All parameters for the simulation have been chosen to match the mathematical model of Section 7.1. The input voltage of 221.2 V is connected to input pin 'a', while the 9.63 μ V at pin 'VC' model the on-time of 9.63 μ s. The Pins 'Ip', 'fsw' and 'dc' output some of the calculated values as voltages⁵. The transformer TX1 is an ideal 'DC' transformer with a turns ratio of 39/5 (the negative sign in the schematic is just to omit crossing lines at the secondary side). The secondary is loaded with the same elements as in Figure 13. One specialty of the schematic in Figure 17 is R_{loss} . Since the averaged switch model is a lossless one, R_{loss} arbitrarily adds about 10% loss to end up with the 90% efficiency we assumed in our mathematical model.

When doing an AC analysis, SPICE first calculates a steady state solution before doing the frequency sweep of V2 in this case. Several values from this steady state analysis are given in the schematic. The output voltage is almost perfectly at 21 V and the reflected voltage visible at pin is calculated to be 169.7 V, compared to 169.3 V from Equation 53.

The voltage at Ip is equivalent to a peak current of 1.95 A (1.95 A), a switching frequency at fsw reads as 45.08 kHz (design assumption was 45 kHz) and the calculated duty-cycle at 'DC' is 0.434.

⁵ Resistors R1 .. R3 are dummy loads of 1 k Ω .

Feedback circuit

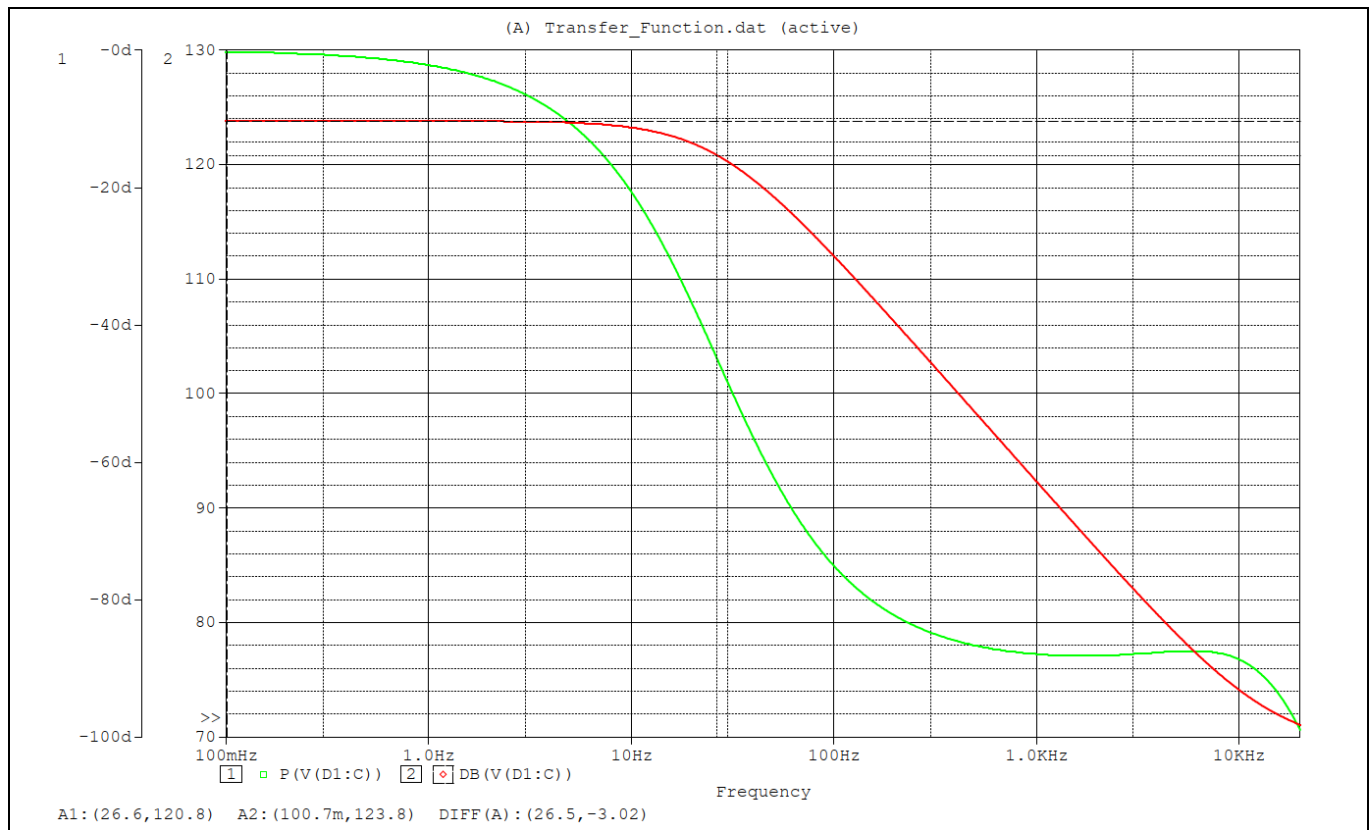


Figure 18 Simulated bode plot of QR flyback

The simulated bode plot as well shows a fair match to the mathematical model of Section 7.1. The low frequency gain is 123.8 dB and the pole can be found at 26.5 Hz. But the behavior at frequencies above several kHz differs considerably. Since the closed-loop corner frequency will be in the low kHz range, the detailed behavior at 10 kHz is of minor interest.

7.1.2 On-time Modulator

So far, we investigated the pure power stage that is on-time controlled. The ICC80QSG contains an on-time modulator that converts the feedback signal, which is the current drawn from pin 'VS', into a corresponding on-time.

The large-signal transfer function of the on-time modulator is given by:

$$t_{ON}(I_{VS}) = t_{ONmax} \cdot \min\left(1, 2^{\frac{I_{VS}-I_{VSmin}}{50 \mu A}}\right) \left[\frac{s}{A}\right]$$

Equation 109

Where,

I_{VS} : Current drawn from pin VS

t_{ONmax} : Maximum on-time. This value changes with input voltage, see datasheet.

I_{VSmin} : Minimum ADC current that leads to t_{ONmax} at minimum input voltage. 210 μA typical.

Feedback circuit

This means the t_{ON} is halved with every 50 μA I_{VS} is higher than the minimum of 210 μA (typ.). If the current drawn out of 'VS' is below 210 μA then t_{ON} stays at t_{ONmax} . Nevertheless, a resistor from VS to GND should ensure a minimum current flow close to 210 μA , as stated in the device datasheet.

The small signal transfer function is determined by the first derivative with respect to I_{VS} , evaluated at the desired steady-state operating point I_{VSop} .

$$H_{MOD}(s) = \left. \frac{d t_{ON}(I_{VS})}{d I_{VS}} \right|_{I_{VS}=I_{VSop}} = t_{ONmax} \cdot \frac{\ln(2)}{50 \mu A} \cdot 2^{-\frac{I_{VSop}-210 \mu A}{50 \mu A}}$$

Equation 110

Obviously, the gain varies with I_{VSop} and halves every 50 μA I_{VSop} is higher than I_{VSmin} . Again, you need to evaluate the gain at full output power which corresponds to an on-time t_{ONop} of 9.63 μs . This on-time occurs at an VS pin current I_{VSop} of:

$$I_{VSop} = 210 \mu A - \log_2 \left(\frac{t_{ONfp}}{t_{ONmax}} \right) \cdot 50 \mu A = 210 \mu A - \log_2 \left(\frac{9.63 \mu s}{12 \mu s} \right) \cdot 50 \mu A = 225.9 \mu A$$

Equation 111

In this operation point the gain of the on-time modulator is:

$$H_{MOD}(s) = t_{ONmax} \cdot \frac{\ln(2)}{50 \mu A} \cdot 2^{-\frac{I_{VSop}-210 \mu A}{50 \mu A}} = 12 \mu s \cdot \frac{\ln(2)}{50 \mu A} \cdot 2^{-\frac{225.9 \mu A-210 \mu A}{50 \mu A}} = -0.1335 \frac{s}{A}$$

Equation 112

7.1.3 Optocoupler

The transfer function of the optocoupler is its current transfer ratio (CTR). The latter is essentially independent of the frequency up to a pole which is determined by the collector pullup resistor. Since ICC80QSG has low impedance at pin VS, this pole does not affect frequency compensation.

Note that the CTR strongly depends on actual optocoupler current and it decreases considerably at low collector currents. At the same time, CTR drops with increasing temperature.

Since ICC80QSG feedback pin is controlled by current and the error amplifier output is a voltage, R_{LED} , the resistor that converts between the two, is included in the transfer function.

$$H_{OPTO}(s) = \frac{CTR}{100 \cdot R_{LED}} \left[\frac{A}{V} \right]$$

Equation 113

When an optocoupler is selected for an application, make sure that CTR is specified for collector currents below ~600 μA and that it is as high as possible at these currents.

Feedback circuit

7.1.4 Resistor Divider

In output voltage regulation mode, the divider network R_1 / R_2 sets the DC output voltage but does not affect the loop gain. This is because the inverting input of OP1 is a virtual ground, i.e., the voltage at this input is kept identical to the voltage at the non-inverting input. The latter is constant and so will be the voltage across R_2 . Only R_1 determines, together with the components in the feedback path of OP1, the gain of the compensator. Thus, the gain of the divider network in voltage regulation mode is,

$$H_{DIV}^{CV}(s) = 1 \left[\frac{V}{V} \right]$$

Equation 114

This is different for the current regulation mode. In this mode instead of the output voltage the voltage across R_S , which is proportional to the output current, is regulated. The transfer function is

$$H_{DIV}^{CC}(s) = R_S \left[\frac{V}{A} \right]$$

Equation 115

7.1.5 Error amplifier and loop compensation

The compensator for the voltage regulation loops is a type 2, which provides a zero at ω_{Zcv} and a pole at ω_{Pcv} . The transfer function for the voltage loop compensator is as follows:

$$H_{EA}^{CV}(s) = \frac{-R_3}{R_1} \cdot \frac{C_3}{C_3 + C_4} \cdot \frac{1 + \frac{1}{R_3 \cdot C_3 \cdot s}}{1 + s \cdot R_3 \cdot \frac{C_4 \cdot C_3}{C_4 + C_3}} = H_{0,EA}^{CV} \cdot \frac{1 + \frac{\omega_{Zcv}}{s}}{1 + \frac{\omega_{Pcv}}{s}} \left[\frac{V}{V} \right]$$

$$H_{0,EA}^{CV} \stackrel{\text{def}}{=} -\frac{R_3}{R_1} \cdot \frac{C_3}{C_3 + C_4}, \quad \omega_{Zcv} \stackrel{\text{def}}{=} \frac{1}{R_3 \cdot C_3}, \quad \omega_{Pcv} \stackrel{\text{def}}{=} \frac{1}{R_3 \cdot \frac{C_3 \cdot C_4}{C_3 + C_4}}$$

Equation 116

Feedback circuit

$$H_{EA}^{CC}(s) = -\frac{R_{30}}{R_{10}} \cdot \frac{C_{30}}{C_{30} + C_{40}} \cdot \frac{1 + \frac{1}{R_{30} \cdot C_{30} \cdot s}}{1 + s \cdot R_{30} \cdot \frac{C_{40} \cdot C_{30}}{C_{40} + C_{30}}} = H_{0,EA}^{CC} \cdot \frac{1 + \frac{\omega_{ZCC}}{s}}{1 + \frac{s}{\omega_{PCC}}} \left[\frac{V}{V} \right]$$

$$H_{0,EA}^{CC} \stackrel{\text{def}}{=} -\frac{R_{30}}{R_{10}} \cdot \frac{C_{30}}{C_{30} + C_{40}}, \quad \omega_{ZCC} \stackrel{\text{def}}{=} \frac{1}{R_{30} \cdot C_{30}}, \quad \omega_{PCC} \stackrel{\text{def}}{=} \frac{1}{R_{30} \cdot \frac{C_{40} \cdot C_{30}}{C_{40} + C_{30}}}$$

Equation 117

In case you have a very well defined R_{BAT} that varies only a little, you may use the type 2 for the current loop as well.

7.2 Selection of R_{LED}

Start with the calculation of the maximum value of R_{LED} :

$$R_{LED} < \frac{V_{AUX} - V_{LED} - V_D - V_{OPmin}}{I_{VS}} \cdot \frac{CTR_{min}}{100}$$

$$R_{LED} < \frac{12\text{ V} - 1.5\text{ V} - 0.6\text{ V} - 1.5\text{ V}}{650\text{ }\mu\text{A}} \cdot \frac{100}{100} = \frac{8.4\text{ V}}{650\text{ }\mu\text{A}} = \mathbf{12.9\text{ k}\Omega}$$

Equation 118

Where,

- V_{AUX} : Auxiliary supply voltage, assume 12 V.
- V_{LED} : Maximum LED forward voltage, typically 1.5 V.
- V_D : Forward voltage of diode in series to optocoupler, use 0.6 V.
- V_{OPmin} : Minimum output voltage of operational amplifier, assume 1.5 V unless you use a rail-to-rail output amplifier.
- I_{VS} : Current at pin VS to drive the device into burst mode, use 650 μA to have some margin.
- CTR_{min} : Worst case CTR, 100 in case of TLP383 G

Since this resistor influences the DC loop gain, a much smaller value can be deliberately chosen to prepare for degradation of CTR over the optocoupler lifetime. This will reduce the gain of this stage, but the loop gain is determined by the compensator, which can be adjusted to compensate. It is recommended to use between 30% and 50% of the calculated value. For example, selecting $R_{LED} = \mathbf{4.7\text{ k}\Omega}$ would provide a significant margin.

7.3 Selecting the components of CV mode feedback network

7.3.1 Divider network R_1 and R_2

With an assumed reference voltage of 3.3⁶ V the divider ratio will be as follows:

$$\frac{R_1}{R_2} = \frac{V_{OUT}}{V_{REF}} - 1 = \frac{21\text{ V}}{3.3\text{ V}} - 1 = 5.364$$

Equation 119

It can be easily determined that this ratio is well approximated by $R_1 = 30\text{ k}\Omega$ and $R_2 = 5.6\text{ k}\Omega$.

Now, it is possible to create the bode plot for the transfer function in voltage regulation mode of the combination flyback, gain modulator, optocoupler, and divider network.

It is given by $H_{FB}^{CV}(s) \cdot H_{MOD}(s) \cdot H_{OPTO}(s) \cdot H_{DIV}(s)$ (Figure 19). As stated before, there is mainly a single pole at 36.1 Hz, while the zero is outside the plot range.

7.3.2 Voltage loop compensation

Let us target to achieve a closed-loop crossover frequency $f_c = 1\text{ kHz}$. This is the recommended f_c since the internal A/D converter of ICC80QSG does not support much higher frequencies.

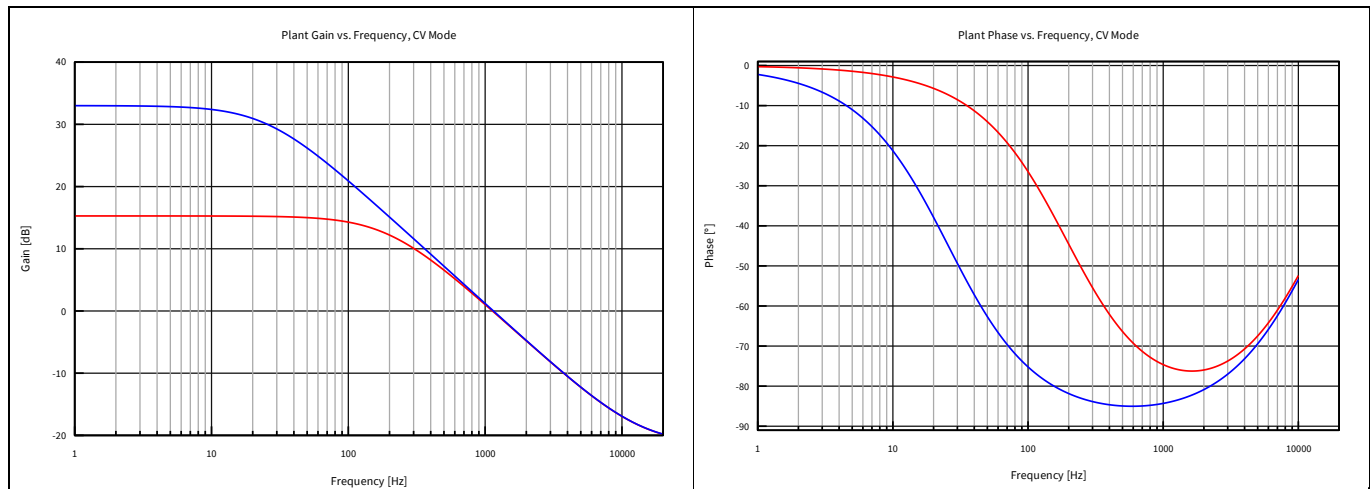


Figure 19 Calculated gain (left) and phase (right) of the plant transfer function in voltage regulation mode. Red: $V_{BAT} = 0\text{ V}$, $R_{BAT} = 5.25\text{ }\Omega$, Blue: $V_{BAT} = 20\text{ V}$, $R_{BAT} = 0.25\text{ }\Omega$.

Even without the plots of Figure 19, the loop compensation can easily be determined.

$$\omega_{P,FB} = \frac{12.3\text{ }\Omega + 0.5\text{ }\Omega}{12.3\text{ }\Omega \cdot 0.5\text{ }\Omega \cdot 1680\text{ }\mu\text{F}} = 1238.8\text{ s}^{-1} \text{ (equivalent 197.2 Hz)}$$

Equation 120

⁶ A 3.3 V have been chosen with the assumption that the setpoint might be controlled by a MCU.

Feedback circuit

The dominant pole is at 197.2 Hz. From there the gain drops by 20 dB/decade. The gain drop is $20 \cdot \log(197.2/1000) = -14.1 \text{ dB}$.

At low frequencies, the flyback has a gain of **105.9 dB** (Equation 103).

The modulator gain is 0.1335 (Equation 110) or **-17.5 dB**

The optocoupler has a gain of 1/4700 (Equation 113) or **-73.4 dB**.

Hence the plant gain is 105.9 dB -73.4 dB -17.5 dB = **15 dB** at low frequencies and drops to 1 = **0.9 dB** at 1 kHz.

This value is also evident in the Bode plot of Figure 19. However, having a plot of the plant response is not strictly necessary. Knowing the low-frequency gain and the frequency of the pole is sufficient.

Now, for $f_c = 1 \text{ kHz}$ a mid-frequency gain of about -1 dB is needed. This gain is provided by the term $H_{0,EA}^{CV}$ of the error amplifier transfer function. Since C_3 is about ten times C_2 in most cases, the term $C_3/(C_3+C_2)$ can be assumed to be 0.9 and the gain is mainly determined by the ratio R_3/R_1 .

$$R_3 = \frac{C_3+C_4}{C_3} \cdot 10^{-\frac{0.9}{20}} \cdot R_1 \approx 1.1 \cdot 0.9 \cdot 30 \text{ k}\Omega = 29.8 \text{ k}\Omega$$

Equation 121

Select the next closest standard value, which is **$R_3 = 30 \text{ k}\Omega$** .

The type 2 error amplifier could add up to -90° phase shift to the loop response which would lead to a total shift of -180° and in turn an unstable (oscillating) loop. To prevent this, add phase boost around f_c . The amount of phase boost needed for good loop-response with a phase margin φ_M of 60° [5]:

$$\varphi_B = -90^\circ + \varphi_M - \varphi_{PL} = -90^\circ + 60^\circ + 75^\circ = 45^\circ$$

Equation 122

where φ_{PL} the phase of the plant transfer function at f_c that can be taken as -75° from Figure 15. Knowing the needed phase boost φ_B , next step is to determine the frequencies of the pole and zero of the compensator transfer function [5]:

$$f_p = \tan\left(\frac{\varphi_B}{2} + 45^\circ\right) \cdot f_c = \tan(67.5^\circ) \cdot 1 \text{ kHz} = 2.41 \text{ kHz}$$

$$f_z = \frac{f_c}{\tan\left(\frac{\varphi_B}{2} + 45^\circ\right)} = \frac{1 \text{ kHz}}{\tan(67.5^\circ)} = 414.2 \text{ Hz}$$

Equation 123

Feedback circuit

Now you can calculate the values of C_3 and C_4 .

$$C_3 = \frac{1}{2 \cdot \pi \cdot f_Z \cdot R_3} = \frac{1}{2 \cdot \pi \cdot 414.2 \text{ Hz} \cdot 30 \text{ k}\Omega} = 11.6 \text{ nF}$$

$$C_4 = \frac{C_3}{2 \cdot \pi \cdot f_p \cdot C_3 \cdot R_3 - 1} = \frac{11.6 \text{ nF}}{2 \cdot \pi \cdot 2.41 \text{ kHz} \cdot 11.6 \text{ nF} \cdot 30 \text{ k}\Omega - 1} = 2.41 \text{ nF}$$

Equation 124

Next closest standard values are $C_3 = 12 \text{ nF}$ and $C_4 = 2.2 \text{ nF}$.

The calculated compensator response shown in [Figure 20](#) reveals the desired behavior. Especially from the asymptotic behavior the desired zero at slightly more than 400 Hz, the -1 dB mid-band gain and the pole just below 3 kHz are clearly visible.

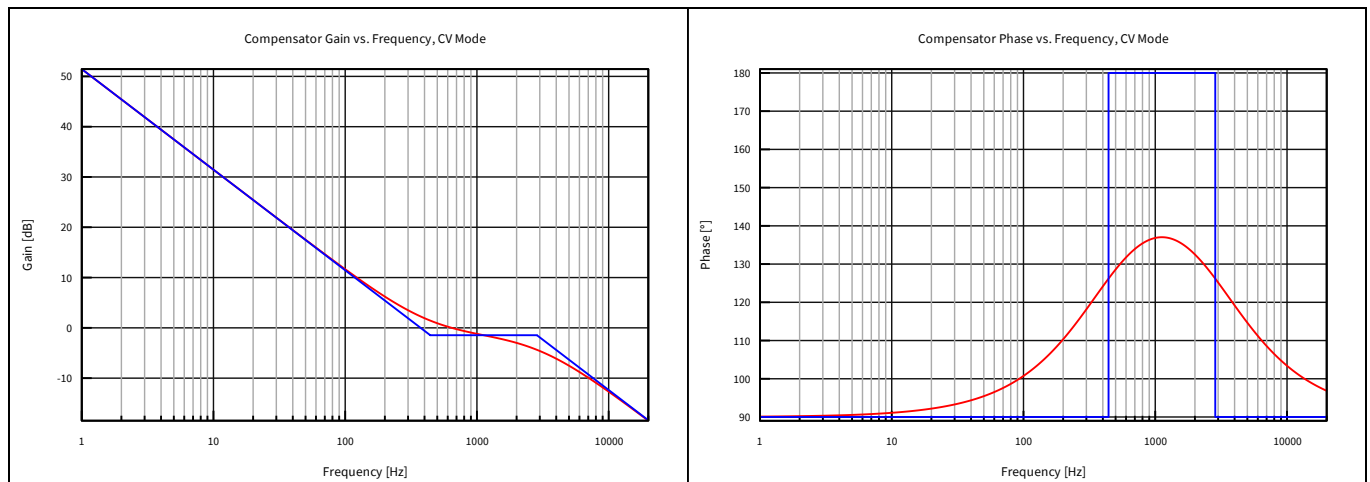


Figure 20 Calculated gain (left) and phase (right) of the error amplifier transfer function in voltage regulation mode. The calculated response is shown in red, while the asymptotic behavior is given in blue.

Now it is possible to calculate $H_{FB}^{CV}(s) \cdot H_{MOD}(s) \cdot H_{OPTO}(s) \cdot H_{DIV}(s) \cdot H_{EA}^{CV}(s)$, the open-loop transfer function in voltage regulation mode and create the bode-plot as displayed in ([Figure 21](#)).

The gain response is close to the defined target for both cases: with battery model (red curve) and a pure resistive load (blue). Furthermore, both the zero-crossing frequency and phase margin are very close to the targeted values.

Feedback circuit

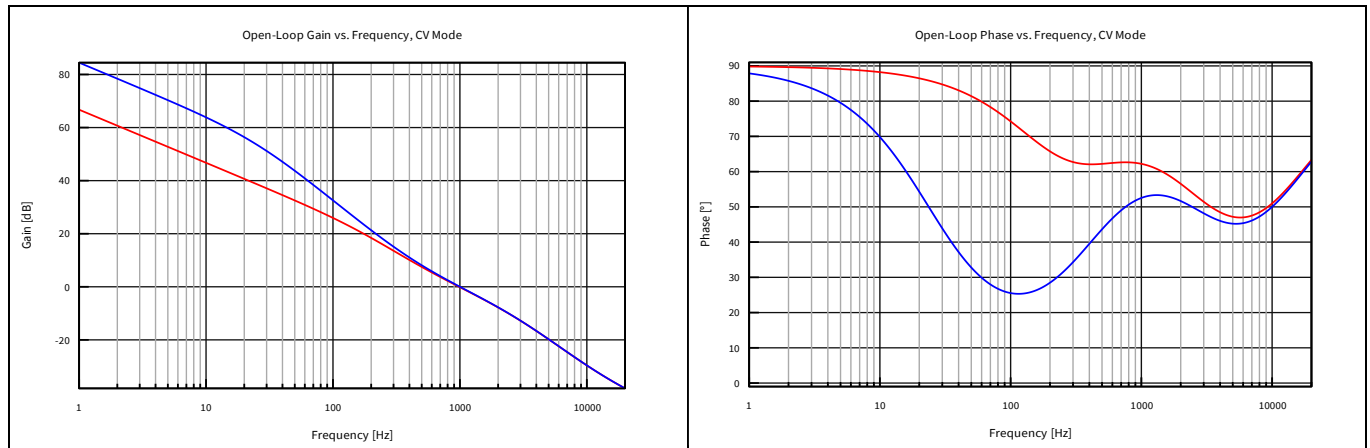


Figure 21 Calculated gain (left) and phase (right) of the open-loop transfer function in voltage regulation mode. Red: $V_{BAT} = 0\text{ V}$, $R_{BAT} = 5.25\ \Omega$, Blue: $V_{BAT} = 20\text{ V}$, $R_{BAT} = 0.25\ \Omega$

7.4 Selecting the components of CC mode feedback network

If the load of the charger would be purely resistive, the transfer function in constant current mode, $H_{FB}^{CC}(s)$, would be essentially the same as that for constant voltage mode, except that the gain term was smaller by a factor $1/RL$. But, as we have seen, with a battery the response in current regulation mode is substantially different from that in voltage regulation.

7.4.1 Current sense resistor

The error amplifier gets its input signal from shunt resistor R_S . A higher value of that resistor results in a higher input signal, which in turn improves the signal-to-noise ratio and accuracy. At the same time, the power loss increases as well, and a compromise is necessary.

Select the value of R_S such that the full-scale signal is between 100 mV and 200 mV. This optimal range typically provides a decent signal-to-noise ratio, even with lower-cost operational amplifiers.

With the targeted 4 A output, a 200 mV drop would cause 800 mW loss, most likely causing a hotspot on the PCB, disregarding the efficiency loss. Therefore, select the lower end, i.e., a 100 mV drop, and use a low-offset operational amplifier.

$$R_S = \frac{V_{Rsense}}{I_{OUTmax}} = \frac{100\text{ mV}}{4\text{ A}} = 25\text{ m}\Omega$$

Equation 125

Although such resistor is readily available, using several higher resistance ones in parallel can increase the robustness and spread the heat more evenly. For instance, four 120 mΩ and one 150 mΩ resistors in parallel would, for example be a suitable solution.

The ratio of resistors R40 and R50 can be determined from [Equation 92](#).

Feedback circuit

$$\frac{R_{50}}{R_{40}} = \frac{V_{REF}}{I_{OUTmax} \cdot V_{Rsense}} = \frac{3.3 V}{100 mV} = 33$$

Equation 126

If you select $R_{40} = 1 \text{ k}\Omega$, then $R_{50} = 33 \text{ k}\Omega$.

7.4.2 Compensation of the current regulation loop

For the compensation of the current loop, follow exactly the same scheme as that of the voltage loop. Since the position of the pole, the slope of the gain at higher frequencies and the phase-response are exactly the same as those of the voltage loop, your job looks very easy at first. But unlike before, the plant gain varies by more than 25 dB at the desired f_c of 1 kHz between $R_{BAT} = 5.25 \Omega$ and $R_{BAT} = 0.5 \Omega$. For the selection of the mid band gain, focus and the gain curve with $R_{BAT} = 0.5 \Omega$ since that is the most realistic value.

Unlike the voltage loop, the current loop might show marginal stability or even be unstable with other loads than the battery or the battery model.

The dominant pole remains unchanged, located at 197.2 Hz.

From 197.2 Hz to 1 kHz, the gain drop is same as before: **-14.1 dB**.

At low frequencies, the flyback has a gain of **111.9 dB** (Equation 108).

Modulator and optocoupler gain are the same as before, **-17.5 dB** and **-73.4 dB**, respectively.

The current sense adds a gain of $0.025 = \text{-32 dB}$ (Equation 115).

The plant gain is calculated as $111.9 \text{ dB} - 73.4 \text{ dB} - 17.5 \text{ dB} - 32 \text{ dB} = \text{-11 dB}$ at low frequencies and drops to **-25.1 dB** at 1 kHz. With the needed gain of 25 dB and the selection of $R_1 = 1 \text{ k}\Omega$, you get for R_3 :

$$R_3 = \frac{C_3 + C_4}{C_3} \cdot 10^{\frac{25}{20}} \cdot R_1 \simeq 1.1 \cdot 17.8 \cdot 1 \text{ k}\Omega = \textbf{19.6 k}\Omega$$

Equation 127

Next closest standard value is $R_3 = 20 \text{ k}\Omega$. Since the phase response isn't changed, exactly the same phase boost of 45° is needed, leading for $f_p = 2.41 \text{ kHz}$ and $f_z = 414.2 \text{ Hz}$ as before. Now calculate the values of C_3 and C_4 :

$$C_3 = \frac{1}{2 \cdot \pi \cdot f_z \cdot R_3} = \frac{1}{2 \cdot \pi \cdot 414.2 \text{ Hz} \cdot 20 \text{ k}\Omega} = \textbf{19.6 nF}$$

$$C_4 = \frac{C_3}{2 \cdot \pi \cdot f_p \cdot C_3 \cdot R_3 - 1} = \frac{19.6 \text{ nF}}{2 \cdot \pi \cdot 2.41 \text{ kHz} \cdot 19.6 \text{ nF} \cdot 20 \text{ k}\Omega - 1} = \textbf{3.96 nF}$$

Equation 128

Next closest standard values are $C_3 = 22 \text{ nF}$ and $C_4 = 3.9 \text{ nF}$.

Feedback circuit

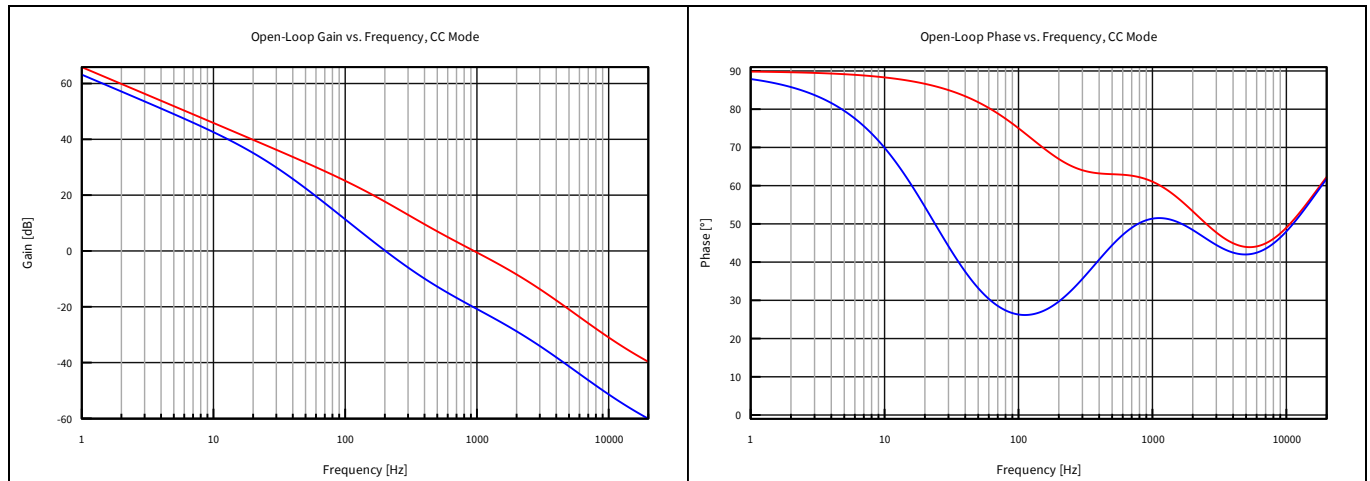


Figure 22 Calculated gain (left) and phase (right) of the open-loop transfer function in voltage regulation mode. Red: $V_{BAT} = 19\text{ V}$, $R_{BAT} = 0.5\ \Omega$, Blue: $V_{BAT} = 0\text{ V}$, $R_{BAT} = 5.25\ \Omega$.

Finally, you can create the bode plots for the current regulation loop as shown in [Figure 22](#). Again, the expected response is well met in case of the $0.5\ \Omega / 19\text{ V}$ load, but, unlike the voltage loop, the response differs considerably in case of the resistor only load of $5.25\ \Omega$. For this case, the gain crossover frequency is lowered to 200 Hz. While this in itself is not a major issue, the slope at crossover is 2nd order (-40 dB/decade) and phase margin is 30°. This indicates that the loop has marginal stability for this load or is even unstable. It would be a good idea to verify this through by simulation before testing it in hardware. Alternatively, you can simply ignore this load since it is not a realistic one for a charger.

Appendix A: Rectification and bulk capacitor

It's a well-known fact that the input current of a rectifier circuit followed by a bulk capacitor is anything else than sinusoidal when driven by a sinusoidal input voltage.

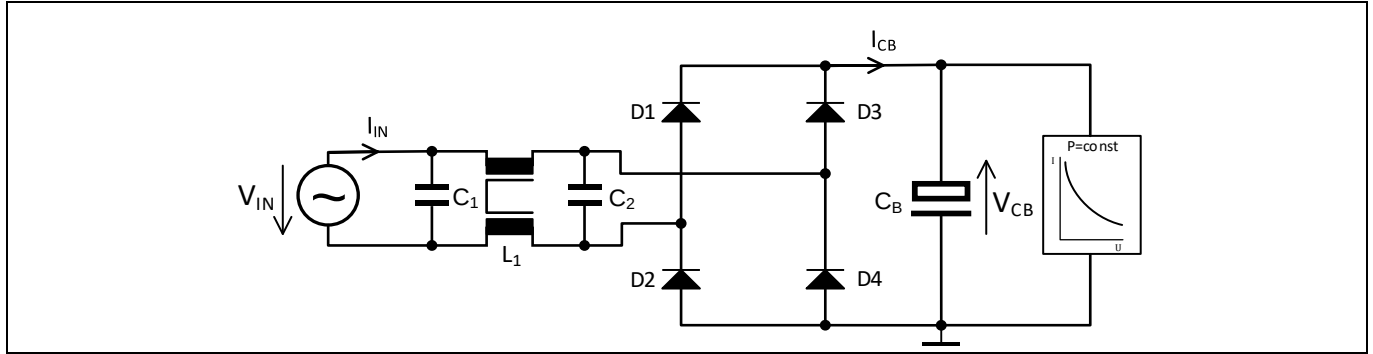


Figure 23 Typical full bridge rectifier circuit with EMI filter

Note: The flyback stage is modeled by a constant power load consuming power P_{Lo} .

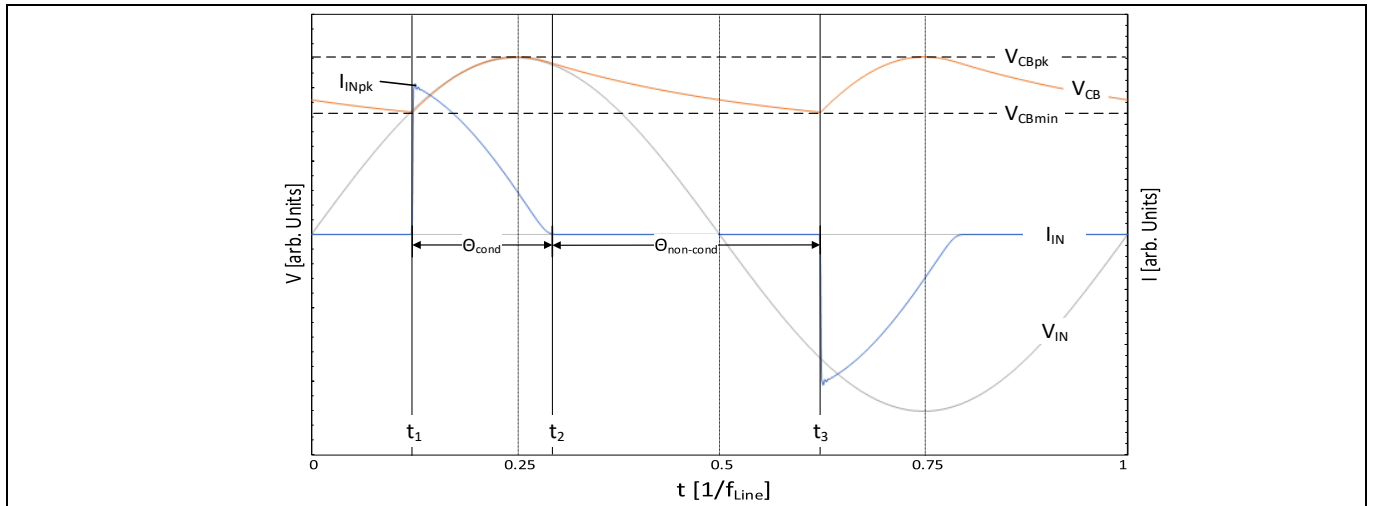


Figure 24 Waveforms of input voltage (V_{IN} , grey), input current (I_{IN} , blue) and bulk capacitor voltage (V_{CB} , orange) of rectifier circuit

An input current is only possible when either D1 and D4 or D3 and D3 are forward biased i.e. when at time t_1 the instantaneous input voltage $V_{IN}(t_1)$ is higher than the bus capacitor voltage $V_{CB}(t_1)$. The input current almost immediately jumps to its peak value I_{INpk} , which is determined by the sum of the load current and the current needed to charge C_B :

$$I_{INpk} = C_B \cdot \frac{d}{dt} V_{IN}(t) + I_L = C_B \cdot V_{INpk} \cdot \omega \cdot \cos(\omega \cdot t_1) + \frac{P_L}{V_{CB}(t_1)}$$

Equation 129

After t_1 , the current decays with a non-linear like shape. When the input voltage reaches its maximum, the capacitor charging current becomes zero and the input current is identical to the load current at this point in time.

Appendix A: Rectification and bulk capacitor

After the line voltage reaches its maximum, the capacitor C_B begins to discharge. However, as long as the load current would discharge C_B at a higher dU/dt than determined by the sinusoidal input waveform, the diodes stay forward-biased, and the input current will keep flowing. At t_2 , the point in time where the load current starts to discharge the capacitor C_B at a lower rate than the input waveform, the input current stops.

$$t_2 = \frac{\arcsin\left(\frac{2 \cdot P_L}{V_{INpk}^2 \cdot C_B \cdot \omega}\right)}{2 \cdot \omega} + \frac{1}{4 \cdot f_{Line}}$$

Equation 130

The interval $t_3 - t_1$ is equal to half the period of the input waveform i.e. $1/(2 \cdot f_{Line})$. Then the conduction angle of the input current per half-wave becomes:

$$\theta_{Cond} = \frac{t_2 - t_1}{t_3 - t_1} \cdot 180^\circ = 2 \cdot (t_2 - t_1) \cdot f_{Line} \cdot 180^\circ \stackrel{\text{def}}{=} d_{IN} \cdot 180^\circ$$

Equation 131

Unfortunately, there is no closed-form solution for the calculation of t_1 and it must be calculated by numerical methods.

It was mentioned that the input current falls with a nonlinear shape after t_1 . Actually, it can be approximated quite well by a linear decay, leading to a relatively simple approximation of the input RMS current:

$$I_{INrms} \cong I_{INpk} \cdot \sqrt{\frac{d_{IN}}{3}} = \left(C_B \cdot V_{INpk} \cdot \omega \cdot \cos(\omega \cdot t_1) + \frac{P_L}{V_{INpk} \cdot \sin(\omega \cdot t_1)} \right) \cdot \sqrt{\frac{2 \cdot (t_2 - t_1) \cdot f_{Line}}{3}}$$

Equation 132

To determine t_3 the shape of V_{CB} between t_2 and t_3 is needed. In this interval C_B is discharged by the load current I_L :

$$V_{CB}(t) = \sqrt{V_{CB}(t_2)^2 - \frac{2 \cdot P_L}{C_B} \cdot (t - t_2)} \quad , \quad t_2 \leq t \leq t_3$$

Equation 133

If the forward voltage of the rectifier is neglected, at t_3 the rising input voltage becomes equal to $V_{CB}(t_3)$.

$$V_{INpk} \cdot \sin(\omega \cdot t_3) = \sqrt{V_{CB}(t_2)^2 - \frac{2 \cdot P_L}{C_B} \cdot (t_3 - t_2)}$$

Equation 134

Appendix A: Rectification and bulk capacitor

As said, the above equation needs to be solved numerically to determine t_3 . Finally, t_1 is equal to $t_3 - 1/(2 \cdot f_{Line})$ and the minimum capacitor voltage V_{CBmin} is:

$$V_{CBmin} = V_{INpk} \cdot \sin(\omega \cdot t_3)$$

Equation 135

In many applications a minimum capacitor voltage V_{CBmin} will be a given input parameter and the required minimum capacitance C_B to achieve this needs to be calculated. This could as well be done numerically. But with the fair assumption that $t_2 = 1/(4 \cdot f_{Line})$, i.e., the first term in [Equation 130](#) can be neglected. This assumption is fair for two reasons. First, that term is typically well below 1 ms and therefore really much smaller than the second. Secondly, and even more important, the value for C_B does not need to be calculated with the highest precision. Electrolytic capacitors anyway have a huge tolerance of typically -20%/+50% and the next higher standard value needs to be selected anyway. With the above-mentioned simplification C_B can be estimated:

$$C_B > \frac{P_{IN} \cdot \left(\frac{\arcsin\left(\frac{V_{CBmin}}{V_{INpk}}\right)}{\pi} + \frac{1}{2} \right)}{f_{LI} \cdot (V_{INpk}^2 - V_{CBmin}^2)}$$

Equation 136

If the V_{MIN} of [Equation 136](#) is the absolute minimum you can tolerate, the value of C_B should be at least 25% higher than calculated.

When a suitable value for C_B has been found with the help of [Equation 136](#), then [Equation 135](#) can be used to calculate the true minimum voltage. Finally, peak and RMS input current is determined with the rest of the equations presented above.

Appendix B: Input voltage doubler

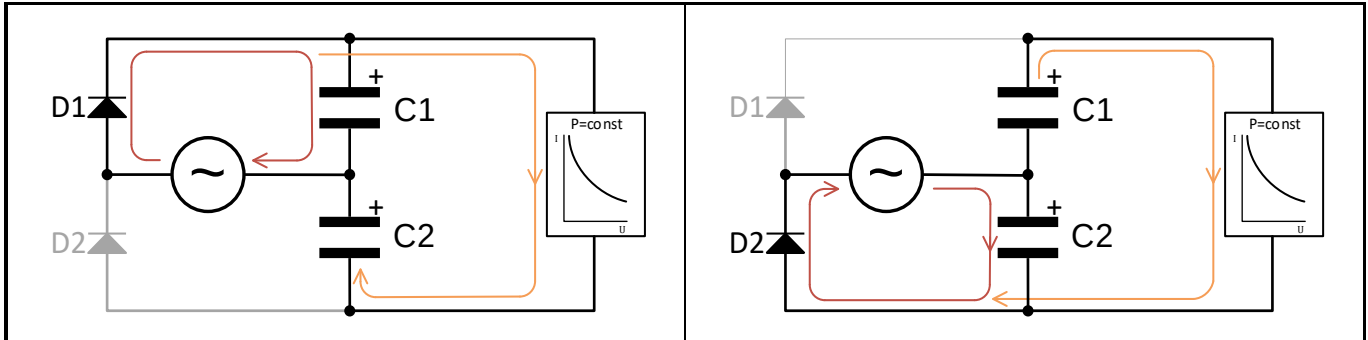


Figure 25 Voltage doubler principle of operation for positive and negative half-wave.

The voltage doubler is an effective solution for the supply of a DC/DC stage that was designed for a higher input voltage with a low line voltage. It does not exactly double the input voltage but comes close to that. As visible from [Figure 25](#), the capacitor C_1 is charged in the positive half of the power line and C_2 in the negative half. With a 50 Hz input that means that each of them carries a 50 Hz ripple but with 180° phase shift ([Figure 26](#)). The downstream converter sees the sum of the two capacitor voltages which is almost double the peak input voltage and has a 100 Hz ripple.

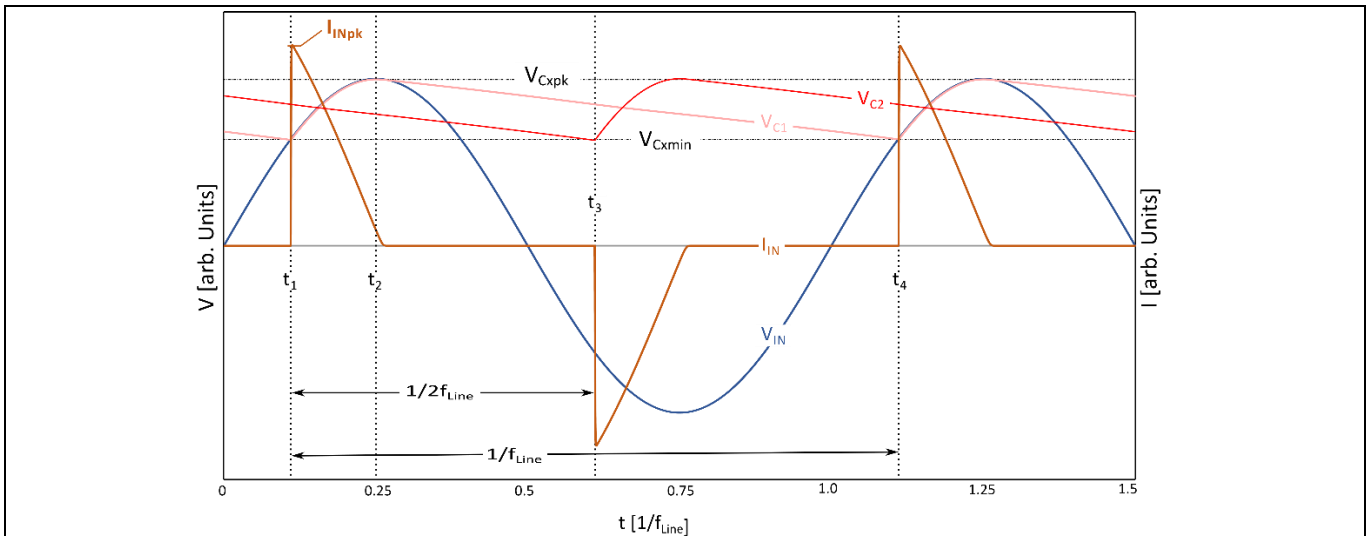


Figure 26 Input voltage, input current and capacitor voltages of C_1 and C_2

The doubler configuration is mathematically more complicated than the bridge rectifier. Whenever one of the capacitors is charged and its voltage is forced to follow the input voltage, the other is discharged by the load current, which is inversely proportional to the sum of the capacitor voltages, at the same time.

Fortunately, the treatment can be simplified by making some basic simplifications. First of all, C_1 and C_2 shall have identical values, which is the case in virtually all practical applications.

The second assumption is that the charging of the respective capacitor stops exactly at a maximum of the input voltage which implies that $t_2 = 1/(4 \cdot f_{Line}) = T/4$.

Last assumption is that in the discharge phase of a capacitor, say C_1 , it is discharged as if it had to contribute half the load power during its complete discharge time. In other words, the discharge current of C_1 is assumed to be only determined by the voltage of C_1 itself and not influenced by the voltage of C_2 . And vice versa.

Appendix B: Input voltage doubler

With the above assumptions [Equation 133](#) can be rewritten for C_1 as shown in [Equation 137](#). A similar expression holds for the discharge of C_2 as well.

$$V_{C1}(t) \cong \sqrt{V_{INpk}^2 - \frac{P_L}{C_1} \cdot \left(t - \frac{T}{4}\right)} \quad \text{with} \quad \frac{T}{4} \leq t \leq t_4$$

Equation 137

Now t_4 , the point in time C_1 starts to be charged again, can be approximated by numerically solving [Equation 138](#).

$$V_{INpk} \cdot \sin(\omega \cdot t_4) = \sqrt{V_{INpk}^2 - \frac{P_L}{C_1} \cdot \left(t_4 - \frac{T}{4}\right)}$$

Equation 138

With t_4 the minimum output voltage can be estimated to be:

$$V_{BUSdou,min} \cong V_{C1min} + V_{C2}(t_4) = V_{INpk} \cdot \sin(\omega \cdot t_4) + \sqrt{V_{INpk}^2 - \frac{P_L}{C_2} \cdot \left(t_4 - \frac{3 \cdot T}{4}\right)}$$

Equation 139

The second term comes from the fact that the C_2 had been charged to V_{INpk} at time $3/(4 \cdot f_{Line})$.

Similarly, the maximum bus voltage is approximately given by [Equation 140](#) and will be the closer to $2 \cdot V_{INpk}$ as the larger the values of C_1 and C_2 are:

$$V_{BUSdou,max} \cong V_{C1pk} + V_{C2}\left(\frac{5}{4 \cdot f_{Line}}\right) = V_{INpk} + \sqrt{V_{INpk}^2 - \frac{P_L}{C_2 \cdot 2 \cdot f_{Line}}}$$

Equation 140

There is no closed form solution for the minimum capacitor values needed for C_1 and C_2 to achieve a given minimum bus voltage. But each of the two capacitors has to provide half of the load power at about half of the minimum bus voltage V_{CBmin} . It seems logical then that [Equation 136](#) is a fair starting point if used with half the power and half of V_{CBmin} and one half-wave longer discharge time. It's not surprising that we end up with about double the capacitor values as in the bridge rectifier case finally.

Appendix B: Input voltage doubler

$$C_1 = C_2 \approx \frac{P_{IN} \cdot \left(\frac{a \sin\left(\frac{V_{CBmin}}{2 \cdot V_{INpk}}\right)}{\pi} + \frac{3}{2} \right)}{2 \cdot f_{Line} \cdot \left(V_{INpk}^2 - \frac{1}{4} \cdot V_{CBmin}^2 \right)}$$

Equation 141

Equation 141 estimates a too big value for C_1 and C_2 and you should check whether next smaller standard value fits the requirements.

The peak input current of the doubler is calculated similarly to Equation 129 with the modification that the capacitor being charged, say C_2 , provides only half the load power while the other half is provided from C_1 :

$$I_{INdou,pk} = C_2 \cdot V_{INpk} \cdot \omega \cdot \cos(\omega \cdot t_1) + \frac{P_{IN}}{2 \cdot V_{INpk} \cdot |\sin(t_1 \cdot \omega)|}$$

Equation 142

The "duty cycle" of the input current differs from the bridge rectifier where t_2 is assumed to be $T/4$.

$$dc_{INdou} = 2 \cdot \left(\frac{T}{4} - t_1 \right) \cdot f_{Line}$$

Equation 143

Although the voltage doubler needs only two diodes for rectification, it is strongly recommended to use a bridge rectifier nevertheless. You can easily understand the reason why this is the more robust solution with the help of Figure 27.

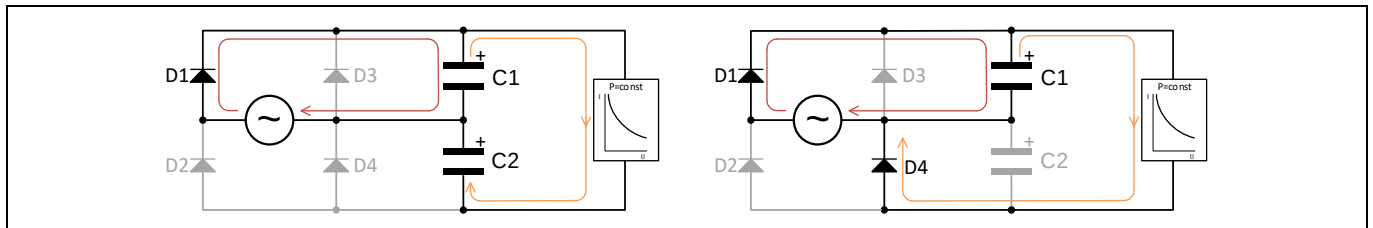


Figure 27 Voltage doubler circuit with bridge rectifier prevents reverse bias of electrolytic capacitors

In a doubler circuit, the two capacitors are discharged in series. Right at the line voltage maximum one capacitor will contain a much higher charge than the other. In Figure 27, C_1 contains a higher charge than C_2 . In an overload condition it might happen now that C_2 will be completely discharged and even reverse biased since C_1 is still providing current to the load. The same is possible with C_1 in the other half-wave.

The bridge rectifier configuration prevents such reverse biasing which could lead to capacitor damage.

Another advantage of the bridge rectifier is that it is relatively easy to make the design suitable for the universal input range.

Appendix B: Input voltage doubler

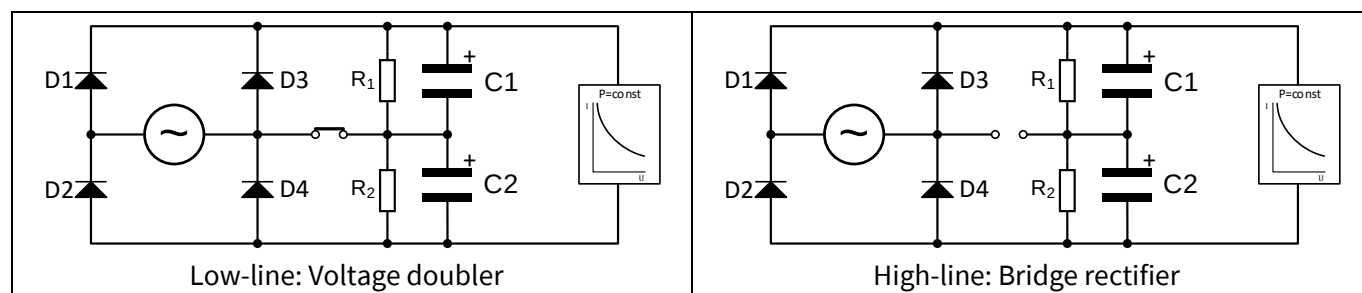


Figure 28 Input voltage doubler configuration

By placing a simple wire connection or not the input can be changed from voltage doubler to bridge rectifier configuration. This way the power supply can either work with low- or high-line and no redesign of the flyback stage is needed.

Appendix C: Estimating diode forward loss

Because of their non-linear voltage-current characteristics, it is not so easy to provide a simple formula for the forward loss of a diode if the current is not a pure DC. However, with an extremely simple approximation of the diode forward characteristic, you get a formula for loss estimation that is accurate enough for most purposes.

Mathematically, the diode forward loss P_{Dfwd} can be expressed as:

$$P_{Dfwd} = \frac{1}{T} \int_0^T V_{Dfwd}(t) \cdot I_D(t) dt = \frac{1}{T} \int_0^T V_{Dfwd}(I_D(t)) \cdot I_D(t) dt$$

Equation 144

V_{Dfwd} is a function of the current flowing through the diode and you get a mathematical representation of it by inverting the Shockley diode equation [7]. But the parameters in this equation are not known a priori and you have to determine these by fitting the values of the mathematical representation to the measured ones.

A much simpler to use but nevertheless fairly accurate approximation is found by modeling the diode forward characteristic by a voltage source in series to a resistor as visualized in Figure 29.

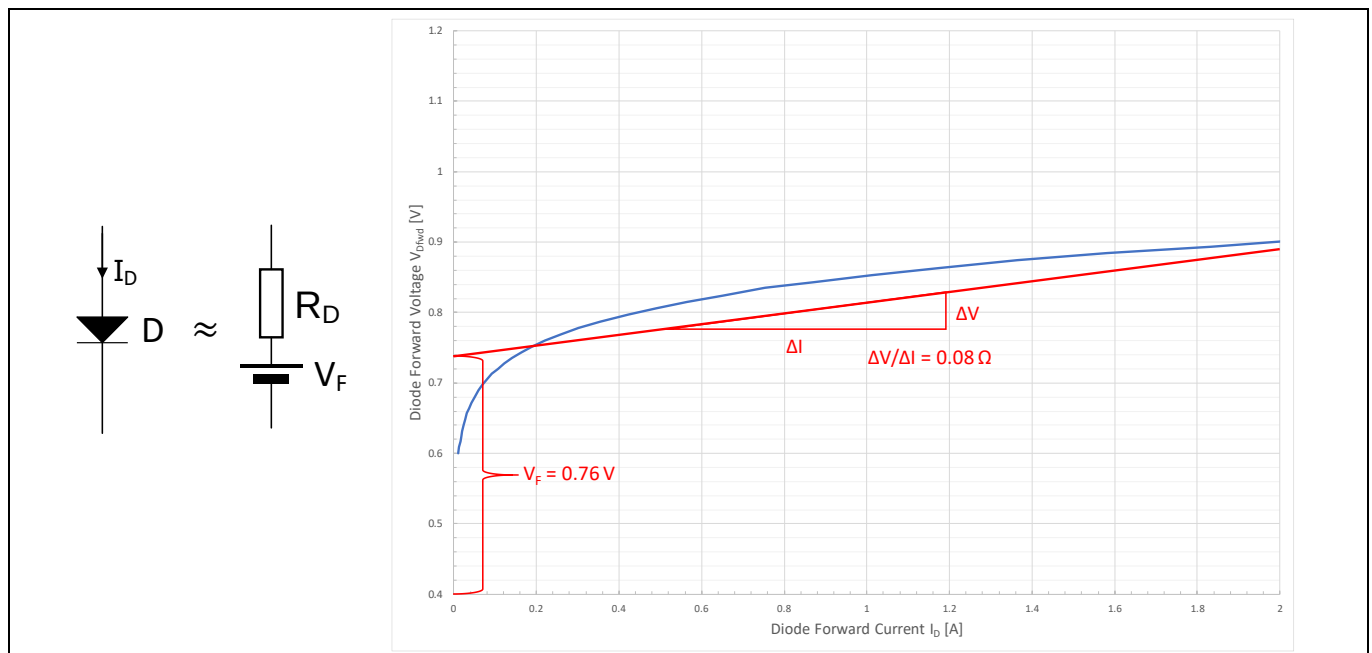


Figure 29 Approximation of diode forward characteristic by voltage source V_F in series to resistor R_D

With the above-mentioned model Equation 144 becomes:

$$P_{Dfwd} = \frac{1}{T} \int_0^T (V_F + R_D \cdot I_D(t)) \cdot I_D(t) dt = V_F \cdot I_{Davg} + R_D \cdot I_{Drms}^2$$

Equation 145

Now the diode forward loss can be easily estimated based on readily available values like average diode current I_{Davg} and its RMS-value I_{Drms} . Still, you need to find the two parameters V_F and R_D by manually fitting a line to the datasheet curve, as shown in Figure 29. This is more an art than a science and absolute accuracy is not

Appendix C: Estimating diode forward loss

needed. But you definitely need to use the right scaling of the diode characteristic. For example, if your currents are in the range of, say, 2 A you should make the fit look reasonable in the range between 0 A and 2 A and not in the range between 10 A and 20 A.

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ICC80QSG QR flyback controller for battery charger applications of up to 120 W



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Revision history

Document revision	Date	Description of changes
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