512 Mb (64 MB) FS-S Flash

SPI Multi-I/O, 1.8 V

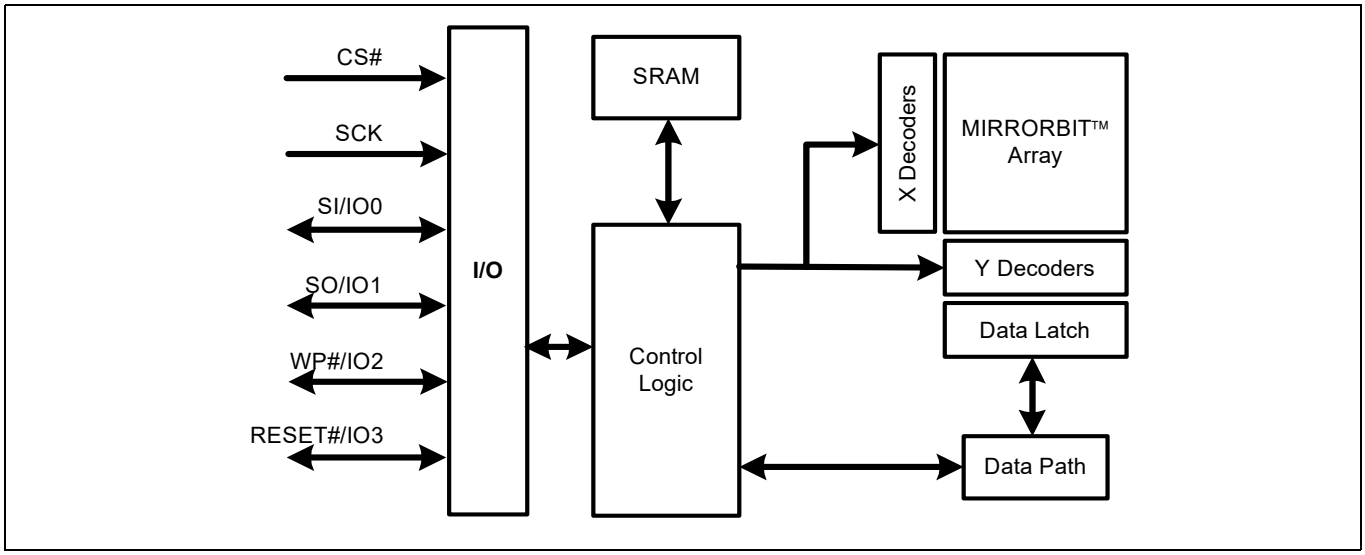
Features

- Serial peripheral interface (SPI) with multi-I/O
  - SPI clock polarity and phase modes 0 and 3
  - Double data rate (DDR) option
  - Extended addressing: 24- or 32-bit address options
  - Serial command subset and footprint compatible with S25FL-A, S25FL-K, S25FL-P, and S25FL-S SPI families
  - Multi I/O command subset and footprint compatible with S25FL-P, and S25FL-S SPI families
- Read
  - Commands: Normal, Fast, Dual I/O, Quad I/O, DDR Quad I/O
  - Modes: Burst wrap, continuous (XIP), QPI
  - Serial flash discoverable parameters (SFDP) and common flash interface (CFI) for configuration information
- Program
  - 256 or 512 bytes page programming buffer
  - Program suspend and resume
  - Automatic error checking and correction (ECC) – Internal hardware ECC with single bit error correction
- Erase
  - Hybrid sector option
    - Physical set of eight 4-KB sectors and one 224-KB sector at the top or bottom of address space with all remaining sectors of 256-KB
  - Uniform sector option
    - Uniform 256-KB blocks
  - Erase suspend and resume
  - Erase status evaluation
- Cycling endurance
  - 100,000 program-erase cycles, minimum
- Data retention
  - 20 year data retention, minimum
- Security features
  - One time program (OTP) array of 1024 bytes
  - Block protection:
    - Status Register bits to control protection against program or erase of a contiguous range of sectors.
    - Hardware and software control options
  - Advanced sector protection (ASP)
    - Individual sector protection controlled by boot code or password
    - Option for password control of read access
- Technology
  - 65-nm MIRRORBIT™ technology with Eclipse architecture
- Supply voltage
  - 1.7 V to 2.0 V

Logic block diagram

- Temperature range / grade
  - Industrial (-40°C to +85°C)
  - Industrial plus (-40°C to +105°C)
  - Automotive, AEC-Q100 grade 3 (-40°C to +85°C)
  - Automotive, AEC-Q100 grade 2 (-40°C to +105°C)
  - Automotive, AEC-Q100 grade 1 (-40°C to +125°C)
- Packages (all Pb-free)
  - 16-lead SOIC 300 mil (SO3016)
  - WSON 6 × 8 mm (WNH008)
  - BGA-24 6 × 8 mm
    - 5 × 5 ball (FAB024) footprint
  - Known good die and known tested die

Logic block diagram



Performance summary

Maximum read rates

Command	Clock rate (MHz)	MBps
Read	50	6.25
Fast Read	133	16.5
Dual Read	133	33
Quad Read	133	66
DDR Quad I/O Read	80	80

Typical program and erase rates

Operation	KBps
Page programming (256-bytes page buffer)	711
Page programming (512-bytes page buffer)	1078
4-KB Physical sector erase (Hybrid sector option)	17
256-KB Sector erase (Uniform logical sector option)	275

Typical current consumption, –40°C to +85°C

Operation	Current (mA)
Serial Read 50 MHz	10
Serial Read 133 MHz	20
Quad Read 133 MHz	60
Quad DDR Read 80 MHz	70
Program	60
Erase	60
Standby	0.07
Deep power down	0.006

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1 Overview

1.1 General description

The S25FS512S device is a flash non-volatile memory product using:

- MIRRORBIT™ technology - that stores two data bits in each memory array transistor
- Eclipse architecture - that dramatically improves program and erase performance
- 65-nm process lithography

The S25FS512S connects to a host system via a serial peripheral interface (SPI). Traditional SPI single bit serial input and output (Single I/O or SIO) is supported as well as optional two-bit (Dual I/O or DIO) and four-bit wide Quad I/O (QIO) or quad peripheral interface (QPI) serial commands. This multiple-width interface is called SPI Multi-I/O or MIO. In addition, there are double data rate (DDR) read commands for QIO and QPI that transfer address and read data on both edges of the clock.

The FS-S Eclipse architecture features a Page Programming Buffer that allows up to 512 bytes to be programmed in one operation, resulting in faster effective programming and erase than prior generation SPI program or erase algorithms.

Executing code directly from flash memory is often called eXecute-In-Place (XIP). By using S25FS512S devices at the higher clock rates supported, with Quad or DDR-Quad commands, the instruction read transfer rate can match or exceed traditional parallel interface, asynchronous, NOR flash memories, while reducing signal count dramatically.

The S25FS512S products offer high densities coupled with the flexibility and fast performance required by a variety of mobile or embedded applications. They are an excellent solution for systems with limited space, signal connections, and power. They are ideal for code shadowing to RAM, executing code directly (XIP), and storing reprogrammable data.

1.2 Migration notes

1.2.1 Features comparison

The S25FS512S is command subset and footprint compatible with prior generation FL-S, FL-K, and FL-P families. However, the power supply and interface voltages are nominal 1.8 V.

Table 1 SPI families comparison

Parameter	FS-S	FL-S	FL-K	FL-P
Technology Node	65-nm	65-nm	90-nm	90-nm
Architecture	MIRRORBIT™ Eclipse	MIRRORBIT™ Eclipse	Floating Gate	MIRRORBIT™
Density	128 Mb - 512 Mb	128 Mb - 1 Gb	4 Mb - 128 Mb	32 Mb - 256 Mb
Bus Width	x1, x2, x4	x1, x2, x4	x1, x2, x4	x1, x2, x4
Supply Voltage	1.7 V - 2.0 V	2.7 V - 3.6 V / 1.65 V - 3.6 V V_{IO}	2.7 V - 3.6 V	2.7 V - 3.6 V
Normal Read Speed (SDR)	6 MB/s (50 MHz)	6 MB/s (50 MHz)	6 MB/s (50 MHz)	5 MB/s (40 MHz)
Fast Read Speed (SDR)	16.5 MB/s (133 MHz)	17 MB/s (133 MHz)	13 MB/s (104 MHz)	13 MB/s (104 MHz)
Dual Read Speed (SDR)	33 MB/s (133 MHz)	26 MB/s (104 MHz)	26 MB/s (104 MHz)	20 MB/s (80 MHz)
Quad Read Speed (SDR)	66 MB/s (133 MHz)	52 MB/s (104 MHz)	52 MB/s (104 MHz)	40 MB/s (80 MHz)
Quad Read Speed (DDR)	80 MB/s (80 MHz)	80 MB/s (80 MHz)	—	—
Program Buffer Size	256B / 512B	256B / 512B	256B	256B
Erase Sector Size	64 KB / 256 KB	64 KB / 256 KB	4 KB / 32 KB / 64 KB	64 KB / 256 KB
Parameter Sector Size	4 KB (option)	4 KB (option)	4 KB	4 KB
Sector Erase Rate (typ.)	500 KB/s	500 KB/s	136 KB/s (4 KB) 437 KB/s (64 KB)	130 KB/s
Page Programming Rate (typ.)	0.71 MB/s (256B) 1.08 MB/s (512B)	1.2 MB/s (256B) 1.5 MB/s (512B)	365 KB/s	170 KB/s
OTP	1024B	1024B	768B (3x256B)	506B
Advanced Sector Protection	Yes	Yes	No	No
Auto Boot Mode	No			
Erase Suspend/Resume	Yes		Yes	
Program Suspend/Resume				
Deep Power-Down Mode		No		Yes
Operating Temperature	-40°C to +85°C / +105°C	-40°C to +85°C / +105°C / +125°C	-40°C to +85°C	-40°C to +85°C / +105°C

Notes
1. 256B program page option only for 128 Mb and 256 Mb density FL-S devices.
2. FL-P column indicates FL129P MIO SPI device (for 128 Mb density), FL128P does not support MIO, OTP, or 4 KB sectors.
3. 64-KB sector erase option only for 128 Mb / 256 Mb density FL-P, FL-S, and FS-S devices.
4. FL-K family devices can erase 4-KB sectors in groups of 32 KB or 64 KB.
5. Only 128 Mb/256 Mb density FL-S devices have 4-KB parameter sector option.
6. 512 Mb / 1 Gb FL-S devices support 256 KB-sector only.
7. The FS512 device does not support 64 KB-sectors.
8. Refer to individual product datasheets for further details.

1.2.2 Known differences from prior generations

1.2.2.1 Error reporting

FL-K and FL-P memories either do not have error status bits or do not set them if program or erase is attempted on a protected sector. The FS-S and FL-S families do have error reporting status bits for program and erase operations. These can be set when there is an internal failure to program or erase, or when there is an attempt to program or erase a protected sector. In these cases the program or erase operation did not complete as requested by the command. The P_ERR or E_ERR bits and the WIP bit will be set to and remain 1 in SR1V. The clear status register command must be sent to clear the errors and return the device to standby state.

1.2.2.2 Secure silicon region (OTP)

The FS-S size and format (address map) of the One Time Program area is different from FL-K and FL-P generations. The method for protecting each portion of the OTP area is different. For additional details, see **"Secure silicon region (OTP)"** on page 68.

1.2.2.3 Configuration Register Freeze Bit

The Configuration Register 1 Freeze Bit CR1V[0], locks the state of the Block Protection bits (SR1NV[4:2] and SR1V[4:2]), TBPARM_O bit (CR1NV[2]), and TBPROT_O bit (CR1NV[5]), as in prior generations. In the FS-S and FL-S families the Freeze Bit also locks the state of the Configuration Register 1 BPNV_O bit (CR1NV[3]), and the Secure Silicon Region (OTP) area.

1.2.2.4 Sector Erase commands

The command for erasing a 4-KB sector is supported only for use on 4-KB parameter sectors at the top or bottom of the FS-S device address space.

The command for erasing an 8-KB area (two 4-KB sectors) is not supported.

The command for erasing a 32-KB area (eight 4-KB sectors) is not supported.

The 64 KB erase command is not supported for the 512 Mb density FS-S device.

1.2.2.5 Deep power-down

A Deep Power-Down (DPD) function is supported in the FS-S family devices.

1.2.2.6 WRR single register write

In some legacy SPI devices, a Write Registers (WRR) command with only one data byte would update Status Register 1 and clear some bits in Configuration Register 1, including the Quad mode bit. This could result in unintended exit from Quad mode. The S25FS512S only updates Status Register 1 when a single data byte is provided. The Configuration Register 1 is not modified in this case.

1.2.2.7 Hold input not supported

In some legacy SPI devices, the IO3 input has an alternate function as a HOLD# input used to pause information transfer without stopping the serial clock. This function is not supported in the FS-S family.

1.2.2.8 Separate reset input not supported

In some legacy SPI devices, a separate hardware RESET# input is supported in packages having more than eight connections. The FS-S family does not support a separate RESET# input. The FS-S family provides an alternate function for the IO3 input as a RESET# input. When the CS# signal is HIGH and the IO3 / RESET feature is enabled, the IO3 / RESET# input is used to initiate a hardware reset when the input goes LOW.

1.2.2.9 Other legacy commands not supported

- Autoboot related commands
- Bank Address related commands
- Dual Output Read
- Quad Output Read
- Quad Page Program (QPP) — replaced by page program in QPI mode
- DDR Fast Read
- DDR Dual I/O Read

1.2.2.10 New features

The FS-S family introduces new features to SPI category memories:

- Single 1.8 V power supply for core and I/O voltage.
- Configurable initial read latency (number of dummy cycles) for faster initial access time or higher clock rate read commands.
- QPI (QPI, 4-4-4) read mode in which all transfers are 4 bits wide, including instructions.
- JEDEC JESD216 standard, serial flash discoverable parameters (SFDP) that provide device feature and configuration information.
- Evaluate Erase Status command to determine if the last erase operation on a sector completed successfully. This command can be used to detect incomplete erase due to power loss or other causes. This command can be helpful to Flash File System software in file system recovery after a power loss.
- Advanced sector protection (ASP) permanent protection. A bit is added to the ASP register to provide the option to make protection of the Persistent Protection Bits (PPB) permanent. Also, when one of the two ASP protection modes is selected, all OTP configuration bits in all registers are protected from further programming so that all OTP configuration settings are made permanent. The OTP address space is not protected by the selection of an ASP protection mode. The Freeze bit (CR1V[0]) may be used to protect the OTP Address Space.

2 SPI with multiple input / output (SPI-MIO)

Many memory devices connect to their host system with separate parallel control, address, and data signals that require a large number of signal connections and larger package size. The large number of connections increase power consumption due to so many signals switching and the larger package increases cost.

The S25FS512S reduces the number of signals for connection to the host system by serially transferring all control, address, and data information over 4 to 6 signals. This reduces the cost of the memory package, reduces signal switching power, and either reduces the host connection count or frees host connectors for use in providing other features.

The S25FS512S uses the industry standard single bit SPI and also supports optional extension commands for two-bit (Dual) and four-bit (Quad) wide serial transfers. This multiple width interface is called SPI multi-I/O or SPI-MIO.

3 Pinout and signal description

3.1 SOIC 16-lead package

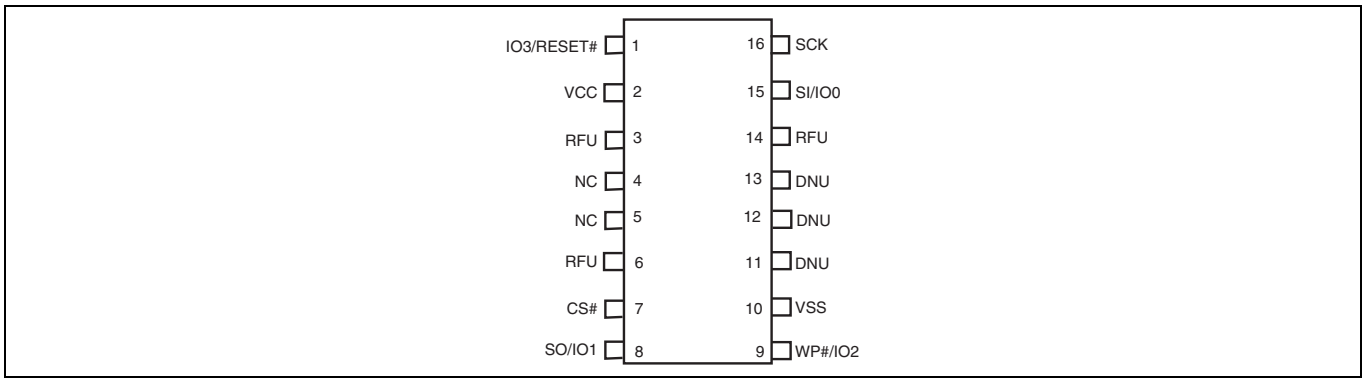


Figure 1 16-lead SOIC package, Top view[9]

3.2 8-connector package

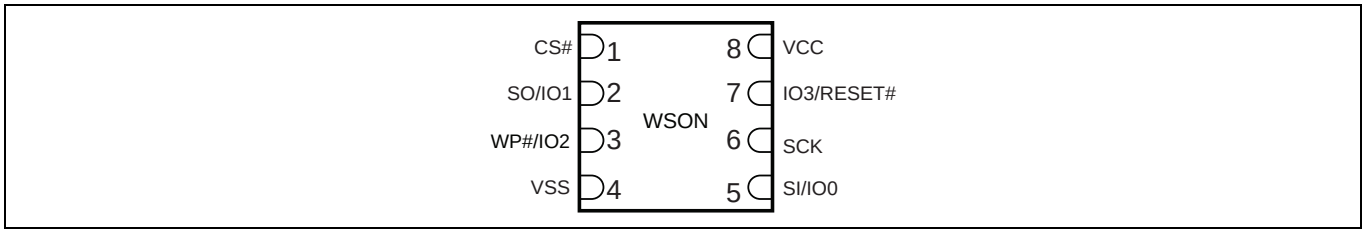


Figure 2 8-connector package (WSON 6 x 8), top view[9, 10]

3.3 BGA connection diagram

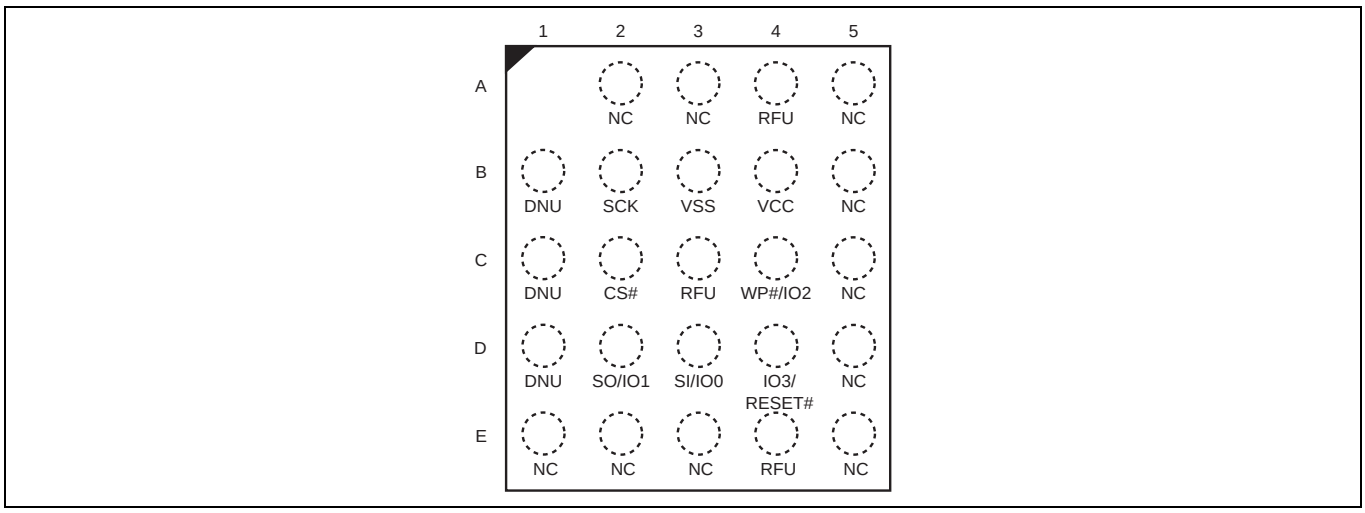


Figure 3 24-ball BGA, 5 x 5 ball footprint (FAB024), top view[9, 11]

Notes
9. The RESET# input has an internal pull-up and may be left unconnected in the system if Quad mode and hardware reset are not in use.
10. There is an exposed central pad on the underside of the WSON package. This should not be connected to any voltage or signal line on the PCB. Connecting the central pad to GND (VSS) is possible, provided PCB routing ensures 0mV difference between voltage at the WSON GND (VSS) lead and the central exposed pad.
11. Signal connections are in the same relative positions as FAC024 BGA, allowing a single PCB footprint to use either package.

Table 2 Signal description

Signal name	Type	Description
SCK	Input	**Serial Clock**
CS#	Input	**Chip Select**
SI / IO0	I/O	**Serial Input** for single bit data commands or IO0 for Dual or Quad commands.
SO / IO1	I/O	**Serial Output** for single bit data commands. IO1 for Dual or Quad commands.
WP# / IO2	I/O	**Write Protect** when not in Quad mode (CR1V[1] = 0 and SR1NV[7] = 1) (see **Table 20**). **IO2** when in Quad mode (CR1V[1] = 1). The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands or write protection. If write protection is enabled by SR1NV[7] = 1 and CR1V[1] = 0, the host system is required to drive WP# HIGH or LOW during a WRR or WRAR command.
IO3 / RESET#	I/O	**IO3** in Quad-I/O mode, when Configuration Register 1 QUAD bit, CR1V[1] = 1, and CS# is LOW. **RESET#** when enabled by CR2V[5] = 1 and not in Quad-I/O mode, CR1V[1] = 0, or when enabled in quad mode, CR1V[1] = 1 and CS# is HIGH. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands or RESET#.
V_{CC}	Supply	**Power Supply**
V_{SS}	Supply	**Ground**
NC	Unused	**Not Connected.** No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB). However, any signal connected to an NC must not have voltage levels higher than V_{CC}.
RFU	Reserved	**Reserved for Future Use.** No device internal signal is currently connected to the package connector but there is potential future use of the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.
DNU	Reserved	**Do Not Use.** A device internal signal may be connected to the package connector. The connection may be used by Infineon for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to this connection.

3.4 Multiple Input / Output (MIO)

Traditional SPI single bit wide commands (Single or SIO) send information from the host to the memory only on the Serial Input (SI) signal. Data may be sent back to the host serially on the Serial Output (SO) signal.

Dual or Quad Input / Output (I/O) commands send instructions to the memory only on the SI / IO0 signal. Address or data is sent from the host to the memory as bit pairs on IO0 and IO1 or four-bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as bit pairs on IO0 and IO1 or four-bit (nibble) groups on IO0, IO1, IO2, and IO3.

QPI mode transfers all instructions, address, and data from the host to the memory as four-bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as four-bit (nibble) groups on IO0, IO1, IO2, and IO3.

3.5 Serial Clock (SCK)

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the SCK signal. Data output changes after the falling edge of SCK, in SDR commands, and after every edge in DDR commands.

3.6 Chip Select (CS#)

The chip select signal indicates when a command is transferring information to or from the device and the other signals are relevant for the memory device.

When the CS# signal is at the logic HIGH state, the device is not selected and all input signals are ignored and all output signals are high impedance. The device will be in the Standby Power mode, unless an internal embedded operation is in progress. An embedded operation is indicated by the Status Register 1 Write-In-Progress bit (SR1V[1]) set to '1', until the operation is completed. Some example embedded operations are: Program, Erase, or Write Registers (WRR) operations.

Driving the CS# input to the logic LOW state enables the device, placing it in the Active Power mode. After Power-up, a falling edge on CS# is required prior to the start of any command.

3.7 Serial Input (SI) / IO0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial SCK clock signal.

SI becomes IO0 — an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

3.8 Serial Output (SO) / IO1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial SCK clock signal.

SO becomes IO1 — an input and output during Dual and Quad commands for receiving addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

3.9 Write Protect (WP#) / IO2

When WP# is driven Low (V_{IL}), during a WRR or WRAR command and while the Status Register Write Disable (SRWD_NV) bit of Status Register 1 (SR1NV[7]) is set to '1', it is not possible to write to Status Register 1 or Configuration Register 1 related registers. In this situation, a WRR command is ignored, a WRAR command selecting SR1NV, SR1V, CR1NV, or CR1V is ignored, and no error is set.

This prevents any alteration of the Block Protection settings. As a consequence, all the data bytes in the memory area that are protected by the Block Protection feature are also hardware protected against data modification if WP# is Low during a WRR or WRAR command with SRWD_NV set to '1'.

The WP# function is not available when the Quad mode is enabled (CR1V[1] = 1). The WP# function is replaced by IO2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

WP# has an internal pull-up resistance; when unconnected, WP# is at V_{IH} and may be left unconnected in the host system if not used for Quad mode or protection.

3.10 IO3 / RESET#

IO3 is used for input and output during Quad mode (CR1V[1] = 1) for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

The IO3 / RESET# signal may also be used to initiate the hardware reset function when the reset feature is enabled by writing Configuration Register 2 non-volatile bit 5 (CR2V[5] = 1). The input is only treated as RESET# when the device is not in Quad-I/O mode, CR1V[1] = 0, or when CS# is HIGH. When Quad I/O mode is in use, CR1V[1] = 1, and the device is selected with CS# LOW, the IO3 / RESET# is used only as IO3 for information transfer. When CS# is HIGH, the IO3 / RESET# is not in use for information transfer and is used as the RESET# input. By conditioning the reset operation on CS# HIGH during Quad mode, the reset function remains available during Quad mode.

When the system enters a reset condition, the CS# signal must be driven HIGH as part of the reset process and the IO3 / RESET# signal is driven LOW. When CS# goes HIGH, the IO3 / RESET# input transitions from being IO3 to being the RESET# input. The reset condition is then detected when CS# remains HIGH and the IO3 / RESET# signal remains LOW for t_{RP}. If a reset is not intended, the system is required to actively drive IO3 / Reset# to HIGH along with CS# being driven HIGH at the end of a transfer of data to the memory. Following transfers of data to the host system, the memory will drive IO3 HIGH during t_{CS}. This will ensure that IO3 / Reset is not left floating or being pulled slowly to HIGH by the internal or an external passive pull-up. Thus, an unintended reset is not triggered by the IO3 / RESET# not being recognized as HIGH before the end of t_{RP}.

The IO3 / RESET# signal is unused when the reset feature is disabled (CR2V[5] = 0).

The IO3 / RESET# signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad mode or the reset function. The internal pull-up will hold IO3 / Reset HIGH after the host system has actively driven the signal high and then stops driving the signal.

Note that IO3 / Reset# cannot be shared by more than one SPI-MIO memory if any of them are operating in Quad I/O mode as IO3 being driven to or from one selected memory may look like a reset signal to a second non-selected memory sharing the same IO3 / RESET# signal.

3.11 Voltage Supply (V_{CC})

V_{CC} is the voltage source for all device internal logic. It is the single voltage used for all device internal functions including read, program, and erase.

3.12 Supply and Signal Ground (V_{SS})

V_{SS} is the common voltage drain and ground reference for the device core, input signal receivers, and output drivers.

3.13 Not Connected (NC)

No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB).

3.14 Reserved for Future Use (RFU)

No device internal signal is currently connected to the package connector but there is potential future use of the connector. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.

3.15 Do Not Use (DNU)

A device internal signal may be connected to the package connector. The connection may be used by Infineon for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections.

3.16 Block diagrams

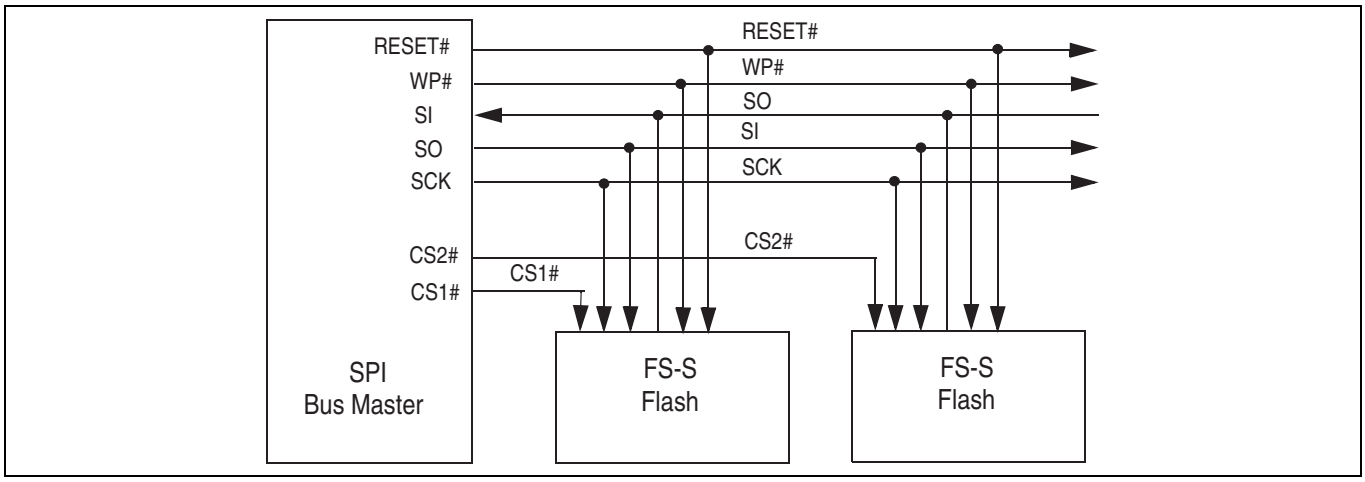


Figure 4 Bus master and memory devices on the SPI bus — single bit data path

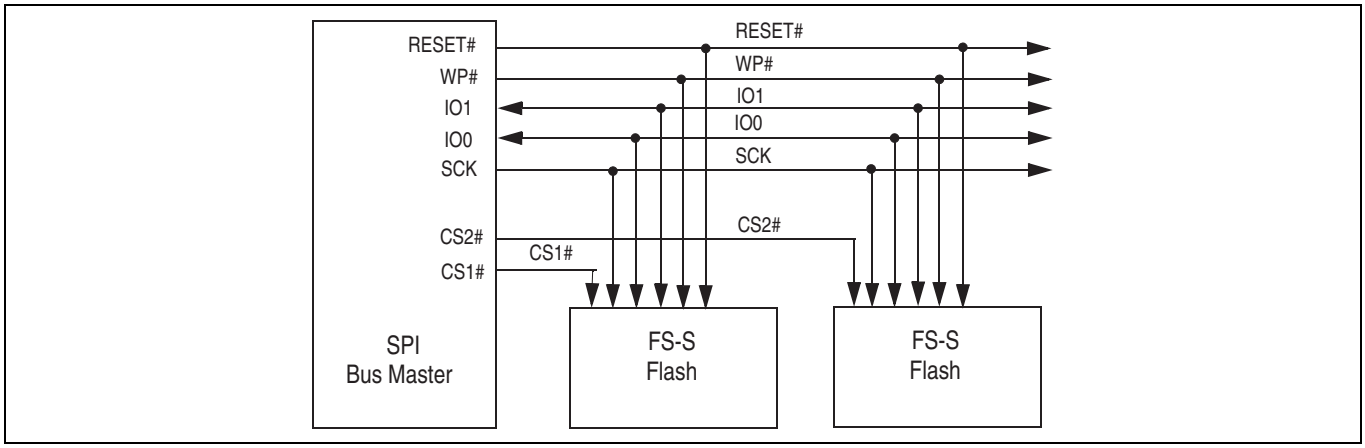


Figure 5 Bus master and memory devices on the SPI bus — dual bit data path

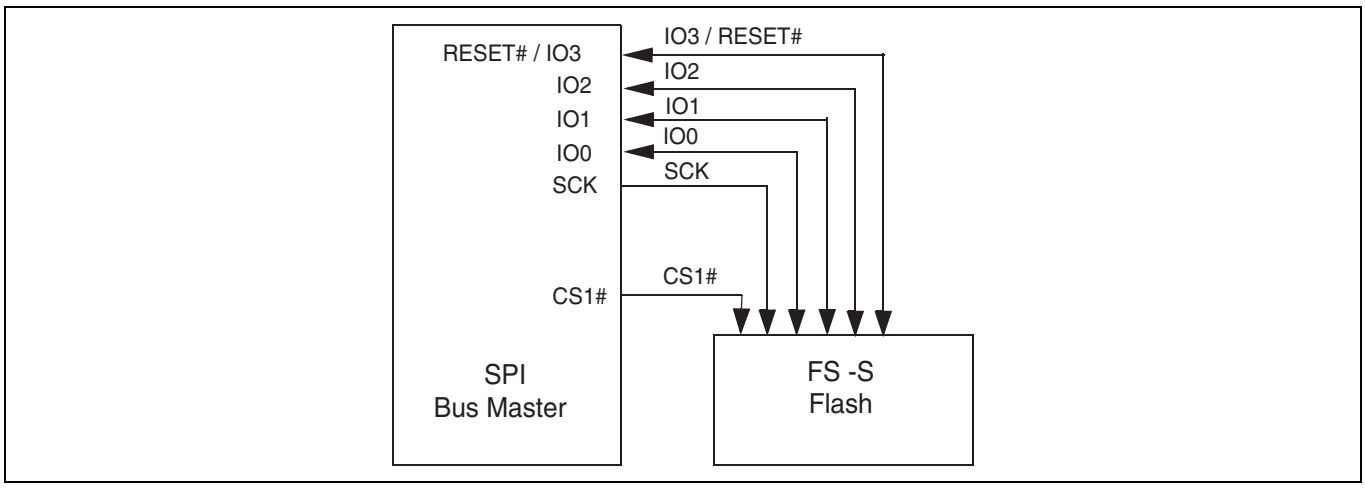


Figure 6 Bus master and memory devices on the SPI bus — quad bit data path

4 Signal protocols

4.1 SPI clock modes

4.1.1 Single data rate (SDR)

The S25FS512S can be driven by an embedded microcontroller (bus master) in either of the two following clocking modes.

- **Mode 0** with Clock Polarity (CPOL) = 0 and, Clock Phase (CPHA) = 0
- **Mode 3** with CPOL = 1 and, CPHA = 1

For these two modes, input data into the device is always latched in on the rising edge of the SCK signal and the output data is always available from the falling edge of the SCK clock signal.

The difference between the two modes is the clock polarity when the bus master is in standby mode and not transferring any data.

- SCK will stay at logic LOW state with CPOL = 0, CPHA = 0
- SCK will stay at logic HIGH state with CPOL = 1, CPHA = 1

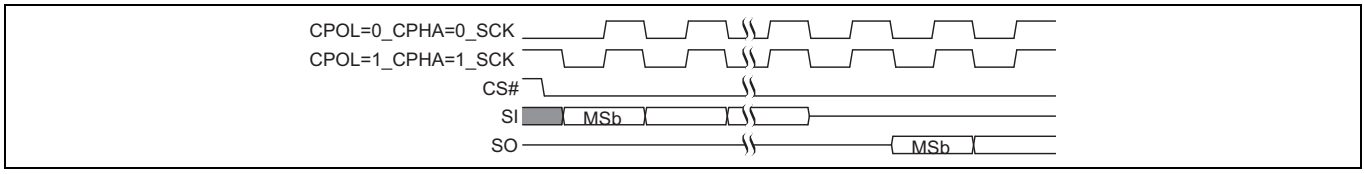


Figure 7 SPI SDR modes supported

Timing diagrams throughout the remainder of the document are generally shown as both Mode 0 and 3 by showing SCK as both HIGH and LOW at the fall of CS#. In some cases, a timing diagram may show only Mode 0 with SCK LOW at the fall of CS#. In such a case, Mode 3 timing simply means clock is HIGH at the fall of CS# so no SCK rising edge set up or hold time to the falling edge of CS# is needed for Mode 3.

SCK cycles are measured (counted) from one falling edge of SCK to the next falling edge of SCK. In Mode 0, the beginning of the first SCK cycle in a command is measured from the falling edge of CS# to the first falling edge of SCK because SCK is already low at the beginning of a command.

4.1.2 Double data rate (DDR)

Mode 0 and Mode 3 are also supported for DDR commands. In DDR commands, the instruction bits are always latched on the rising edge of clock, the same as in SDR commands. However, the address and input data that follow the instruction are latched on both the rising and falling edges of SCK. The first address bit is latched on the first rising edge of SCK following the falling edge at the end of the last instruction bit. The first bit of output data is driven on the falling edge at the end of the last access latency (dummy) cycle.

SCK cycles are measured (counted) in the same way as in SDR commands, from one falling edge of SCK to the next falling edge of SCK. In Mode 0, the beginning of the first SCK cycle in a command is measured from the falling edge of CS# to the first falling edge of SCK because SCK is already LOW at the beginning of a command.

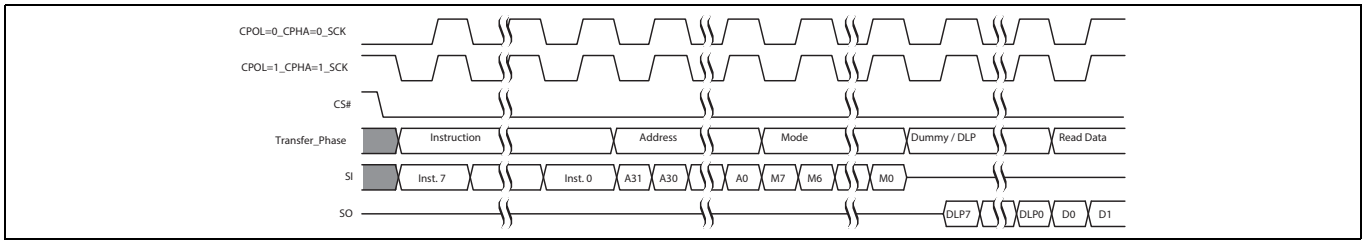


Figure 8 SPI DDR modes supported

4.2 Command protocol

All communication between the host system and S25FS512S devices is in the form of units called commands.

All commands begin with an 8-bit instruction that selects the type of information transfer or device operation to be performed. Commands may also have an address, instruction modifier, latency period, data transfer to the memory, or data transfer from the memory. All instruction, address, and data information is transferred sequentially between the host system and memory device.

Command protocols are also classified by a numerical nomenclature using three numbers to reference the transfer width of three command phases:

- instruction;
- address and instruction modifier (continuous read mode bits);
- data

Single-bit wide commands start with an instruction and may provide an address or data, all sent only on the SI signal. Data may be sent back to the host serially on the SO signal. This is referenced as a 1-1-1 command protocol for single-bit width instruction, single-bit width address and modifier, single-bit data.

Dual or Quad Input / Output (I/O) commands provide an address sent from the host as bit pairs on IO0 and IO1 or, four-bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as bit pairs on IO0 and IO1 or, four-bit (nibble) groups on IO0, IO1, IO2, and IO3. This is referenced as 1-2-2 for Dual I/O and 1-4-4 for Quad I/O command protocols.

The S25FS512S also supports a QPI mode in which all information is transferred in 4-bit width, including the instruction, address, modifier, and data. This is referenced as a 4-4-4 command protocol.

Commands are structured as follows:

- Each command begins with CS# going LOW and ends with CS# returning HIGH. The memory device is selected by the host driving the Chip Select (CS#) signal LOW throughout a command.
- The serial clock (SCK) marks the transfer of each bit or group of bits between the host and memory.
- Each command begins with an eight bit (byte) instruction. The instruction selects the type of information transfer or device operation to be performed. The instruction transfers occur on SCK rising edges. However, some read commands are modified by a prior read command, such that the instruction is implied from the earlier command. This is called Continuous Read Mode. When the device is in Continuous Read mode, the instruction bits are not transmitted at the beginning of the command because the instruction is the same as the read command that initiated the Continuous Read Mode. In Continuous Read mode, the command will begin with the read address. Thus, Continuous Read Mode removes eight instruction bits from each read command in a series of same type read commands.
- The instruction may be standalone or may be followed by address bits to select a location within one of several address spaces in the device. The instruction determines the address space used. The address may be either a 24-bit or a 32-bit, byte boundary, address. The address transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- In legacy SPI mode, the width of all transfers following the instruction are determined by the instruction sent. Following transfers may continue to be single bit serial on only the SI or Serial Output (SO) signals, they may be done in two bit groups per (dual) transfer on the IO0 and IO1 signals, or they may be done in 4-bit groups per (quad) transfer on the IO0-IO3 signals. Within the dual or quad groups the least significant bit is on IO0. More significant bits are placed in significance order on each higher numbered IO signal. Single bits or parallel bit groups are transferred in most to least significant bit order.
- In QPI mode, the width of all transfers is a 4-bit wide (quad) transfer on the IO0-IO3 signals.
- Dual and Quad I/O read instructions send an instruction modifier called Continuous Read mode bits, following the address, to indicate whether the next command will be of the same type with an implied, rather than an explicit, instruction. These mode bits initiate or end the continuous read mode. In continuous read mode, the next command thus does not provide an instruction byte, only a new address and mode bits. This reduces the time needed to send each command when the same command type is repeated in a sequence of commands. The mode bit transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.

- The address or mode bits may be followed by write data to be stored in the memory device or by a read latency period before read data is returned to the host.
- Write data bit transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- SCK continues to toggle during any read access latency period. The latency may be zero to several SCK cycles (also referred to as dummy cycles). At the end of the read latency cycles, the first read data bits are driven from the outputs on SCK falling edge at the end of the last read latency cycle. The first read data bits are considered transferred to the host on the following SCK rising edge. Each following transfer occurs on the next SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- If the command returns read data to the host, the device continues sending data transfers until the host takes the CS# signal HIGH. The CS# signal can be driven HIGH after any transfer in the read data sequence. This will terminate the command.
- At the end of a command that does not return data, the host drives the CS# input HIGH. The CS# signal must go HIGH after the eighth bit, of a standalone instruction or, of the last write data byte that is transferred. That is, the CS# signal must be driven HIGH when the number of bits after the CS# signal was driven low is an exact multiple of eight bits. If the CS# signal does not go high exactly at the eight-bit boundary of the instruction or write data, the command is rejected and not executed.
- All instruction, address, and mode bits are shifted into the device with the Most Significant Bits (MSb) first. The data bits are shifted in and out of the device MSb first. All data is transferred in byte units with the lowest address byte sent first. Following bytes of data are sent in lowest to highest byte address order i.e. the byte address increments.
- All attempts to read the flash memory array during a program, erase, or a write cycle (embedded operations) are ignored. The embedded operation will continue to execute without any affect. A very limited set of commands are accepted during an embedded operation. These are discussed in the individual command descriptions.
- Depending on the command, the time for execution varies. A command to read status information from an executing command is available to determine when the command completes execution and whether the command was successful.

4.2.1 Command sequence examples

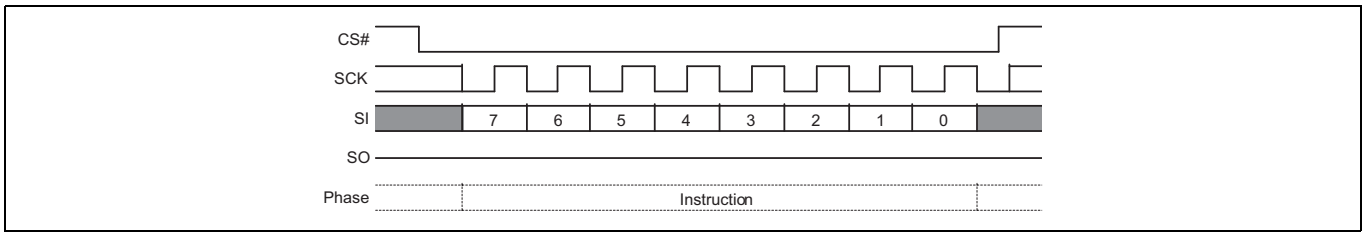


Figure 9 Standalone Instruction command

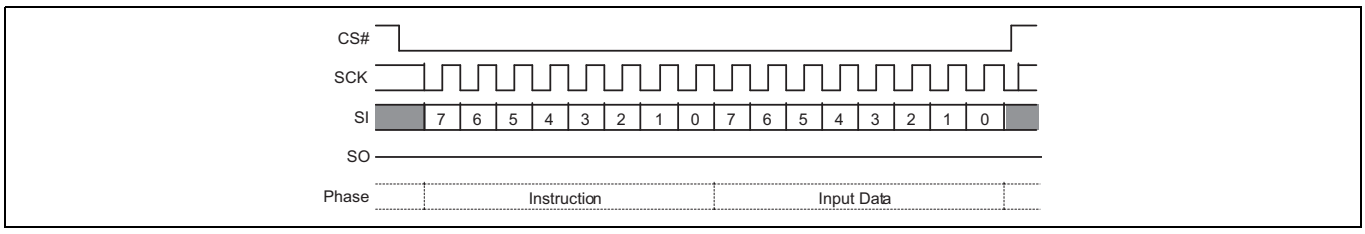


Figure 10 Single Bit Wide Input command

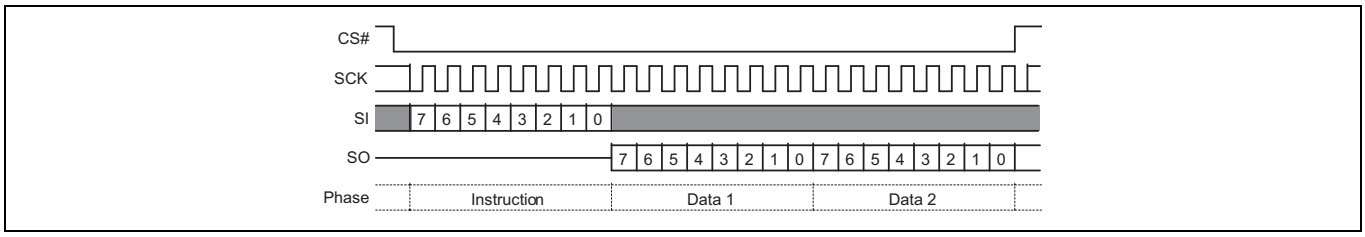


Figure 11 Single Bit Wide Output command

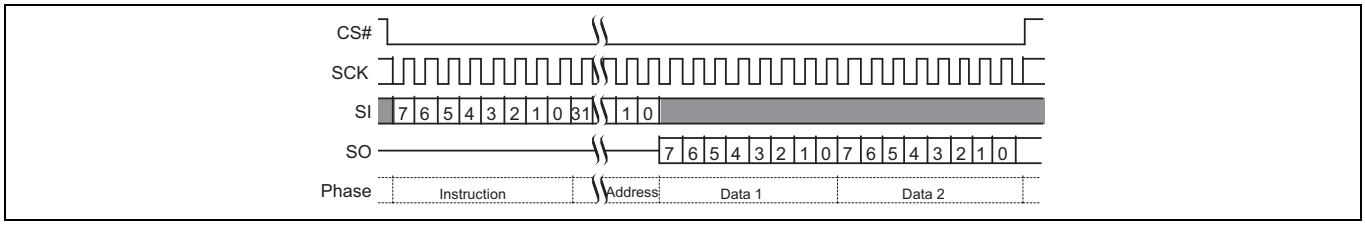


Figure 12 Single Bit Wide I/O command without latency

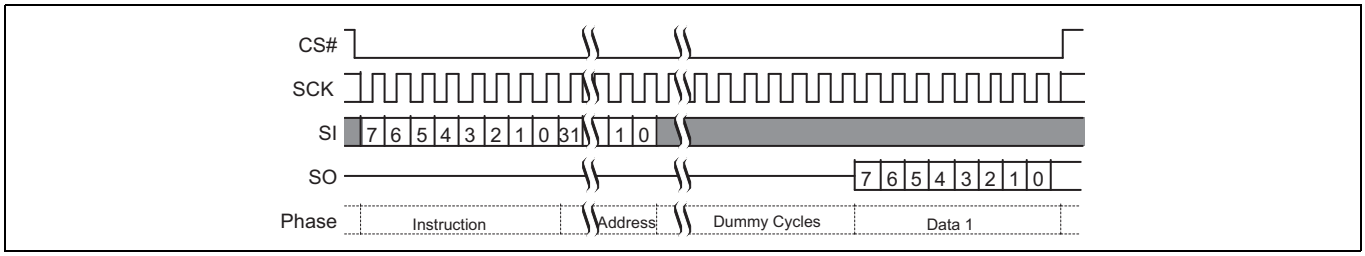


Figure 13 Single Bit Wide I/O command with latency

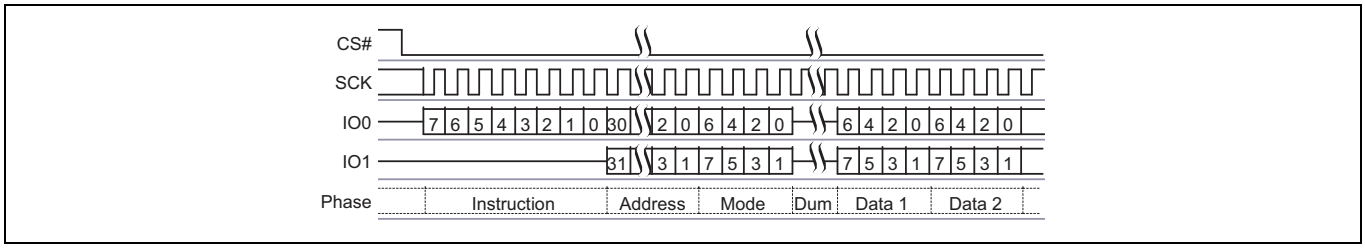


Figure 14 Dual I/O command

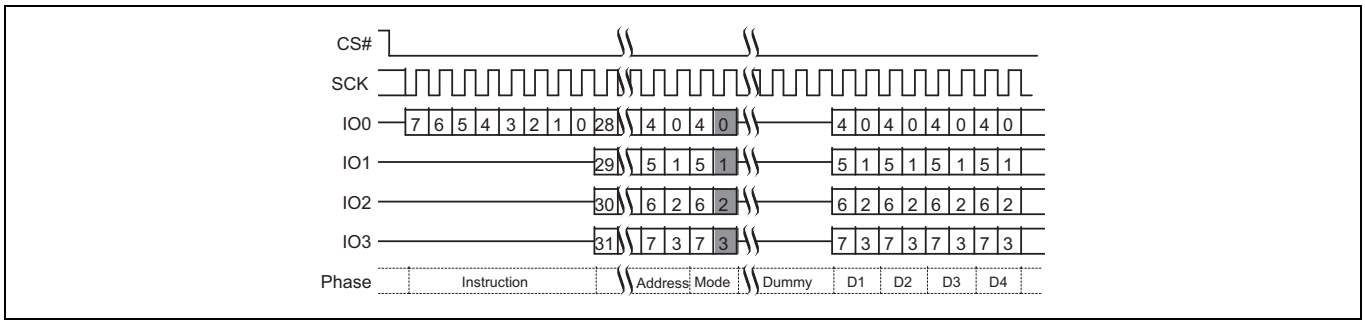


Figure 15 Quad I/O command

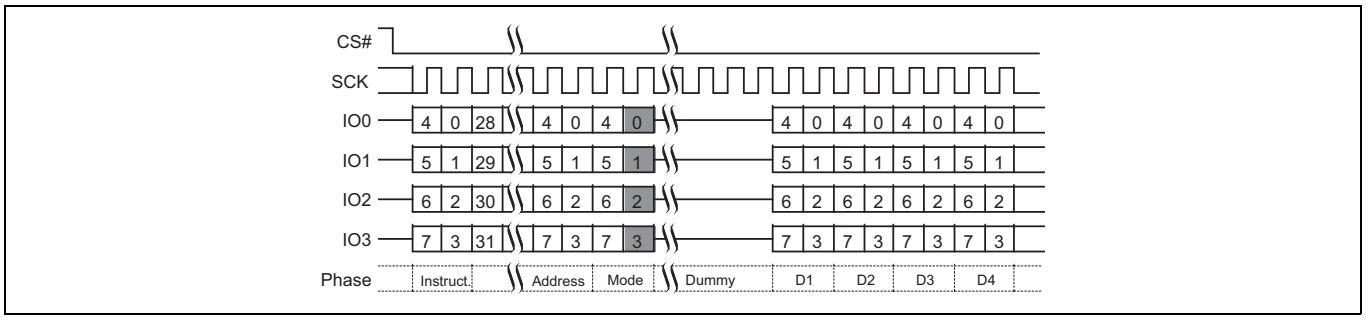


Figure 16 Quad I/O Read command in QPI mode

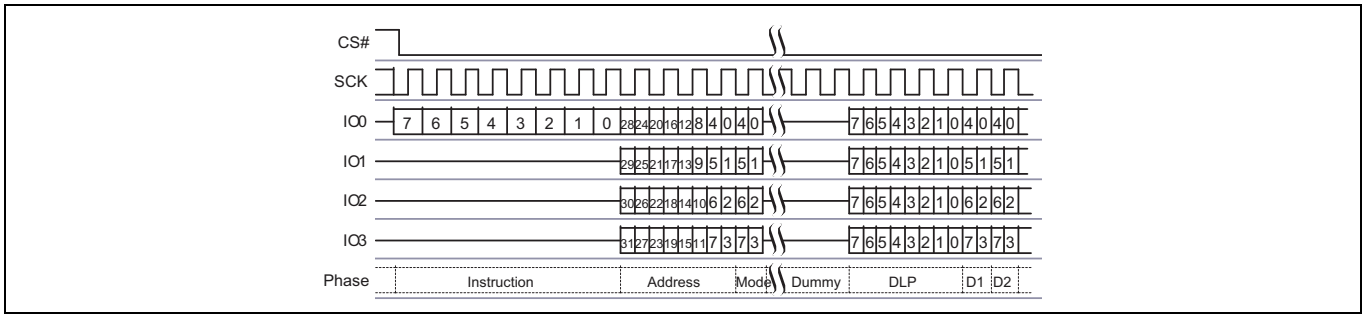


Figure 17 DDR Quad I/O Read

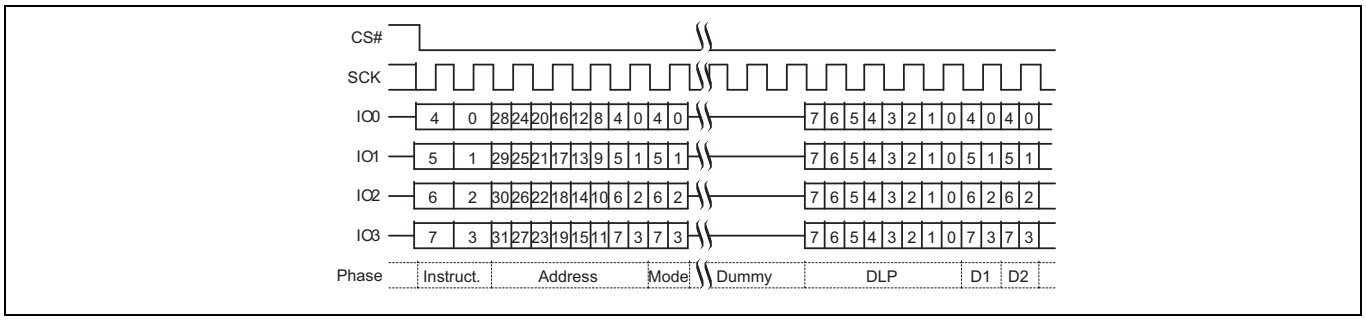


Figure 18 DDR Quad I/O Read in QPI mode

Additional sequence diagrams, specific to each command, are provided in **"Commands"** on page 76.

4.3 Interface states

This section describes the input and output signal levels as related to the SPI interface behavior.

Table 3 Interface states summary

Interface state	V_{CC}	SCK	CS#	IO3 / RESET#	WP# / IO2	SO / IO1	SI / IO0
Power-off	<V_{CC}(low)	X	X	X	X	Z	X
Low power Hardware data protection	<V_{CC}(cut-off)	X	X	X	X	Z	X
Power-on (Cold) reset	≥V_{CC}(min)	X	HH	X	X	Z	X
Hardware (Warm) reset non-quad mode	≥V_{CC}(min)	X	X	HL	X	Z	X
Hardware (Warm) reset quad mode	≥V_{CC}(min)	X	HH	HL	X	Z	X
Interface standby	≥V_{CC}(min)	X	HH	X	X	Z	X
Instruction cycle (Legacy SPI)	≥V_{CC}(min)	HT	HL	HH	HV	Z	HV
Single input cycle Host to Memory transfer	≥V_{CC}(min)	HT	HL	HH	X	Z	HV
Single latency (Dummy) cycle	≥V_{CC}(min)	HT	HL	HH	X	Z	X
Single output cycle Memory to Host transfer	≥V_{CC}(min)	HT	HL	HH	X	MV	X
Dual input cycle Host to Memory transfer	≥V_{CC}(min)	HT	HL	HH	X	HV	HV
Dual latency (Dummy) cycle	≥V_{CC}(min)	HT	HL	HH	X	X	X
Dual output cycle Memory to Host transfer	≥V_{CC}(min)	HT	HL	HH	X	MV	MV
Quad input cycle Host to Memory transfer	≥V_{CC}(min)	HT	HL	HV	HV	HV	HV
Quad latency (Dummy) cycle	≥V_{CC}(min)	HT	HL	X	X	X	X
Quad output cycle Memory to Host transfer	≥V_{CC}(min)	HT	HL	MV	MV	MV	MV
DDR Quad input cycle Host to Memory transfer	≥V_{CC}(min)	HT	HL	HV	HV	HV	HV
DDR Latency (Dummy) cycle	≥V_{CC}(min)	HT	HL	MV or Z	MV or Z	MV or Z	MV or Z
DDR Quad output cycle Memory to Host transfer	≥V_{CC}(min)	HT	HL	MV	MV	MV	MV

Legend

Z = No driver – floating signal

HL = Host driving V_{IL}

HH = Host driving V_{IH}

HV = Either HL or HH

X = HL or HH or Z

HT = Toggling between HL and HH

ML = Memory driving V_{IL}

MH = Memory driving V_{IH}

MV = Either ML or MH

4.3.1 Power-off

When the core supply voltage is at or below the $V_{CC\ (Low)}$ voltage, the device is considered to be powered off. The device does not react to external signals, and is prevented from performing any program or erase operation.

4.3.2 Low-power hardware data protection

When V_{CC} is less than $V_{CC\ (Cut\text{-}off)}$ the memory device will ignore commands to ensure that program and erase operations can not start when the core supply voltage is out of the operating range.

4.3.3 Power-on (Cold) reset

When the core voltage supply remains at or below the $V_{CC\ (Low)}$, voltage for ≥ t_{PD} time, then rises to ≥ $V_{CC\ (Minimum)}$ the device will begin its Power On Reset (POR) process. POR continues until the end of t_{PU}. During t_{PU} the device does not react to external input signals nor drive any outputs. Following the end of t_{PU} the device transitions to the Interface Standby state and can accept commands. For additional information on POR see **"Power on (cold) reset"** on page 39.

4.3.4 Hardware (Warm) reset

A configuration option is provided to allow IO3 to be used as a hardware reset input when the device is not in Quad mode or when it is in Quad mode and CS# is HIGH. When IO3 / RESET# is driven LOW for t_{RP} time the device starts the hardware reset process. The process continues for t_{RPH} time. Following the end of both t_{RPH} and the reset hold time following the rise of RESET# (t_{RH}) the device transitions to the Interface Standby state and can accept commands.

4.3.5 Interface standby

When CS# is HIGH, the SPI interface is in standby state. Inputs other than RESET# are ignored. The interface waits for the beginning of a new command. The next interface state is Instruction Cycle when CS# goes LOW to begin a new command.

While in interface standby state, the memory device draws standby current (I_{SB}) if no embedded algorithm is in progress. If an embedded algorithm is in progress, the related current is drawn until the end of the algorithm when the entire device returns to standby current draw.

A Deep Power Down (DPD) mode is supported by the S25FS512S devices. If the device has been placed in DPD mode by the DPD (B9h) command, the interface standby current is (I_{DPD}). The DPD command is accepted only while the device is not performing an embedded algorithm as indicated by the Status Register-1 volatile Write In Progress (WIP) bit being cleared to zero (SR1V[0] = 0). While in DPD mode the device ignores all commands except the Release from DPD (RES ABh) command, that will return the device to the Interface Standby state after a delay of t_{RES}.

4.3.6 Instruction cycle (Legacy SPI mode)

When the host drives the MSb of an instruction and CS# goes LOW, on the next rising edge of SCK the device captures the MSb of the instruction that begins the new command. On each following rising edge of SCK the device captures the next lower significance bit of the 8-bit instruction. The host keeps CS# LOW, and drives the Write Protect (WP#) and IO3/RESET signals as needed for the instruction. However, WP# is only relevant during instruction cycles of a WRR or WRAR command and is otherwise ignored. IO3 / RESET# is driven HIGH when the device is not in Quad Mode (CR1V[1] = 0) or QPI Mode (CR2V[6] = 0) and hardware reset is not required.

Each instruction selects the address space that is operated on and the transfer format used during the remainder of the command. The transfer format may be Single, Dual I/O, Quad I/O, or DDR Quad I/O. The expected next interface state depends on the instruction received.

Some commands are standalone, needing no address or data transfer to or from the memory. The host returns CS# HIGH after the rising edge of SCK for the eighth bit of the instruction in such commands. The next interface state in this case is Interface Standby.

4.3.7 Instruction cycle (QPI mode)

In QPI mode, when CR2V[6] = 1, instructions are transferred 4 bits per cycle. In this mode instruction cycles are the same as a Quad Input Cycle (see **"Quad input cycle — Host to Memory transfer"** on page 28).

4.3.8 Single input cycle — Host to Memory transfer

Several commands transfer information after the instruction on the single serial input (SI) signal from host to the memory device. The host keeps RESET# HIGH, CS# LOW, and drives SI as needed for the command. The memory does not drive the Serial Output (SO) signal.

The expected next interface state depends on the instruction. Some instructions continue sending address or data to the memory using additional Single Input Cycles. Others may transition to Single Latency, or directly to Single, Dual, or Quad Output cycle states.

4.3.9 Single latency (Dummy) cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the configuration register (CR2V[3:0]). During the latency cycles, the host keeps RESET# HIGH, CS# LOW. The Write Protect (WP#) signal is ignored. The host may drive the SI signal during these cycles or the host may leave SI floating. The memory does not use any data driven on SI / I/O0 or other I/O signals during the latency cycles. The memory does not drive the Serial Output (SO) or I/O signals during the latency cycles.

The next interface state depends on the command structure, i.e., the number of latency cycles, and whether the read is single, dual, or quad width.

4.3.10 Single output cycle — Memory to Host transfer

Several commands transfer information back to the host on the single Serial Output (SO) signal. The host keeps RESET# HIGH, CS# LOW. The Write Protect (WP#) signal is ignored. The memory ignores the Serial Input (SI) signal. The memory drives SO with data.

The next interface state continues to be Single Output Cycle until the host returns CS# to HIGH ending the command.

4.3.11 Dual input cycle — Host to Memory transfer

The Read Dual I/O command transfers two address or mode bits to the memory in each cycle. The host keeps RESET# HIGH, CS# LOW. The Write Protect (WP#) signal is ignored. The host drives address on SI / IO0 and SO / IO1.

The next interface state following the delivery of address and mode bits is a Dual Latency Cycle if there are latency cycles needed or Dual Output Cycle if no latency is required.

4.3.12 Dual latency (Dummy) cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the configuration register (CR2V[3:0]). During the latency cycles, the host keeps RESET# HIGH, CS# LOW. The Write Protect (WP#) signal is ignored. The host may drive the SI / IO0 and SO / IO1 signals during these cycles or the host may leave SI / IO0 and SO / IO1 floating. The memory does not use any data driven on SI / IO0 and SO / IO1 during the latency cycles. The host must stop driving SI / IO0 and SO / IO1 on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving them during all latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the SI / IO0 and SO / IO1 signals during the latency cycles.

The next interface state following the last latency cycle is a Dual Output Cycle.

4.3.13 Dual output cycle — Memory to Host transfer

The Read Dual Output and Read Dual I/O return data to the host two bits in each cycle. The host keeps RESET# HIGH, CS# LOW. The Write Protect (WP#) signal is ignored. The memory drives data on the SI / IO0 and SO / IO1 signals during the dual output cycles.

The next interface state continues to be Dual Output Cycle until the host returns CS# to HIGH ending the command.

4.3.14 Quad input cycle — Host to Memory transfer

The Quad I/O Read command transfers four address or mode bits to the memory in each cycle. In QPI mode, the Quad I/O Read and Page Program commands transfer four data bits to the memory in each cycle, including the instruction cycles. The host keeps CS# LOW, and drives the IO signals.

For Quad I/O Read the next interface state following the delivery of address and mode bits is a Quad Latency Cycle if there are latency cycles needed or Quad Output Cycle if no latency is required. For QPI mode Page Program, the host returns CS# HIGH following the delivery of data to be programmed and the interface returns to standby state.

4.3.15 Quad latency (Dummy) cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the configuration register (CR2V[3:0]). During the latency cycles, the host keeps CS# LOW. The host may drive the IO signals during these cycles or the host may leave the IO floating. The memory does not use any data driven on IO during the latency cycles. The host must stop driving the IO signals on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving them during all latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the IO signals during the latency cycles.

The next interface state following the last latency cycle is a Quad Output Cycle.

4.3.16 Quad output cycle — Memory to Host transfer

The Quad I/O Read returns data to the host four bits in each cycle. The host keeps CS# LOW. The memory drives data on IO0-IO3 signals during the Quad output cycles.

The next interface state continues to be Quad Output Cycle until the host returns CS# to HIGH ending the command.

4.3.17 DDR Quad input cycle — Host to Memory transfer

The DDR Quad I/O Read command sends address, and mode bits to the memory on all the IO signals. Four bits are transferred on the rising edge of SCK and four bits on the falling edge in each cycle. The host keeps CS# LOW.

The next interface state following the delivery of address and mode bits is a DDR Latency Cycle.

4.3.18 DDR latency cycle

DDR Read commands may have one to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the configuration register (CR2V[3:0]). During the latency cycles, the host keeps CS# LOW. The host may not drive the IO signals during these cycles. So that there is sufficient time for the host drivers to turn off before the memory begins to drive. This prevents driver conflict between host and memory when the signal direction changes. The memory has an option to drive all the IO signals with a Data Learning Pattern (DLP) during the last four latency cycles. The DLP option should not be enabled when there are fewer than five latency cycles so that there is at least one cycle of high impedance for turn around of the IO signals before the memory begins driving the DLP. When there are more than four cycles of latency the memory does not drive the IO signals until the last four cycles of latency.

The next interface state following the last latency cycle is a DDR Single, or Quad Output Cycle, depending on the instruction.

4.3.19 DDR Quad output cycle — Memory to Host transfer

The DDR Quad I/O Read command returns bits to the host on all the IO signals. Four bits are transferred on the rising edge of SCK and four bits on the falling edge in each cycle. The host keeps CS# LOW.

The next interface state continues to be DDR Quad Output Cycle until the host returns CS# to HIGH ending the command.

4.4 Configuration Register effects on the interface

The Configuration Register 2 volatile bits 3 to 0 (CR2V[3:0]) select the variable latency for all array read commands except Read and Read SDFP (RSFDP). Read always has zero latency cycles. RSFDP always has eight latency cycles. The variable latency is also used in the OTPR and RDAR commands.

The configuration register bit 1 (CR1V[1]) selects whether Quad mode is enabled to switch WP# to IO2 function, RESET# to IO3 function, and thus allow Quad I/O Read and QPI mode commands. Quad mode must also be selected to allow DDR Quad I/O Read commands.

4.5 Data protection

Some basic protection against unintended changes to stored data are provided and controlled purely by the hardware design. These are described in **“Data protection”** on page 68. Other software managed protection methods are discussed in the software section of this document.

4.5.1 Power-up

When the core supply voltage is at or below the $V_{CC\ (Low)}$ voltage, the device is considered to be powered off. The device does not react to external signals, and is prevented from performing any program or erase operation. Program and erase operations continue to be prevented during the Power-on Reset (POR) because no command is accepted until the exit from POR to the Interface Standby state.

4.5.2 Low power

When V_{CC} is less than $V_{CC\ (Cut\text{-}off)}$ the memory device will ignore commands to ensure that program and erase operations can not start when the core supply voltage is out of the operating range.

4.5.3 Clock pulse count

The device verifies that all non-volatile memory and register data modifying commands consist of a clock pulse count that is a multiple of eight bit transfers (byte boundary) before executing them. A command not ending on an 8-bit (byte) boundary is ignored and no error status is set for the command.

4.5.4 DPD

In DPD mode the device responds only to the Release from DPD command (RES ABh). All other commands are ignored during DPD mode, thereby protecting the memory from program and erase operations.

5 Electrical specifications

5.1 Absolute maximum ratings

Storage temperature plastic packages	-65°C to +150°C
Ambient temperature with power applied	-65°C to +125°C
V_{CC}	-0.5 V to +2.5 V
Input voltage with respect to Ground (V_{SS})[13]	-0.5 V to V_{CC} + 0.5 V
Output short circuit current[14]	100 mA

Notes
12. See **"Input signal overshoot"** on page 31 for allowed maximums during signal transition.
13. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
14. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Thermal resistance

Table 4 Thermal resistance

Parameter	Description	SO3016	WNH008	FAB024	Unit
Theta JA	Junction to Ambient	37.4	30	38.5	°C/W
Theta JB	Junction to Board	8	10.6	10.2	
Theta JC	Junction to Case	9	11.2	11.6	

5.3 Latchup characteristics

Table 5 Latchup specification

Description	Min	Max	Unit
Input voltage with respect to V_{SS} on all input only connections	-1.0	V_{CC} + 1.0	V
Input voltage with respect to V_{SS} on all I/O connections			
V_{CC} current	-100	+100	mA

Note
15. Excludes power supply V_{CC}. Test conditions: V_{CC} = 1.8 V, one connection at a time tested, connections not being tested are at V_{SS}.

5.4 Operating ranges

Operating ranges define those limits between which the functionality of the device is guaranteed.

5.4.1 Power supply voltages

V_{CC}	1.7 V to 2.0 V

5.4.2 Temperature ranges

Parameter	Symbol	Devices	Spec		Unit
			Min	Max	
Ambient temperature	T_A	Industrial (I)	-40	+85	°C
		Industrial Plus devices (V)		+105	
		Automotive, AEC-Q100 grade 3 (A)		+85	
		Automotive, AEC-Q100 grade 2 (B)		+105	
		Automotive, AEC-Q100 grade 1 (M)		+125	

Note
16. Industrial Plus operating and performance parameters will be determined by device characterization and may vary from standard industrial temperature range devices as currently shown in this specification.

5.4.3 Input signal overshoot

During DC conditions, input or I/O signals should remain equal to or between V_{SS} and V_{CC}. During voltage transitions, inputs or I/Os may overshoot V_{SS} to -1.0 V or overshoot to V_{CC} +1.0 V, for periods up to 20 ns.

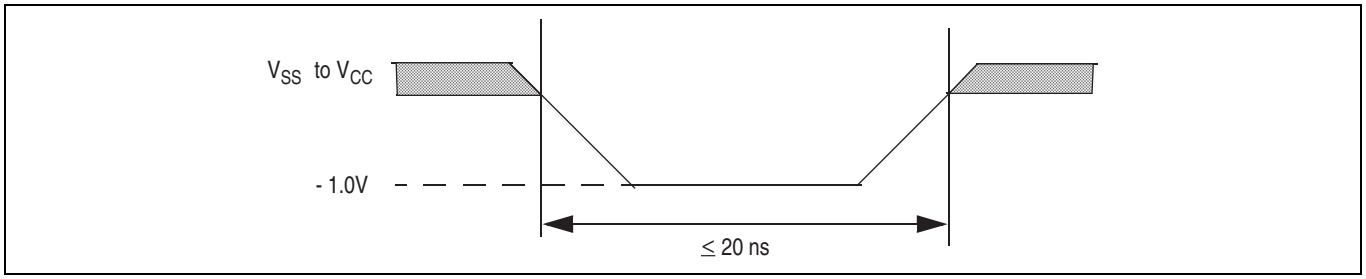


Figure 19 Maximum negative overshoot waveform

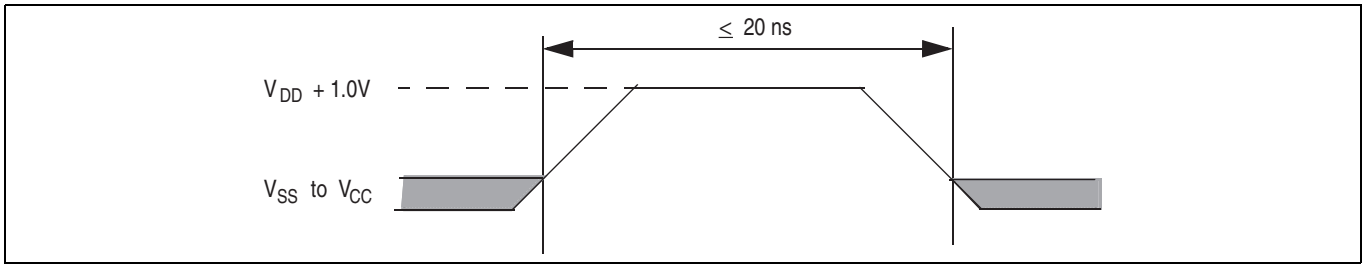


Figure 20 Maximum positive overshoot waveform

5.5 Power-up and power-down

The device must not be selected at power-up or power-down (that is, CS# must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value as follows:

- V_{CC} (min) at power-up, and then for a further delay of t_{PU}
- V_{SS} at power-down

A simple pull-up resistor on Chip Select (CS#) can usually be used to insure safe and proper power-up and power-down.

The device ignores all instructions until a time delay of t_{PU} has elapsed after the moment that V_{CC} rises above the minimum V_{CC} threshold (see **Figure 21**). However, correct operation of the device is not guaranteed if V_{CC} returns below V_{CC} (min) during t_{PU}. No command should be sent to the device until the end of t_{PU}.

The device draws I_{POR} during t_{PU}. After power-up (t_{PU}), the device is in Standby mode, draws CMOS standby current (I_{SB}), and the WEL bit is reset.

During power-down or voltage drops below V_{CC}(cut-off), the voltage must drop below V_{CC}(low) for a period of t_{PD} for the part to initialize correctly on power-up (see **Figure 22**). If during a voltage drop the V_{CC} stays above V_{CC}(cut-off) the part will stay initialized and will work correctly when V_{CC} is again above V_{CC}(min). In the event Power-on Reset (POR) did not complete correctly after power up, the assertion of the RESET# signal or receiving a software reset command (RESET) will restart the POR process.

Normal precautions must be taken for supply rail decoupling to stabilize the V_{CC} supply at the device. Each device in a system should have the V_{CC} rail decoupled by a suitable capacitor close to the package supply connection (this capacitor is generally of the order of 0.1µf).

Table 6 FS-S power-up / power-down voltage and timing

Symbol	Parameter	Min	Max	Unit
V_{CC} (min)	V_{CC} (minimum operation voltage)	1.7	–	V
V_{CC} (cut-off)	V_{CC} (cut-off where re-initialization is needed)	1.5	–	
V_{CC} (low)	V_{CC} (low voltage for initialization to occur)	0.7	–	
t_{PU}	V_{CC} (min) to Read operation	–	300	µs
t_{PD}	V_{CC} (low) time	10.0	–	

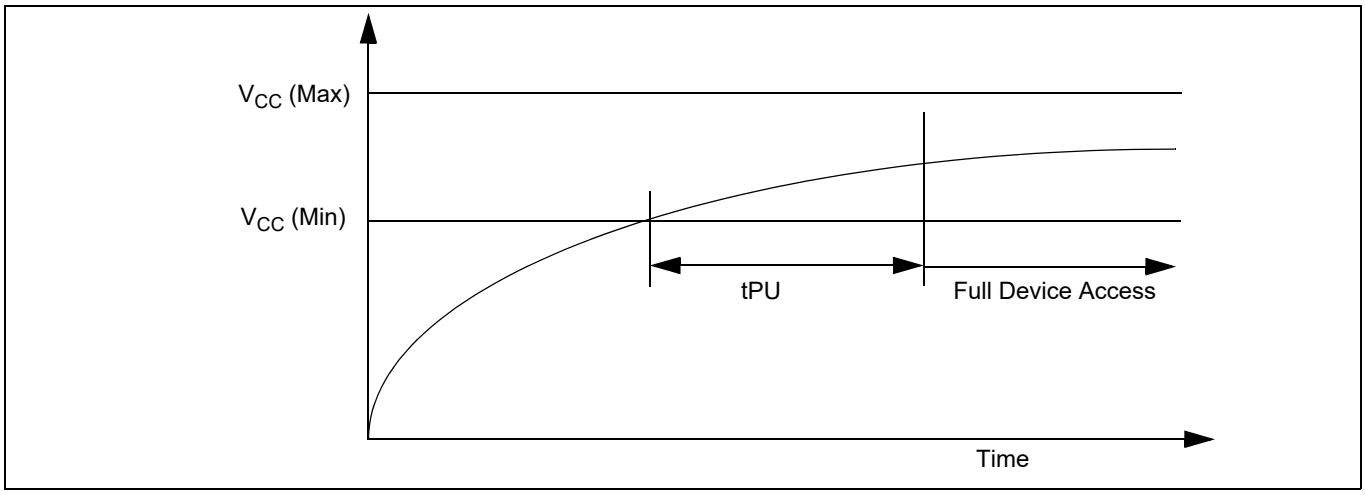


Figure 21 Power-up

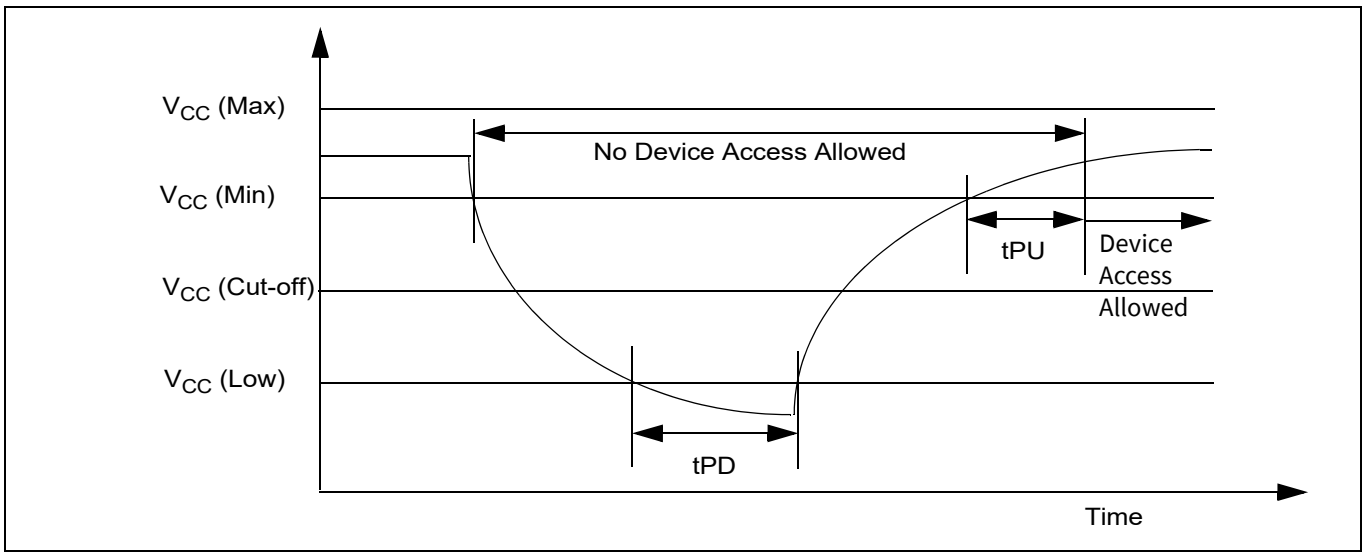


Figure 22 Power-down and voltage drop

5.6 DC characteristics

Table 7 DC characteristics — Operating temperature range (–40°C to +85°C)

Sym-bol	Parameter	Test conditions	Min	Typ[17]	Max	Unit
V_{IL}	Input low voltage	–	-0.5	-	0.3 x V_{CC}	V
V_{IH}	Input high voltage	-	0.7 x V_{CC}	-	V_{CC} + 0.4	
V_{OL}	Output low voltage	I_{OL} = 0.1 mA	-	-	0.2	
V_{OH}	Output high voltage	I_{OH} = –0.1 mA	V_{CC} - 0.2	-		
I_{LI}	Input leakage current	V_{CC} = V_{CC} Max, V_{IN} = V_{IH} or V_{SS}, CS# = V_{IH}	-	-	±2	µA
I_{LO}	Output leakage current	V_{CC} = V_{CC} Max, V_{IN} = V_{IH} or V_{SS}, CS# = V_{IH}	-	-	±2	
I_{CC1}	Active power supply current (READ)[18]	Serial SDR@54 MHz Serial SDR@133 MHz Quad SDR@133 MHz Quad DDR@80 MHz	-	10 25 60 70	18 30 65 90	mA
I_{CC2}	Active power supply current (Page Program)	CS# = V_{CC}	-	60	100	
I_{CC3}	Active power supply current (WRR or WRAR)	CS# = V_{CC}	-	60	100	
I_{CC4}	Active power supply current (SE)	CS# = V_{CC}	-	60	100	
I_{CC5}	Active power supply current (BE)	CS# = V_{CC}	-	60	100	
I_{SB}	Standby current	IO3 / RESET#, CS# = V_{CC}; SI, SCK = V_{CC} or V_{SS}	-	25	100	µA
I_{DPD}	Deep power-down current	IO3 / RESET#, CS# =V_{CC}; SI, SCK = V_{CC} or V_{SS}	-	8	50	
I_{POR}	Power-on reset current	IO3 / RESET#, CS# =V_{CC}; SI, SCK = V_{CC} or V_{SS}	-		80	mA

Notes
17. Typical values are at T_{AI} = 25°C and V_{CC} = 1.8 V.
18. Outputs unconnected during read data return. Output switching current is not included.

Table 8 DC characteristics — Operating temperature range –40°C to +105°C

Symbol	Parameter	Test Conditions	Min	Typ[19]	Max	Unit
V_{IL}	Input low voltage	–	-0.5	–	0.3 x V_{CC}	V
V_{IH}	Input high voltage	–	0.7 x V_{CC}	–	V_{CC} + 0.4	
V_{OL}	Output low voltage	I_{OL} = 0.1 mA		–	0.2	
V_{OH}	Output high voltage	I_{OH} = –0.1 mA	V_{CC} - 0.2	–		
I_{LI}	Input leakage current	V_{CC} = V_{CC} Max, V_{IN} = V_{IH} or V_{SS}, CS# = V_{IH}	–	–	±4	µA
I_{LO}	Output leakage current		–	–	±4	

Notes
19. Typical values are at T_{AI} = 25°C and V_{CC} = 1.8 V.
20. Outputs unconnected during read data return. Output switching current is not included.

Table 8 DC characteristics — Operating temperature range –40°C to +105°C *(continued)*

Symbol	Parameter	Test Conditions	Min	Typ[19]	Max	Unit
I_{CC1}	Active power supply current (READ)[20]	Serial SDR@54 MHz Serial SDR@133 MHz Quad SDR@133 MHz Quad DDR@80 MHz	–	10 25 60 70	18 30 65 90	mA
I_{CC2}	Active power supply current (Page Program)	CS# = V_{CC}	–	60	100	
I_{CC3}	Active power supply current (WRR or WRAR)		–	60	100	
I_{CC4}	Active power supply current (SE)		–	60	100	
I_{CC5}	Active power supply current (BE)		–	60	100	
I_{SB}	Standby current	IO3 / RESET#, CS# =V_{CC}; SI, SCK = V_{CC} or V_{SS}	–	25	300	µA
I_{DPD}	Deep power-down current		–	8	150	
I_{POR}	Power-on reset current		–		80	mA

Notes
19. Typical values are at T_{AI} = 25°C and V_{CC} = 1.8 V.
20. Outputs unconnected during read data return. Output switching current is not included.

Table 9 DC characteristics — Operating temperature range –40°C to +125°C

Symbol	Parameter	Test Conditions	Min	Typ[21]	Max	Unit
V_{IL}	Input LOW voltage	–	-0.5	–	0.3 x V_{CC}	V
V_{IH}	Input HIGH voltage	–	0.7 x V_{CC}	–	V_{CC} + 0.4	
V_{OL}	Output LOWvoltage	I_{OL} = 0.1 mA	–	–	0.2	
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA	V_{CC} - 0.2	–	–	
I_{LI}	Input leakage current	V_{CC} = V_{CC} Max, V_{IN} = V_{IH} or V_{SS}, CS# = V_{IH}	–	–	±4	µA
I_{LO}	Output leakage current	V_{CC} = V_{CC} Max, V_{IN} = V_{IH} or V_{SS}, CS# = V_{IH}	–	–	±4	
I_{CC1}	Active power supply current (READ)[22]	Serial SDR@54 MHz Serial SDR@133 MHz Quad SDR@133 MHz Quad DDR@80 MHz	–	10 25 60 70	18 40 65 90	mA
I_{CC2}	Active power supply current (Page Program)	CS# = V_{CC}	–	60	100	
I_{CC3}	Active power supply current (WRR or WRAR)		–	60	100	
I_{CC4}	Active power supply current (SE)		–	60	100	
I_{CC5}	Active power supply current (BE)		–	60	100	
I_{SB}	Standby current	IO3 / RESET#, CS# =V_{CC}; SI, SCK = V_{CC} or V_{SS}	–	25	300	µA
I_{DPD}	Deep power-down current		–	8	250	
I_{POR}	Power-on reset current		–	–	80	mA

Notes
21. Typical values are at T_{AI} = 25°C and V_{CC} = 1.8 V.
22. Outputs unconnected during read data return. Output switching current is not included.

5.6.1 Active power and standby power modes

The device is enabled and in the Active Power mode when Chip Select (CS#) is LOW. When CS# is HIGH, the device is disabled, but may still be in an Active Power mode until all program, erase, and write operations have completed. The device then goes into the Standby Power mode, and power consumption drops to I_{SB}.

5.6.2 Deep power down mode (DPD)

DPD mode is supported by the S25FS512S devices. If the device has been placed in DPD mode by the DPD (B9h) command, the interface standby current is (I_{DPD}). The DPD command is accepted only while the device is not performing an embedded algorithm as indicated by the Status Register-1 volatile Write In Progress (WIP) bit being cleared to zero (SR1V[0] = 0). While in DPD mode, the device ignores all commands except the Release from DPD (RES ABh) command, which will return the device to the Interface Standby state after a delay of t_{RES}.

Table 10 Valid enter DPD mode and release from DPD mode sequence

Current mode	CS#	SCK	Command	Next mode	Comments
Active	Low to High	N/A	N/A	Standby	–
Standby	High to Low	Toggling	B9h Enter DPD	DPD	DPD entered after CS# goes HIGH and after the t_{DPD} duration (see **Table 14**).
DPD	High to Low	Not Toggling	N/A	DPD	If SCK is toggling and Command is not ABh, device remains in DPD
		Toggling	Command not ABh		
DPD	High to Low	Toggling	ABh Release from DPD	Standby	Release from DPD after CS# goes HIGH and after the t_{RES} duration (see **Table 14**). After CS# goes HIGH to start the release from DPD, it is an invalid sequence to have a CS# transition when the SCK is not toggling.

6 Timing specifications

6.1 Key to switching waveforms

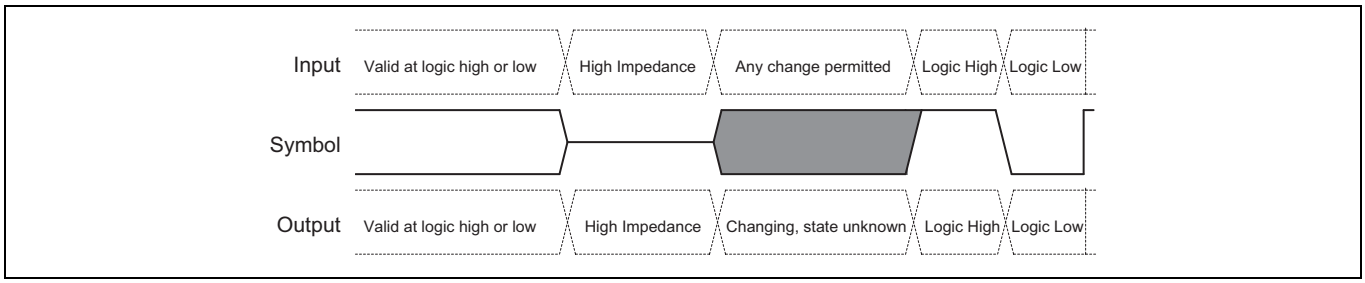


Figure 23 Waveform element meaning

6.2 AC test conditions

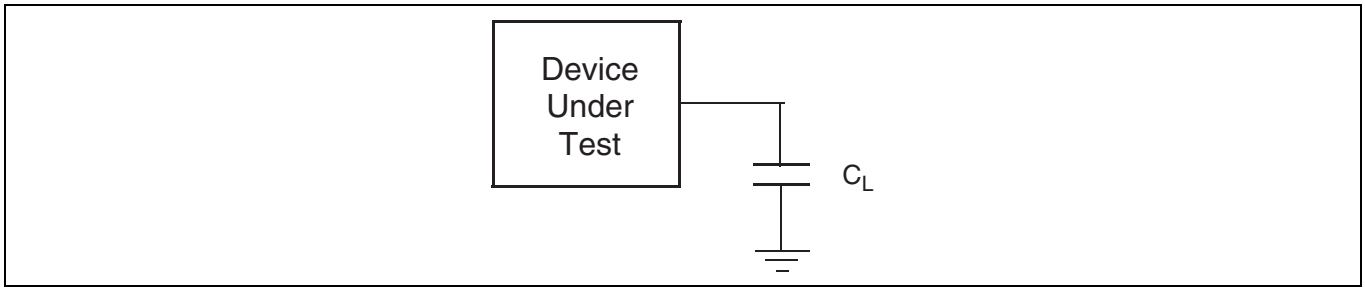


Figure 24 Test setup

Table 11 AC measurement conditions

Symbol	Parameter	Min	Max	Unit
C_L	Load capacitance	–	30	pF
–	Input pulse voltage	0.2 x V_{CC}	0.8 V_{CC}	V
	Input slew rate	0.23	1.25	V/ns
	Input rise and fall times	0.9	5	ns
	Input timing ref voltage	0.5 V_{CC}		V
	Output timing ref voltage	0.5 V_{CC}		

Notes
23. Input slew rate measured from input pulse min to max at V_{CC} max. Example: (1.9V x 0.8) - (1.9V x 0.2) = 1.14 V; 1.14 V/ 1.25 V/ns = 0.9 ns rise or fall time.
24. AC characteristics tables assume clock and data signals have the same slew rate (slope).

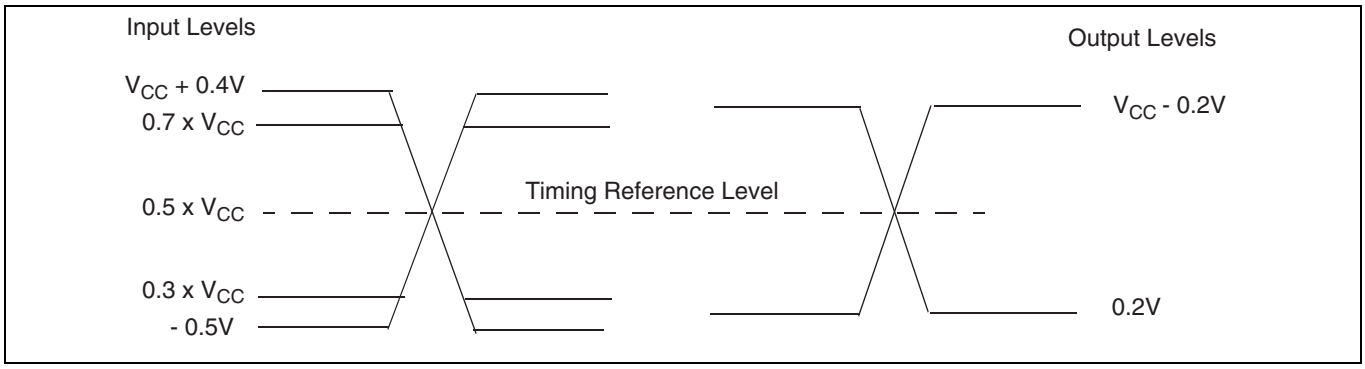


Figure 25 Input, output, and timing reference levels

6.2.1 Capacitance characteristics

Table 12 FS512S capacitance

	Parameter	Test conditions	Min	Max	Unit
C_{IN}	Input capacitance (Applies to SCK, CS#, IO3 / RESET#)	1 MHz	-	8	pF
C_{OUT}	Output capacitance (Applies to all I/O)				

Note
25. Parameter values are not 100% tested. For more details, please refer to the IBIS models.

6.3 Reset

6.3.1 Power on (cold) reset

The device executes a Power-On Reset (POR) process until a time delay of t_{PU} has elapsed after the moment that V_{CC} rises above the minimum V_{CC} threshold (see **Figure 21** and **Table 6**). The device must not be selected (CS# to go HIGH with V_{CC}) during power-up (t_{PU}), i.e. no commands may be sent to the device until the end of t_{PU}.

The IO3 / RESET# signal functions as the RESET# input when CS# is HIGH for more than t_{CS} time or when Quad Mode is not enabled CR1V[1] = 0.

RESET# is ignored during POR. If RESET# is LOW during POR and remains low through and beyond the end of t_{PU}, CS# must remain HIGH until t_{RH} after RESET# returns HIGH. RESET# must return HIGH for greater than t_{RS} before returning low to initiate a hardware reset.

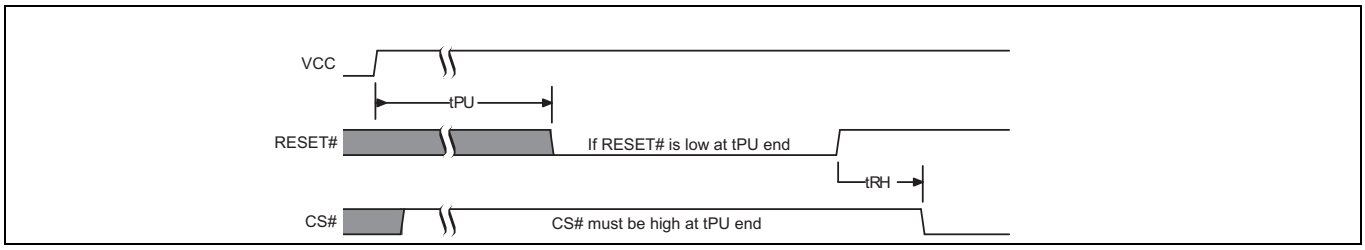


Figure 26 Reset LOW at the end of POR

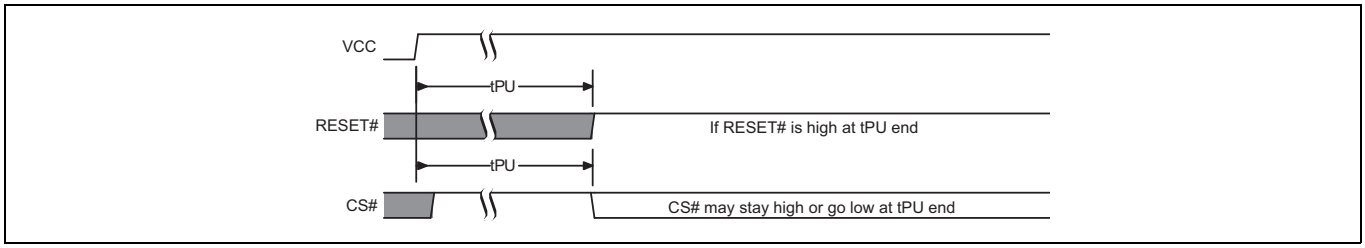


Figure 27 Reset HIGH at the end of POR

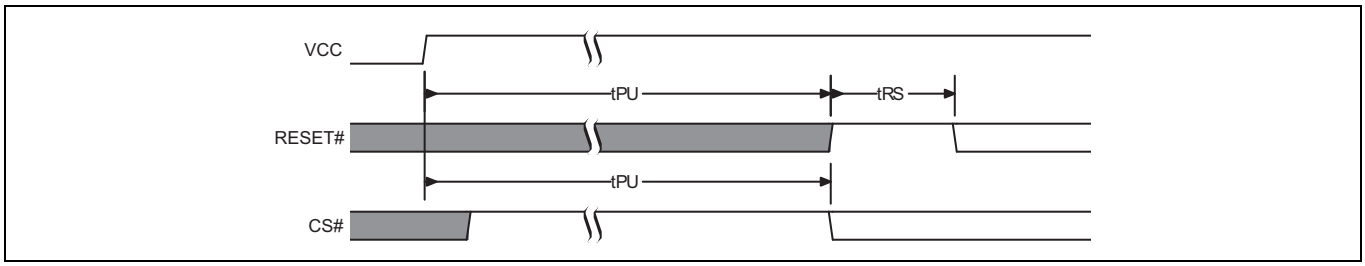


Figure 28 POR followed by hardware reset

6.3.2 IO3 / RESET# input initiated hardware (warm) reset

The IO3 / RESET# signal functions as the RESET# input when CS# is HIGH for more than t_{CS} time or when Quad Mode is not enabled CR1V[1] = 0. The IO3 / RESET# input has an internal pull-up to V_{CC} and may be left unconnected if Quad mode is not used. The t_{CS} delay after CS# goes HIGH gives the memory or host system time to drive IO3 HIGH after its use as a Quad mode I/O signal while CS# was LOW. The internal pull-up to V_{CC} will then hold IO3 / RESET# HIGH until the host system begins driving IO3 / RESET#. The IO3 / RESET# input is ignored while CS# remains HIGH during t_{CS}, to avoid an unintended Reset operation. If CS# is driven LOW to start a new command, IO3 / RESET# is used as IO3.

When the device is not in quad mode or, when CS# is HIGH, and IO3 / RESET# transitions from V_{IH} to V_{IL} for > t_{RP}, following t_{CS}, the device will reset register states in the same manner as power-on reset but, does not go through the full reset process that is performed during POR. The hardware reset process requires a period of t_{RPH} to complete. If the POR process did not complete correctly for any reason during power-up (t_{PU}), RESET# going LOW will initiate the full POR process instead of the hardware reset process and will require t_{PU} to complete the POR process.

The RESET command is independent of the state of IO3 / RESET#. If IO3 / RESET# is high or unconnected, and the RESET instruction is issued, the device will perform software reset.

Additional IO3 RESET# notes:

- IO3 / RESET# must be high for t_{RS} following t_{PU} or t_{RPH}, before going low again to initiate a hardware reset.
- When IO3 / RESET# is driven LOW for at least a minimum period of time (t_{RP}), following t_{CS}, the device terminates any operation in progress, makes all outputs high impedance, and ignores all read/write commands for the duration of t_{RPH}. The device resets the interface to standby state.
- If Quad mode and the IO3 / RESET# feature are enabled, the host system should not drive IO3 low during $t_{CS,}$ to avoid driver contention on IO3. Immediately following commands that transfer data to the host in Quad mode, e.g. Quad I/O Read, the memory drives IO3 / Reset high during $t_{CS,}$ to avoid an unintended Reset operation. Immediately following commands that transfer data to the memory in Quad mode, e.g. Page Program, the host system should drive IO3 / Reset high during $t_{CS,}$ to avoid an unintended Reset operation.
- If Quad mode is not enabled, and if CS# is LOW at the time IO3 / RESET# is asserted LOW, CS# must return HIGH during t_{RPH} before it can be asserted low again after t_{RH}.

Table 13 Hardware reset parameters

Parameter	Description	Limit	Time	Unit
t_{RS}	Reset setup – Prior reset end and RESET# HIGH before RESET# LOW	Min	50	ns
t_{RPH}	Reset pulse hold – RESET# LOW to CS# LOW		35	µs
t_{RP}	RESET# pulse width		200	ns
t_{RH}	Reset Hold – RESET# HIGH before CS# LOW		50	

Notes
26. IO3 / RESET# LOW is ignored during power-up (t_{PU}). If Reset# is asserted during the end of t_{PU}, the device will remain in the reset state and t_{RH} will determine when CS# may go LOW.
27. If Quad mode is enabled, IO3 / RESET# Low is ignored during $t_{CS.}$
28. Sum of t_{RP} and t_{RH} must be equal to or greater than $t_{RPH.}$

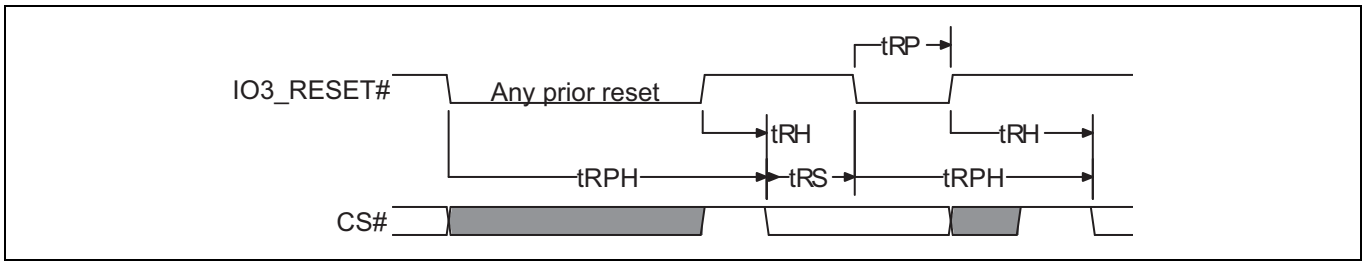


Figure 29 Hardware reset when Quad mode is not enabled and IO3 / reset# is enabled

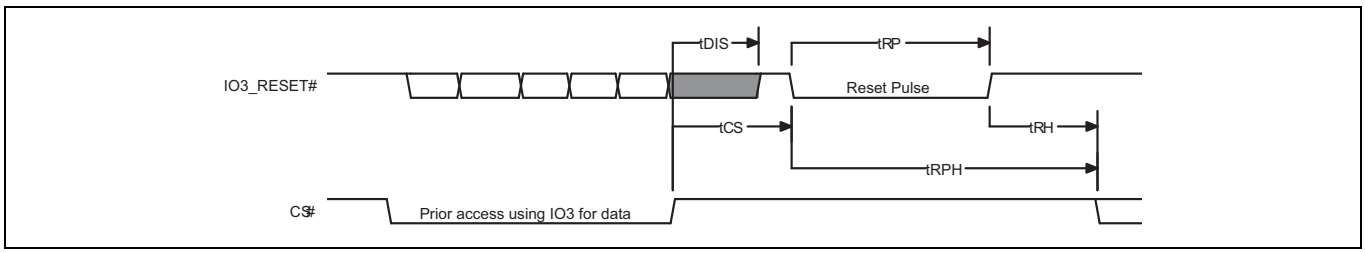


Figure 30 Hardware reset when Quad mode and IO3 / reset# are enabled

6.4 SDR AC characteristics

Table 14 AC characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$F_{SCK, R}$	SCK clock frequency for READ and 4READ instructions	DC	–	50	MHz
$F_{SCK, C}$	SCK clock frequency for the following dual and quad commands: QOR, 4QOR, DIOR, 4DIOR, QIOR, 4QIOR			133	
$F_{SCK, D}$	SCK clock frequency for the following DDR commands: QIOR, 4QIOR			80	
P_{SCK}	SCK clock period	1/ F_{SCK}		∞	ns
t_{WH}, t_{CH}	Clock HIGH time	50% P_{SCK} -5%		50% P_{SCK} +5%	
t_{WL}, t_{CL}	Clock LOW time				
t_{CRT}, t_{CLCH}	Clock rise time (Slew rate)	0.1		–	V/ns
t_{CFT}, t_{CHCL}	Clock fall time (Slew rate)				
t_{CS}	CS# high time (Read Instructions) CS# high time (Read Instructions when reset feature and Quad mode are both enabled) CS# high time (Program / erase Instructions)	10 20 [33] 50			ns
t_{CSS}	CS# active setup time (relative to SCK)	2			
t_{CSH}	CS# active hold time (relative to SCK)	3			
t_{SU}	Data in setup time	2			
t_{HD}	Data in hold time	3			
t_V	Clock LOW to output valid	–		8 [30] 6 [31]	
t_{HO}	Output hold time	1		–	
t_{DIS}	Output disable time [32] Output disable time (when reset feature and Quad mode are both enabled)	–		8 20 [33]	
t_{WPS}	WP# setup time [29]	20		–	
t_{WPH}	WP# hold time [29]	100			
t_{DPD}	CS# HIGH to Power-down mode	–		3	µs
t_{RES}	CS# HIGH to Standby mode without electronic signature Read			30	µs

Notes
29. Only applicable as a constraint for WRR or WRAR instruction when SRWD is set to '1'.
30. Full V_{CC} range and CL = 30 pF.
31. Full V_{CC} range and CL = 15 pF.
32. Output Hi-Z is defined as the point where data is no longer driven.
33. t_{CS} and t_{DIS} require additional time when the Reset feature and Quad mode are enabled (CR2V[5] = 1 and CR1V[1] = 1).

6.4.1 Clock timing

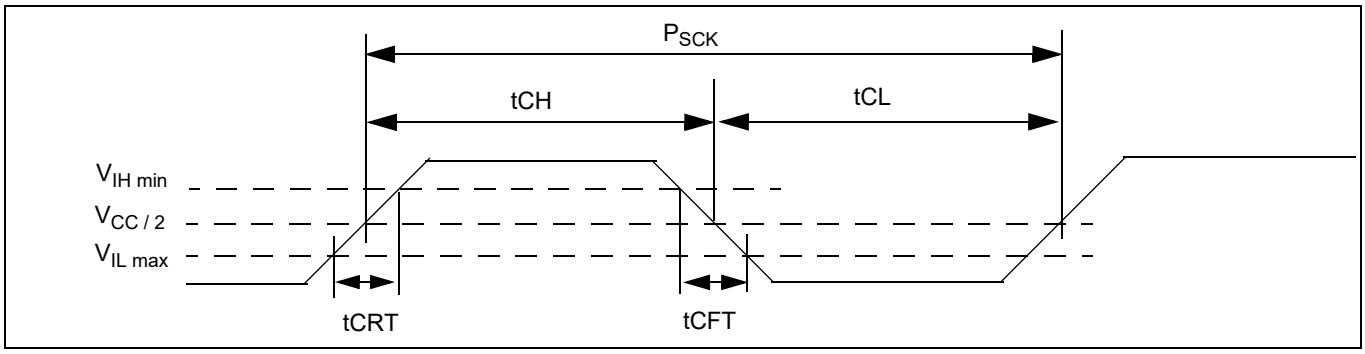


Figure 31 Clock timing

6.4.2 Input / output timing

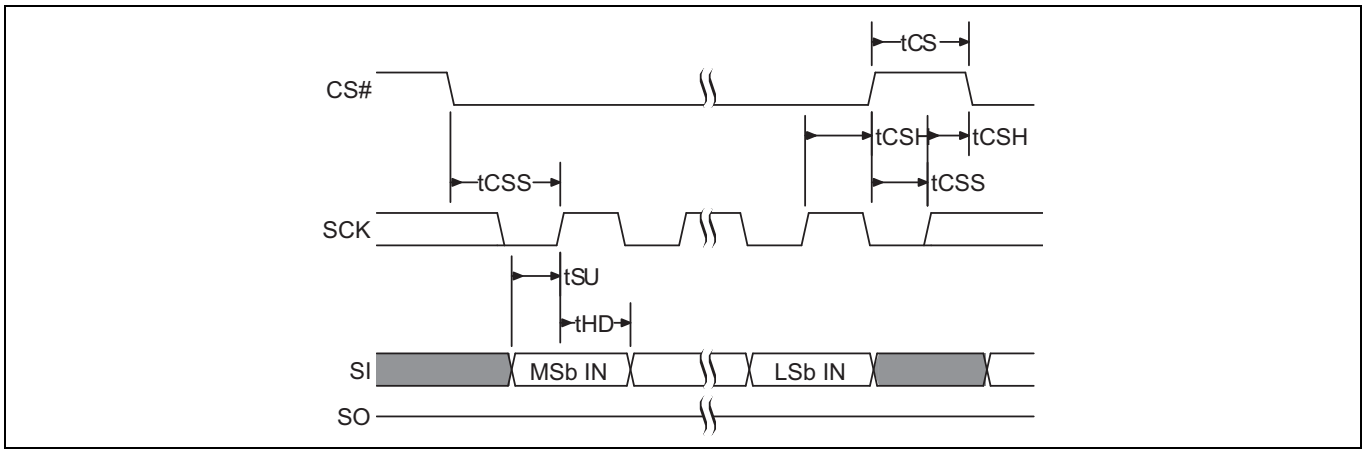


Figure 32 SPI single bit input timing

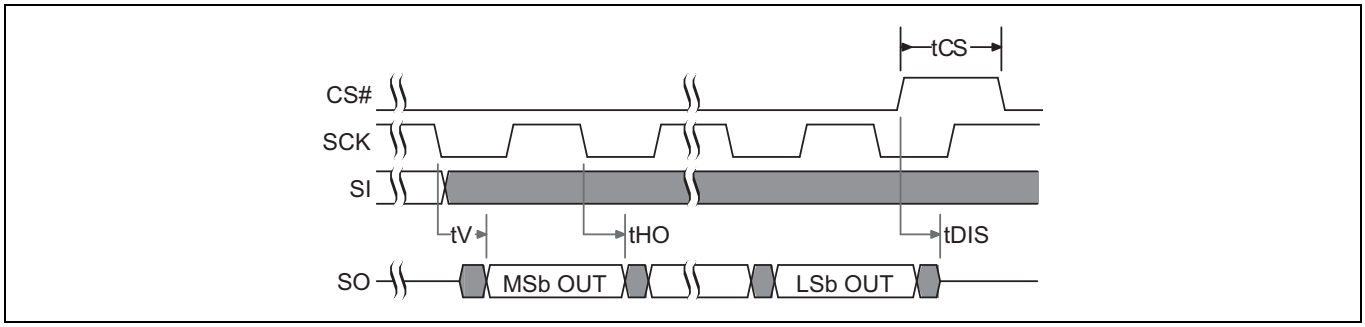


Figure 33 SPI single bit output timing

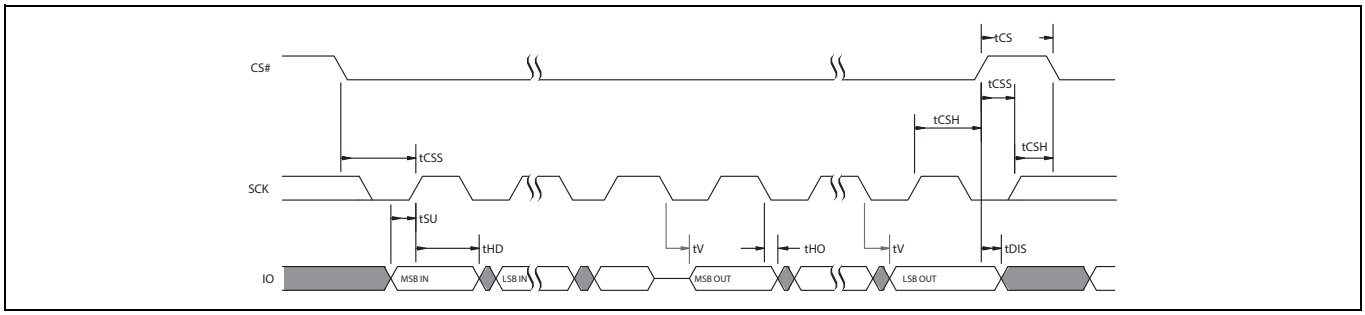


Figure 34 SPI SDR MIO timing

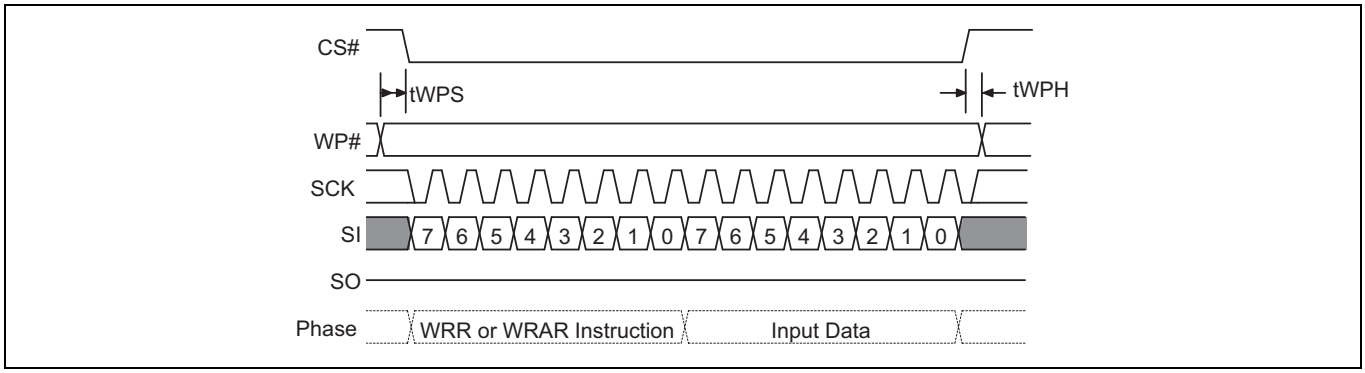


Figure 35 WP# input timing

6.5 DDR AC characteristics

Table 15 DDR 80 MHz AC characteristics operation

Symbol	Parameter	Min	Typ	Max	Unit
$F_{SCK, R}$	SCK clock frequency for DDR READ instruction	DC	–	80	MHz
$P_{SCK, R}$	SCK clock period for DDR READ instruction	12.5		∞	ns
t_{WH}, t_{CH}	Clock HIGH time	50% P_{SCK} - 5%		50% P_{SCK} + 5%	
t_{WL}, t_{CL}	Clock LOW time	50% P_{SCK} - 5%		50% P_{SCK} + 5%	
t_{CS}	CS# high time (Read instructions) CS# high time (Read instructions when reset feature is enabled)	10 20		–	
t_{CSS}	CS# active setup time (relative to SCK)	2			
t_{CSH}	CS# active hold time (relative to SCK)	3			
t_{SU}	IO in setup time	1.5			
t_{HD}	IO in hold time				
t_V	Clock LOW to output valid			6.0 [34]	
t_{HO}	Output hold time	1			
t_{DIS}	Output disable time Output disable time (when reset feature is enabled)	–		8 20	
t_{IO_skew}	First IO to last IO data valid time			400	ps
t_{DPD}	CS# HIGH to Power-down mode			3	µs
t_{RES}	CS# HIGH to Standby mode without electronic signature read			30	

Note
34. CL = 15 pF.

6.5.1 DDR input timing

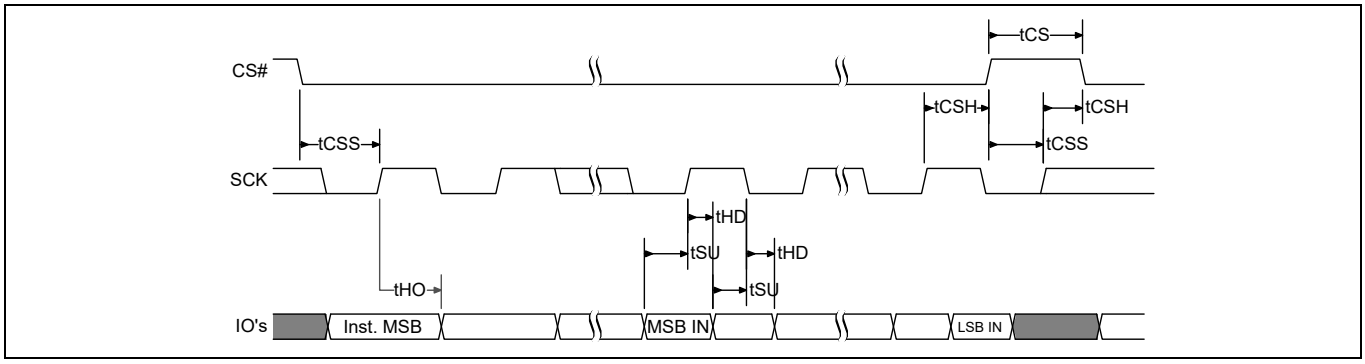


Figure 36 SPI DDR input timing

6.5.2 DDR output timing

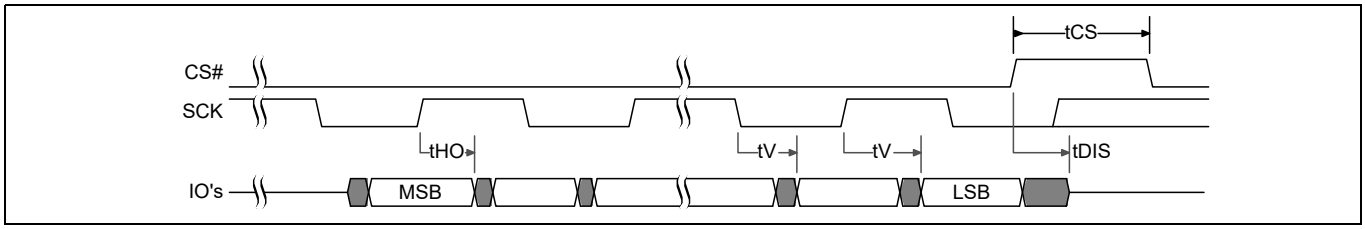


Figure 37 SPI DDR output timing

6.5.3 DDR data valid timing using DLP

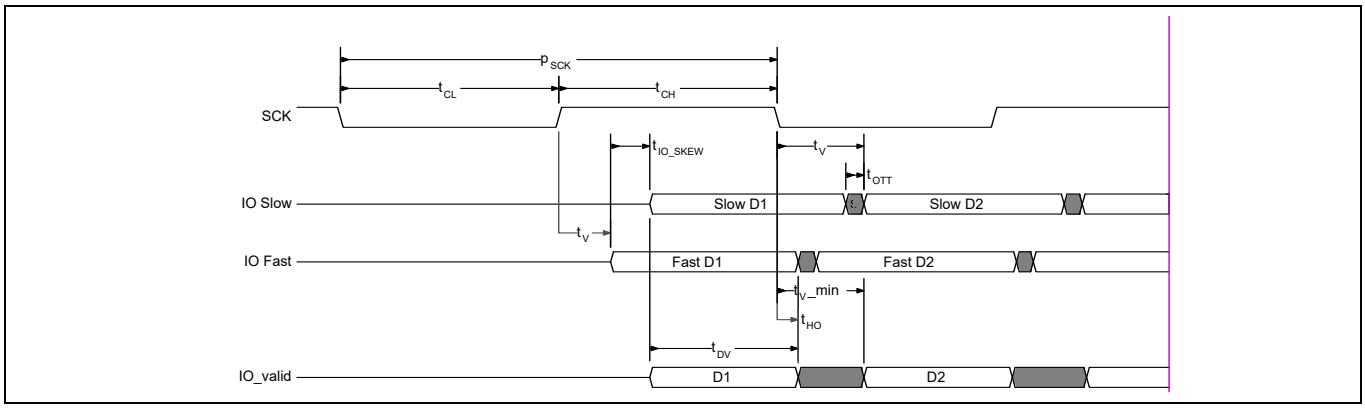


Figure 38 SPI DDR data valid window

The minimum data valid window (t_{DV}) and t_V minimum can be calculated as follows:

t_{DV} = Minimum half clock cycle time (t_{CLH}) [35] - t_{OTT}[37]- t_{IO_SKEW}[36]

t_V _min = t_{HO} + t_{IO_SKEW} + t_{OTT}

Example:

80 MHz clock frequency = 12.5 ns clock period, DDR operations and duty cycle of 45% or higher

t_{CLH} = 0.45 × PSCK = 0.45 × 12.5 ns = 5.625 ns

Bus impedance of 45 Ω and capacitance of 22 pf, with timing reference of 0.75$V_{CC,}$ the rise time from 0 to 1 or fall time 1 to 0 is 1.4[40] × RC time constant (Tau)[39] = 1.4 × 0.99 ns = 1.39 ns

t_{OTT} = Rise time or fall time = 1.39 ns.

Data valid window

t_{DV} = t_{CLH} - t_{IO_SKEW} - t_{OTT} = 5.625 ns - 400 ps - 1.39 ns = 3.835 ns

t_V minimum

t_V _min = t_{HO} + t_{IO_SKEW} + t_{OTT} = 1.0 ns + 400 ps + 1.39 ns = 2.79 ns

Notes

35. t_{CLH} is the shorter duration of t_{CL} or t_{CH}.
36. t_{IO_SKEW} is the maximum difference (delta) between the minimum and maximum t_V (output valid) across all IO signals.
37. t_{OTT} is the maximum Output Transition Time from one valid data value to the next valid data value on each IO. t_{OTT} is dependent on system level considerations including:
    a. Memory device output impedance (drive strength).
    b. System level parasitics on the IOs (primarily bus capacitance).
    c. Host memory controller input V_{IH} and V_{IL} levels at which 0 to 1 and 1 to 0 transitions are recognized.
    d. t_{OTT} is not a specification tested by Infineon, it is system dependent and must be derived by the system designer based on the above considerations.
38. t_{DV} is the data valid window.
39. Tau = R (Output Impedance) x C (Load capacitance).
40. Multiplier of Tau time for voltage to rise to 75% of V_{CC}.

7 Address space maps

7.1 Overview

7.1.1 Extended address

The S25FS512S supports 32-bit (4-byte) addresses to enable higher density devices than allowed by previous generation (legacy) SPI devices that supported only 24-bit (3-byte) addresses. A 24-bit, byte resolution, address can access only 16 MB (128-Mb) maximum density. A 32-bit, byte resolution, address allows direct addressing of up to a 4 GB (32 Gb) address space.

Legacy commands continue to support 24-bit addresses for backward software compatibility. Extended 32-bit addresses are enabled in two ways:

- Extended address mode — a volatile configuration register bit that changes all legacy commands to expect 32 bits of address supplied from the host system.
- 4-byte address commands — that perform both legacy and new functions, which always expect 32-bit address.

The default condition for extended address mode, after power-up or reset, is controlled by a non-volatile configuration bit. The default extended address mode may be set for 24 or 32-bit addresses. This enables legacy software compatible access to the first 128 Mb of a device or for the device to start directly in 32-bit address mode.

7.1.2 Multiple address spaces

Many commands operate on the main flash memory array. Some commands operate on address spaces separate from the main flash array. Each separate address space uses the full 24- or 32-bit address but may only define a small portion of the available address space.

7.2 Flash memory array

The main flash array is divided into erase units called physical sectors.

The FS-S family physical sectors may be configured as a hybrid combination of eight 4-KB parameter sectors at the top or bottom of the address space with all but one of the remaining sectors being uniform size. Because the group of eight 4-KB parameter sectors is in total smaller than a uniform sector, the group of 4-KB physical sectors respectively overlay (replace) the top or bottom 32-KB of the highest or lowest address uniform sector.

The parameter sector erase commands (20h or 21h) must be used to erase the 4-KB sectors individually. The sector (uniform block) erase commands (D8h or DCh) must be used to erase any of the remaining sectors, including the portion of highest or lowest address sector that is not overlaid by the parameter sectors. The uniform block erase command has no effect on parameter sectors.

Configuration Register 1 non-volatile bit 2 (CR1NV[2]) equal to 0 overlays the parameter sectors at the bottom of the lowest address uniform sector. CR1NV[2] = 1 overlays the parameter sectors at the top of the highest address uniform sector. See **“Registers”** on page 51 for more information.

There is also a configuration option to remove the 4-KB parameter sectors from the address map so that all sectors are uniform size. Configuration Register 3 volatile bit 3 (CR3V[3]) equal to 0 selects the hybrid sector architecture with 4-KB parameter sectors. CR3V[3] = 1 selects the uniform sector architecture without parameter sectors. Uniform physical sectors are:

- 256 KB in FS512S

The sector erase (SE) commands erase the physical 256 KB sectors of the 512 Mb device.

Table 16 S25FS512S sector address map, Bottom 4-KB sectors

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Note
4	8	SA00	00000000h-00000FFFh	Sector Starting Address — Sector Ending Address
		:	:	
		SA7	00007000h-00007FFFh	
224	1	SA8	00008000h-0003FFFFh	
256	255	SA9	00040000h-0007FFFFh	
		:	:	
		SA263	03FC0000h-03FFFFFFh	

Table 17 S25FS512S sector address map, Top 4-KB sectors

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Note
256	255	SA00	0000000h-003FFFFh	Sector Starting Address — Sector Ending Address
		:	:	
		SA254	03F80000h - 03FBFFFFh	
224	1	SA255	03FC0000h -03FF7FFFh	
4	8	SA256	03FF8000h-03FF8FFFh	
		:	:	
		SA263	03FFF000h-03FFFFFFh	

Table 18 S25FS512S sector address map (Uniform sectors)

Sector size (KB)	Sector count	Sector range	Address range (Byte address)	Note
256	256	SA00	00000000h-0003FFFFh	Sector Starting Address — Sector Ending Address
		:	:	
		SA255	03FC0000h-03FFFFFFh	

Note These are condensed tables that use a couple of sectors as references. There are address ranges that are not explicitly listed. All 4-KB sectors have the pattern XXXX000h-XXXXFFFh. All 256-KB sectors have the pattern XX00000h-XX3FFFFh, XX40000h-XX7FFFFh, XX80000h-XXCFFFFh, or XXD0000h-XXFFFFFh.

7.3 ID-CFI address space

The RDID command (9Fh) reads information from a separate flash memory address space for device identification (ID) and Common Flash Interface (CFI) information. See **"Device ID and common flash interface (ID-CFI) address map"** on page 136 for the tables defining the contents of the ID-CFI address space. The ID-CFI address space is programmed by Infineon and read-only for the host system.

7.4 JEDEC JESD216 serial flash discoverable parameters (SFDP) space

The RSFDP command (5Ah) reads information from a separate flash memory address space for device identification, feature, and configuration information, in accord with the JEDEC JESD216 standard for Serial Flash Discoverable Parameters. The ID-CFI address space is incorporated as one of the SFDP parameters. See **"Serial flash discoverable parameters (SFDP) address map"** on page 132 for the tables defining the contents of the SFDP address space. The SFDP address space is programmed by Infineon and read-only for the host system.

7.4.1 OTP address space

Each FS-S Family memory device has a 1024-byte OTP address space that is separate from the main flash array. The OTP area is divided into 32, individually lockable, 32-byte aligned and length regions.

In the 32-byte region starting at address zero:

- The 16 lowest address bytes are programmed by Infineon with a 128-bit random number. Only Infineon is able to program zeros in these bytes. Programming ones in these byte locations is ignored and does not affect the value programmed by Infineon. Attempting to program any zero in these byte locations will fail and set P_ERR.
- The next four higher address bytes (OTP Lock Bytes) are used to provide one bit per OTP region to permanently protect each region from programming. The bytes are erased when shipped from Infineon. After an OTP region is programmed, it can be locked to prevent further programming, by programming the related protection bit in the OTP Lock Bytes.
- The next higher 12 bytes of the lowest address region are Reserved for Future Use (RFU). The bits in these RFU bytes may be programmed by the host system but it must be understood that a future device may use those bits for protection of a larger OTP space. The bytes are erased when shipped from Infineon.

The remaining regions are erased when shipped from Infineon, and are available for programming of additional permanent data.

Refer to **Figure 39** for a pictorial representation of the OTP memory space.

The OTP memory space is intended for increased system security. OTP values, such as the random number programmed by Infineon, can be used to "mate" a flash component with the system CPU/ASIC to prevent device substitution.

The configuration register FREEZE (CR1V[0]) bit protects the entire OTP memory space from programming when set to '1'. This allows trusted boot code to control programming of OTP regions then set the FREEZE bit to prevent further OTP memory space programming during the remainder of normal power-on system operation.

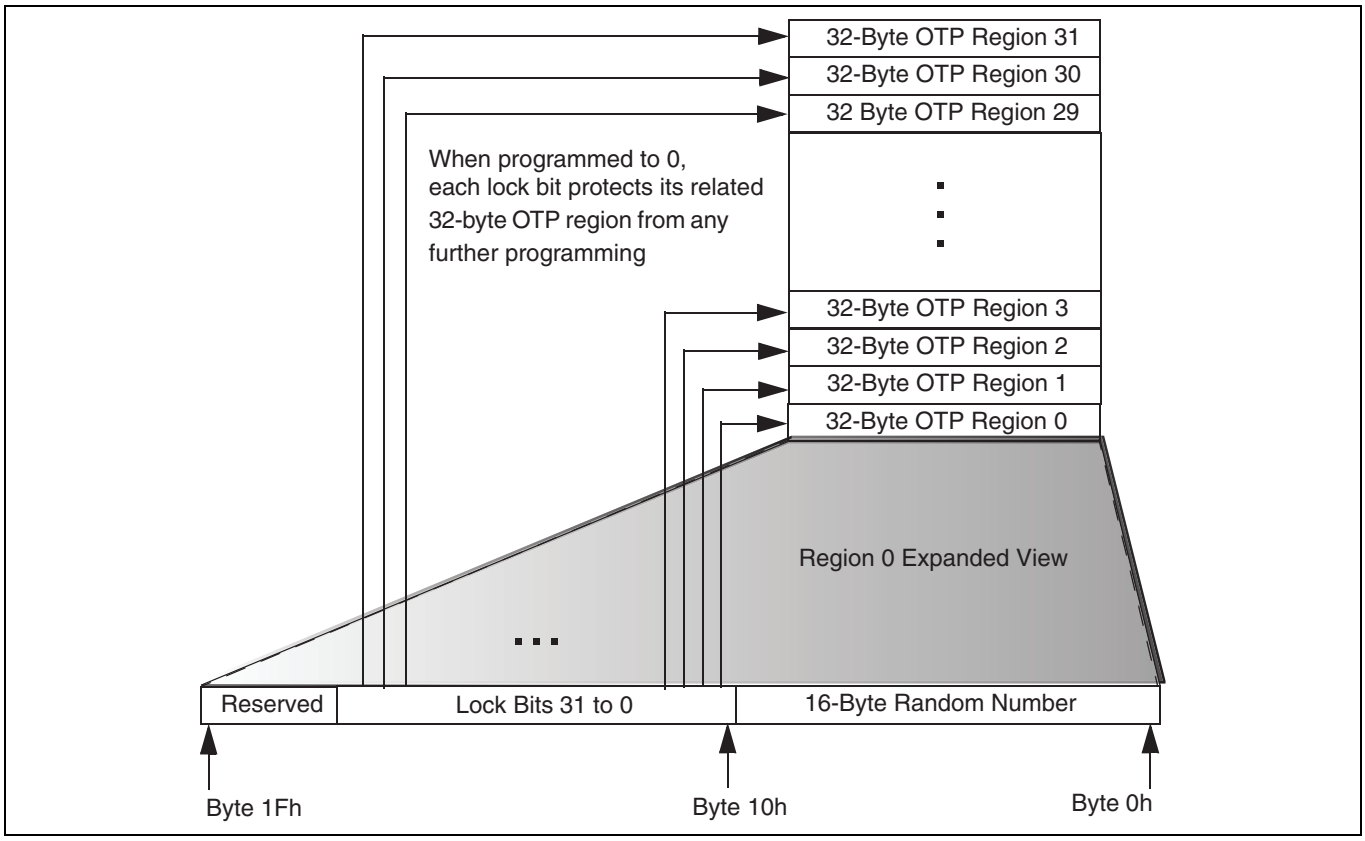


Figure 39 OTP address space

Table 19 OTP address map

Region	Byte address range (Hex)	Contents	Initial delivery state (Hex)
Region 0	000	Least Significant Byte of Infineon Programmed Random Number	Infineon Programmed Random Number
	...	...	
	00F	Most Significant Byte of Infineon Programmed Random Number	
	010 to 013	Region Locking Bits Byte 10 [bit 0] locks region 0 from programming when = 0 ... Byte 13 [bit 7] locks region 31from programming when = 0	All Bytes = FF
	014 to 01F	Reserved for Future Use (RFU)	
Region 1	020 to 03F	Available for User Programming	
Region 2	040 to 05F		
...	...		
Region 31	3E0 to 3FF		

7.5 Registers

Registers are small groups of memory cells used to configure how the S25FS512S memory device operates or to report the status of device operations. The registers are accessed by specific commands. The commands (and hexadecimal instruction codes) used for each register are noted in each register description.

In legacy SPI memory devices the individual register bits could be a mixture of volatile, non-volatile, or OTP bits within the same register. In some configuration options the type of a register bit could change e.g. from non-volatile to volatile.

The S25FS512S uses separate non-volatile or volatile memory cell groups (areas) to implement the different register bit types. However, the legacy registers and commands continue to appear and behave as they always have for legacy software compatibility. There is a non-volatile and a volatile version of each legacy register when that legacy register has volatile bits or when the command to read the legacy register has zero read latency. When such a register is read the volatile version of the register is delivered. During Power-On Reset (POR), hardware reset, or software reset, the non-volatile version of a register is copied to the volatile version to provide the default state of the volatile register. When non-volatile register bits are written the non-volatile version of the register is erased and programmed with the new bit values and the volatile version of the register is updated with the new contents of the non-volatile version. When OTP bits are programmed the non-volatile version of the register is programmed and the appropriate bits are updated in the volatile version of the register. When volatile register bits are written, only the volatile version of the register has the appropriate bits updated.

The type for each bit is noted in each register description. The default state shown for each bit refers to the state after power-on reset, hardware reset, or software reset if the bit is volatile. If the bit is non-volatile or OTP, the default state is the value of the bit when the device is shipped from Infineon. Non-volatile bits have the same cycling (erase and program) endurance as the main flash array.

Table 20 Register descriptions

Register	Abbreviation	Type	Bit location
Status Register 1	SR1NV[7:0]	Non-volatile	7:0
Status Register 1	SR1V[7:0]	Volatile	
Status Register 2	SR2V[7:0]	Volatile	
Configuration Register 1	CR1NV[7:0]	Non-volatile	
Configuration Register 1	CR1V[7:0]	Volatile	
Configuration Register 2	CR2NV[7:0]	Non-volatile	
Configuration Register 2	CR2V[7:0]	Volatile	
Configuration Register 3	CR3NV[7:0]	Non-volatile	
Configuration Register 3	CR3V[7:0]	Volatile	
Configuration Register 4	CR4NV[7:0]	Non-volatile	
Configuration Register 4	CR4V[7:0]	Volatile	
ECC Status Register	ECCSR [7:0]	Volatile	
ASP Register	ASPR[15:1]	OTP	15:1
ASP Register	ASPR[0]	RFU	0
Password Register	PASS[63:0]	Non-volatile OTP	63:0
PPB Lock Register	PPBL[7:1]	Volatile	7:1
PPB Lock Register	PPBL[0]	Volatile Read Only	0
PPB Access Register	PPBAR[7:0]	Non-volatile	7:0
DYB Access Register	DYBAR[7:0]	Volatile	
SPI DDR Data Learning Registers	NVDLR[7:0]	Non-volatile	
SPI DDR Data Learning Registers	VDLR[7:0]	Volatile	

7.5.1 Status Register 1

7.5.1.1 Status Register 1 Non-volatile (SR1NV)

Related Commands: Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 21 Status Register 1 Non-volatile (SR1NV)

Bits	Field name	Function	Type	Default state	Description
7	SRWD_NV	Status Register Write Disable Default	Non-volatile	0	1 = Locks state of SRWD, BP, and Configuration Register-1 bits when WP# is LOW by not executing WRR or WRAR commands that would affect SR1NV, SR1V, CR1NV, or CR1V. 0 = No protection, even when WP# is LOW.
6	P_ERR_D	Programming Error Default	Non-volatile Read only		Provides the default state for the Programming Error Status. Not user programmable.
5	E_ERR_D	Erase Error Default	Non-volatile Read only		Provides the default state for the Erase Error Status. Not user programmable.
4	BP_NV2	Block Protection Non-volatile	Non-volatile	000b	Protects the selected range of sectors (Block) from Program or Erase when the BP bits are configured as non-volatile (CR1NV[3] = 0). Programmed to 111b when BP bits are configured to volatile (CR1NV[3] = 1).- after which these bits are no longer user programmable.
3	BP_NV1				
2	BP_NV0				
1	WEL_D	WEL Default	Non-volatile Read only	0	Provides the default state for the WEL Status. Not user programmable.
0	WIP_D	WIP Default			Provides the default state for the WIP Status. Not user programmable.

Status Register Write Non-volatile (SRWD_NV) SR1NV[7]: Places the device in the Hardware Protected mode when this bit is set to '1' and the WP# input is driven LOW. In this mode, the Write Registers (WRR) and Write Any Register (WRAR) commands (that select Status Register 1 or Configuration Register 1) are ignored and not accepted for execution, effectively locking the state of the Status Register 1 and Configuration Register 1 (SR1NV, SR1V, CR1NV, or CR1V) bits, by making the registers read-only. If WP# is HIGH, Status Register 1 and Configuration Register 1 may be changed by the WRR or WRAR commands. If SRWD_NV is 0, WP# has no effect and Status Register 1 and Configuration Register 1 may be changed by the WRR or WRAR commands. WP# has no effect on the writing of any other registers. The SRWD_NV bit has the same non-volatile endurance as the main flash array. The SRWD (SR1V[7]) bit serves only as a copy of the SRWD_NV bit to provide zero read latency.

Program Error Default (P_ERR_D) SR1NV[6]: Provides the default state for the Programming Error Status in SR1V[6]. This bit is not user programmable.

Erase Error (E_ERR) SR1V[5]: Provides the default state for the Erase Error Status in SR1V[5]. This bit is not user programmable.

Block Protection (BP_NV2, BP_NV1, BP_NV0) SR1NV[4:2]: These bits define the main flash array area to be software-protected against program and erase commands. The BP bits are selected as either volatile or non-volatile, depending on the state of the BP non-volatile bit (BPNV_O) in the configuration register CR1NV[3]. When CR1NV[3] = 0 the non-volatile version of the BP bits (SR1NV[4:2]) are used to control Block Protection and the WRR command writes SR1NV[4:2] and updates SR1V[4:2] to the same value. When CR1NV[3] = 1 the volatile version of the BP bits (SR1V[4:2]) are used to control Block Protection and the WRR command writes SR1V[4:2] and does not affect SR1NV[4:2]. When one or more of the BP bits is set to '1', the relevant memory area is protected against program and erase. The Bulk Erase (BE) command can be executed only when the BP bits are cleared to 0's. See **"Block protection"** on page 69 for a description of how the BP bit values select the memory array area protected. The non-volatile version of the BP bits have the same non-volatile endurance as the main flash array.

Write Enable Latch Default (WEL_D) SR1NV[1]: Provides the default state for the WEL Status in SR1V[1]. This bit is programmed by Infineon and is not user programmable.

Write In Progress Default (WIP_D) SR1NV[0]: Provides the default state for the WIP Status in SR1V[0]. This bit is programmed by Infineon and is not user programmable.

7.5.1.2 Status Register 1 Volatile (SR1V)

Related Commands: Read Status Register (RDSR1 05h), Write Registers (WRR 01h), Write Enable (WREN 06h), Write Disable (WRDI 04h), Clear Status Register (CLSR 30h or 82h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h). This is the register displayed by the RDSR1 command.

Table 22 Status Register 1 Volatile (SR1V)

Bits	Field name	Function	Type	De-fault state	Description
7	SRWD	Status Register Write Disable	Volatile Read only	SR1NV	Volatile copy of SR1NV[7].
6	P_ERR	Programming Error Occurred			1 = Error occurred 0 = No Error
5	E_ERR	Erase Error Occurred			
4	BP2	Block Protection Volatile	Volatile		Protects selected range of sectors (Block) from Program or Erase when the BP bits are configured as volatile (CR1NV[3] = 1). Volatile copy of SR1NV[4:2] when BP bits are configured as non-volatile. User writable when BP bits are configured as volatile.
3	BP1				
2	BP0				
1	WEL	Write Enable Latch			1 = Device accepts Write Registers (WRR and WRAR), program, or erase commands. 0 = Device ignores Write Registers (WRR and WRAR), program, or erase commands. This bit is not affected by WRR or WRAR, only WREN and WRDI commands affect this bit.
0	WIP	Write in Progress	Volatile Read only		1= Device Busy, an embedded operation is in progress such as program or erase. 0 = Ready Device is in standby mode and can accept commands. This bit is not affected by WRR or WRAR, it only provides WIP status.

Status Register Write (SRWD) SR1V[7]: SRWD is a volatile copy of SR1NV[7]. This bit tracks any changes to the non-volatile version of this bit.

Program Error (P_ERR) SR1V[6]: The Program Error Bit is used as a program operation success or failure indication. When the Program Error bit is set to '1', it indicates that there was an error in the last program operation. This bit will also be set when the user attempts to program within a protected main memory sector, or program within a locked OTP region. When the Program Error bit is set to '1', this bit can be cleared to zero with the Clear Status Register (CLSR) command. This is a read-only bit and is not affected by the WRR or WRAR commands.

Erase Error (E_ERR) SR1V[5]: The Erase Error Bit is used as an Erase operation success or failure indication. When the Erase Error bit is set to '1', it indicates that there was an error in the last erase operation. This bit will also be set when the user attempts to erase an individual protected main memory sector. The Bulk Erase command will not set E_ERR if a protected sector is found during the command execution. When the Erase Error bit is set to '1', this bit can be cleared to zero with the Clear Status Register (CLSR) command. This is a read-only bit and is not affected by the WRR or WRAR commands.

Block Protection (BP2, BP1, BP0) SR1V[4:2]: These bits define the main flash array area to be software-protected against program and erase commands. The BP bits are selected as either volatile or non-volatile, depending on the state of the BP non-volatile bit (BPNV_O) in the configuration register CR1NV[3]. When CR1NV[3] = 0 the non-volatile version of the BP bits (SR1NV[4:2]) are used to control Block Protection and the WRR command writes SR1NV[4:2] and updates SR1V[4:2] to the same value. When CR1NV[3] = 1 the volatile version of the BP bits (SR1V[4:2]) are used to control Block Protection and the WRR command writes SR1V[4:2] and does not affect SR1NV[4:2]. When one or more of the BP bits is set to '1', the relevant memory area is protected against program and erase. The Bulk Erase (BE) command can be executed only when the BP bits are

cleared to 0's. See **"Block protection"** on page 69 for a description of how the BP bit values select the memory array area protected.

Write Enable Latch (WEL) SR1V[1]: The WEL bit must be set to '1' to enable program, write, or erase operations as a means to provide protection against inadvertent changes to memory or register values. The Write Enable (WREN) command execution sets the Write Enable Latch to '1' to allow any program, erase, or write commands to execute afterwards. The Write Disable (WRDI) command can be used to set the Write Enable Latch to '0' to prevent all program, erase, and write commands from execution. The WEL bit is cleared to 0 at the end of any successful program, write, or erase operation. Following a failed operation the WEL bit may remain set and should be cleared with a WRDI command following a CLSR command. After a power down / power up sequence, hardware reset, or software reset, the Write Enable Latch is set to '0' The WRR or WRAR command does not affect this bit.

Write In Progress (WIP) SR1V[0]: Indicates whether the device is performing a program, write, erase operation, or any other operation, during which a new operation command will be ignored. When the bit is set to '1', the device is busy performing an operation. While WIP is 1, only Read Status (RDSR1 or RDSR2), Read Any Register (RDAR), Erase Suspend (ERSP), Program Suspend (PGSP), Clear Status Register (CLSR), and Software Reset (RESET) commands are accepted. ERSP and PGSP will only be accepted if memory array erase or program operations are in progress. The status register E_ERR and P_ERR bits are updated while WIP = 1. When P_ERR or E_ERR bits are set to one, the WIP bit will remain set to one indicating the device remains busy and unable to receive new operation commands. A Clear Status Register (CLSR) command must be received to return the device to standby mode. When the WIP bit is cleared to 0 no operation is in progress. This is a read-only bit.

7.5.2 Status Register 2 Volatile (SR2V)

Related Commands: Read Status Register 2 (RDSR2 07h), Read Any Register (RDAR 65h). Status Register-2 does not have user programmable non-volatile bits, all defined bits are volatile read only status. The default state of these bits are set by hardware.

Table 23 Status Register 2 Volatile (SR2V)

Bits	Field name	Function	Type	Default state	Description
7	RFU	Reserved	-		Reserved for Future Use
6					
5					
4					
3					
2	ESTAT	Erase Status	Volatile Read only	0	1 = Sector Erase Status command result = Erase Completed 0 = Sector Erase Status command result = Erase Not Completed
1	ES	Erase Suspend			1 = In erase suspend mode 0 = Not in erase suspend mode
0	PS	Program Suspend			1 = In program suspend mode 0 = Not in program suspend mode

Erase Status (ESTAT) SR2V[2]: The Erase Status bit indicates whether the sector, selected by an immediately preceding Erase status command, completed the last erase command on that sector. The Erase Status command must be issued immediately before reading SR2V to get valid erase status. Reading SR2V during a program or erase suspend does not provide valid erase status. The erase status bit can be used by system software to detect any sector that failed its last erase operation. This can be used to detect erase operations failed due to loss of power during the erase operation.

Erase Suspend (ES) SR2V[1]: The Erase Suspend bit is used to determine when the device is in Erase Suspend mode. This is a status bit that cannot be written by the user. When Erase Suspend bit is set to '1', the device is in erase suspend mode. When Erase Suspend bit is cleared to 0, the device is not in erase suspend mode. Refer to

"Erase or Program Suspend (EPS 85h, 75h, B0h)" on page 114 for details about the Erase Suspend / Resume commands.

Program Suspend (PS) SR2V[0]: The Program Suspend bit is used to determine when the device is in Program Suspend mode. This is a status bit that cannot be written by the user. When Program Suspend bit is set to '1', the device is in program suspend mode. When the Program Suspend bit is cleared to 0, the device is not in program suspend mode. Refer to **"Erase or Program Suspend (EPS 85h, 75h, B0h)"** on page 114 for details.

7.5.3 Configuration Register 1

Configuration Register 1 controls certain interface and data protection functions. The register bits can be changed using the WRR command with sixteen input cycles or with the WRAR command.

7.5.3.1 Configuration Register 1 Non-volatile (CR1NV)

Related Commands: Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 24 Configuration Register 1 Non-volatile (CR1NV)

Bits	Field name	Function	Type	De-fault state	Description
7	RFU	Reserved for Future Use	Non-volatile	0	Reserved
6				0	
5	TBPROT_O	Configures Start of Block Protection	OTP	0	1 = BP starts at bottom (LOW address) 0 = BP starts at top (HGH address)
4	RFU	Reserved for Future Use	RFU		Reserved.
3	BPNV_O	Configures BP2-0 in Status Register	OTP		1 = Volatile 0 = Non-volatile
2	TBPARM_O	Configures Parameter Sectors location			1 = 4-KB physical sectors at top (high address) 0 = 4-KB physical sectors at bottom (low address) RFU in uniform sector configuration
1	QUAD_NV	Quad Non-volatile	Non-volatile		Provides the default state for the QUAD bit
0	FREEZE_D	FREEZE Default	Non-volatile Read only		Provides the default state for the Freeze bit. Not user programmable

Top or Bottom Protection (TBPROT_O) CR1NV[5]: This bit defines the operation of the Block Protection bits BP2, BP1, and BP0 in the Status Register. As described in the status register section, the BP2-0 bits allow the user to optionally protect a portion of the array, ranging from 1/64, ¼, ½, and so on, up to the entire array. When TBPROT_O is set to '0', the Block Protection is defined to start from the top (maximum address) of the array. When TBPROT_O is set to '1', the Block Protection is defined to start from the bottom (zero address) of the array. The TBPROT_O bit is OTP and set to '0' when shipped from Infineon. If TBPROT_O is programmed to 1, writing the bit with a zero does not change the value or set the Program Error bit (P_ERR in SR1V[6]).

The desired state of TBPROT_O must be selected during the initial configuration of the device during system manufacture; before the first program or erase operation on the main flash array. TBPROT_O must not be programmed after programming or erasing is done in the main flash array.

CR1NV[4]: Reserved for Future Use.

Block Protection Non-volatile (BPNV_O) CR1NV[3]: The BPNV_O bit defines whether the BP_NV 2-0 bits or the BP 2-0 bits in the Status Register are selected to control the Block Protection feature. The BPNV_O bit is OTP and cleared to '0' with the BP_NV bits cleared to '000' when shipped from Infineon. When BPNV_O is set to '0' the BP_NV 2-0 bits in the Status Register are selected to control the block protection and are written by the WRR command. The time required to write the BP_NV bits is t_W. When BPNV is set to '1', the BP2-0 bits in the Status Register are selected to control the block protection and the BP_NV 2-0 bits will be programmed to binary '111'. This will cause the BP 2-0 bits to be set to binary 111 after POR, hardware reset, or command reset. When BPNV is set to '1', the WRR command writes only the volatile version of the BP bits (SR1V[4:2]). The non-volatile version of the BP bits (SR1NV[4:2]) are no longer affected by the WRR command. This allows the BP bits to be written an unlimited number of times because they are volatile and the time to write the volatile BP bits is the much faster

t_{CS} volatile register write time. If BPNV_O is programmed to '1', writing the bit with a zero does not change the value or set the Program Error bit (P_ERR in SR1V[6]).

TBPARM_O CR1NV[2]: TBPARM_O defines the logical location of the parameter block. The parameter block consists of eight 4-KB parameter sectors, which replace a 32 KB portion of the highest or lowest address sector. When TBPARM_O is set to '1', the parameter block is in the top of the memory array address space. When TBPARM_O is set to '0' the parameter block is at the Bottom of the array. TBPARM_O is OTP and set to '0' when it ships from Infineon. If TBPARM_O is programmed to 1, writing the bit with a zero does not change the value or set the Program Error bit (P_ERR in SR1V[6]).

The desired state of TBPARM_O must be selected during the initial configuration of the device during system manufacture; before the first program or erase operation on the main flash array. TBPARM_O must not be programmed after programming or erasing is done in the main flash array.

TBPROT_O can be set or cleared independent of the TBPARM_O bit. Therefore, the user can elect to store parameter information from the bottom of the array and protect boot code starting at the top of the array, or vice versa. Or, the user can elect to store and protect the parameter information starting from the top or bottom together.

When the memory array is configured as uniform sectors, the TBPARM_O bit is Reserved for Future Use (RFU) and has no effect because all sectors are uniform size.

Quad Data Width Non-volatile (QUAD_NV) CR1NV[1]: Provides the default state for the QUAD bit in CR1V[1]. The WRR or WRAR command affects this bit. Non-volatile selection of QPI mode, by programming CR2NV[6] = 1, will also program QUAD_NV = 1 to change the non-volatile default to Quad data width mode. While QPI mode is selected by CR2V[6] = 1, the Quad_NV bit cannot be cleared to 0.

Freeze Protection Default (FREEZE) CR1NV[0]: Provides the default state for the FREEZE bit in CR1V[0]. This bit is not user programmable.

7.5.3.2 Configuration Register 1 Volatile (CR1V)

Related Commands: Read Configuration Register (RDCR 35h), Write Registers (WRR 01h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h). This is the register displayed by the RDCR command.

Table 25 Configuration Register 1 Volatile (CR1V)

Bits	Field name	Function	Type	Default state	Description
7	RFU	Reserved for Future Use	Volatile	CR1NV	Reserved
6					
5	TBPROT	Volatile copy of TBPROT_O	Volatile Read only		Not user writable. See CR1NV[5] TBPROT_O
4	RFU	Reserved for Future Use	RFU		Reserved
3	BPNV	Volatile copy of BPNV_O	Volatile Read only		Not user writable. See CR1NV[3] BPNV_O
2	TBPARM	Volatile copy of TBPARM_O			Not user writable.See CR1NV[2] TBPARM_O
1	QUAD	Quad I/O Mode	Volatile		1 = Quad 0 = Dual or Serial The WRR command writes the Non-Volatile Quad bit (CR1NV[1]). See full description below.
0	FREEZE	Lock-Down Block Protection until next power cycle			Lock current state of Block Protection control bits, and OTP regions. 1 = Block Protection and OTP locked 0 = Block Protection and OTP unlocked

TBPROT, BPNV, and TBPARM CR1V[5,3,2]: These bits are volatile copies of the related non-volatile bits of CR1NV. These bits track any changes to the related non-volatile version of these bits.

Quad Data Width (QUAD) CR1V[1]: When set to '1', this bit switches the data width of the device to 4-bit Quad mode. That is, WP# becomes IO2 and IO3 / RESET# becomes an active I/O signal when CS# is LOW or the RESET# input when CS# is HIGH. The WP# input is not monitored for its normal function and is internally set to HIGH (inactive). The commands for Serial, and Dual I/O Read still function normally but, there is no need to drive the

WP# input for those commands when switching between commands using different data path widths. Similarly, there is no requirement to drive the IO3 / RESET# during those commands (while CS# is LOW).

The QUAD bit must be set to one when using the Quad I/O Read, DDR Quad I/O Read, QPI mode (CR2V[6] = 1), and Read Quad ID commands. While QPI mode is selected by CR2V[6] = 1, the Quad bit cannot be cleared to 0. The WRR command writes the non-volatile version of the Quad bit (CR1NV[1]), which also causes an update to the volatile version CR1V[1]. The WRR command can not write the volatile version CR1V[1] without first affecting the non-volatile version CR1NV[1]. The WRAR command must be used when it is desired to write the volatile Quad bit CR1V[1] without affecting the non-volatile version CR1NV[1].

Freeze Protection (FREEZE) CR1V[0]: The Freeze Bit, when set to '1', locks the current state of the Block Protection control bits and OTP area:

- BPNV_2-0 bits in the non-volatile Status Register 1 (SR1NV[4:2])
- BP 2-0 bits in the volatile Status Register 1 (SR1V[4:2])
- TBPROT_O, TBPARM_O, and BPNV_O bits in the non-volatile Configuration Register (CR1NV[5,3, 2])
- TBPROT, TBPARM, and BPNV bits in the volatile Configuration Register (CR1V[5, 3, 2]) are indirectly protected in that they are shadows of the related CR1NV OTP bits and are read only
- the entire OTP memory space
- Any attempt to change the above listed bits while FREEZE = 1 is prevented.
- The WRR command does not affect the listed bits and no error status is set.
- The WRAR command does not affect the listed bits and no error status is set.
- The OTPP command, with an address within the OTP area, fails and the P-ERR status is set.

As long as the FREEZE bit remains cleared to logic 0 the Block Protection control bits and FREEZE are writable, and the OTP address space is programmable.

Once the FREEZE bit has been written to a logic 1 it can only be cleared to a logic 0 by a power-off to power-on cycle or a hardware reset. Software reset will not affect the state of the FREEZE bit.

The CR1V[0] FREEZE bit is volatile and the default state of FREEZE after power-on comes from FREEZE_D in CR1NV[0]. The FREEZE bit can be set in parallel with updating other values in CR1V by a single WRR or WRAR command.

The FREEZE bit does not prevent the WRR or WRAR commands from changing the SRWD_NV (SR1NV[7]), Quad_NV (CR1NV[1]), or QUAD (CR1V[1]) bits.

7.5.4 Configuration Register 2

Configuration Register 2 controls certain interface functions. The register bits can be read and changed using the Read Any Register and Write Any Register commands. The non-volatile version of the register provides the ability to set the POR, hardware reset, or software reset state of the controls. These configuration bits are OTP and may only have their default state changed to the opposite value one time during system configuration. The volatile version of the register controls the feature behavior during normal operation.

7.5.4.1 Configuration Register 2 Non-volatile (CR2NV)

Related Commands: Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 26 Configuration Register 2 Non-volatile (CR2NV)

Bits	Field name	Function	Type	Default state	Description
7	AL_NV	Address Length	OTP	0	1 = 4-byte address 0 = 3-byte address
6	QA_NV	QPI		0	1 = Enabled – QPI (4-4-4) protocol in use. 0 = Disabled – Legacy SPI protocols in use, instruction is always serial on SI.
5	IO3R_NV	IO3 Reset		0	1 = Enabled – IO3 is used as RESET# input when CS# is HIGH or Quad Mode is disabled CR1V[1] = 0. 0 = Disabled – IO3 has no alternate function, hardware reset is disabled.
4	RFU	Reserved		0	Reserved for Future Use
3	RL_NV	Read Latency		1	0 to 15 latency (dummy) cycles following read address or continuous mode bits. Note that bit 3 has a default value of 1 and may be programmed one time to 0 but cannot be returned to 1.
2				0	
1				0	
0				0	

Address Length Non-volatile CR2NV[7]: This bit controls the POR, hardware reset, or software reset state of the expected address length for all commands that require address and are not fixed 3-byte only or 4-byte (32 bit) only address. Most commands that need an address are legacy SPI commands that traditionally used 3-byte (24 bit) address. For device densities greater than 128 Mb a 4-byte address is required to access the entire memory array. The address length configuration bit is used to change most 3-byte address commands to expect 4-byte address. See **Table 45** for command address length. This non-volatile Address Length configuration bit enables the device to start immediately (boot) in 4-byte address mode rather than the legacy 3-byte address mode.

QPI Non-volatile CR2NV[6]: This bit controls the POR, hardware reset, or software reset state of the expected instruction width for all commands. Legacy SPI commands always send the instruction one bit wide (serial I/O) on the SI (IO0) signal. The S25FS512S also supports the QPI mode in which all transfers between the host system and memory are 4 bits wide on IO0 to IO3, including all instructions. This non-volatile QPI configuration bit enables the device to start immediately (boot) in QQPIPI mode rather than the legacy serial instruction mode. When this bit is programmed to QPI mode, the QUAD_NV bit is also programmed to Quad mode (CR1NV[1] = 1). The recommended procedure for moving to QPI mode is to first use the WRAR command to set CR2V[6] = 1, QPI mode. The volatile register write for QPI mode has a short and well defined time (t_{CS}) to switch the device interface into QPI mode. Following commands can then be immediately sent in QPI protocol. The WRAR command can be used to program CR2NV[6] = 1, followed by polling of SR1V[0] to know when the programming operation is completed. Similarly, to exit QPI mode, the WRAR command is used to clear CR2V[6] = 0. CR2NV[6] cannot be erased to 0 because it is OTP.

IO3 Reset Non-volatile CR2NV[5]: This bit controls the POR, hardware reset, or software reset state of the IO3 signal behavior. Most legacy SPI devices do not have a hardware reset input signal due to the limited signal count and connections available in traditional SPI device packages. The S25FS512S provides the option to use the IO3 signal as a hardware reset input when the IO3 signal is not in use for transferring information between the host system and the memory. This non-volatile IO3 Reset configuration bit enables the device to start immediately (boot) with IO3 enabled for use as a RESET# signal.

Read Latency Non-volatile CR2NV[3:0]: This bit controls the POR, hardware reset, or software reset state of the read latency (dummy cycle) delay in all variable latency read commands. The following read commands have a variable latency period between the end of address or mode and the beginning of read data returning to the host:

- Fast Read
- Dual I/O Read

- Quad I/O Read
- DDR Quad I/O Read
- OTPR
- RDAR

This non-volatile read latency configuration bit sets the number of read latency (dummy cycles) in use so the device can start immediately (boot) with an appropriate read latency for the host system.

Table 27 Latency code (cycles) versus frequency

Latency code	Read command maximum frequency (MHz)			
	Fast Read (1-1-1) OTPR (1-1-1) RDAR (1-1-1) RDAR (4-4-4)	**Dual I/O (1-2-2)**	**Quad I/O (1-4-4) Quad I/O (4-4-4)**	**DDR Quad I/O (1-4-4) DDR Quad I/O (4-4-4) [44]**
	Mode cycles = 0	**Mode cycles = 4**	**Mode cycles = 2**	**Mode cycles = 1**
0	50	80	40	N/A
1	66	92	53	22
2	80	104	66	34
3	92	116	80	45
4	104	129	92	57
5	116	133	104	68
6	129		116	80
7	133		129	
8			133	
9				
10				
11				
12				
13				
14				
15				

Notes
41. SCK frequency > 133 MHz SDR, or 80 MHz DDR is not supported by this family of devices.
42. The Dual I/O, Quad I/O, QPI, DDR Quad I/O, and DDR QPI, command protocols include Continuous Read Mode bits following the address. The clock cycles for these bits are not counted as part of the latency cycles shown in the table. Example: the legacy Quad I/O command has 2 Continuous Read Mode cycles following the address. Therefore, the legacy Quad I/O command without additional read latency is supported only up to the frequency shown in the table for a read latency of 0 cycles. By increasing the variable read latency the frequency of the Quad I/O command can be increased to allow operation up to the maximum supported 133 MHz frequency.
43. Other read commands have fixed latency, e.g. Read always has zero read latency. RSFDP always has eight cycles of latency.
44. DDR QPI is only supported for Latency cycles 1 through 5 and for clock frequency of up to 68 MHz.

7.5.4.2 Configuration Register 2 Volatile (CR2V)

Related Commands: Read Any Register (RDAR 65h), Write Any Register (WRAR 71h), 4BAM.

Table 28 Configuration Register 2 Volatile (CR2V)

Bits	Field name	Function	Type	Default state	Description
7	AL	Address Length	Volatile	CR2NV	1 = 4-byte address 0 = 3-byte address
6	QA	QPI			1 = Enabled – QPI (4-4-4) protocol in use 0 = Disabled – Legacy SPI protocols in use, instruction is always serial on SI.
5	IO3R_S	IO3 Reset			1 = Enabled – IO3 is used as RESET# input when CS# is HIGH or Quad mode is disabled CR1V[1] = 0 0 = Disabled – IO3 has no alternate function, hardware reset is disabled
4	RFU	Reserved			Reserved for Future Use
3	RL	Read Latency			0 to 15 latency (dummy) cycles following read address or continuous mode bits.
2					
1					
0					

Address Length CR2V[7]: This bit controls the expected address length for all commands that require address and are not fixed 3-byte only or 4-byte (32 bit) only address. See **Table 45** for command address length. This volatile Address Length configuration bit enables the address length to be changed during normal operation. The 4-byte address mode (4BAM) command directly sets this bit into 4-byte address mode.

QPI CR2V[6]: This bit controls the expected instruction width for all commands. This volatile QPI configuration bit enables the device to enter and exit QPI mode during normal operation. When this bit is set to QPI mode, the QUAD bit is also set to Quad mode (CR1V[1] = 1). When this bit is cleared to legacy SPI mode, the QUAD bit is not affected.

IO3 Reset CR2V[5]: This bit controls the IO3 / RESET# signal behavior. This volatile IO3 Reset configuration bit enables the use of IO3 as a RESET# input during normal operation.

Read Latency CR2V[3:0]: This bit controls the read latency (dummy cycle) delay in variable latency read commands These volatile configuration bits enable the user to adjust the read latency during normal operation to optimize the latency for different commands or, at different operating frequencies, as needed.

7.5.5 Configuration Register 3

Configuration Register 3 controls certain command behaviors. The register bits can be read and changed using the Read Any Register and Write Any Register commands. The non-volatile register provides the POR, hardware reset, or software reset state of the controls. These configuration bits are OTP and may be programmed to their opposite state one time during system configuration if needed. The volatile version of Configuration Register 3 allows the configuration to be changed during system operation or testing.

7.5.5.1 Configuration Register 3 Non-volatile (CR3NV)

Related Commands: Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 29 Configuration Register 3 Non-volatile (CR3NV)

Bits	Field name	Function	Type	Default state	Description
7	RFU	Reserved	OTP	0	Reserved for Future Use
6					
5	BC_NV	Blank Check			1 = Blank Check during erase enabled 0 = Blank Check disabled
4	02h_NV	Page Buffer Wrap			1 = Wrap at 512 bytes 0 = Wrap at 256 bytes
3	20h_NV	4 KB Erase			1 = 4 KB Erase disabled (Uniform Sector Architecture) 0 = 4 KB Erase enabled (Hybrid Sector Architecture)
2	30h_NV	Clear Status / Resume Select			1 = 30h is Erase or Program Resume command 0 = 30h is clear status command
1	RFU	Reserved			Reserved for Future Use
0	F0h_NV	Legacy Software Reset Enable			1 = F0h Software Reset is enabled 0 = F0h Software Reset is disabled (ignored)

Blank Check Non-volatile CR3NV[5]: This bit controls the POR, hardware reset, or software reset state of the blank check during erase feature.

02h Non-volatile CR3NV[4]: This bit controls the POR, hardware reset, or software reset state of the page programming buffer address wrap point.

20h Non-volatile CR3NV[3]: This bit controls the POR, hardware reset, or software reset state of the availability of 4-KB parameter sectors in the main flash array address map.

30h Non-volatile CR3NV[2]: This bit controls the POR, hardware reset, or software reset state of the 30h instruction code is used.

F0h Non-volatile CR3NV[0]: This bit controls the POR, hardware reset, or software reset state of the availability of the Infineon legacy FL-S family software reset instruction.

7.5.5.2 Configuration Register 3 Volatile (CR3V)

Related Commands: Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 30 Configuration Register 3 Volatile (CR3V)

Bits	Field name	Function	Type	Default state	Description
7 6	RFU	Reserved	Volatile	CR3NV	Reserved for Future Use
5	BC_V	Blank Check			1 = Blank Check during erase enabled 0 = Blank Check disabled
4	02h_V	Page Buffer Wrap			1 = Wrap at 512 bytes 0 = Wrap at 256 bytes
3	20h_V	4 KB Erase	Volatile, Read Only		1 = 4 KB Erase disabled (Uniform Sector architecture) 0 = 4 KB Erase enabled (Hybrid Sector architecture)
2	30h_V	Clear Status / Resume Select	Volatile		1 = 30h is Erase or Program Resume command 0 = 30h is clear status command
1	RFU	Reserved			Reserved for Future Use
0	F0h_V	Legacy Software Reset Enable			1= F0h Software Reset is enabled 0= F0h Software Reset is disabled (ignored)

Blank Check Volatile CR3V[5]: This bit controls the blank check during erase feature. When this feature is enabled an erase command first evaluates the erase status of the sector. If the sector is found to have not completed its last erase successfully, the sector is unconditionally erased. If the last erase was successful, the sector is read to determine if the sector is still erased (blank). The erase operation is started immediately after finding any programmed zero. If the sector is already blank (no programmed zero bit found) the remainder of the erase operation is skipped. This can dramatically reduce erase time when sectors being erased do not need the erase operation. When enabled the blank check feature is used within the parameter erase, sector erase, and bulk erase commands. When blank check is disabled an erase command unconditionally starts the erase operation.

02h Volatile CR3V[4]: This bit controls the page programming buffer address wrap point. Legacy SPI devices generally have used a 256-byte page programming buffer and defined that if data is loaded into the buffer beyond the 255-byte location, the address at which additional bytes are loaded would be wrapped to address zero of the buffer. The S25FS512S provides a 512-byte page programming buffer that can increase programming performance. For legacy software compatibility, this configuration bit provides the option to continue the wrapping behavior at the 256-byte boundary or to enable full use of the available 512-byte buffer by not wrapping the load address at the 256-byte boundary.

20h Volatile CR3V[3]: This bit controls the availability of 4-KB parameter sectors in the main flash array address map. The parameter sectors can overlay the highest or lowest 32-KB address range of the device or they can be removed from the address map so that all sectors are uniform size. This bit shall not be written to a value different than the value of CR3NV[3]. The value of CR3V[3] may only be changed by writing CR3NV[3].

30h Volatile CR3V[2]: This bit controls how the 30h instruction code is used. The instruction may be used as a clear status command or as an alternate program / erase resume command. This allows software compatibility with either Infineon legacy SPI devices or alternate vendor devices.

F0h Volatile CR3V[0]: This bit controls the availability of the Infineon legacy FL-S family software reset instruction. The S25FS512S supports the industry common 66h + 99h instruction sequence for software reset. This configuration bit allows the option to continue use of the legacy F0h single command for software reset.

7.5.6 Configuration Register 4

Configuration Register 4 controls the main flash array read commands burst wrap behavior. The burst wrap configuration does not affect commands reading from areas other than the main flash array e.g. read commands for registers or OTP array. The non-volatile version of the register provides the ability to set the start up (boot) state of the controls as the contents are copied to the volatile version of the register during the POR, hardware reset, or software reset. The volatile version of the register controls the feature behavior during normal operation. The register bits can be read and changed using the Read Any Register and Write Any Register commands. The volatile version of the register can also be written by the Set Burst Length (C0h) command.

7.5.6.1 Configuration Register 4 Non-volatile (CR4NV)

Related Commands: Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

Table 31 Configuration Register 4 Non-volatile (CR4NV)

Bits	Field name	Function	Type	Default state	Description
7	OI_O	Output Impedance	OTP	0	See **Table 32**
6					
5					
4	WE_O	Wrap Enable		1	0 = Wrap Enabled 1 = Wrap Disabled
3	RFU	Reserved		00	Reserved for Future Use
2	RFU	Reserved			
1	WL_O	Wrap Length			00 = 8-byte wrap 01 = 16-byte wrap 10 = 32-byte wrap 11 = 64-byte wrap
0					

Output Impedance Non-volatile CR4NV[7:5]: These bits control the POR, hardware reset, or software reset state of the IO signal output impedance (drive strength). Multiple drive strength are available to help match the output impedance with the system printed circuit board environment to minimize overshoot and ringing. These non-volatile output impedance configuration bits enable the device to start immediately (boot) with the appropriate drive strength.

Table 32 Output impedance control

CR4NV[7:5] impedance selection	Typical impedance to V_{SS} (Ω)	Typical impedance to V_{CC} (Ω)	Notes
000	47	45	Factory default
001	124	105	–
010	71	64	
011	47	45	
100	34	35	
101	26	28	
110	22	24	
111	18	21	

Wrap Enable Non-volatile CR4NV[4]: This bit controls the POR, hardware reset, or software reset state of the wrap enable. The commands affected by Wrap Enable are: Quad I/O Read, and DDR Quad I/O Read. This configuration bit enables the device to start immediately (boot) in wrapped burst read mode rather than the legacy sequential read mode.

Wrap Length Non-volatile CR4NV[1:0]: These bits controls the POR, hardware reset, or software reset state of the wrapped read length and alignment. These non-volatile configuration bits enable the device to start immediately (boot) in wrapped burst read mode rather than the legacy sequential read mode.

7.5.6.2 Configuration Register 4 Volatile (CR4V)

Related Commands: Read Any Register (RDAR 65h), Write Any Register (WRAR 71h), Set Burst Length (SBL C0h).

Table 33 Configuration Register 4 Volatile (CR4V)

Bits	Field name	Function	Type	Default state	Description
7	OI	Output Impedance	Volatile	CR4NV	See **Table 32**
6					
5					
4	WE	Wrap Enable			0 = Wrap Enabled 1 = Wrap Disabled
3	RFU	Reserved			Reserved for Future Use
2					
1	WL	Wrap Length			00 = 8-byte wrap 01 = 16-byte wrap 10 = 32-byte wrap 11 = 64-byte wrap
0					

Output Impedance CR2V[7:5]: These bits control the IO signal output impedance (drive strength). This volatile output impedance configuration bit enables the user to adjust the drive strength during normal operation.

Wrap Enable CR4V[4]: This bit controls the burst wrap feature. This volatile configuration bit enables the device to enter and exit burst wrapped read mode during normal operation.

Wrap Length CR4V[1:0]: These bits controls the wrapped read length and alignment during normal operation. These volatile configuration bits enable the user to adjust the burst wrapped read length during normal operation.

7.5.7 ECC Status Register (ECCSR)

Related Commands: ECC Read (ECCRD 18h or 19h). ECCSR does not have user programmable non-volatile bits, all defined bits are volatile read only status. The default state of these bits are set by hardware.

The status of ECC in each ECC unit is provided by the 8-bit ECC Status Register (ECCSR). The ECC Register Read command is written followed by an ECC unit address. The contents of the status register then indicates, for the selected ECC unit, whether there is an error in the ECC, the ECC unit data, or that ECC is disabled for that ECC unit.

Table 34 ECC Status Register (ECCSR)

Bits	Field name	Function	Type	Default state	Description
7 to 3	RFU	Reserved	Volatile, Read only	0	Reserved for Future Use
2	EECC	Error in ECC			1 = Single Bit Error found in the ECC unit error correction code 0 = No error
1	EECCD	Error in ECC unit data			1 = Single Bit Error corrected in ECC unit data 0 = No error
0	ECCDI	ECC Disabled			1 = ECC is disabled in the selected ECC unit 0 = ECC is enabled in the selected ECC unit

ECCSR[2] = 1 indicates an error was corrected in the ECC. ECCSR[1] = 1 indicates an error was corrected in the ECC unit data. ECCSR[0] = 1 indicates the ECC is disabled. The default state of “0” for all these bits indicates no failures and ECC is enabled.

The ECCSR[7:3] are reserved. These have undefined HIGH or LOW values that can change from one ECC status read to another. These bits should be treated as “don’t care” and ignored by any software reading status.

7.5.8 ASP Register (ASPR)

Related Commands: ASP Read (ASPRD 2Bh) and ASP Program (ASPP 2Fh), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

The ASP register is a 16-bit OTP memory location used to permanently configure the behavior of Advanced Sector Protection (ASP) features. ASPR does not have user programmable volatile bits, all defined bits are OTP.

The default state of the ASPR bits are programmed by Infineon.

Table 35 ASP Register (ASPR)

Bits	Field name	Function	Type	Default state	Description
15 to 9	RFU	Reserved	OTP	1	Reserved for Future Use
8					
7					
6					
5					
4					
3					
2	PWDMLB	Password Protection Mode Lock Bit			0 = Password Protection Mode permanently enabled 1 = Password Protection Mode not permanently enabled
1	PSTMLB				
0	RFU	Reserved	RFU		Reserved for Future Use

Password Protection Mode Lock Bit (PWDMLB) ASPR[2]: When programmed to 0, the Password Protection Mode is permanently selected.

Persistent Protection Mode Lock Bit (PSTMLB) ASPR[1]: When programmed to 0, the Persistent Protection Mode is permanently selected.

PWDMLB (ASPR[2]) and PSTMLB (ASPR[1]) are mutually exclusive, only one may be programmed to zero.

ASPR bits may only be programmed while ASPR[2:1] = 11b. Attempting to program ASPR bits when ASPR[2:1] is not = 11b will result in a programming error with P_ERR (SR1V[6]) set to '1'. After the ASP protection mode is selected by programming ASPR[2:1] = 10b or 01b, the state of all ASPR bits are locked and permanently protected from further programming. Attempting to program ASPR[2:1] = 00b will result in a programming error with P_ERR (SR1V[6]) set to '1'.

Similarly, OTP configuration bits listed in the ASP Register description (see **"ASP register"** on page 72), may only be programmed while ASPR[2:1] = 11b. The OTP configuration must be selected before selecting the ASP protection mode. The OTP configuration bits are permanently protected from further change when the ASP protection mode is selected. Attempting to program these OTP configuration bits when ASPR[2:1] is not = 11b will result in a programming error with P_ERR (SR1V[6]) set to '1'.

The ASP protection mode should be selected during system configuration to ensure that a malicious program does not select an undesired protection mode at a later time. By locking all the protection configuration via the ASP mode selection, later alteration of the protection methods by malicious programs is prevented.

7.5.9 Password Register (PASS)

Related Commands: Password Read (PASSRD E7h) and Password Program (PASSP E8h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h). The PASS register is a 64-bit OTP memory location used to permanently define a password for the Advanced Sector Protection (ASP) feature. PASS does not have user programmable volatile bits, all defined bits are OTP. A volatile copy of PASS is used to satisfy read latency requirements but the volatile register is not user writable or further described.

Table 36 Password Register (PASS)

Bits	Field name	Function	Type	Default state	Description
63 to 0	PWD	Hidden Password	OTP	FFFFFFFF-FFFFFFFFh	Non-volatile OTP storage of 64-bit password. The password is no longer readable after the password protection mode is selected by programming ASP register bit 2 to zero.

7.5.10 PPB Lock Register (PPBL)

Related Commands: PPB Lock Read (PLBRD A7h, PLBWR A6h), Read Any Register (RDAR 65h).

PPBL does not have separate user programmable non-volatile bits, all defined bits are volatile read only status. The default state of the RFU bits is set by hardware. The default state of the PPBLOCK bit is defined by the ASP protection mode bits in ASPR[2:1]. There is no non-volatile version of the PPBL register.

The PPBLOCK bit is used to protect the PPB bits. When PPBL[0] = 0, the PPB bits can not be programmed.

Table 37 PPB Lock Register (PPBL)

Bits	Field name	Function	Type	Default state	Description
7 to 1	RFU	Reserved	Volatile	00h	Reserved for Future Use
0	PPBLOCK	Protect PPB Array	Volatile Read Only	ASPR[2:1] = 1xb = Persistent Protection Mode = 1 ASPR[2:1] = 01b = Password Protection Mode = 0	0 = PPB array protected 1 = PPB array may be programmed or erased

7.5.11 PPB Access Register (PPBAR)

Related Commands: PPB Read (PPBRD FCh or 4PPBRD E2h), PPB Program (PPBP FDh or 4PPBP E3h), PPB Erase (PPBE E4h).

PPBAR does not have user writable volatile bits, all PPB array bits are non-volatile. The default state of the PPB array is erased to FFh by Infineon. There is no volatile version of the PPBAR register.

Table 38 PPB Access Register (PPBAR)

Bits	Field name	Function	Type	Default state	Description
7 to 0	PPB	Read or Program per sector PPB	Non-volatile	FFh	00h = PPB for the sector addressed by the PPBRD or PPBP command is programmed to 0, protecting that sector from program or erase operations. FFh = PPB for the sector addressed by the PPBRD command is 1, not protecting that sector from program or erase operations.

7.5.12 DYB Access Register (DYBAR)

Related Commands: DYB Read (DYBRD FAh or 4DYBRD E0h) and DYB Write (DYBWR FBh or 4DYBWR E1h).

DYBAR does not have user programmable non-volatile bits, all bits are a representation of the volatile bits in the DYB array. The default state of the DYB array bits is set by hardware. There is no non-volatile version of the DYBAR register.

Table 39 DYB Access Register (DYBAR)

Bits	Field name	Function	Type	Default state	Description
7 to 0	DYB	Read or Write per sector DYB	Volatile	FF	00h = DYB for the sector addressed by the DYBRD or DYBWR command is cleared to 0, protecting that sector from program or erase operations. FFh = DYB for the sector addressed by the DYBRD or DYBWR command is set to '1', not protecting that sector from program or erase operations.

7.5.13 SPI DDR Data Learning Registers

Related Commands: Program NVDLR (PNVDLR 43h), Write VDLR (WVDLR 4Ah), Data Learning Pattern Read (DLPRD 41h), Read Any Register (RDAR 65h), Write Any Register (WRAR 71h).

The Data Learning Pattern (DLP) resides in an 8-bit non-volatile Data Learning Register (NVDLR) as well as an 8-bit Volatile Data Learning Register (VDLR). When shipped from Infineon, the NVDLR value is 00h. Once programmed, the NVDLR cannot be reprogrammed or erased; a copy of the data pattern in the NVDLR will also be written to the VDLR. The VDLR can be written to at any time, but on power cycles the data pattern will revert back to what is in the NVDLR. During the learning phase described in the SPI DDR modes, the DLP will come from the VDLR. Each IO will output the same DLP value for every clock edge. For example, if the DLP is 34h (or binary 00110100) then during the first clock edge all IO's will output 0; subsequently, the 2nd clock edge all I/O's will output 0, the 3rd will output 1, etc.

When the VDLR value is 00h, no preamble data pattern is presented during the dummy phase in the DDR commands.

Table 40 Non-volatile Data Learning Register (NVDLR)

Bits	Field name	Function	Type	Default state	Description
7 to 0	NVDLP	Non-volatile Data Learning Pattern	OTP	00h	OTP value that may be transferred to the host during DDR read command latency (dummy) cycles to provide a training pattern to help the host more accurately center the data capture point in the received data bits.

Table 41 Volatile Data Learning Register (VDLR)

Bits	Field name	Function	Type	Default state	Description
7 to 0	VDLP	Volatile Data Learning Pattern	Volatile	Takes the value of NVDLR during POR or Reset	Volatile copy of the NVDLP used to enable and deliver the Data Learning Pattern (DLP) to the outputs. The VDLP may be changed by the host during system operation.

8 Data protection

8.1 Secure silicon region (OTP)

The device has a 1024-byte One Time Program (OTP) address space that is separate from the main flash array. The OTP area is divided into 32, individually lockable, 32-byte aligned and length regions.

The OTP memory space is intended for increased system security. OTP values can “mate” a flash component with the system CPU/ASIC to prevent device substitution. See **“OTP address space”** on page 49, **“OTP Program (OTPP 42h)”** on page 118, and **“OTP Read (OTPR 4Bh)”** on page 118.

8.1.1 Reading OTP memory space

The OTP Read command uses the same protocol as Fast Read. OTP Read operations outside the valid 1-KB OTP address range will yield indeterminate data.

8.1.2 Programming OTP memory space

The protocol of the OTP programming command is the same as Page Program. The OTP Program command can be issued multiple times to any given OTP address, but this address space can never be erased.

Automatic ECC is programmed on the first programming operation to each 16 byte region. Programming within a 16 byte region more than once disables the ECC. It is recommended to program each 16 byte portion of each 32 byte region once so that ECC remains enabled to provide the best data integrity.

The valid address range for OTP Program is depicted in **Figure 39**. OTP Program operations outside the valid OTP address range will be ignored, without P_ERR in SR1V set to ‘1’. OTP Program operations within the valid OTP address range, while FREEZE = 1, will fail with P_ERR in SR1V set to ‘1’. The OTP address space is not protected by the selection of an ASP protection mode. The Freeze bit (CR1V[0]) may be used to protect the OTP Address Space.

8.1.3 Infineon programmed random number

Infineon standard practice is to program the low order 16 bytes of the OTP memory space (locations 0x0 to 0xF) with a 128-bit random number using the Linear Congruential Random Number Method. The seed value for the algorithm is a random number concatenated with the day and time of tester insertion.

8.1.4 Lock bytes

The LSb of each Lock byte protects the lowest address region related to the byte, the MSb protects the highest address region related to the byte. The next higher address byte similarly protects the next higher eight regions. The LSb bit of the lowest address Lock Byte protects the higher address 16 bytes of the lowest address region. In other words, the LSb of location 0x10 protects all the Lock Bytes and RFU bytes in the lowest address region from further programming. See **“OTP address space”** on page 49.

8.1.5 Write Enable command

The Write Enable (WREN) command must be written prior to any command that modifies non-volatile data. The WREN command sets the Write Enable Latch (WEL) bit. The WEL bit is cleared to 0 (disables writes) during power-up, hardware reset, or after the device completes the following commands:

- Reset
- Page Program (PP or 4PP)
- Parameter 4-KB Erase (P4E or 4P4E)
- Sector Erase (SE or 4SE)
- Bulk Erase (BE)
- Write Disable (WRDI)
- Write Registers (WRR)
- Write Any Register (WRAR)
- OTP Byte Programming (OTPP)
- Advanced Sector Protection Register Program (ASPP)
- Persistent Protection Bit Program (PPBP)
- Persistent Protection Bit Erase (PPBE)
- Password Program (PASSP)
- Program Non-volatile Data Learning Register (PNVDLR)

8.2 Block protection

The Block Protect bits (Status Register bits BP2, BP1, BP0) in combination with the Configuration Register TBPROT_O bit can be used to protect an address range of the main flash array from program and erase operations. The size of the range is determined by the value of the BP bits and the upper or lower starting point of the range is selected by the TBPROT_O bit of the configuration register (CR1NV[5]).

Table 42 Upper array start of protection (TBPROT_O = 0)

Status Register content			Protected fraction of memory array	Protected memory (KB)
BP2	BP1	BP0		FS512S 512 Mb
0	0	0	None	0
		1	Upper 64th	1024
	1	0	Upper 32nd	2048
		1	Upper 16th	4096
1	0	0	Upper 8th	8192
		1	Upper 4th	16384
	1	0	Upper Half	32768
		1	All Sectors	65536

Table 43 Lower array start of protection (TBPROT_O = 1)

Status Register content			Protected fraction of memory array	Protected memory (KB)
BP2	BP1	BP0		FS512S 512 Mb
0	0	0	None	0
		1	Lower 64th	1024
	1	0	Lower 32nd	2048
		1	Lower 16th	4096
1	0	0	Lower 8th	8192
		1	Lower 4th	16384
	1	0	Lower Half	32768
		1	All Sectors	65536

When Block Protection is enabled (i.e., any BP2-0 are set to '1'), Advanced Sector Protection (ASP) can still be used to protect sectors not protected by the Block Protection scheme. In the case that both ASP and Block Protection are used on the same sector the logical OR of ASP and Block Protection related to the sector is used.

8.2.1 Freeze bit

Bit 0 of Configuration Register 1 (CR1V[0]) is the FREEZE bit. The Freeze Bit, when set to '1', locks the current state of the Block Protection control bits and OTP area until the next power off-on cycle. Additional details in **"Configuration Register 1 Volatile (CR1V)"** on page 56

8.2.2 Write Protect signal

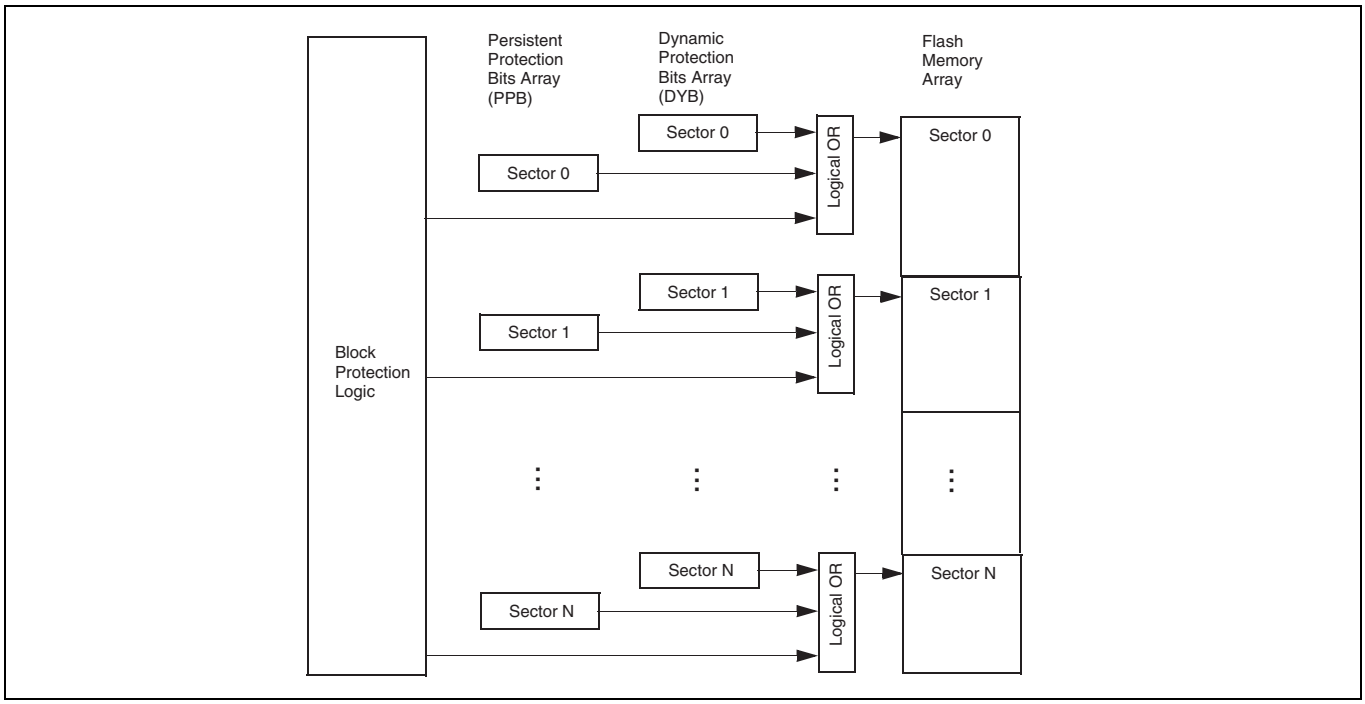
The Write Protect (WP#) input in combination with the Status Register Write Disable (SRWD) bit (SR1NV[7]) provide hardware input signal controlled protection. When WP# is Low and SRWD is set to '1' Status Register-1 (SR1NV and SR1V) and Configuration Register 1 (CR1NV and CR1V) are protected from alteration. This prevents disabling or changing the protection defined by the Block Protect bits (see **Table 22**).

8.2.3 Advanced sector protection

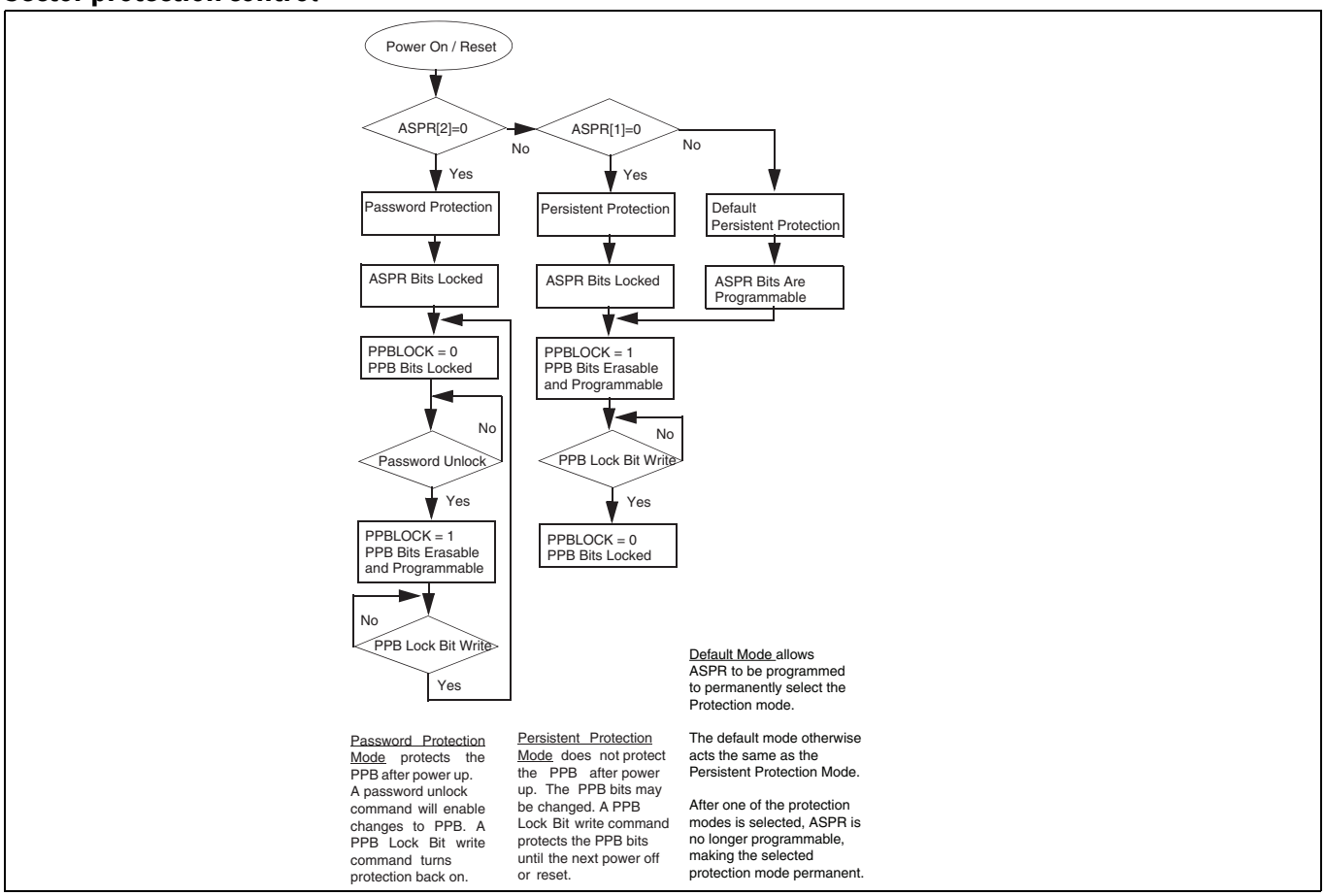
Advanced sector protection (ASP) is the name used for a set of independent hardware and software methods used to disable or enable programming or erase operations, individually, in any or all sectors.

Every main flash array sector has a non-volatile Persistent Protection Bit (PPB) and a volatile Dynamic Protection Bit (DYB) associated with it. When either bit is 0, the sector is protected from program and erase operations. The PPB bits are protected from program and erase when the volatile PPB Lock bit is 0. There are two methods for managing the state of the PPB Lock bit: Password Protection, and Persistent Protection. An overview of these methods is shown in **Figure 41**.

Block Protection and ASP protection settings for each sector are logically ORed to define the protection for each sector i.e. if either mechanism is protecting a sector the sector cannot be programmed or erased. Refer to **"Block protection"** on page 69 for full details of the BP2-0 bits.



Sector protection control



Advanced sector protection overview The Persistent Protection method sets the PPB Lock bit to 1 during POR, or Hardware Reset so that the PPB bits are unprotected by a device reset. There is a command to clear the PPB Lock bit to 0 to protect the PPB. There is no command in the Persistent Protection method to set the PPB Lock bit to 1, therefore the PPB Lock bit will remain at 0 until the next power-off or hardware reset. The Persistent

Protection method allows boot code the option of changing sector protection by programming or erasing the PPB, then protecting the PPB from further change for the remainder of normal system operation by clearing the PPB Lock bit to 0. This is sometimes called Boot-code controlled sector protection.

The Password method clears the PPB Lock bit to 0 during POR, or Hardware Reset to protect the PPB. A 64-bit password may be permanently programmed and hidden for the password method. A command can be used to provide a password for comparison with the hidden password. If the password matches, the PPB Lock bit is set to '1' to unprotect the PPB. A command can be used to clear the PPB Lock bit to 0. This method requires use of a password to control PPB protection.

The selection of the PPB Lock bit management method is made by programming OTP bits in the ASP Register so as to permanently select the method used.

8.2.4 ASP register

The ASP register is used to permanently configure the behavior of Advanced Sector Protection (ASP) features (see **Table 35**).

As shipped from the factory, all devices default ASP to the Persistent Protection mode, with all sectors unprotected, when power is applied. The device programmer or host system must then choose which sector protection method to use. Programming either of the, one-time programmable, Protection Mode Lock Bits, locks the part permanently in the selected mode:

- ASPR[2:1] = 11 = No ASP mode selected, Persistent Protection Mode is the default.
- ASPR[2:1] = 10 = Persistent Protection Mode permanently selected.
- ASPR[2:1] = 01 = Password Protection Mode permanently selected.
- ASPR[2:1] = 00 is an Illegal condition, attempting to program more than one bit to zero results in a programming failure.

ASP register programming rules:

- If the password mode is chosen, the password must be programmed prior to setting the Protection Mode Lock Bits.
- Once the Protection Mode is selected, the following OTP configuration register bits are permanently protected from programming and no further changes to the OTP register bits is allowed:
  - CR1NV[5:2]
  - CR2NV
  - CR3NV
  - CR4NV
  - ASPR
  - PASS
  - NVDLR
  - If an attempt to change any of the registers above, after the ASP mode is selected, the operation will fail and P_ERR (SR1V[6]) will be set to '1'.

The programming time of the ASP Register is the same as the typical page programming time. The system can determine the status of the ASP register programming operation by reading the WIP bit in the Status Register. See **Table 21** for information on WIP. See **"Sector protection states summary"** on page 73.

8.2.5 Persistent Protection bits

The Persistent Protection Bits (PPB) are located in a separate non-volatile flash array. One of the PPB bits is related to each sector. When a PPB is 0, its related sector is protected from program and erase operations. The PPB are programmed individually but must be erased as a group, similar to the way individual words may be programmed in the main array but an entire sector must be erased at the same time. The PPB have the same program and erase endurance as the main flash memory array. Preprogramming and verification prior to erasure are handled by the device.

Programming a PPB bit requires the typical page programming time. Erasing all the PPBs requires typical sector erase time. During PPB bit programming and PPB bit erasing, status is available by reading the Status register. Reading of a PPB bit requires the initial access time of the device.

Notes

- Each PPB is individually programmed to 0 and all are erased to 1 in parallel.
- If the PPB Lock bit is 0, the PPB Program or PPB Erase command does not execute and fails without programming or erasing the PPB.
- The state of the PPB for a given sector can be verified by using the PPB Read command.

8.2.6 Dynamic Protection bits

Dynamic Protection Bits are volatile and unique for each sector and can be individually modified. DYB only control the protection for sectors that have their PPB set to '1'. By issuing the DYB Write command, a DYB is cleared to 0 or set to '1', thus placing each sector in the protected or unprotected state respectively. This feature allows software to easily protect sectors against inadvertent changes, yet does not prevent the easy removal of protection when changes are needed. The DYBs can be set or cleared as often as needed as they are volatile bits.

8.2.7 PPB Lock Bit (PPBL[0])

The PPB Lock Bit is a volatile bit for protecting all PPB bits. When cleared to 0, it locks all PPBs, when set to '1', it allows the PPBs to be changed. See **"PPB Lock Register (PPBL)"** on page 66 for more information.

The PLBWR command is used to clear the PPB Lock bit to 0. The PPB Lock Bit must be cleared to 0 only after all the PPBs are configured to the desired settings.

In Persistent Protection mode, the PPB Lock is set to '1' during POR or a hardware reset. When cleared to 0, no software command sequence can set the PPB Lock bit to 1, only another hardware reset or power-up can set the PPB Lock bit.

In the Password Protection mode, the PPB Lock bit is cleared to 0 during POR or a hardware reset. The PPB Lock bit can only be set to '1' by the Password Unlock command.

8.2.8 Sector protection states summary

Each sector can be in one of the following protection states:

- Unlocked — The sector is unprotected and protection can be changed by a simple command. The protection state defaults to unprotected when the device is shipped from Infineon.
- Dynamically locked — A sector is protected and protection can be changed by a simple command. The protection state is not saved across a power cycle or reset.
- Persistently locked — A sector is protected and protection can only be changed if the PPB Lock Bit is set to '1'. The protection state is non-volatile and saved across a power cycle or reset. Changing the protection state requires programming and or erase of the PPB bits.

Table 44 Sector protection states

Protection bit values			Sector state
PPB lock	PPB	DYB	
1	1	1	Unprotected – PPB and DYB are changeable
		0	Protected – PPB and DYB are changeable
	0	1	
		0	
0	1	1	Unprotected – PPB not changeable, DYB is changeable
		0	Protected – PPB not changeable, DYB is changeable
	0	1	
		0	

8.2.9 Persistent protection mode

The Persistent Protection method sets the PPB Lock bit to 1 during POR or Hardware Reset so that the PPB bits are unprotected by a device hardware reset. Software reset does not affect the PPB Lock bit. The PLBWR command can clear the PPB Lock bit to ‘0’ to protect the PPB. There is no command to set the PPB Lock bit therefore the PPB Lock bit will remain at ‘0’ until the next power-off or hardware reset.

8.2.10 Password protection mode

Password Protection Mode allows an even higher level of security than the Persistent Sector Protection Mode, by requiring a 64-bit password for unlocking the PPB Lock bit. In addition to this password requirement, after power up and hardware reset, the PPB Lock bit is cleared to ‘0’ to ensure protection at power-up. Successful execution of the Password Unlock command by entering the entire password sets the PPB Lock bit to ‘1’, allowing for sector PPB modifications.

Password protection notes:

- Once the Password is programmed and verified, the Password Mode (ASPR[2] = 0) must be set in order to prevent reading the password.
- The Password Program Command is only capable of programming 0s. Programming a ‘1’ after a cell is programmed as a ‘0’ results in the cell left as a ‘0’ with no programming error set.
- The password is all 1s when shipped from Infineon. It is located in its own memory space and is accessible through the use of the Password Program, Password Read, RDAR, and WRAR commands.
- All 64-bit password combinations are valid as a password.
- The Password Mode, once programmed, prevents reading the 64-bit password and further password programming. All further program and read commands to the password region are disabled and these commands are ignored or return undefined data. There is no means to verify what the password is after the Password Mode Lock Bit is selected. Password verification is only allowed before selecting the Password Protection mode.
- The Protection Mode Lock Bits are not erasable.
- The exact password must be entered in order for the unlocking function to occur. If the password unlock command provided password does not match the hidden internal password, the unlock operation fails in the same manner as a programming operation on a protected sector. The P_ERR bit is set to ’1’, the WIP Bit remains set, and the PPB Lock bit remains cleared to ‘0’.

- The Password Unlock command cannot be accepted any faster than once every 100 µs ± 20 µs. This makes it take an unreasonably long time (58 million years) for a hacker to run through all the 64-bit combinations in an attempt to correctly match a password. The Read Status Register 1 command may be used to read the WIP bit to determine when the device has completed the password unlock command or is ready to accept a new password command. When a valid password is provided the password unlock command does not insert the 100 µs delay before returning the WIP bit to zero.
- If the password is lost after selecting the Password mode, there is no way to set the PPB Lock bit.
- ECC status may only be read from sectors that are readable. In read protection mode the addresses are forced to the boot sector address. ECC status is only in that sector while read protection mode is ACTIVE.

8.3 Recommended protection process

During system manufacture, the flash device configuration should be defined by:

- Programming the OTP configuration bits in CR1NV[5, 3:2], CR2NV, CR3NV, and CR4NV as desired.
- Program the Secure Silicon Region (OTP area) as desired
- Program the PPB bits as desired via the PPBP commandProgram the NVDLR if it will be used in DDR read commands
- Program the Password register (PASS) if password protection will be used
- Program the ASP Register as desired, including the selection of the persistent or password ASP protection mode in ASPR[2:1]. It is very important to explicitly select a protection mode so that later accidental or malicious programming of the ASP register and OTP configuration is prevented. This is to ensure that only the intended OTP protection and configuration features are enabled.

During system power up and boot code execution:

- Trusted boot code can determine whether there is any need to program additional SSR (OTP area) information. If no SSR changes are needed the FREEZE bit (CR1V[0]) can be set to ‘1’ to protect the SSR from changes during the remainder of normal system operation while power remains ON.
- If the persistent protection mode is in use, trusted boot code can determine whether there is any need to modify the persistent (PPB) sector protection via the PPBP or PPBE commands. If no PPB changes are needed the PPBLOCK bit can be cleared to 0 via the PPBL to protect the PPB bits from changes during the remainder of normal system operation while power remains ON.

The dynamic (DYB) sector protection bits can be written as desired via the DYBAR.

9 Commands

All communication between the host system and S25FS512S memory devices is in the form of units called commands.

All commands begin with an instruction that selects the type of information transfer or device operation to be performed. Commands may also have an address, instruction modifier, latency period, data transfer to the memory, or data transfer from the memory. All instruction, address, and data information is transferred sequentially between the host system and memory device.

Command protocols are also classified by a numerical nomenclature using three numbers to reference the transfer width of three command phases:

- instruction
- address and instruction modifier (mode)
- data

Single bit wide commands start with an instruction and may provide an address or data, all sent only on the SI signal. Data may be sent back to the host serially on the SO signal. This is referenced as a 1-1-1 command protocol for single bit width instruction, single bit width address and modifier, single bit data.

Dual or Quad Input / Output (I/O) commands provide an address sent from the host as bit pairs on IO0 and IO1 or, four-bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as bit pairs on IO0 and IO1 or, four-bit (nibble) groups on IO0, IO1, IO2, and IO3. This is referenced as 1-2-2 for Dual I/O and 1-4-4 for Quad I/O command protocols.

The S25FS512S also supports a QPI mode in which all information is transferred in 4-bit width, including the instruction, address, modifier, and data. This is referenced as a 4-4-4 command protocol.

Commands are structured as follows:

- Each command begins with an eight bit (byte) instruction. However, some read commands are modified by a prior read command, such that the instruction is implied from the earlier command. This is called Continuous Read Mode. When the device is in continuous read mode, the instruction bits are not transmitted at the beginning of the command because the instruction is the same as the Read command that initiated the Continuous Read mode. In Continuous Read mode the command will begin with the read address. Thus, Continuous Read mode removes eight instruction bits from each read command in a series of same type read commands.
- The instruction may be standalone or may be followed by address bits to select a location within one of several address spaces in the device. The address may be either a 24-bit or 32-bit, byte boundary, address.
- The Serial Peripheral Interface with multiple IO provides the option for each transfer of address and data information to be done one, two, or four bits in parallel. This enables a trade off between the number of signal connections (IO bus width) and the speed of information transfer. If the host system can support a two or four bit wide IO bus the memory performance can be increased by using the instructions that provide parallel two bit (dual) or parallel four bit (quad) transfers.
- In legacy SPI multiple IO mode, the width of all transfers following the instruction are determined by the instruction sent. Following transfers may continue to be single bit serial on only the SI or Serial Output (SO) signals, they may be done in two bit groups per (dual) transfer on the IO0 and IO1 signals, or they may be done in 4-bit groups per (quad) transfer on the IO0-IO3 signals. Within the dual or quad groups the least significant bit is on IO0. More significant bits are placed in significance order on each higher numbered IO signal. Single bits or parallel bit groups are transferred in most to least significant bit order.
- In QPI mode, the width of all transfers, including instructions, is a 4-bit wide (quad) transfer on the IO0-IO3 signals.
- Dual I/O and Quad I/O read instructions send an instruction modifier called mode bits, following the address, to indicate that the next command will be of the same type with an implied, rather than an explicit, instruction. The next command thus does not provide an instruction byte, only a new address and mode bits. This reduces the time needed to send each command when the same command type is repeated in a sequence of commands.

- The address or mode bits may be followed by write data to be stored in the memory device or by a read latency period before read data is returned to the host.
- Read latency may be zero to several SCK cycles (also referred to as dummy cycles).
- All instruction, address, mode, and data information is transferred in byte granularity. Addresses are shifted into the device with the most significant byte first. All data is transferred with the lowest address byte sent first. Following bytes of data are sent in lowest to highest byte address order i.e. the byte address increments.
- All attempts to read the flash memory array during a program, erase, or a write cycle (embedded operations) are ignored. The embedded operation will continue to execute without any affect. A very limited set of commands are accepted during an embedded operation. These are discussed in the individual command descriptions. While a program, erase, or write operation is in progress, it is recommended to check that the Write-In Progress (WIP) bit is 0 before issuing most commands to the device, to ensure the new command can be accepted.
- Depending on the command, the time for execution varies. A command to read status information from an executing command is available to determine when the command completes execution and whether the command was successful.
- Although the host software in some cases is used to directly control the SPI interface signals, the hardware interfaces of the host system and the memory device generally handle the details of signal relationships and timing. For this reason, signal relationships and timing are not covered in detail within this software interface focused section of the document. Instead, the focus is on the logical sequence of bits transferred in each command rather than the signal timing and relationships. Following are some general signal relationship descriptions to keep in mind. For additional information on the bit level format and signal timing relationships of commands, see **“Command protocol”** on page 21.
  - The host always controls the Chip Select (CS#), Serial Clock (SCK), and Serial Input (SI) – SI for single bit wide transfers. The memory drives Serial Output (SO) for single bit read transfers. The host and memory alternately drive the IO0-IO3 signals during Dual and Quad transfers.
  - All commands begin with the host selecting the memory by driving CS# LOW before the first rising edge of SCK. CS# is kept LOW throughout a command and when CS# is returned HIGH the command ends. Generally, CS# remains LOW for eight bit transfer multiples to transfer byte granularity information. Some commands will not be accepted if CS# is returned HIGH not at an 8-bit boundary.

9.1 Command set summary

9.1.1 Extended addressing

To accommodate addressing above 128 Mb, there are two options:

1. Instructions that always require a 4-byte address, used to access up to 32 Gb of memory.

Command name	Function	Instruction (hex)
4READ	Read	13
4FAST_READ	Read Fast	0C
4DIOR	Dual I/O Read	BC
4QIOR	Quad I/O Read	EC
4DDRQIOR	DDR Quad I/O Read	EE
4PP	Page Program	12
4P4E	Parameter 4-KB Erase	21
4SE	Erase 64 / 256 KB	DC
4ECCRD	ECC Status Read	18
4DYBRD	DYB Read	E0
4DYBWR	DYBWR	E1
4PPBRD	PPB Read	E2
4PPBP	PPB Program	E3

2. A 4-byte address mode for backward compatibility to the 3-byte address instructions. The standard 3-byte instructions can be used in conjunction with a 4-byte address mode controlled by the address length configuration bit (CR2V[7]). The default value of CR2V[7] is loaded from CR2NV[7] (following power up, hardware reset, or software reset), to enable default 3-byte (24-bit) or 4-byte (32 bit) addressing. When the address length (CR2V[7]) set to '1', the legacy commands are changed to require 4 bytes (32-bits) for the address field. The following instructions can be used in conjunction with the 4-byte address mode configuration to switch from 3 bytes to 4 bytes of address field.

Command name	Function	Instruction (hex)
READ	Read	03
FAST_READ	Read Fast	0B
DIOR	Dual I/O Read	BB
QIOR	Quad I/O Read	EB
DDRQIOR	DDR Quad I/O Read)	ED
PP	Page Program	02
P4E	Parameter 4 KB Erase	20
SE	Erase 256 KB	D8
RDAR	Read Any Register	65
WRAR	Write Any Register	71
EES	Evaluate Erase Status	D0
OTPP	OTP Program	42
OTPR	OTP Read	4B
ECCRD	ECC Status Read	19
DYBRD	DYB Read	FA
DYBWR	DYBWR	FB
PPBRD	PPB Read	FC
PPBP	PPB Program	FD

9.1.2 Command summary by function

Table 45 S25FS512S command set (Sorted by function)

Function	Command name	Command description	Instruction value (hex)	Maximum frequency (MHz)	Address length (bytes)	QPI
Read Device ID	RDID	Read ID (JEDEC Manufacturer ID and JEDEC CFI)	9F	133	0	Yes
	RSFDP	Read JEDEC Serial Flash Discoverable Parameters	5A	50	3	
	RDQID	Read Quad ID	AF	133	0	
Register Access	RDSR1	Read Status Register 1	05	133	0	
	RDSR2	Read Status Register 2	07	133	0	No
	RDCR	Read Configuration Register 1	35	133	0	
	RDAR	Read Any Register	65	133	3 or 4	Yes
	WRR	Write Register (Status 1, Configuration 1)	01	133	0	
	WRDI	Write Disable	04	133	0	
	WREN	Write Enable	06	133	0	
	WRAR	Write Any Register	71	133	3 or 4	
	CLSR	Clear Status Register 1 — Erase / Program Fail Reset This command may be disabled and the instruction value instead used for a program / erase resume command - See **"Configuration Register 3"** on page 61.	30	133	0	
	CLSR	Clear Status Register 1 (Alternate instruction) — Erase / Program Fail Reset	82	133	0	
	4BAM	Enter 4-byte Address Mode	B7	133	0	No
	SBL	Set Burst Length	C0	133	0	
	EES	Evaluate Erase Status	D0	133	3 or 4	Yes
	ECCRD	ECC Read	19	133	3 or 4	
	4ECCRD		18	133	4	
	DLPRD	Data Learning Pattern Read	41	133	0	No
	PNVDLR	Program NV Data Learning Register	43	133	0	
	WVDLR	Write Volatile Data Learning Register	4A	133	0	
Read Flash Array	READ	Read	03	50	3 or 4	
	4READ		13	50	4	
	FAST_READ	Fast Read	0B	133	3 or 4	
	4FAST_READ		0C	133	4	
	DIOR	Dual I/O Read	BB	133	3 or 4	
	4DIOR		BC	133	4	
	QIOR	Quad I/O Read	EB	133	3 or 4	Yes
	4QIOR		EC	133	4	
	DDRQIOR	DDR Quad I/O Read	ED	80	3 or 4	
	4DDRQIOR		EE	80	4	

Note
45. Commands not supported in QPI mode have undefined behavior if sent when the device is in QPI mode.

Table 45 S25FS512S command set (Sorted by function) *(continued)*

Function	Command name	Command description	Instruction value (hex)	Maximum frequency (MHz)	Address length (bytes)	QPI
Program Flash Array	PP	Page Program	02	133	3 or 4	Yes
	4PP		12		4	
Erase Flash Array	P4E	Parameter 4 KB-Sector Erase	20		3 or 4	
	4P4E		21		4	
	SE	Erase 256 KB	D8		3 or 4	
	4SE		DC		4	
	BE	Bulk Erase	60		0	
	BE	Bulk Erase (alternate instruction)	C7			
Erase /Program Suspend /Resume	EPS	Erase / Program Suspend	75			
	EPS	Erase / Program Suspend (alternate instruction)	85			
	EPS		B0			
	EPR	Erase / Program Resume	7A			
	EPR	Erase / Program Resume (alternate instruction)	8A			
	EPR	Erase / Program Resume (alternate instruction This command may be disabled and the instruction value instead used for a clear status command — See **"Configuration Register 3"** on page 61.	30			
One Time Program Array	OTPP	OTP Program	42		3 or 4	No
	OTPR	OTP Read	4B			
Advanced Sector Protection	DYBRD	DYB Read	FA			Yes
	4DYBRD		E0		4	
	DYBWR	DYB Write	FB		3 or 4	
	4DYBWR		E1		4	
	PPBRD	PPB Read	FC		3 or 4	No
	4PPBRD		E2		4	
	PPBP	PPB Program	FD		3 or 4	
	4PPBP		E3		4	
	PPBE	PPB Erase	E4		0	
	ASPRD	ASP Read	2B			
	ASPP	ASP Program	2F			
	PLBRD	PPB Lock Bit Read	A7			
	PLBWR	PPB Lock Bit Write	A6			
	PASSRD	Password Read	E7			
	PASSP	Password Program	E8			
	PASSU	Password Unlock	E9			

Note
45. Commands not supported in QPI mode have undefined behavior if sent when the device is in QPI mode.

Table 45 S25FS512S command set (Sorted by function) *(continued)*

Function	Command name	Command description	Instruction value (hex)	Maximum frequency (MHz)	Address length (bytes)	QPI
Reset	RSTEN	Software Reset Enable	66	133	0	Yes
	RST	Software Reset	99			
	RESET	Legacy Software Reset	F0			No
	MBR	Mode Bit Reset	FF			Yes
DPD	DPD	Enter Deep Power-Down Mode	B9			
	RES	Release from Deep Power-Down Mode	AB			

Note
45. Commands not supported in QPI mode have undefined behavior if sent when the device is in QPI mode.

9.1.3 Read device identification

There are multiple commands to read information about the device manufacturer, device type, and device features. SPI memories from different vendors have used different commands and formats for reading information about the memories. The S25FS512S supports the three device information commands.

9.1.4 Register read or write

There are multiple registers for reporting embedded operation status or controlling device configuration options. There are commands for reading or writing these registers. Registers contain both volatile and non-volatile bits. Non-volatile bits in registers are automatically erased and programmed as a single (write) operation.

9.1.4.1 Monitoring operation status

The host system can determine when a write, program, erase, suspend or other embedded operation is complete by monitoring the Write in Progress (WIP) bit in the Status Register. The Read from Status Register 1 command or Read Any Register command provides the state of the WIP bit. The program error (P_ERR) and erase error (E_ERR) bits in the status register indicate whether the most recent program or erase command has not completed successfully. When P_ERR or E_ERR bits are set to one, the WIP bit will remain set to one indicating the device remains busy and unable to receive most new operation commands. Only status read (RDSR1 05h), Read Any Register (RDAR 65h), status clear (CLSR 30h or 82h), and software reset (RSTEN 66h, RST 99h or RESET F0h) are valid commands when P_ERR or E_ERR is set to ‘1’. A Clear Status Register (CLSR) followed by a Write Disable (WRDI) command must be sent to return the device to standby state. Clear Status Register clears the WIP, P_ERR, and E_ERR bits. WRDI clears the WEL bit. Alternatively, Hardware Reset, or Software Reset (RST or RESET) may be used to return the device to standby state.

9.1.4.2 Configuration

There are commands to read, write, and protect registers that control interface path width, interface timing, interface address length, and some aspects of data protection.

9.1.5 Read flash array

Data may be read from the memory starting at any byte boundary. Data bytes are sequentially read from incrementally higher byte addresses until the host ends the data transfer by driving CS# input HIGH. If the byte address reaches the maximum address of the memory array, the read will continue at address zero of the array.

There are several different read commands to specify different access latency and data path widths. Double Data Rate (DDR) commands also define the address and data bit relationship to both SCK edges:

- The Read command provides a single address bit per SCK rising edge on the SI signal with read data returning a single bit per SCK falling edge on the SO signal. This command has zero latency between the address and the returning data but is limited to a maximum SCK rate of 50 MHz.
- Other read commands have a latency period between the address and returning data but can operate at higher SCK frequencies. The latency depends on a configuration register read latency value.
- The Fast Read command provides a single address bit per SCK rising edge on the SI signal with read data returning a single bit per SCK falling edge on the SO signal.
- Dual or Quad I/O Read commands provide address two bits or four bits per SCK rising edge with read data returning two bits, or four bits of data per SCK falling edge on the IO0-IO3 signals.
- Quad Double Data Rate read commands provide address four bits per every SCK edge with read data returning four bits of data per every SCK edge on the IO0-IO3 signals.

9.1.6 Program flash array

Programming data requires two commands: Write Enable (WREN), and Page Program (PP).

The Page Program command accepts from 1 byte up to 256 or 512 consecutive bytes of data (page) to be programmed in one operation. Programming means that bits can either be left at 1, or programmed from 1 to 0. Changing bits from 0 to 1 requires an erase operation.

(There is no content about Write Enable command, please add it)

9.1.7 Erase flash array

The Parameter Sector Erase, Sector Erase, or Bulk Erase commands set all the bits in a sector or the entire memory array to ‘1’. A bit needs to be first erased to 1 before programming can change it to ‘0’. While bits can be individually programmed from a ‘1’ to ‘0’, erasing bits from 0 to 1 must be done on a sector-wide or array-wide (bulk) level. The Write Enable (WREN) command must precede an erase command.

9.1.8 One time Programmable (OTP), block protection, and advanced sector protection

There are commands to read and program a separate OTP array for permanent data such as a serial number. There are commands to control a contiguous group (block) of flash memory array sectors that are protected from program and erase operations.There are commands to control which individual flash memory array sectors are protected from program and erase operations.

9.1.9 Reset

There are commands to reset to the default conditions present after power on to the device. However, the software reset commands do not affect the current state of the FREEZE or PPB Lock bits. In all other respects a software reset is the same as a hardware reset.

There is a command to reset (exit from) the Continuous Read Mode.

9.1.10 Deep Power-down (DPD)

A DPD mode is supported by the S25FS512S devices. If the device has been placed in DPD mode by the DPD (B9h) command, the interface standby current is (I_{DPD}). The DPD command is accepted only while the device is not performing an embedded algorithm as indicated by the Status Register-1 volatile Write In Progress (WIP) bit being

cleared to zero (SR1V[0] = 0). While in DPD mode the device ignores all commands except the release from DPD (RES ABh) command, that will return the device to the Interface Standby state after a delay of t_{RES}.

9.1.11 Reserved

Some instructions are reserved for future use. In this generation of the S25FS512S some of these command instructions may be unused and not affect device operation, some may have undefined results.

Some commands are reserved to ensure that a legacy or alternate source device command is allowed without effect. This allows legacy software to issue some commands that are not relevant for the current generation S25FS512S with the assurance these commands do not cause some unexpected action.

Some commands are reserved for use in special versions of the FS-S not addressed by this document or for a future generation. This allows new host memory controller designs to plan the flexibility to issue these command instructions. The command format is defined if known at the time this document revision is published.

9.2 Identification commands

9.2.1 Read Identification (RDID 9Fh)

The Read Identification (RDID) command provides read access to manufacturer identification, device identification, and Common Flash Interface (CFI) information. The manufacturer identification is assigned by JEDEC. The CFI structure is defined by JEDEC standard. The device identification and CFI values are assigned by Infineon.

The JEDEC Common Flash Interface (CFI) specification defines a device information structure, which allows a vendor-specified software flash management program (driver) to be used for entire families of flash devices. Software support can then be device-independent, JEDEC manufacturer ID independent, forward and backward-compatible for the specified flash device families. System vendors can standardize their flash drivers for long-term software compatibility by using the CFI values to configure a family driver from the CFI information of the device in use.

Any RDID command issued while a program, erase, or write cycle is in progress is ignored and has no effect on execution of the program, erase, or write cycle that is in progress.

The RDID instruction is shifted on SI. After the last bit of the RDID instruction is shifted into the device, a byte of manufacturer identification, two bytes of device identification, extended device identification, and CFI information will be shifted sequentially out on SO. As a whole this information is referred to as ID-CFI. See **"Device ID and common flash interface (ID-CFI) address map"** on page 136 for the detail description of the ID-CFI contents.

Continued shifting of output beyond the end of the defined ID-CFI address space will provide undefined data. The RDID command sequence is terminated by driving CS# to the logic HIGH state anytime during data output.

The maximum clock frequency for the RDID command is 133 MHz.

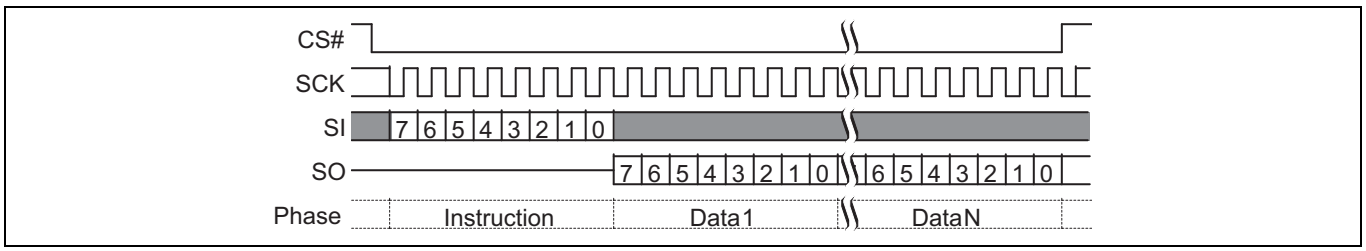


Figure 40 Read Identification (RDID) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0-IO3 and the returning data is shifted out on IO0-IO3.

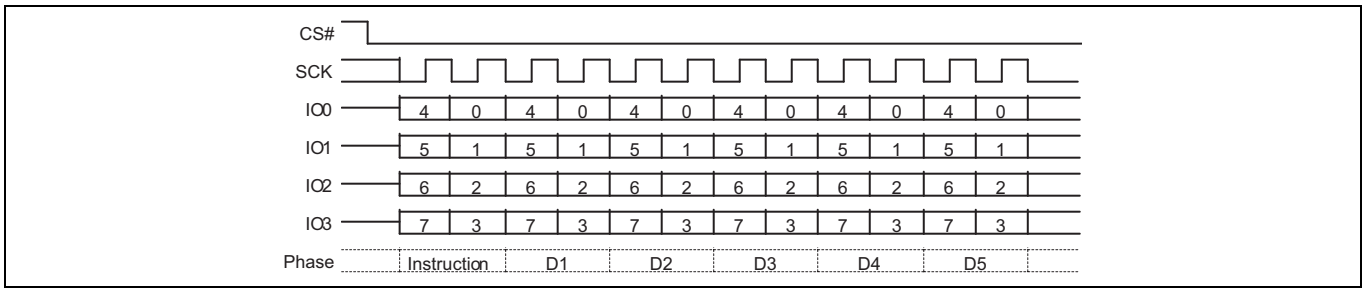


Figure 41 Read Identification (RDID) QPI mode command

9.2.2 Read Quad Identification (RDQID AFh)

The Read Quad Identification (RDQID) command provides read access to manufacturer identification, device identification, and Common Flash Interface (CFI) information. This command is an alternate way of reading the same information provided by the RDID command while in QPI mode. In all other respects the command behaves the same as the RDID command.

The command is recognized only when the device is in QPI Mode (CR2V[6] = 1). The instruction is shifted to IO0-IO3. After the last bit of the instruction is shifted into the device, a byte of manufacturer identification, two bytes of device identification, extended device identification, and CFI information will be shifted sequentially out on IO0-IO3. As a whole this information is referred to as ID-CFI. See **"Device ID and common flash interface (ID-CFI) address map"** on page 136 for the detail description of the ID-CFI contents.

Continued shifting of output beyond the end of the defined ID-CFI address space will provide undefined data. The command sequence is terminated by driving CS# to the logic HIGH state anytime during data output.

The maximum clock frequency for the command is 133 MHz.

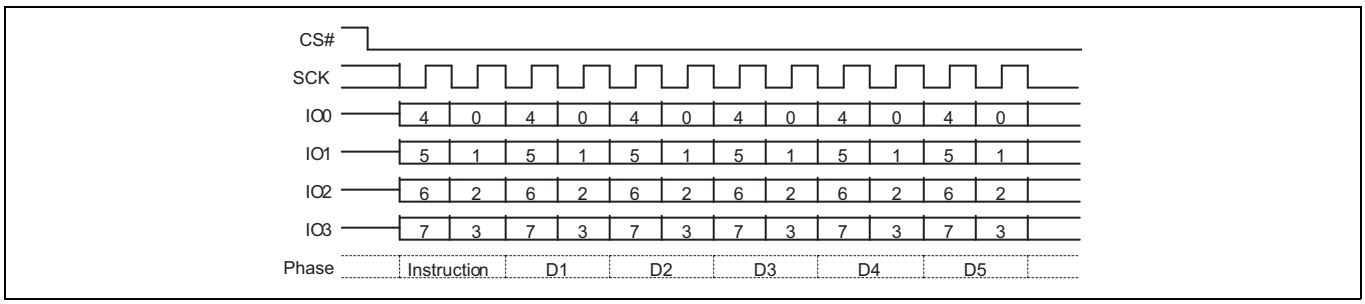


Figure 42 Read Quad Identification (RDQID) command sequence

9.2.3 Read serial flash discoverable parameters (RSFDP 5Ah)

The command is initiated by shifting on SI the instruction code ‘5Ah’, followed by a 24-bit address of 000000h, followed by 8 dummy cycles. The SFDP bytes are then shifted out on SO starting at the falling edge of SCK after the dummy cycles. The SFDP bytes are always shifted out with the MSb first. If the 24-bit address is set to any other value, the selected location in the SFDP space is the starting point of the data read. This enables random access to any parameter in the SFDP space. The RSFDP command is supported up to 50 MHz.

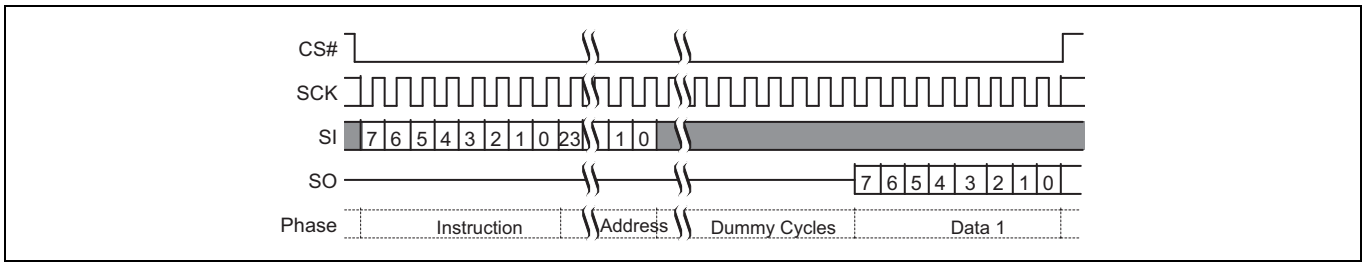


Figure 43 RSFDP command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted to IO0-IO3 and the returning data is shifted to IO0-IO3.

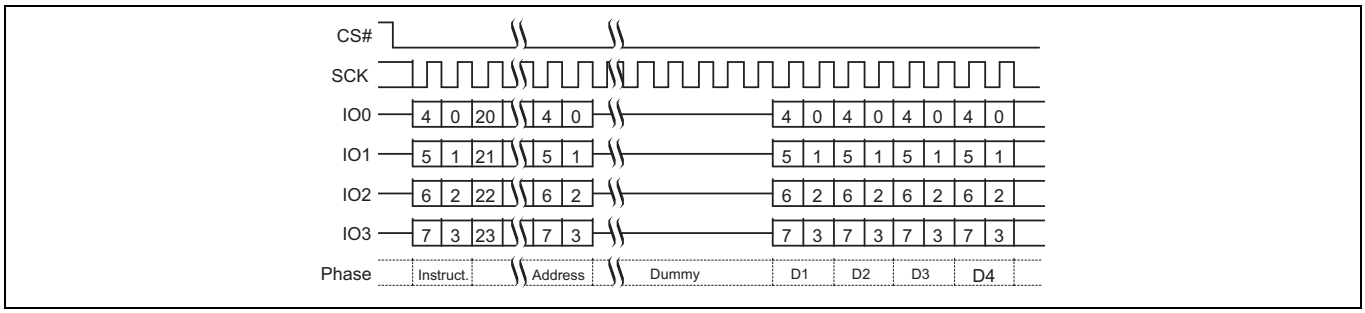


Figure 44 RSFDP QPI mode command sequence

9.3 Register access commands

9.3.1 Read Status Register 1 (RDSR1 05h)

The Read Status Register 1 (RDSR1) command allows the Status Register 1 contents to be read from SO. The volatile version of Status Register 1 (SR1V) contents may be read at any time, even while a program, erase, or write operation is in progress. It is possible to read Status Register 1 continuously by providing multiples of eight clock cycles. The status is updated for each eight cycle read. The maximum clock frequency for the RDSR1 (05h) command is 133 MHz.

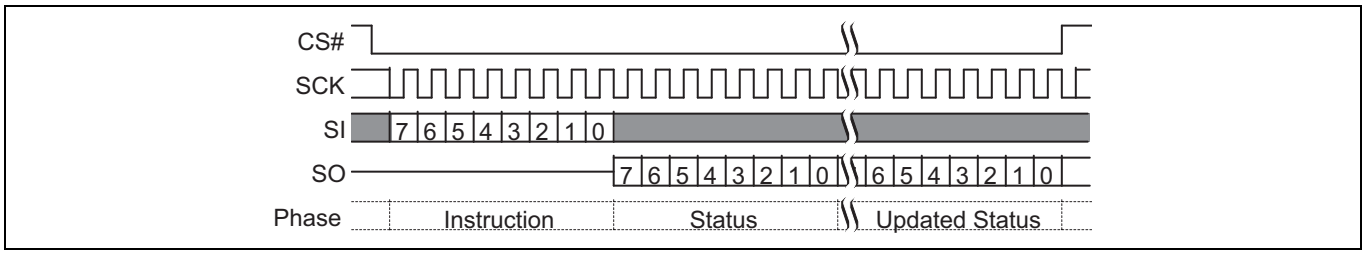


Figure 45 Read Status Register 1 (RDSR1) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted to IO0-IO3 and the returning data is shifted to IO0-IO3, two clock cycles per byte.

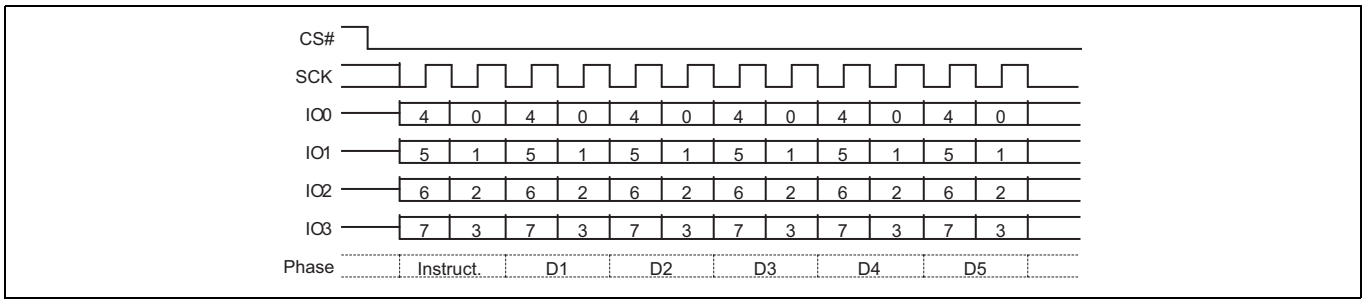


Figure 46 Read Status Register 1 (RDSR1) QPI Mode command

9.3.2 Read Status Register 2 (RDSR2 07h)

The Read Status Register 2 (RDSR2) command allows the Status Register 2 contents to be read from SO. The Status Register 2 contents may be read at any time, even while a program, erase, or write operation is in progress. It is possible to read the Status Register 2 continuously by providing multiples of eight clock cycles. The status is updated for each eight cycle read. The maximum clock frequency for the RDSR2 command is 133 MHz.

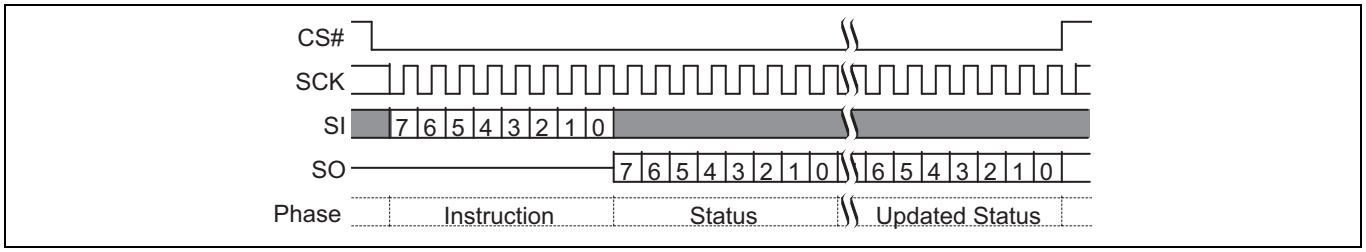


Figure 47 Read Status Register 2 (RDSR2) command

In QPI mode, Status Register 2 may be read via the Read Any Register command, see **"Read Any Register (RDAR 65h)"** on page 94.

9.3.3 Read Configuration Register (RDCR 35h)

The Read Configuration Register (RDCR) command allows the volatile Configuration Register (CR1V) contents to be read from SO. It is possible to read CR1V continuously by providing multiples of eight clock cycles. The configuration register contents may be read at any time, even while a program, erase, or write operation is in progress.

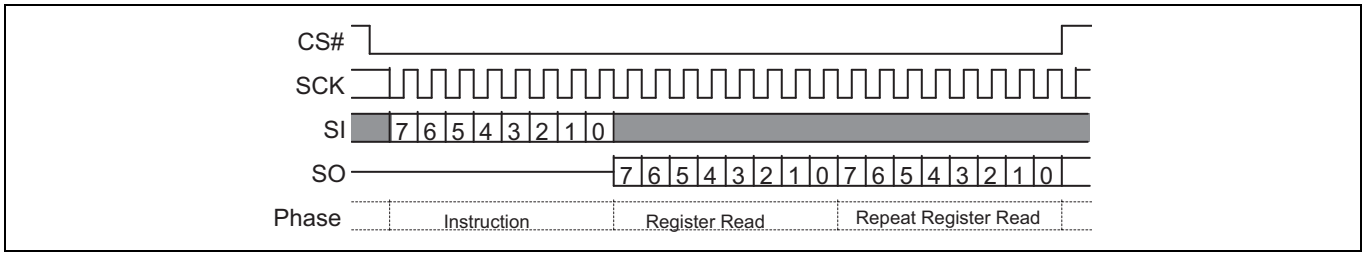


Figure 48 Read Configuration Register (RDCR) command sequence

In QPI mode, Configuration Register 1 may be read via the Read Any Register command, see **"Read Any Register (RDAR 65h)"** on page 94.

9.3.4 Write Registers (WRR 01h)

The Write Registers (WRR) command allows new values to be written to both the Status Register 1 and Configuration Register 1. Before the Write Registers (WRR) command can be accepted by the device, a Write Enable (WREN) command must be received. After the Write Enable (WREN) command has been decoded successfully, the device will set the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The Write Registers (WRR) command is entered by shifting the instruction and the data bytes on SI. The Status Register is one data byte in length.

The WRR operation first erases the register then programs the new value as a single operation. The Write Registers (WRR) command will set the P_ERR or E_ERR bits if there is a failure in the WRR operation. See **"Status Register 1 Volatile (SR1V)"** on page 53 for a description of the error bits. Any status or configuration register bit reserved for the future must be written as '0'.

CS# must be driven to the logic HIGH state after the eighth or sixteenth bit of data has been latched. If not, the Write Registers (WRR) command is not executed. If CS# is driven HIGH, after the eighth cycle then only the Status Register 1 is written; otherwise, after the sixteenth cycle both the status and configuration registers are written.

As soon as CS# is driven to the logic HIGH state, the self-timed Write Registers (WRR) operation is initiated. While the Write Registers (WRR) operation is in progress, the Status Register may still be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is a '1' during the self-timed Write Registers (WRR) operation, and is a '0' when it is completed. When the Write Registers (WRR) operation is completed, the Write Enable Latch (WEL) is set to '0'. The maximum clock frequency for the WRR command is 133 MHz.

This command is also supported in QPI mode. In QPI mode, the instruction and data is shifted to IO0-IO3, two clock cycles per byte.

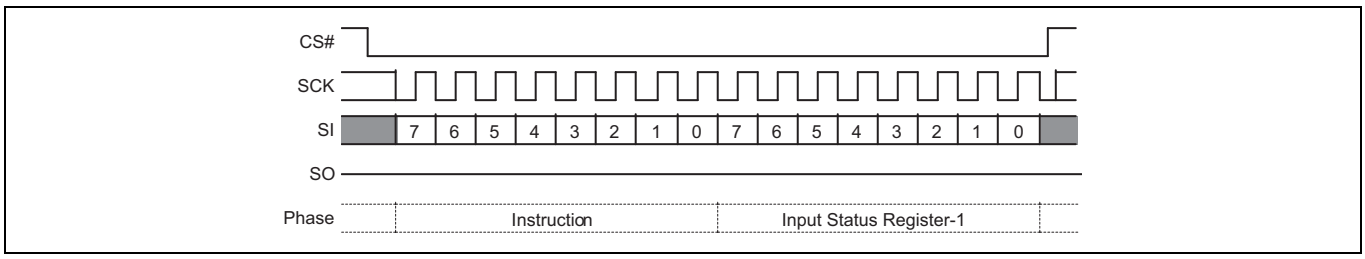


Figure 49 Write Registers (WRR) command sequence – 8 data bits

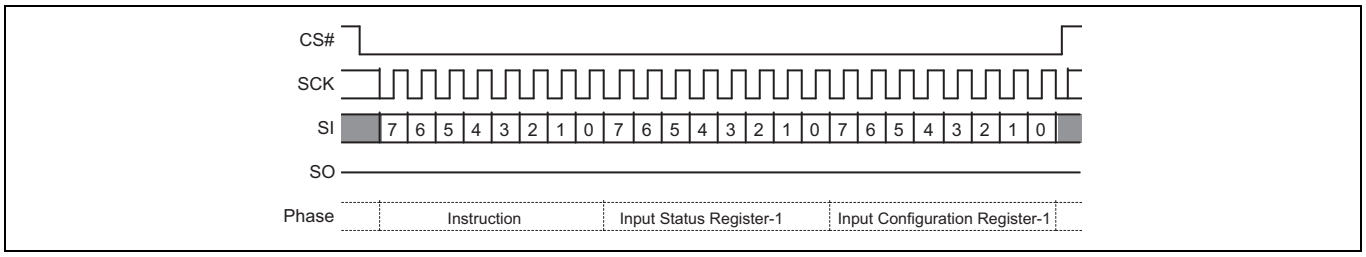


Figure 50 Write Registers (WRR) command sequence – 16 data bits

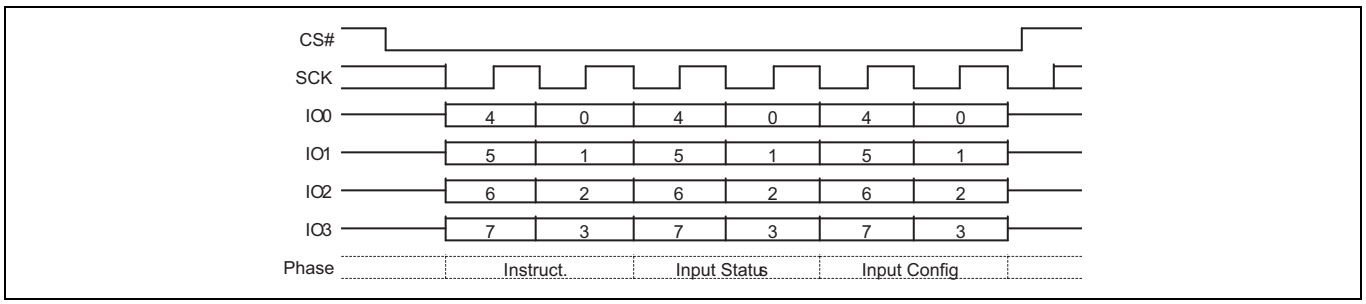


Figure 51 Write Registers (WRR) command sequence – 16 data bits QPI mode

The Write Register (WRR) command writes the non-volatile version of the Quad bit (CR1NV[1]), which also causes an update to the volatile version CR1V[1]. The WRR command can not write the volatile version CR1V[1] without first affecting the non-volatile version CR1NV[1]. The WRAR command must be used when it is desired to write the volatile Quad bit CR1V[1] without affecting the non-volatile version CR1NV[1].

The Write Registers (WRR) command allows the user to change the values of the Block Protect (BP2, BP1, and BP0) bits in either the Non-volatile Status Register 1 or in the volatile Status Register 1, to define the size of the area that is to be treated as read-only. The BPNV_O bit (CR1NV[3]) controls whether WRR writes the non-volatile or volatile version of Status Register 1. When CR1NV[3] = 0 WRR writes SR1NV[4:2]. When CR1NV[3] = 1 WRR writes SR1V[4:2].

The Write Registers (WRR) command also allows the user to set the Status Register Write Disable (SRWD) bit to ‘1’ or a ‘0’. The Status Register Write Disable (SRWD) bit and Write Protect (WP#) signal allow the BP bits to be hardware protected.

When the Status Register Write Disable (SRWD) bit of the Status Register is a ‘0’ (its initial delivery state), it is possible to write to the status register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) command, regardless of the whether Write Protect (WP#) signal is driven to the logic HIGH or logic LOW state.

When the Status Register Write Disable (SRWD) bit of the status register is set to ‘1’, two cases need to be considered, depending on the state of Write Protect (WP#):

- If the Write Protect (WP#) signal is driven to the logic HIGH state, it is possible to write to the status and configuration registers provided that the Write Enable Latch (WEL) bit has previously been set to ‘1’ by initiating a Write Enable (WREN) command.
- If the Write Protect (WP#) signal is driven to the logic LOW state, it is not possible to write to the status and configuration registers even if the Write Enable Latch (WEL) bit has previously been set to ‘1’ by a Write Enable (WREN) command. Attempts to write to the status and configuration registers are rejected, not accepted for execution, and no error indication is provided. As a consequence, all the data bytes in the memory area that are protected by the Block Protect (BP2, BP1, BP0) bits of the status register, are also hardware protected by WP#.

The WP# hardware protection can be provided:

- by setting the Status Register Write Disable (SRWD) bit after driving Write Protect (WP#) signal to the logic LOW state;

- or by driving Write Protect (WP#) signal to the logic LOW state after setting the Status Register Write Disable (SRWD) bit to '1'.

The only way to release the hardware protection is to pull the Write Protect (WP#) signal to the logic HIGH state. If WP# is permanently tied HIGH, hardware protection of the BP bits can never be activated.

Table 46 Block protection modes

WP#	SRWD Bit	Mode	Write protection of registers	Memory content	
				Protected area	Unprotected area
1	1	Software Protected	Status and Configuration Registers are Writable (if WREN command has set the WEL bit). The values in the SRWD, BP2, BP1, and BP0 bits and those in the Configuration Register can be changed	Protected against Page Program, Sector Erase, and Bulk Erase	Ready to accept Page Program, and Sector Erase commands
1	0				
0	0				
0	1	Hardware Protected	Status and Configuration Registers are Hardware Write Protected. The values in the SRWD, BP2, BP1, and BP0 bits and those in the Configuration Register cannot be changed	Protected against Page Program, Sector Erase, and Bulk Erase	Ready to accept Page Program or Erase commands

Notes
46. The Status Register originally shows 00h when the device is first shipped from Infineon to the customer.
47. Hardware protection is disabled when Quad Mode is enabled (CR1V[1] = 1). WP# becomes IO2; therefore, it cannot be utilized.

9.3.5 Write Enable (WREN 06h)

The Write Enable (WREN) command sets the Write Enable Latch (WEL) bit of the Status Register 1 (SR1V[1]) to '1'. The Write Enable Latch (WEL) bit must be set to '1' by issuing the Write Enable (WREN) command to enable write, program and erase commands.

CS# must be driven into the logic HIGH state after the eighth bit of the instruction byte has been latched in on SI. Without CS# being driven to the logic HIGH state after the eighth bit of the instruction byte has been latched to SI, the write enable operation will not be executed.

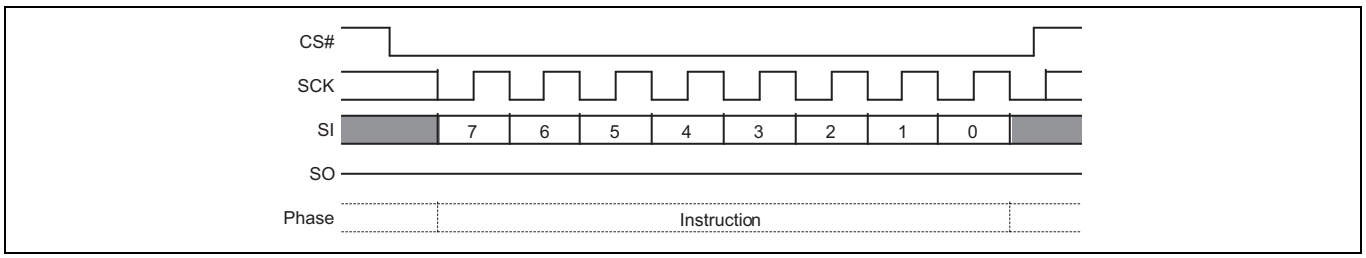


Figure 52 Write Enable (WREN) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted to IO0-IO3, two clock cycles per byte.

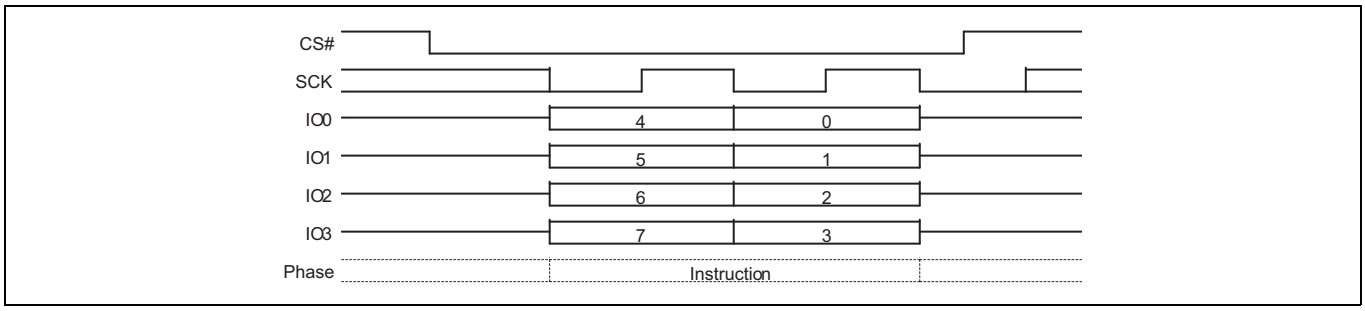


Figure 53 Write Enable (WREN) command sequence QPI mode

9.3.6 Write Disable (WRDI 04h)

The Write Disable (WRDI) command clears the Write Enable Latch (WEL) bit of the Status Register 1 (SR1V[1]) to a '0'.

The Write Enable Latch (WEL) bit may be cleared to '0' by issuing the Write Disable (WRDI) command to disable Page Program (PP), Sector Erase (SE), Bulk Erase (BE), Write Registers (WRR or WRAR), OTP Program (OTPP), and other commands, that require WEL be set to '1' for execution. The WRDI command can be used by the user to protect memory areas against inadvertent writes that can possibly corrupt the contents of the memory. The WRDI command is ignored during an embedded operation while WIP bit = 1.

CS# must be driven into the logic HIGH state after the eighth bit of the instruction byte has been latched in on SI. Without CS# being driven to the logic HIGH state after the eighth bit of the instruction byte has been latched in on SI, the write disable operation will not be executed.

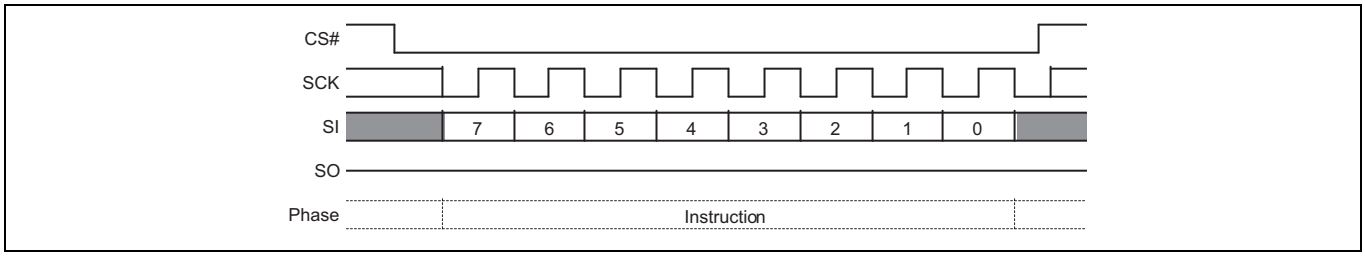


Figure 54 Write Disable (WRDI) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0-IO3, two clock cycles per byte.

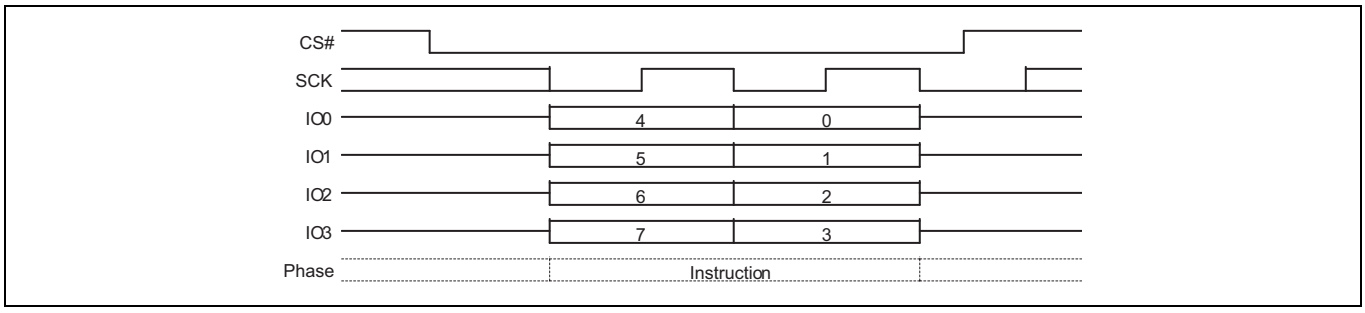


Figure 55 Write Disable (WRDI) command sequence QPI mode

9.3.7 Clear Status Register (CLSR 30h or 82h)

The Clear Status Register command resets bit SR1V[5] (Erase fail flag) and bit SR1V[6] (Program fail flag). It is not necessary to set the WEL bit before a Clear Status Register command is executed. The Clear Status Register command will be accepted even when the device remains busy with WIP set to '1', as the device does remain busy when either error bit is set. The WEL bit will be unchanged after this command is executed.

The legacy Clear Status Register (CLSR 30h) instruction may be disabled and the 30h instruction value instead used for a program / erase resume command, see **"Configuration Register 3"** on page 61. The Clear Status Register alternate instruction (CLSR 82h) is always available to clear the status register.

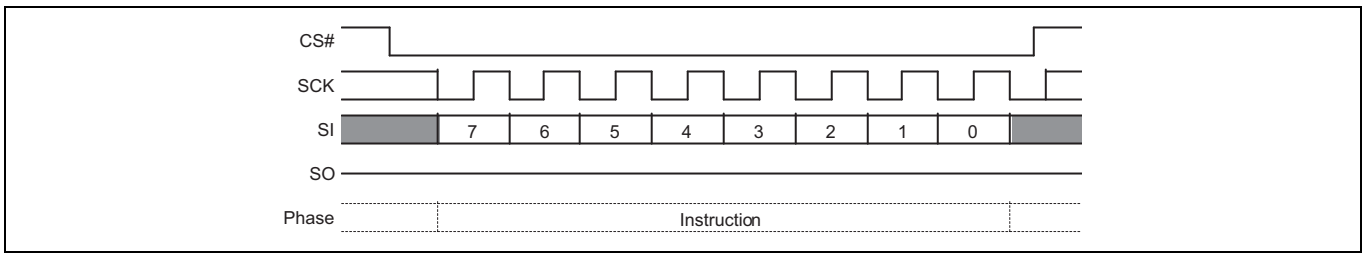


Figure 56 Clear Status Register (CLSR) command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted to IO0-IO3, two clock cycles per byte.

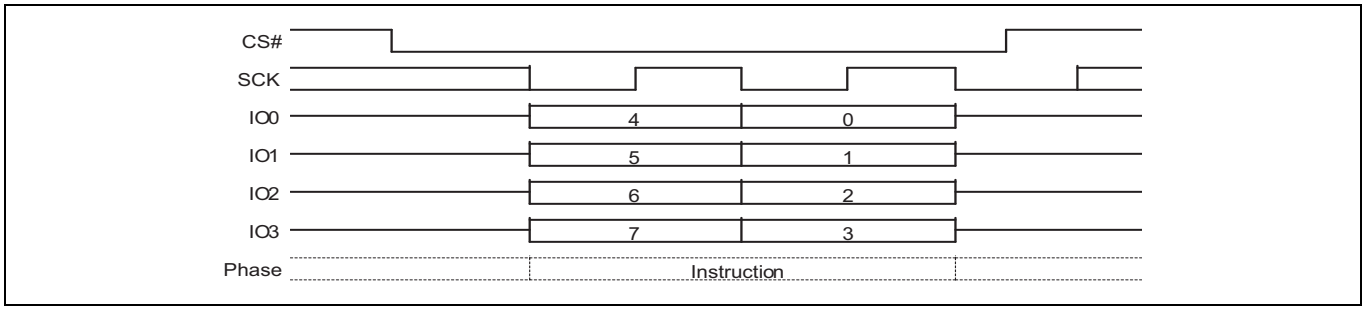


Figure 57 Clear Status Register (CLSR) command sequence QPI mode

9.3.8 ECC Status Register Read (ECCRD 19h or 4EECRD 18h)

To read the ECC Status Register, the command is followed by the ECC unit address, the four least significant bits (LSb) of address must be set to '0'. This is followed by the number of dummy cycles selected by the read latency value in CR2V[3:0]. Then the 8-bit contents of the ECC Register, for the ECC unit selected, are shifted out on SO 16 times, once for each byte in the ECC Unit. If CS# remains LOW the next ECC unit status is sent through SO 16 times, once for each byte in the ECC Unit. The maximum operating clock frequency for the ECC READ command is 133 MHz.

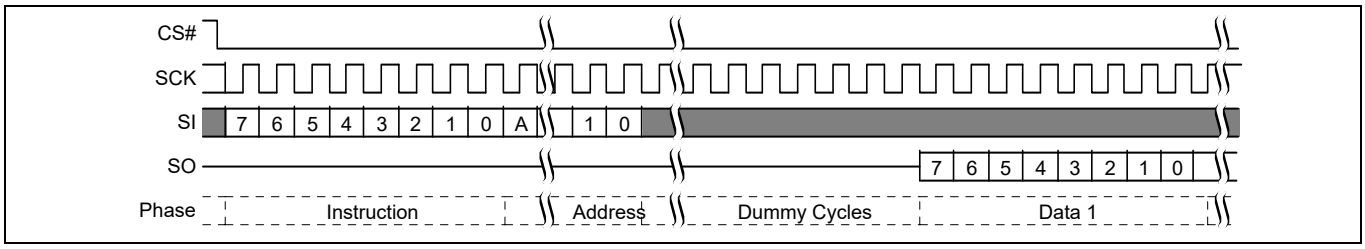


Figure 58 ECC Status Register Read command sequence[48, 49]

This command is also supported in QPI mode. In QPI mode, the instruction is shifted to IO0-IO3, two clock cycles per byte.

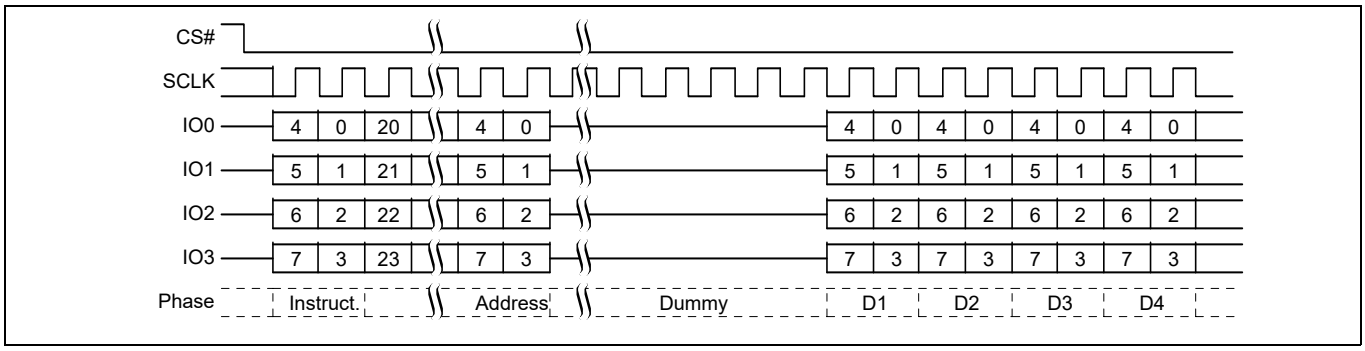


Figure 59 ECCRD (19h), QPI mode, CR2[7] = 0, command sequence

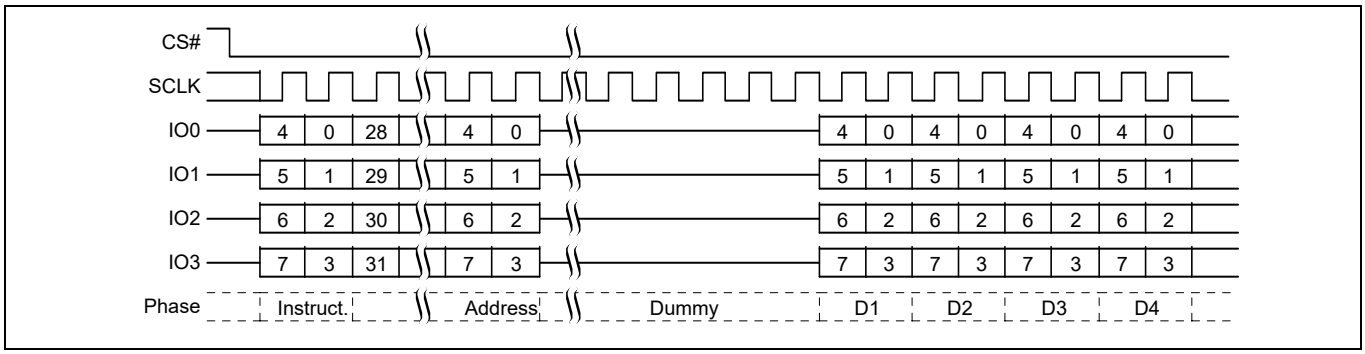


Figure 60 ECCRD (19h), QPI mode, CR2[7] = 1, or 4ECCRD (18h) command sequence

Notes
48. A = MSb of address = 23 for Address length (CR2V[7] = 0, or 31 for CR2V[7] = 1 with command 19h.
49. A = MSb of address = 31 with command 18h.

9.3.9 Program NVDLR (PNVDLR 43h)

Before the Program NVDLR (PNVDLR) command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device. After the Write Enable (WREN) command has been decoded successfully, the device will set the Write Enable Latch (WEL) to enable the PNVDLR operation.

The PNVDLR command is entered by shifting the instruction and the data byte on SI.

CS# must be driven to the logic HIGH state after the eighth (8th) bit of data has been latched. If not, the PNVDLR command is not executed. As soon as CS# is driven to the logic HIGH state, the self-timed PNVDLR operation is initiated. While the PNVDLR operation is in progress, the Status Register may be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is a '1' during the self-timed PNVDLR cycle, and is a '0' when it is completed. The PNVDLR operation can report a program error in the P_ERR bit of the status register. When the PNVDLR operation is completed, the Write Enable Latch (WEL) is set to '0'. The maximum clock frequency for the PNVDLR command is 133 MHz.

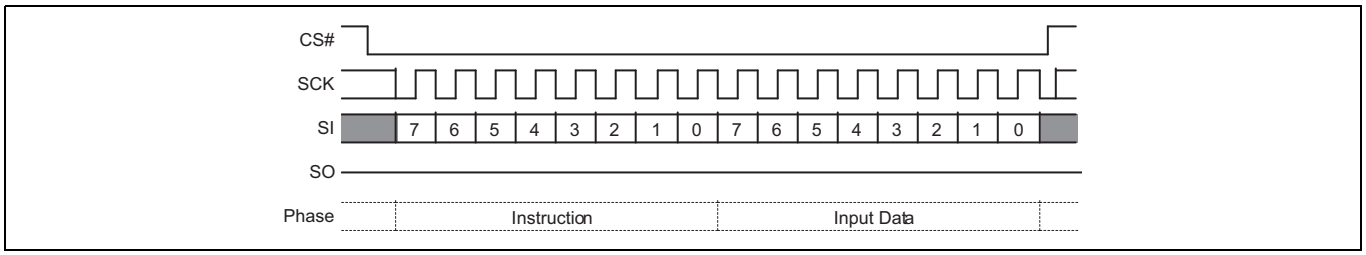


Figure 61 Program NVDLR (PNVDLR) command sequence

9.3.10 Write VDLR (WVDLR 4Ah)

Before the Write VDLR (WVDLR) command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device. After the Write Enable (WREN) command has been decoded successfully, the device will set the Write Enable Latch (WEL) to enable WVDLR operation.

The WVDLR command is entered by shifting the instruction and the data byte on SI.

CS# must be driven to the logic HIGH state after the eighth (8th) bit of data has been latched. If not, the WVDLR command is not executed. As soon as CS# is driven to the logic HIGH state, the WVDLR operation is initiated with no delays. The maximum clock frequency for the PNVDLR command is 133 MHz.

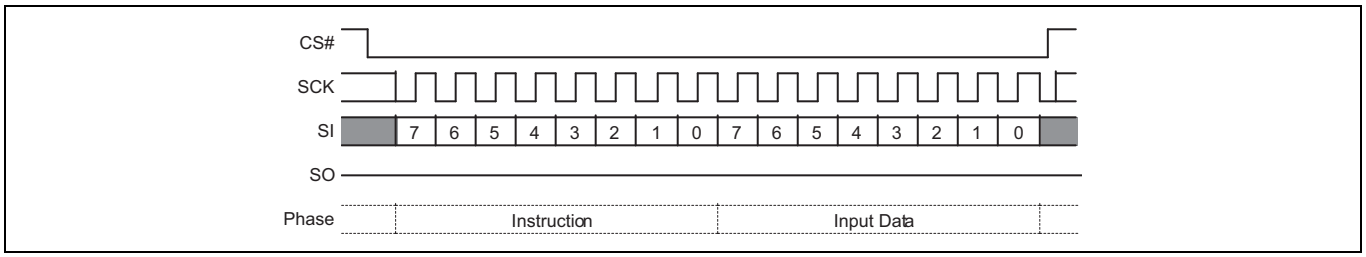


Figure 62 Write VDLR (WVDLR) command sequence

9.3.11 Data Learning Pattern Read (DLPRD 41h)

The instruction is shifted on SI, then the 8-bit DLP is shifted to SO. It is possible to read the DLP continuously by providing multiples of eight clock cycles. The maximum operating clock frequency for the DLPRD command is 133 MHz.

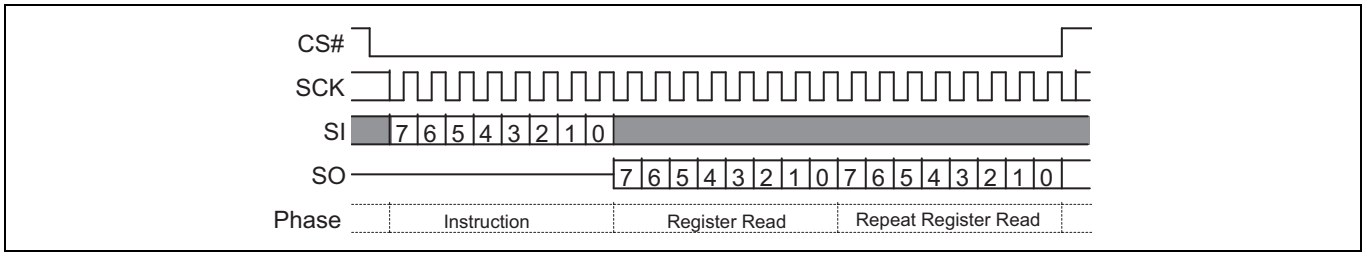


Figure 63 DLP Read (DLPRD) command sequence

9.3.12 Enter 4-Byte Address Mode (4BAM B7h)

The enter 4-byte Address Mode (4BAM) command sets the volatile Address Length bit (CR2V[7]) to 1 to change most 3-byte address commands to require 4 bytes of address. The Read SFDP (RSFDP) command is the only 3-byte command that is not affected by the Address Length bit. RSFDP is required by the JEDEC JESD216 standard to always have only 3 bytes of address.

A hardware or software reset is required to exit the 4-byte address mode.

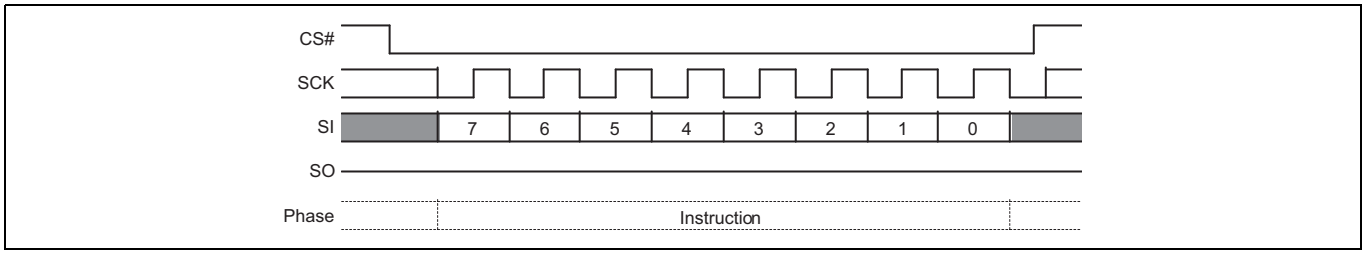


Figure 64 Enter 4-Byte Address mode (4BAM B7h) command sequence

9.3.13 Read Any Register (RDAR 65h)

The Read Any Register (RDAR) command provides a way to read all device registers - non-volatile and volatile. The instruction is followed by a 3- or 4-byte address (depending on the address length configuration CR2V[7], followed by a number of latency (dummy) cycles set by CR2V[3:0]. Then the selected register contents are returned. If the read access is continued the same addressed register contents are returned until the command is terminated – only one register is read by each RDAR command.

Reading undefined locations provides undefined data.

The RDAR command may be used during embedded operations to read Status Register 1 (SR1V).

The RDAR command is not used for reading registers that act as a window into a larger array: PPBAR, and DYBAR. There are separate commands required to select and read the location in the array accessed.

The RDAR command will read invalid data from the PASS register locations if the ASP Password protection mode is selected by programming ASPR[2] to ‘0’.

Table 47 Register address map

Byte address (Hex)	Register name	Description
00000000	SR1NV	Non-volatile Status and Configuration Registers
00000001	N/A	
00000002	CR1NV	
00000003	CR2NV	
00000004	CR3NV	
00000005	CR4NV	
...	N/A	N/A
00000010	NVDLR	Non-volatile Data Learning Register
...	N/A	N/A
00000020	PASS[7:0]	Non-volatile Password Register
00000021	PASS[15:8]	
00000022	PASS[23:16]	
00000023	PASS[31:24]	
00000024	PASS[39:32]	
00000025	PASS[47:40]	
00000026	PASS[55:48]	
00000027	PASS[63:56]	
...	N/A	N/A
00000030	ASPR[7:0]	Non-volatile
00000031	ASPR[15:8]	
...	N/A	
00800000	SR1V	Volatile Status and Configuration Registers
00800001	SR2V	
00800002	CR1V	
00800003	CR2V	
00800004	CR3V	
00800005	CR4V	
...	N/A	N/A
00800010	VDLR	Volatile Data Learning Register
...	N/A	N/A
00800040	PPBL	Volatile PPB Lock Register
...	N/A	N/A

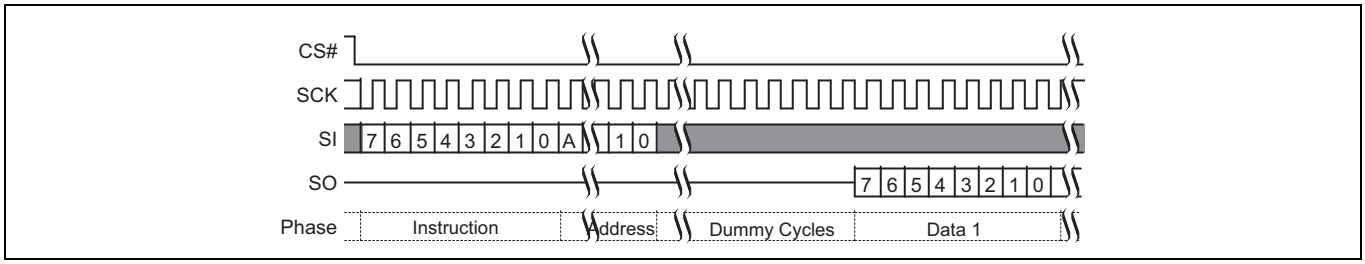


Figure 65 Read Any Register Read command sequence[50]

This command is also supported in QPI mode. In QPI mode, the instruction is shifted to IO0-IO3, two clock cycles per byte.

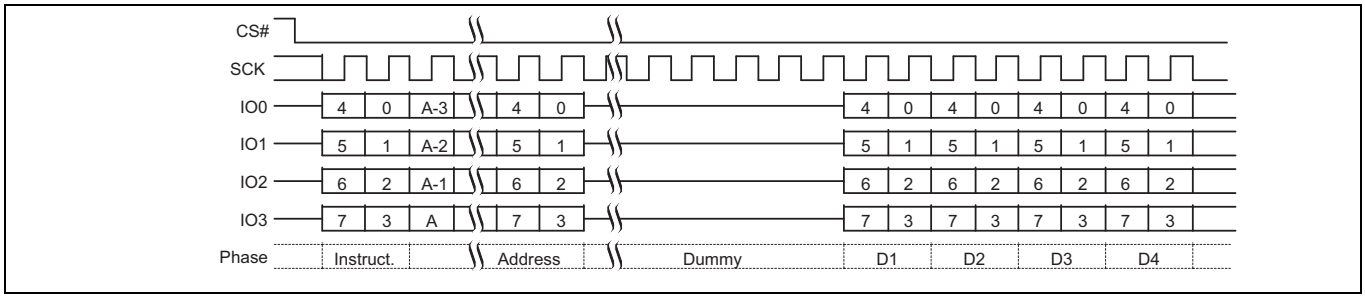


Figure 66 Read Any Register, QPI Mode, command sequence[50]

9.3.14 Write Any Register (WRAR 71h)

The Write Any Register (WRAR) command provides a way to write any device register - non-volatile/volatile. The instruction is followed by a 3 or 4-byte address (depending on the address length configuration CR2V[7], followed by one byte of data to write in the address selected register.

Before the WRAR command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write

Note
50. A = MSb of address = 23 for Address length CR2V[7] = 0, or 31 for CR2V[7] = 1.

operations. The WIP bit in SR1V may be checked to determine when the operation is completed. The P_ERR and E_ERR bits in SR1V may be checked to determine if any error occurred during the operation.

Some registers have a mixture of bit types and individual rules controlling which bits may be modified. Some bits are read only, some are OTP.

Read only bits are never modified and the related bits in the WRAR command data byte are ignored without setting a program or erase error indication (P_ERR or E_ERR in SR1V). Hence, the value of these bits in the WRAR data byte do not matter.

OTP bits may only be programmed to the level opposite of their default state. Writing of OTP bits back to their default state is ignored and no error is set.

Non-volatile bits which are changed by the WRAR data, require non-volatile register write time (t_{W}) to be updated. The update process involves an erase and a program operation on the non-volatile register bits. If either the erase or program portion of the update fails the related error bit and WIP in SR1V will be set to '1'.

Volatile bits which are changed by the WRAR data, require the volatile register write time (t_{CS}) to be updated.

Status Register 1 may be repeatedly read (polled) to monitor the Write-In-Progress (WIP) bit (SR1V[0]) and the error bits (SR1V[6,5]) to determine when the register write is completed or failed. If there is a write failure, the clear status command is used to clear the error status and enable the device to return to standby state.

However, the PPBL register can not be written by the WRAR command. Only the PPB Lock Bit Write (PLBWR) command can write the PPBL register.

The command sequence and behavior is the same as the PP or 4PP command with only a single byte of data provided. See **"Page Program (PP 02h or 4PP 12h)"** on page 108.

The address map of the registers is the same as shown for **"Read Any Register (RDAR 65h)"** on page 94.

9.3.15 Set Burst Length (SBL C0h)

The Set Burst Length (SBL) command is used to configure the Burst Wrap feature. Burst Wrap is used in conjunction with Quad I/O Read and DDR Quad I/O Read, in legacy SPI or QPI mode, to access a fixed length and alignment of data. Certain applications can benefit from this feature by improving the overall system code execution performance. The Burst Wrap feature allows applications that use cache, to start filling a cache line with instruction or data from a critical address first, then fill the remainder of the cache line afterwards within a fixed length (8/16/32/64-bytes) of data, without issuing multiple read commands.

The Set Burst Length (SBL) command writes the CR4V register bits 4, 1, and 0 to enable or disable the wrapped read feature and set the wrap boundary. Other bits of the CR4V register are not affected by the SBL command. When enabled the wrapped read feature changes the related read commands from sequentially reading until the command ends, to reading sequentially wrapped within a group of bytes.

When CR4V[4] = 1, the wrap mode is not enabled and unlimited length sequential read is performed.

When CR4V[4] = 0, the wrap mode is enabled and a fixed length and aligned group of 8-, 16-, 32-, or 64- bytes is read starting at the byte address provided by the read command and wrapping around at the group alignment boundary.

The group of bytes is of length and aligned on an 8-, 16-, 32-, or 64- byte boundary. CR4V[1:0] selects the boundary. See **"Configuration Register 4 Volatile (CR4V)"** on page 64.

The starting address of the read command selects the group of bytes and the first data returned is the addressed byte. Bytes are then read sequentially until the end of the group boundary is reached. If the read continues the

address wraps to the beginning of the group and continues to read sequentially. This wrapped read sequence continues until the command is ended by CS# returning HIGH.

Table 48 Example burst wrap sequences

CR4V[4,1:0] value (hex)	Wrap boundary (bytes)	Start address (hex)	Address sequence (hex)
1X	Sequential	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, ...
00	8	XXXXXX00	00, 01, 02, 03, 04, 05, 06, 07, 00, 01, 02, ...
		XXXXXX07	07, 00, 01, 02, 03, 04, 05, 06, 07, 00, 01, ...
01	16	XXXXXX02	02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 00, 01, 02, 03, ...
		XXXXXX0C	0C, 0D, 0E, 0F, 00, 01, 02, 03, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, ...
02	32	XXXXXX0A	0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, ...
		XXXXXX1E	1E, 1F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, ...
03	64	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 00, 01, 02 ...
		XXXXXX2E	2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, ...

The power-on reset, hardware reset, or software reset default burst length can be changed by programming CR4NV with the desired value using the WRAR command.

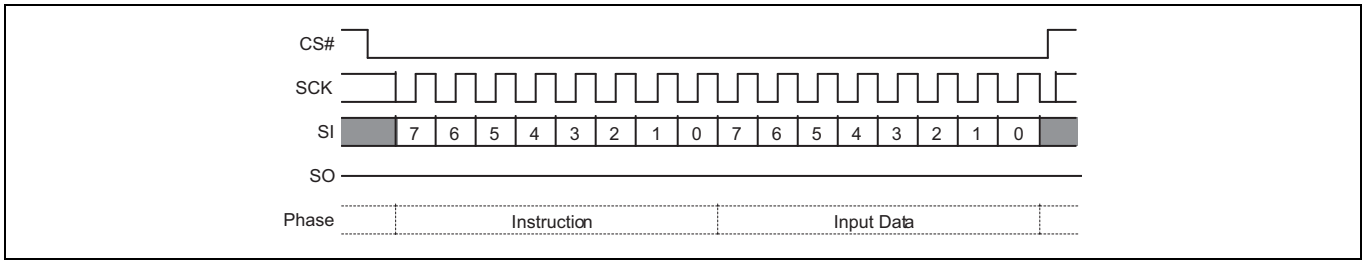


Figure 67 Set Burst Length command sequence

9.4 Read memory array commands

Read commands for the main flash array provide many options for prior generation SPI compatibility or enhanced performance SPI:

- Some commands transfer address or data on each rising edge of SCK. These are called Single Data Rate commands (SDR).
- Some SDR commands transfer address one bit per rising edge of SCK and return data 1 bit of data per rising edge of SCK. These are called Single width commands.
- Some SDR commands transfer both address and data 2 or 4 bits per rising edge of SCK. These are called Dual I/O for 2 bit, Quad I/O, and QPI for 4 bit. QPI also transfers instructions 4 bits per rising edge.
- Some commands transfer address and data on both the rising edge and falling edge of SCK. These are called Double Data Rate (DDR) commands.

- There are DDR commands for 4 bits of address or data per SCK edge. These are called Quad I/O DDR and QPI DDR for 4 bit per edge transfer.

All of these commands, except QPI Read, begin with an instruction code that is transferred one bit per SCK rising edge. QPI Read transfers the instruction 4 bits per SCK rising edge.The instruction is followed by either a 3- or 4-byte address transferred at SDR or DDR. Commands transferring address or data 2 or 4 bits per clock edge are called Multiple I/O (MIO) commands. For S25FS512S devices, the traditional SPI 3-byte addresses are unable to directly address all locations in the memory array. Separate 4-byte address read commands are provided for access to the entire address space. These devices may be configured to take a 4-byte address from the host system with the traditional 3-byte address commands. The 4-byte address mode for traditional commands is activated by setting the Address Length bit in Configuration Register 2 to 0.

The Quad I/O and QPI commands provide a performance improvement option controlled by mode bits that are sent following the address bits. The mode bits indicate whether the command following the end of the current read will be another read of the same type, without an instruction at the beginning of the read. These mode bits give the option to eliminate the instruction cycles when doing a series of Quad read accesses.

Some commands require delay cycles following the address or mode bits to allow time to access the memory array - read latency. The delay or read latency cycles are traditionally called dummy cycles. The dummy cycles are ignored by the memory thus any data provided by the host during these cycles is ‘don’t care’ and the host may also leave the SI signal at high impedance during the dummy cycles. When MIO commands are used the host must stop driving the IO signals (outputs are high impedance) before the end of last dummy cycle. When DDR commands are used the host must not drive the I/O signals during any dummy cycle. The number of dummy cycles varies with the SCK frequency or performance option selected via the Configuration Register 2 (CR2V[3:0]) Latency Code. Dummy cycles are measured from SCK falling edge to next SCK falling edge. SPI outputs are traditionally driven to a new value on the falling edge of each SCK. Zero dummy cycles means the returning data is driven by the memory on the same falling edge of SCK that the host stops driving address or mode bits.

The DDR commands may optionally have an 8-edge Data Learning Pattern (DLP) driven by the memory, on all data outputs, in the dummy cycles immediately before the start of data. The DLP can help the host memory controller determine the phase shift from SCK to data edges so that the memory controller can capture data at the center of the data eye.

When using SDR I/O commands at higher SCK frequencies (>50 MHz), an LC that provides 1 or more dummy cycles should be selected to allow additional time for the host to stop driving before the memory starts driving data, to minimize I/O driver conflict. When using DDR I/O commands with the DLP enabled, an LC that provides 5 or more dummy cycles should be selected to allow 1 cycle of additional time for the host to stop driving before the memory starts driving the 4-cycle DLP.

Each read command ends when CS# is returned HIGH at any point during data return. CS# must not be returned High during the mode or dummy cycles before data returns as this may cause mode bits to be captured incorrectly; making it indeterminate as to whether the device remains in Continuous Read mode.

9.4.1 Read (Read 03h or 4READ 13h)

The instruction

- 03h (CR2V[7] = 0) is followed by a 3-byte address (A23-A0) or
- 03h (CR2V[7] = 1) is followed by a 4-byte address (A31-A0) or
- 13h is followed by a 4-byte address (A31-A0)

Then the memory contents, at the address given, are shifted to SO. The maximum operating clock frequency for the READ command is 50 MHz.

The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached,

the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.

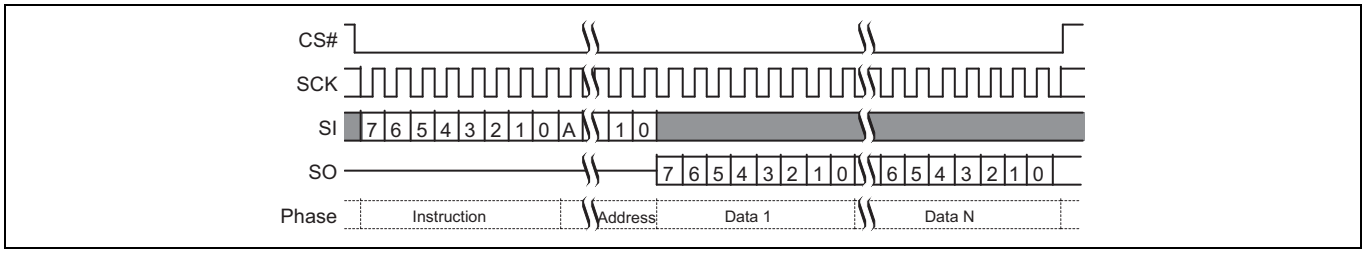


Figure 68 Read command sequence (3-byte address, 03h or 13h)

9.4.2 Fast Read (FAST_READ 0Bh or 4FAST_READ 0Ch)

The instruction

- 0Bh (CR2V[7] = 0) is followed by a 3-byte address (A23-A0) or
- 0Bh (CR2V[7] = 1) is followed by a 4-byte address (A31-A0) or
- 0Ch is followed by a 4-byte address (A31-A0)

The address is followed by dummy cycles depending on the latency code set in the Configuration Register CR2V[3:0]. The dummy cycles allow the device internal circuits additional time for accessing the initial address location. During the dummy cycles the data value on SO is ‘don’t care’ and may be high impedance. Then the memory contents, at the address given, are shifted out’ on SO.

The maximum operating clock frequency for FAST READ command is 133 MHz.

The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached, the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.

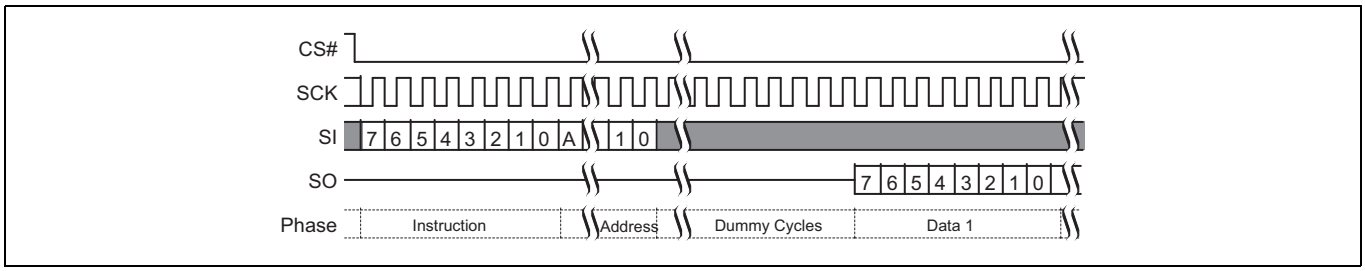


Figure 69 Fast Read (FAST_READ) command sequence (3-byte address, 0Bh [CR2V[7] = 0)[52]

Notes
51. A = MSb of address = 23 for CR2V[7] = 0, or 31 for CR2V[7] = 1 or command 13h.
52. A = MSb of address = 23 for CR2V[7] = 0, or 31 for CR2V[7] = 1 or command 0Ch.

9.4.3 Dual I/O Read (DIOR BBh or 4DIOR BCh)

The instruction

- BBh (CR2V[7] = 0) is followed by a 3-byte address (A23-A0) or
- BBh (CR2V[7] = 1) is followed by a 4-byte address (A31-A0) or
- BCh is followed by a 4-byte address (A31-A0)

The Dual I/O Read commands improve throughput with two I/O signals — IO0 (SI) and IO1 (SO). This command takes input of the address and returns read data two bits per SCK rising edge. In some applications, the reduced address input and data output time might allow for code execution in place (XIP) i.e. directly from the memory device.

The maximum operating clock frequency for Dual I/O Read is 133 MHz.

The Dual I/O Read command has continuous read mode bits that follow the address so, a series of Dual I/O Read commands may eliminate the 8-bit instruction after the first Dual I/O Read command sends a mode bit pattern of Axh that indicates the following command will also be a Dual I/O Read command. The first Dual I/O Read command in a series starts with the 8-bit instruction, followed by address, followed by four cycles of mode bits, followed by an optional latency period. If the mode bit pattern is Axh the next command is assumed to be an additional Dual I/O Read command that does not provide instruction bits. That command starts with address, followed by mode bits, followed by optional latency.

Variable latency may be added after the mode bits are shifted into SI and SO before data begins shifting out of IO0 and IO1. This latency period (dummy cycles) allows the device internal circuitry enough time to access data at the initial address. During the dummy cycles, the data value on SI and SO are ‘don’t care’ and may be high impedance. The number of dummy cycles is determined by the frequency of SCK. The latency is configured in CR2V[3:0].

The continuous read feature removes the need for the instruction bits in a sequence of read accesses and greatly improves code execution (XIP) performance. The upper nibble (bits 7-4) of the Mode bits control the length of the next Dual I/O Read command through the inclusion or exclusion of the first byte instruction code. The lower nibble (bits 3-0) of the Mode bits are ‘don’t care’ (“x”) and may be high impedance. If the Mode bits equal Axh, then the device remains in Dual I/O Continuous Read Mode and the next address can be entered (after CS# is raised high and then asserted low) without the BBh or BCh instruction, as shown in **Figure 71**; thus, eliminating eight cycles of the command sequence. The following sequences will release the device from Dual I/O Continuous Read mode; after which, the device can accept standard SPI commands:

1. During the Dual I/O continuous read command sequence, if the mode bits are any value other than Axh, then the next time CS# is raised HIGH the device will be released from Dual I/O continuous read mode.
2. Send the Mode Reset command.

Note that the four-mode bit cycles are part of the device’s internal circuitry latency time to access the initial address after the last address cycle that is clocked into IO0 (SI) and IO1 (SO).

It is important that the I/O signals be set to high-impedance at or before the falling edge of the first data out clock. At higher clock speeds the time available to turn off the host outputs before the memory device begins to drive (bus turn around) is diminished. It is allowed and may be helpful in preventing I/O signal contention, for the host system to turn off the I/O signal outputs (make them high impedance) during the last two ‘don’t care’ mode cycles or during any dummy cycles.

Following the latency period the memory content, at the address given, is shifted out two bits at a time through IO0 (SI) and IO1 (SO). Two bits are shifted out at the SCK frequency at the falling edge of SCK signal.

The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached, the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.

CS# should not be driven high during mode or dummy bits as this may make the mode bits indeterminate.

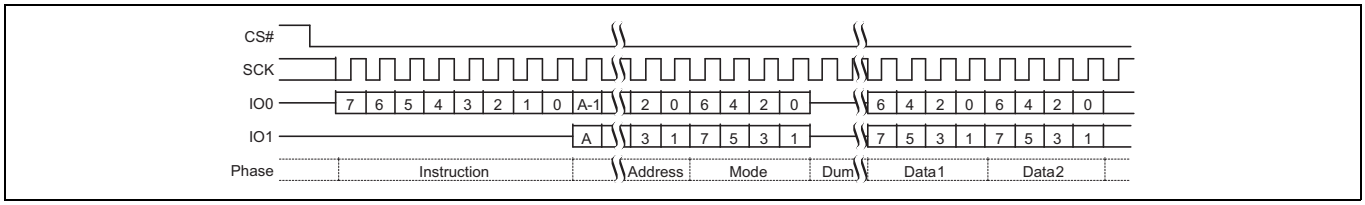


Figure 70 Dual I/O Read command sequence (BBh)[53-55]

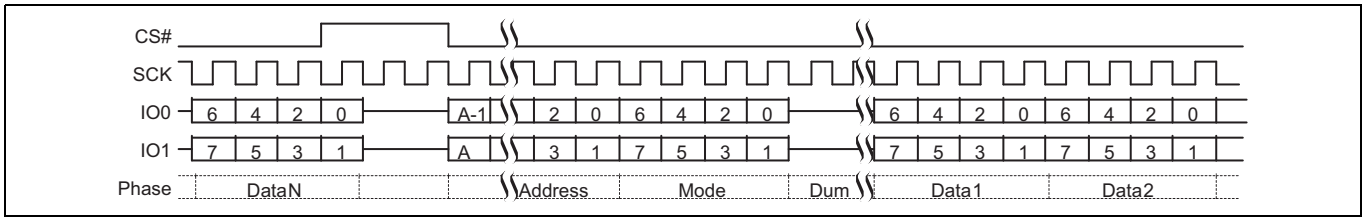


Figure 71 Dual I/O Continuous Read command sequence (BBh])[56, 57]

9.4.4 Quad I/O Read (QIOR EBh or 4QIOR ECh)

The instruction

- EBh (CR2V[7] = 0) is followed by a 3-byte address (A23-A0) or
- EBh (CR2V[7] = 1) is followed by a 4-byte address (A31-A0) or
- ECh is followed by a 4-byte address (A31-A0)

The Quad I/O Read command improves throughput with four I/O signals: IO0-IO3. It allows input of the address bits four bits per serial SCK clock. In some applications, the reduced instruction overhead might allow for code execution (XIP) directly from S25FS512S devices. The QUAD bit of the configuration register must be set (CR1V[1] = 1) to enable the Quad capability of S25FS512S devices.

The maximum operating clock frequency for Quad I/O Read is 133 MHz.

For the Quad I/O Read command, there is a latency required after the mode bits (described below) before data begins shifting out of IO0-IO3. This latency period (i.e., dummy cycles) allows the device's internal circuitry enough time to access data at the initial address. During latency cycles, the data value on IO0-IO3 are 'don't care' and may be high impedance. The number of dummy cycles is determined by the frequency of SCK. The latency is configured in CR2V[3:0].

Following the latency period, the memory contents at the address given, is shifted out four bits at a time through IO0-IO3. Each nibble (4 bits) is shifted out at the SCK frequency by the falling edge of the SCK signal.

The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached,

Notes
53. A = MSb of address = 23 for Address length (CR2V[7] = 0, or 31 for CR2V[7] = 1 with command BBh.
54. A = MSb of address = 31 with command BBh.
55. Least significant 4 bits of Mode are don't care and it is optional for the host to drive these bits. The host may turn OFF drive during these cycles to increase bus turn around time between Mode bits from host and returning data from the memory.
56. A = MSb of address = 23 for Address length (CR2V[7] = 0, or 31 for CR2V[7] = 1 with command BBh.
57. A = MSb of address = 31 with command BBh.

the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.

Address jumps can be done without the need for additional Quad I/O Read instructions. This is controlled through the setting of the Mode bits (after the address sequence, as shown in **Figure 72**). This added feature removes the need for the instruction sequence and greatly improves code execution (XIP). The upper nibble (bits 7-4) of the Mode bits control the length of the next Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble (bits 3-0) of the Mode bits are 'don't care' (x). If the mode bits equal Axh, then the device remains in Quad I/O High Performance Read mode and the next address can be entered (after CS# is raised HIGH and then asserted LOW) without requiring the EBh or ECh instruction, as shown in **Figure 74**; thus, eliminating eight cycles for the command sequence.

The following sequences will release the device from Quad I/O High Performance Read mode; after which, the device can accept standard SPI commands:

1. During the Quad I/O Read Command Sequence, if the Mode bits are any value other than Axh, then the next time CS# is raised HIGH the device will be released from Quad I/O High Performance Read mode.
2. Send the Mode Reset command.

Note that the two mode bit clock cycles and additional wait states (i.e., dummy cycles) allow the device's internal circuitry latency time to access the initial address after the last address cycle that is clocked into IO0-IO3.

It is important that the IO0-IO3 signals be set to high-impedance at or before the falling edge of the first data out clock. At higher clock speeds the time available to turn off the host outputs before the memory device begins to drive (bus turn around) is diminished. It is allowed and may be helpful in preventing IO0-IO3 signal contention, for the host system to turn off the IO0-IO3 signal outputs (make them high impedance) during the last 'don't care' mode cycle or during any dummy cycles.

CS# should not be driven high during mode or dummy bits as this may make the mode bits indeterminate.

In QPI mode (CR2V[6] = 1), the Quad I/O instructions are sent 4 bits per SCK rising edge. The remainder of the command protocol is identical to the Quad I/O commands.

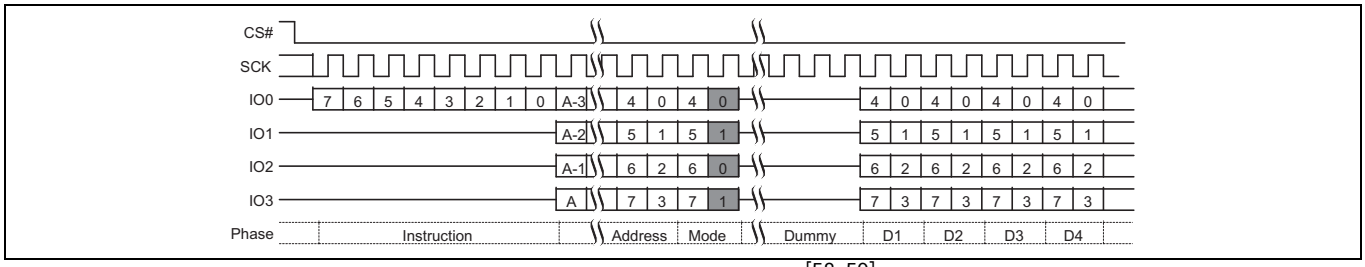


Figure 72 Quad I/O Read command sequence (EBh or ECh)[58, 59]

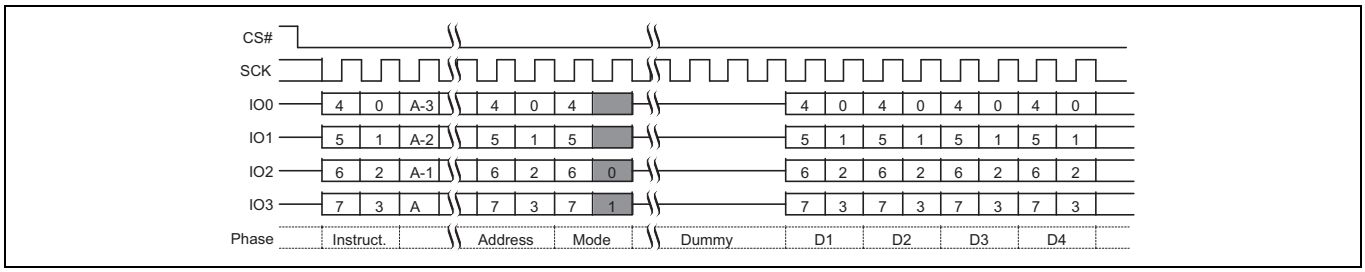


Figure 73 Quad I/O Read command sequence (EBh or ECh), QPI Mode[58, 59]

Notes
58. A = MSb of address = 23 for Address length (CR2V[7] = 0, or 31 for CR2V[7] = 1 with command EBh.
59. A = MSb of address = 31 with command ECh.

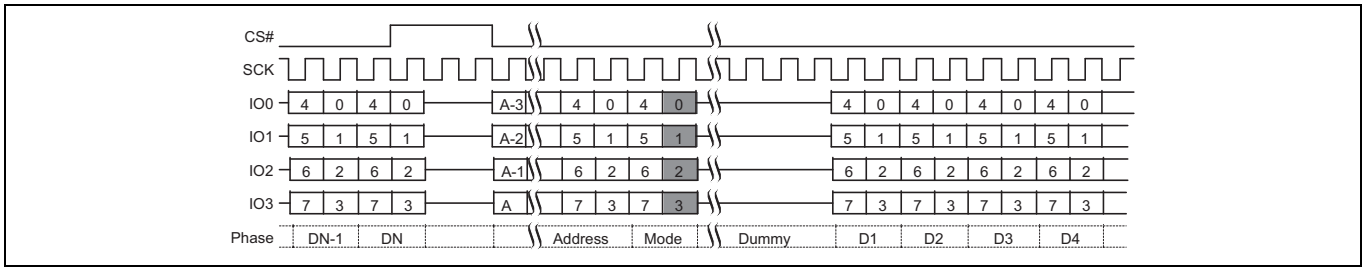


Figure 74 Continuous Quad I/O Read command sequence (EBh or ECh)[60, 61]

9.4.5 DDR Quad I/O Read (EDh, EEh)

The DDR Quad I/O Read command improves throughput with four I/O signals: IO0-IO3. It is similar to the Quad I/O Read command but allows input of the address four bits on every edge of the clock. In some applications, the reduced instruction overhead might allow for code execution (XIP) directly from S25FS512S devices. The QUAD bit of the Configuration Register must be set (CR1V[1] = 1) to enable the Quad capability.

The instruction

- EDh (CR2V[7] = 0) is followed by a 3-byte address (A23-A0) or
- EDh (CR2V[7] = 1) is followed by a 4-byte address (A31-A0) or
- EEh is followed by a 4-byte address (A31-A0)

The address is followed by mode bits. Then the memory contents, at the address given, is shifted out, in a DDR fashion, with four bits at a time on each clock edge through IO0-IO3.

The maximum operating clock frequency for DDR Quad I/O Read command is 80 MHz.

For DDR Quad I/O Read, there is a latency required after the last address and mode bits are shifted into the IO0-IO3 signals before data begins shifting out of IO0-IO3. This latency period (dummy cycles) allows the device's internal circuitry enough time to access the initial address. During these latency cycles, the data value on IO0-IO3 are 'don't care' and may be high impedance. When the Data Learning Pattern (DLP) is enabled the host system must not drive the IO signals during the dummy cycles. The IO signals must be left high impedance by the host so that the memory device can drive the DLP during the dummy cycles.

The number of dummy cycles is determined by the frequency of SCK. The latency is configured in CR2V[3:0].

Mode bits allow a series of Quad I/O DDR commands to eliminate the 8-bit instruction after the first command sends a complementary mode bit pattern, as shown in **Figure 75**. This feature removes the need for the eight bit SDR instruction sequence and dramatically reduces initial access times (improves XIP performance). The Mode bits control the length of the next DDR Quad I/O Read operation through the inclusion or exclusion of the first byte instruction code. If the upper nibble (IO[7:4]) and lower nibble (IO[3:0]) of the Mode bits are complementary (i.e. 5h and Ah) the device transitions to Continuous DDR Quad I/O Read Mode and the next address can be entered (after CS# is raised HIGH and then asserted LOW) without requiring the EDh or EEh instruction, as shown in **Figure 76**, thus eliminating eight cycles from the command sequence. The following sequences will release the device from Continuous DDR Quad I/O Read mode; after which, the device can accept standard SPI commands:

1. During the DDR Quad I/O Read Command Sequence, if the Mode bits are not complementary the next time CS# is raised high and then asserted low the device will be released from DDR Quad I/O Read mode.
2. Send the Mode Reset command.

The address can start at any byte location of the memory array. The address is automatically incremented to the next higher address in sequential order after each byte of data is shifted out. The entire memory can therefore be read out with one single read instruction and address 000000h provided. When the highest address is reached,

Notes
60. A = MSb of address = 23 for Address length (CR2V[7] = 0, or 31 for CR2V[7] = 1 with command EBh.
61. A = MSb of address = 31 with command ECh.

the address counter will wrap around and roll back to 000000h, allowing the read sequence to be continued indefinitely.

CS# should not be driven HIGH during mode or dummy bits as this may make the mode bits indeterminate. Note that the memory devices may drive the IOs with a preamble prior to the first data value. The preamble is a Data Learning Pattern (DLP) that is used by the host controller to optimize data capture at higher frequencies. The preamble drives the IO bus for the four clock cycles immediately before data is output. The host must be sure to stop driving the IO bus prior to the time that the memory starts outputting the preamble.

The preamble is intended to give the host controller an indication about the round trip time from when the host drives a clock edge to when the corresponding data value returns from the memory device. The host controller will skew the data capture point during the preamble period to optimize timing margins and then use the same skew time to capture the data during the rest of the read operation. The optimized capture point will be determined during the preamble period of every read operation. This optimization strategy is intended to compensate for both the PVT (process, voltage, temperature) of both the memory device and the host controller as well as any system level delays caused by flight time on the PCB.

Although the data learning pattern (DLP) is programmable, the following example shows example of the DLP of 34h. The DLP 34h (or 00110100) will be driven on each of the active outputs (i.e. all four SIOs). This pattern was chosen to cover both ‘DC’ and ‘AC’ data transition scenarios. The two DC transition scenarios include data low for a long period of time (two half clocks) followed by a high going transition (001) and the complementary low going transition (110). The two AC transition scenarios include data low for a short period of time (one half clock) followed by a high going transition (101) and the complementary low going transition (010). The DC transitions will typically occur with a starting point closer to the supply rail than the AC transitions that may not have fully settled to their steady state (DC) levels. In many cases the DC transitions will bound the beginning of the data valid period and the AC transitions will bound the ending of the data valid period. These transitions will allow the host controller to identify the beginning and ending of the valid data eye. Once the data eye has been characterized the optimal data capture point can be chosen. See **“SPI DDR Data Learning Registers”** on page 67 for more details.

In QPI mode (CR2V[6] = 1), the DDR Quad I/O instructions are sent 4 bits per SCK rising edge. The remainder of the command protocol is identical to the DDR Quad I/O commands.

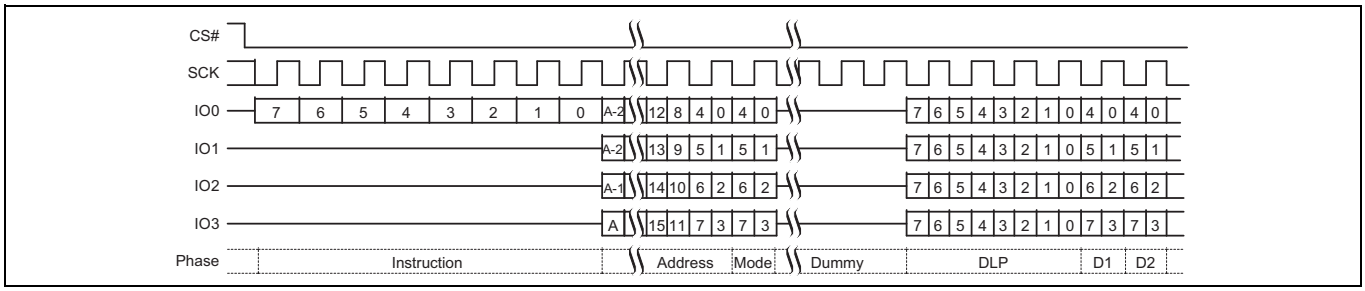


Figure 75 DDR Quad I/O Read Initial Access (EDh or EEh)[62, 63]

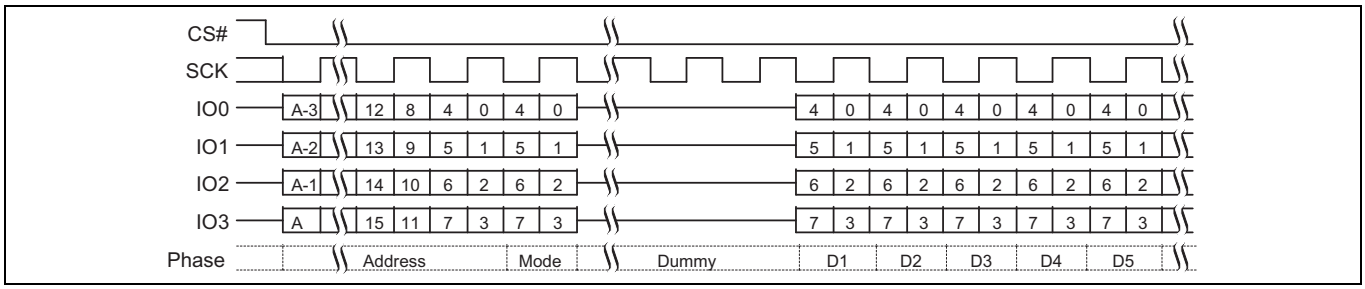


Figure 76 Continuous DDR Quad I/O Read Subsequent Access (EDh or EEh)[62, 63]

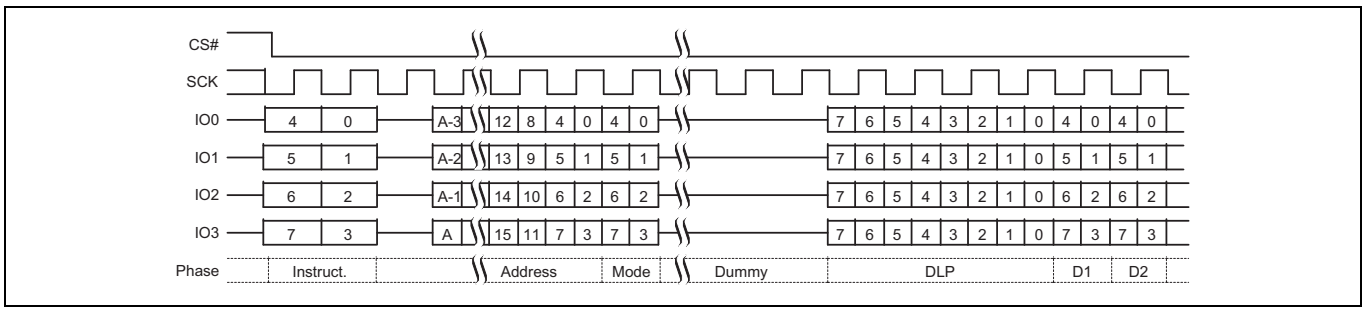


Figure 77 DDR Quad I/O Read Initial Access (EDh or EEh), QPI mode[62, 63]

Notes
62. A = MSb of address = 23 for Address length (CR2V[7] = 0, or 31 for CR2V[7] = 1 with command EDh.
63. A = MSb of address = 31 with command EEh.

9.5 Program Flash array commands

9.5.1 Program granularity

9.5.1.1 Automatic error correction code (ECC)

Each 16-byte aligned and 16 byte length Programming Block has an automatic ECC value. The data block plus ECC form an ECC unit. In combination with error detection and correction (EDC) logic the ECC is used to detect and correct any single bit error found during a read access. When data is first programmed within an ECC unit the ECC value is set for the entire ECC unit. If the same ECC unit is programmed more than once the ECC value is changed to disable the EDC function. A sector erase is needed to again enable Automatic ECC on that Programming Block. The 16-byte Program Block is the smallest program granularity on which automatic ECC is enabled.

These are automatic operations transparent to the user. The transparency of the automatic ECC feature enhances data accuracy for typical programming operations which write data once to each ECC unit but, facilitates software compatibility to previous generations of FL family of products by still allowing for single byte programming and bit walking in which the same ECC unit is programmed more than once. When an ECC unit has automatic ECC disabled, EDC is not done on data read from the ECC unit location.

An ECC status register is provided for determining if ECC is enabled on an ECC unit and whether any errors have been detected and corrected in the ECC unit data or the ECC. The ECC Status Register Read (ECCRD) command is used to read the ECC status on any ECC unit.

The EDCis applied to all parts of the Flash address spaces other than registers. An Error Correction Code (ECC) is calculated for each group of bytes protected and the ECC is stored in a hidden area related to the group of bytes. The group of protected bytes and the related ECC are together called an ECC unit.

- ECC is calculated for each 16-byte aligned and length ECC unit
- Single Bit EDC is supported with 8 ECC bits per ECC unit, plus 1-bit for an ECC disable Flag
- Sector erase resets all ECC disable flags in a sector to the default state (enabled)
- ECC is programmed as part of the standard Program commands operation
- ECC is disabled automatically if multiple programming operations are done on the same ECC unit.
- Single byte programming or bit walking is allowed but disables ECC on the second program to the same 16 byte ECC unit.
- The ECC disable flag is programmed when ECC is disabled
- To re-enable ECC for an ECC unit that has been disabled, the Sector that includes the ECC unit must be erased
- To ensure the best data integrity provided by EDC, each ECC unit should be programmed only once so that ECC is stored for that unit and not disabled.
- The calculation, programming, and disabling of ECC is done automatically as part of programming operations. The detection and correction, if needed is done automatically as part of read operations. The host system gets only corrected data from a read operation.
- ECC protects the OTP region — however a second program operation on the same ECC unit will disable ECC permanently on that ECC unit (OTP is one time programmable, hence an erase operation to re-enable the ECC enable/indicator bit is prohibited).

9.5.1.2 Page programming

The page programming is done by loading a Page Buffer with data to be programmed and issuing a programming command to move data from the buffer to the memory array. This sets an upper limit on the amount of data that can be programmed with a single programming command. The page programming allows up to a page size (either 256 or 512 bytes) to be programmed in one operation. The page size is determined by the configuration register bit CR3V[4]. The page is aligned on the page size address boundary. It is possible to program from one bit up to a page size in each page programming operation. It is recommended that a multiple of 16-byte length and aligned Program Blocks be written. This insures that automatic ECC is not disabled. For the very best performance, programming should be done in full pages of 512 bytes aligned on 512-byte boundaries with each page being programmed only once.

9.5.1.3 Single byte programming

The single byte programming allows full backward compatibility to the legacy standard SPI Page Programming (PP) command by allowing a single byte to be programmed anywhere in the memory array. While single byte programming is supported, this will disable automatic ECC on the 16-byte ECC unit where the byte is located.

9.5.2 Page Program (PP 02h or 4PP 12h)

The Page Program (PP) command allows bytes to be programmed in the memory (changing bits from 1 to 0). Before thePPcommands can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device. After the Write Enable (WREN) command has been decoded successfully, the device sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The instruction

- 02h (CR2V[7] = 0) is followed by a 3-byte address (A23-A0) or
- 02h (CR2V[7] = 1) is followed by a 4-byte address (A31-A0) or
- 12h is followed by a 4-byte address (A31-A0)

and at least one data byte on SI. Depending on CR3V[4], the page size can either be 256 or 512 bytes. Up to a page can be provided on SI after the 3-byte address with instruction 02h or 4-byte address with instruction 12h has been provided.

If more data is sent to the device than the space between the starting address and the page aligned end boundary, the data loading sequence will wrap from the last byte in the page to the zero byte location of the same page and begin overwriting any data previously loaded in the page. The last page worth of data is programmed in the page. This is a result of the device being equipped with a page program buffer that is only page size in length. If less than a page of data is sent to the device, these data bytes will be programmed in sequence, starting at the provided address within the page, without having any affect on the other bytes of the same page.

Using the PP command to load an entire page, within the page boundary, will save overall programming time versus loading less than a page into the program buffer.

The programming process is managed by the flash memory device internal control logic. After a programming command is issued, the programming operation status can be checked using the Read Status Register 1 command. The WIP bit (SR1V[0]) will indicate when the programming operation is completed. The P_ERR bit (SR1V[6]) will indicate if an error occurs in the programming operation that prevents successful completion of programming. This includes attempted programming of a protected area.

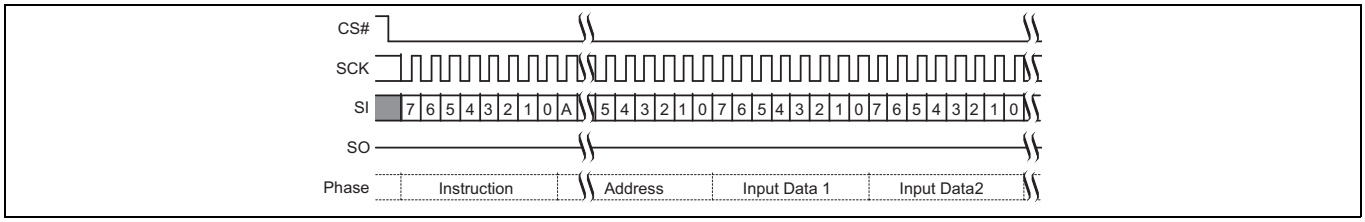


Figure 78 Page Program (PP 02h or 4PP 12h) command sequence[64]

This command is also supported in QPI mode. In QPI mode, the instruction is shifted to IO0-IO3, two clock cycles per byte.

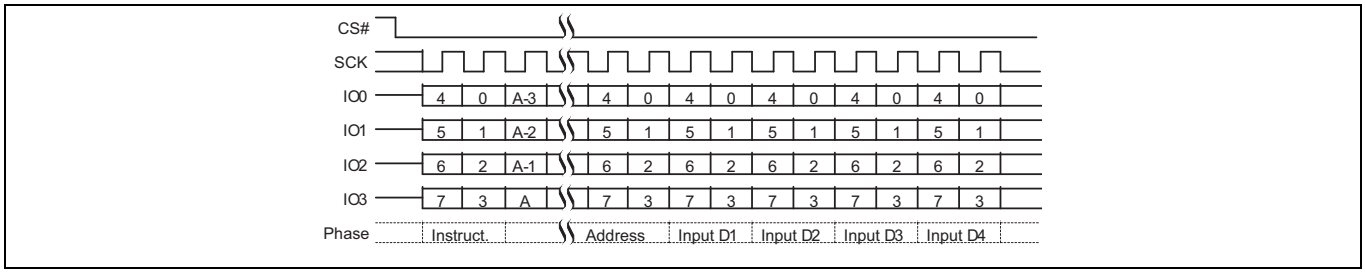


Figure 79 Page Program (PP 02h or 4PP 12h) QPI mode command sequence[64]

9.6 Erase Flash Array commands

9.6.1 Parameter 4 KB-Sector erase (P4E 20h or 4P4E 21h)

The main flash array address map may be configured to overlay 4-KB parameter sectors over the lowest address portion of the lowest address uniform sector (bottom parameter sectors) or over the highest address portion of the highest address uniform sector (top parameter sectors). The main flash array address map may also be configured to have only uniform size sectors. The parameter sector configuration is controlled by the configuration bit CR3V[3]. The P4E and 4P4E commands are ignored when the device is configured for uniform sectors only (CR3V[3] = 1).

The Parameter 4 KB-sector Erase commands set all the bits of a 4-KB parameter sector to 1 (all bytes are FFh). Before the P4E or 4P4E command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The instruction

- 20h [CR2V[7] = 0] is followed by a 3-byte address (A23-A0), or
- 20h [CR2V[7] = 1] is followed by a 4-byte address (A31-A0), or
- 21h is followed by a 4-byte address (A31-A0)

CS# must be driven into the logic HIGH state after the twenty-fourth or thirty-second bit of the address has been latched ito SI. This will initiate the beginning of internal erase cycle, which involves the pre-programming and erase of the chosen sector of the flash memory array. If CS# is not driven HIGH after the last bit of address, the sector erase operation will not be executed.

As soon as CS# is driven HIGH, the internal erase cycle will be initiated. With the internal erase cycle in progress, the user can read the value of the Write-In Progress (WIP) bit to determine when the operation has been

Note
64. A = MSb of address = A23 for PP 02h, or A31 for 4PP 12h.

completed. The WIP bit will indicate a '1'. when the erase cycle is in progress and a '0' when the erase cycle has been completed.

A P4E or 4P4E command applied to a sector that has been write protected through the Block Protection bits or ASP, will not be executed and will set the E_ERR status. A P4E command applied to a sector that is larger than 4 KB will not be executed and will not set the E_ERR status.

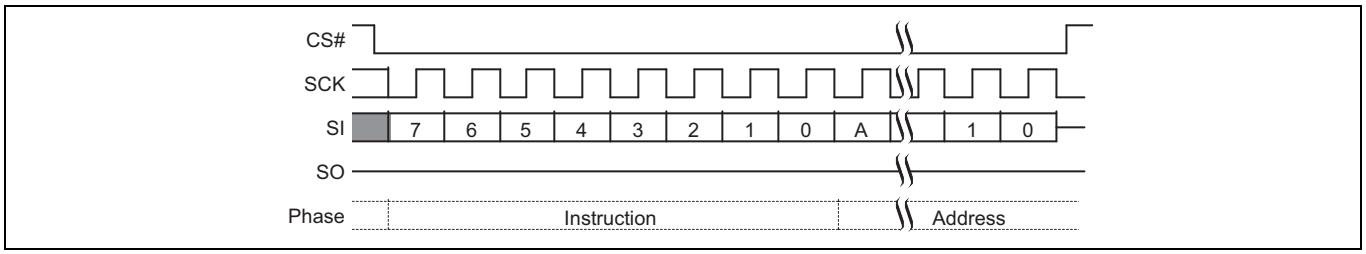


Figure 80 Parameter Sector Erase (P4E 20h or 4P4E 21h) command sequence[65]

This command is also supported in QPI mode. In QPI mode, the instruction is shifted to IO0-IO3, two clock cycles per byte.

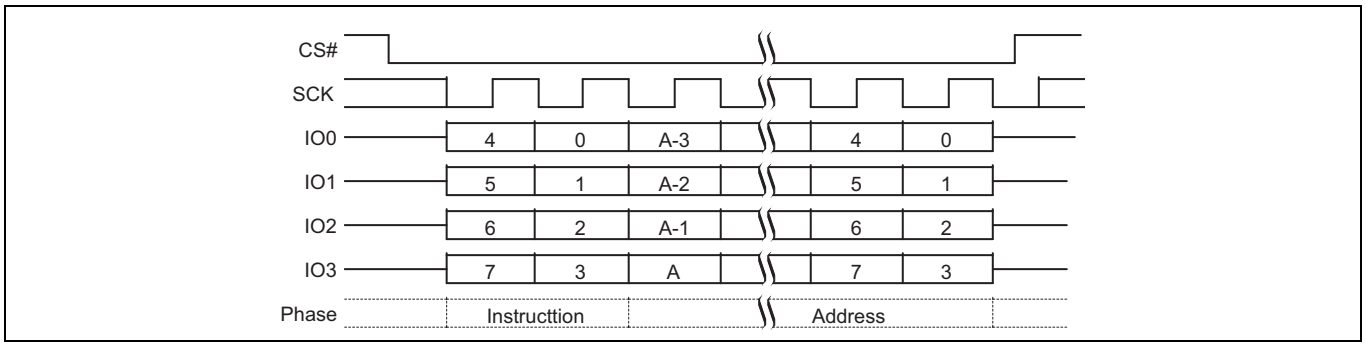


Figure 81 Parameter Sector Erase (P4E 20h or 4P4E 21h) QPI mode command sequence[65]

9.6.2 Sector Erase (SE D8h or 4SE DCh)

The Sector Erase (SE) command sets all bits in the addressed sector to 1 (all bytes are FFh). Before the Sector Erase (SE) command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The instruction

- D8h [CR2V[7] = 0] is followed by a 3-byte address (A23-A0), or
- D8h [CR2V[7] = 1] is followed by a 4-byte address (A31-A0), or
- DCh is followed by a 4-byte address (A31-A0)

CS# must be driven into the logic HIGH state after the twenty-fourth or thirty-second bit of address has been latched in on SI. This will initiate the erase cycle, which involves the pre-programming and erase of the chosen sector. If CS# is not driven HIGH after the last bit of address, the sector erase operation will not be executed.

As soon as CS# is driven into the logic HIGH state, the internal erase cycle will be initiated. With the internal erase cycle in progress, the user can read the value of the Write-In Progress (WIP) bit to check if the operation has been

Note
65. A = MSb of address = A23 for P4E 20h with CR2V[7] = 0, or A31 for P4E 20h with CR2V[7] = 1 or 4P4E 21h.

completed. The WIP bit will indicate a '1' when the erase cycle is in progress and a '0' when the erase cycle has been completed.

A Sector Erase (SE) command applied to a sector that has been Write Protected through the Block Protection bits or ASP, will not be executed and will set the E_ERR status.

A device configuration option (CR3V[3]) determines whether 4-KB parameter sectors are in use. When CR3V[3] = 0, 4-KB parameter sectors overlay a portion of the highest or lowest address 32-KB of the device address space. If a sector erase command is applied to a 256-KB range that is overlaid by 4-KB sectors, the overlaid 4-KB sectors are not affected by the erase. When CR3V[3] = 1, there are no 4-KB parameter sectors in the device address space and the Sector Erase command always operates on fully visible 256-KB sectors.

ASP has a PPB and a DYB protection bit for each physical sector, including any 4-KB sectors.

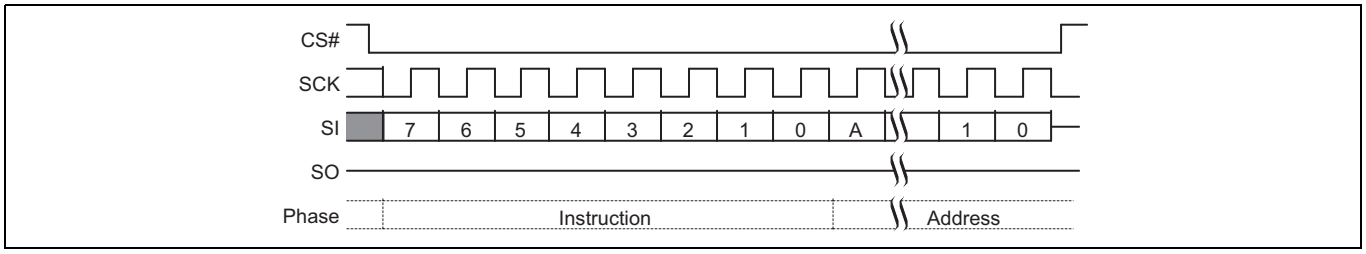


Figure 82 Sector Erase (SE D8h or 4SE DCh) command sequence[66]

This command is also supported in QPI mode. In QPI mode, the instruction is shifted in on IO0-IO3, two clock cycles per byte.

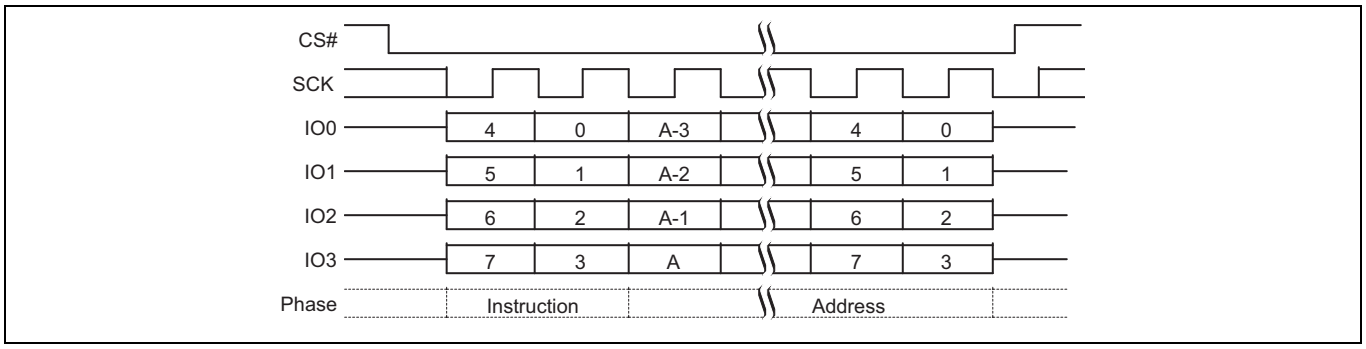


Figure 83 Sector Erase (SE D8h or 4SE DCh) QPI mode command sequence[66]

Note
66. A = MSb of address = A23 for SE D8h with CR2V[7] = 0, or A31 for SE D8h with CR2V[7] = 1 or 4P4E DCh.

9.6.3 Bulk Erase (BE 60h or C7h)

The Bulk Erase (BE) command sets all bits to 1 (all bytes are FFh) inside the entire flash memory array. Before the BE command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

CS# must be driven into the logic HIGH state after the eighth bit of the instruction byte has been latched in on SI. This will initiate the erase cycle, which involves the pre-programming and erase of the entire flash memory array. If CS# is not driven HIGH after the last bit of instruction, the BE operation will not be executed.

As soon as CS# is driven into the logic HIGH state, the erase cycle will be initiated. With the erase cycle in progress, the user can read the value of the Write-In Progress (WIP) bit to determine when the operation has been completed. The WIP bit will indicate a '1' when the erase cycle is in progress and a '0' when the erase cycle has been completed.

A BE command can be executed only when the Block Protection (BP2, BP1, BP0) bits are set to '0's. If the BP bits are not zero, the BE command is not executed and E_ERR is not set. The BE command will skip any sectors protected by the DYB or PPB and the E_ERR status will not be set.

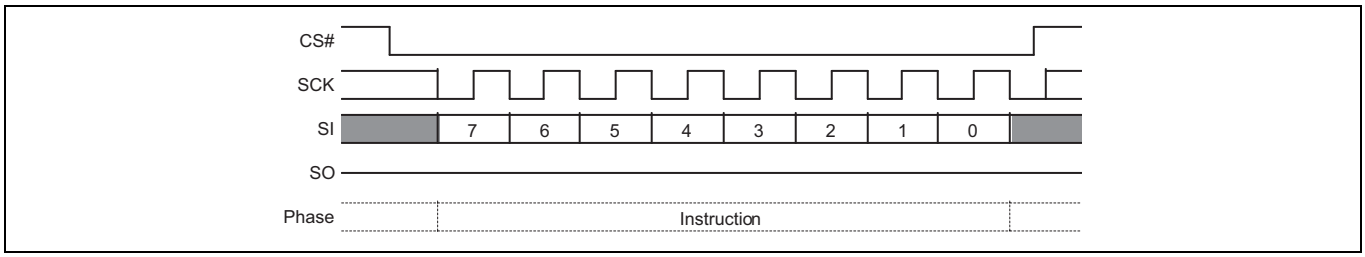


Figure 84 Bulk Erase command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted to IO0-IO3, two clock cycles per byte.

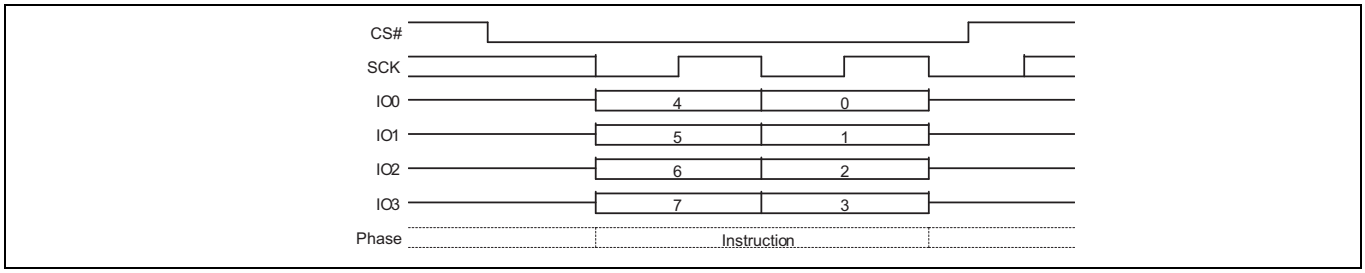


Figure 85 Bulk Erase command sequence QPI mode

9.6.4 Evaluate Erase Status (EES D0h)

The Evaluate Erase Status (EES) command verifies that the last erase operation on the addressed sector was completed successfully. If the selected sector was successfully erased the erase status bit (SR2V[2]) is set to '1'. If the selected sector was not completely erased SR2V[2] is '0'.

The EES command can be used to detect erase operations failed due to loss of power, reset, or failure during the erase operation.

The EES instruction is followed by a 3- or 4-byte address, depending on the address length configuration (CR2V[7]). The EES command requires tEES to complete and update the erase status in SR2V. The WIP bit (SR1V[0]) may be read using the RDSR1 (05h) command, to determine when the EES command is finished. Then the RDSR2 (07h) or the RDAR (65h) command can be used to read SR2V[2]. If a sector is found not erased with SR2V[2] = 0, the sector must be erased again to ensure reliable storage of data in the sector.

The Write Enable command (to set the WEL bit) is not required before the EES command. However, the WEL bit is set by the device itself and cleared at the end of the operation, as visible in SR1V[1] when reading status.

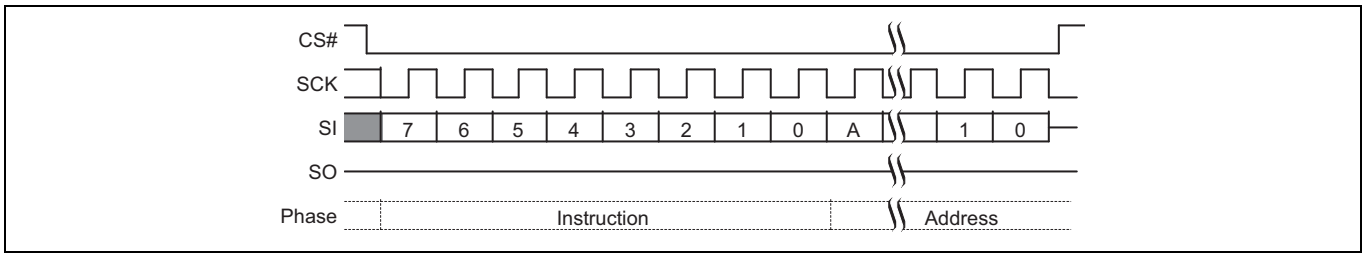


Figure 86 EES command sequence[66]

This command is also supported in QPI mode. In QPI mode, the instruction is shifted to IO0-IO3, two clock cycles per byte.

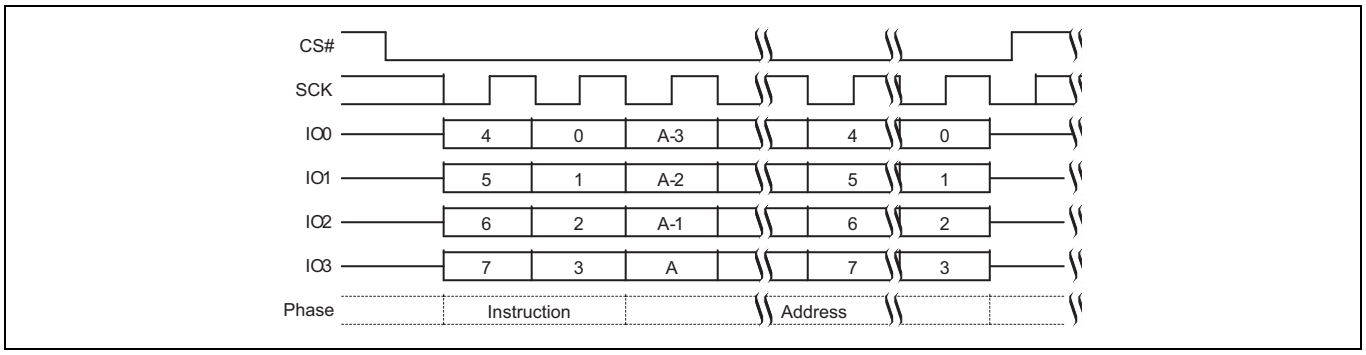


Figure 87 EES QPI mode command sequence[66]

Note
67. A = MSb of address = A23 for CR2V[7] = 0, or A31 for CR2V[7] = 1.

9.6.5 Erase or Program Suspend (EPS 85h, 75h, B0h)

There are three instruction codes for Program or Erase Suspend (EPS) to enable legacy and alternate source software compatibility.

The EPS command allows the system to interrupt a programming or erase operation and then read from any other non-erase-suspended sector or non-program-suspended-page. The program or erase suspend is valid only during a programming or sector erase operation. A Bulk Erase operation cannot be suspended.

The Write-iIn Progress (WIP) bit in Status Register 1 (SR1V[0]) must be checked to know when the programming or erase operation has stopped. The Program Suspend Status bit in the Status Register 2 (SR2[0]) can be used to determine if a programming operation has been suspended or was completed at the time WIP changes to '0'. The Erase Suspend Status bit in the Status Register 2 (SR2[1]) can be used to determine if an erase operation has been suspended or was completed at the time WIP changes to 0. The time required for the suspend operation to complete is t_{SL} (see **Table 51**).

An erase can be suspended to allow a program operation or a read operation. During an erase suspend, the DYB array may be read to examine sector protection and written to remove or restore protection on a sector to be programmed.

A program operation may be suspended to allow a read operation.

A new erase operation is not allowed with an already suspended erase or program operation. An erase command is ignored in this situation.

Table 49 Commands allowed during program or erase suspend

Instruction name	Instruction code (hex)	Allowed during erase suspend	Allowed during program suspend	Comment
PP	02	X	–	Required for array program during erase suspend. Only allowed if there is no other program suspended program operation (SR2V[0] = 0). A program command will be ignored while there is a suspended program. If a program command is sent for a location within an erase suspended sector the program operation will fail with the P_ERR bit set.
READ	03		X	All array reads allowed in suspend.
RDSR1	05			Needed to read WIP to determine end of suspend process.
RDAR	65			Alternate way to read WIP to determine end of suspend process.
WREN	06			Required for program command within erase suspend.
RDSR2	07			Needed to read suspend status to determine whether the operation is suspended or complete.

Table 49 Commands allowed during program or erase suspend *(continued)*

Instruction name	Instruction code (hex)	Allowed during erase suspend	Allowed during program suspend	Comment
4PP	12	X	–	Required for array program during erase suspend. Only allowed if there is no other program suspended program operation (SR2V[0] = 0). A program command will be ignored while there is a suspended program. If a program command is sent for a location within an erase suspended sector the program operation will fail with the P_ERR bit set.
4READ	13		X	All array reads allowed in suspend.
CLSR	30		–	Clear status may be used if a program operation fails during erase suspend. Note the instruction is only valid if enabled for clear status by CR4NV[2=1].
CLSR	82		–	Clear status may be used if a program operation fails during erase suspend.
EPR	30		X	Required to resume from erase or program suspend. Note the command must be enabled for use as a resume command by CR3NV[2] = 1.
EPR	7A			Required to resume from erase or program suspend.
EPR	8A			
RSTEN	66			Reset allowed anytime.
RST	99			
FAST_READ	0B			All array reads allowed in suspend.
4FAST_READ	0C			
EPR	7A		–	Required to resume from erase suspend.
EPR	8A			
DIOR	BB		X	All array reads allowed in suspend.
4DIOR	BC			
DYBRD	FA		–	It may be necessary to remove and restore dynamic protection during erase suspend to allow programming during erase suspend.
DYBWR	FB			It may be necessary to remove and restore dynamic protection during erase suspend to allow programming during erase suspend.
PPBRD	FC			Allowed for checking persistent protection before attempting a program command during erase suspend.

Table 49 Commands allowed during program or erase suspend *(continued)*

Instruction name	Instruction code (hex)	Allowed during erase suspend	Allowed during program suspend	Comment
4DYBRD	E0	X	–	It may be necessary to remove and restore dynamic protection during erase suspend to allow programming during erase suspend.
4DYBWR	E1			
4PPBRD	E2			Allowed for checking persistent protection before attempting a program command during erase suspend.
QIOR	EB		X	All array reads allowed in suspend.
4QIOR	EC			
DDRQIOR	ED			
4DDRQIOR	EE			
RESET	F0			Reset allowed anytime.
MBR	FF			May need to reset a read operation during suspend.

Reading at any address within an erase-suspended sector or program-suspended page produces undetermined data.

The WRR, WRAR, or PPB Erase commands are not allowed during the Erase or Program Suspend, it is therefore not possible to alter the Block Protection or PPB bits during Erase Suspend. If there are sectors that may need programming during Erase suspend, these sectors should be protected only by DYB bits that can be turned OFF during Erase Suspend.

After an erase-suspended program operation is complete, the device returns to the erase-suspend mode. The system can determine the status of the program operation by reading the WIP bit in the Status Register, just as in the standard program operation.

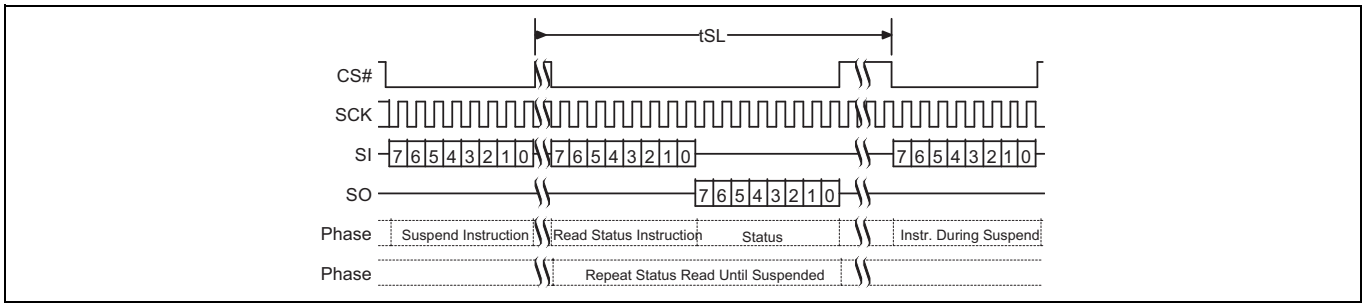


Figure 88 Program or Erase Suspend command sequence

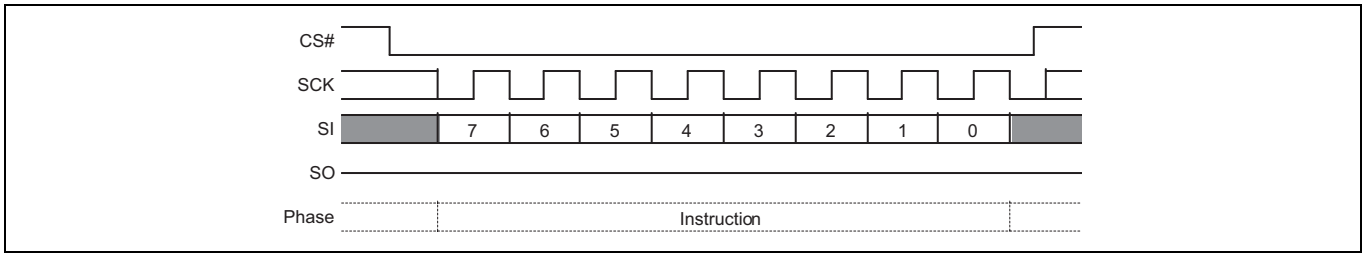


Figure 89 Erase or Program Suspend command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted to IO0-IO3, two clock cycles per byte.

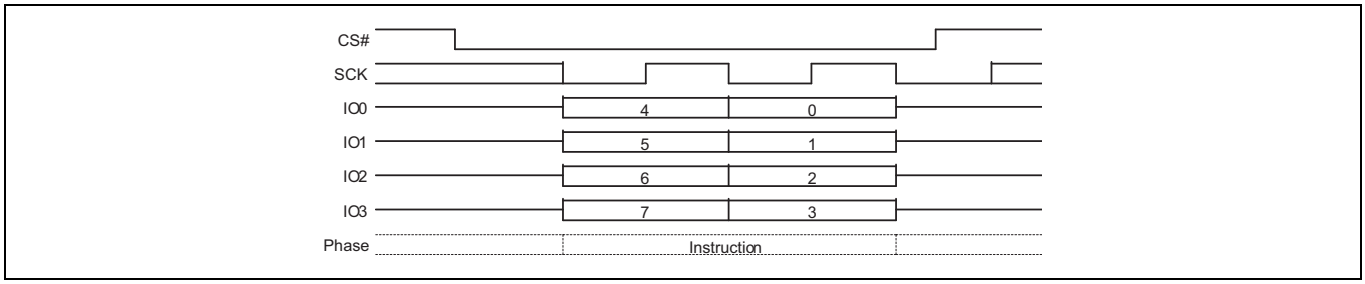


Figure 90 Erase or Program Suspend command sequence QPI mode

9.6.6 Erase or Program Resume (EPR 7Ah, 8Ah, 30h)

An Erase or Program Resume command must be written to resume a suspended operation. There are three instruction codes for Erase or Program Resume (EPR) to enable legacy and alternate source software compatibility.

After program or read operations are completed during a program or erase suspend the Erase or Program Resume command is sent to continue the suspended operation.

After an Erase or Program Resume command is issued, the WIP bit in the Status Register 1 will be set to ‘1’ and the programming operation will resume if one is suspended. If no program operation is suspended the suspended erase operation will resume. If there is no suspended program or erase operation the resume command is ignored.

Program or erase operations may be interrupted as often as necessary, e.g. a program suspend command could immediately follow a program resume command but, in order for a program or erase operation to progress to completion there must be some periods of time between resume and the next suspend command greater than or equal to t_{RS} (see **Table 51**).

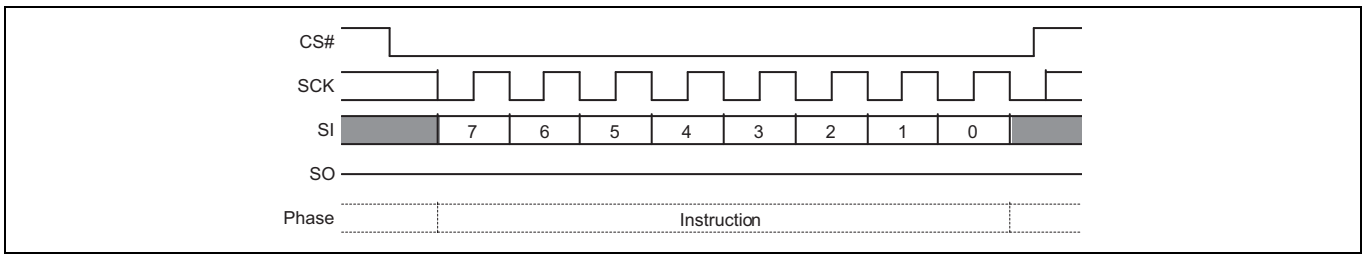


Figure 91 Erase or Program Resume command sequence

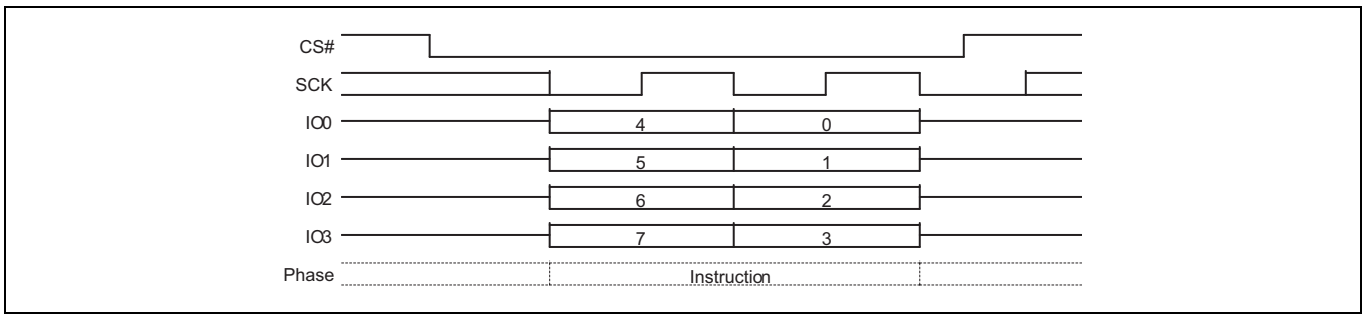


Figure 92 Erase or Program Resume command sequence QPI mode

9.7 One time program array commands

9.7.1 OTP Program (OTPP 42h)

The OTP Program command programs data in the One Time Program region, which is in a different address space from the main array data. The OTP region is 1024 bytes so, the address bits from A31 to A10 must be zero for this command. Refer to **“OTP address space”** on page 49 for details on the OTP region.

Before the OTP Program command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the status register to enable any write operations. The WIP bit in SR1V may be checked to determine when the operation is completed. The P_ERR bit in SR1V may be checked to determine if any error occurred during the operation.

To program the OTP array in bit granularity, the rest of the bits within a data byte can be set to ‘1’.

Each region in the OTP memory space can be programmed one or more times, provided that the region is not locked. Attempting to program zeros in a region that is locked will fail with the P_ERR bit in SR1V set to ‘1’. Programming ones, even in a protected area does not cause an error and does not set P_ERR. Subsequent OTP programming can be performed only on the un-programmed bits (that is, 1 data). Programming more than once within an ECC unit will disable ECC on that unit.

The protocol of the OTP Program command is the same as the Page Program command. See **“Page Program (PP 02h or 4PP 12h)”** on page 108 for the command sequence.

9.7.2 OTP Read (OTPR 4Bh)

The OTP Read command reads data from the OTP region. The OTP region is 1024 bytes so, the address bits from A31 to A10 must be zero for this command. Refer to **“OTP address space”** on page 49 for details on the OTP region. The protocol of the OTP Read command is similar to the Fast Read command except that it will not wrap to the starting address after the OTP address is at its maximum; instead, the data beyond the maximum OTP address will be undefined. The OTP Read command read latency is set by the latency value in CR2V[3:0]. See **“Fast Read (FAST_READ 0Bh or 4FAST_READ 0Ch)”** on page 100 for the command sequence.

9.8 Advanced Sector Protection commands

9.8.1 ASP Read (ASPRD 2Bh)

The ASP Read instruction 2Bh is shifted into SI by the rising edge of the SCK signal. Then the 16-bit ASP register contents are shifted out on the serial output SO, least significant byte first. Each bit is shifted out at the SCK frequency by the falling edge of the SCK signal. It is possible to read the ASP register continuously by providing multiples of 16 clock cycles. The maximum operating clock frequency for the ASP Read (ASPRD) command is 133 MHz.

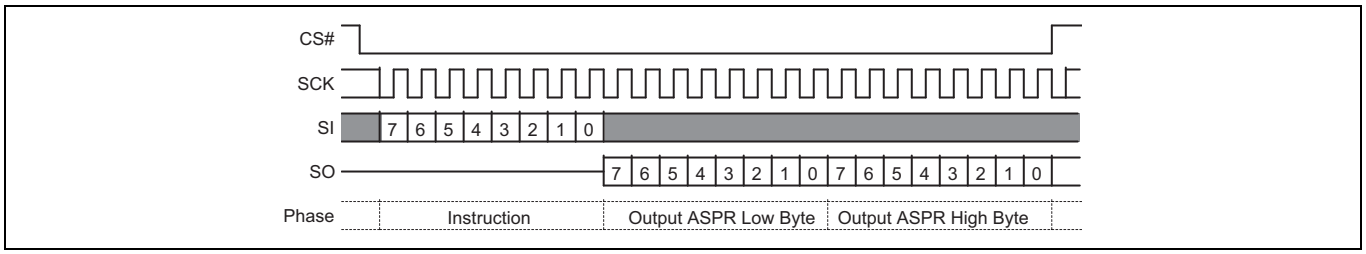


Figure 93 ASPRD command

9.8.2 ASP Program (ASPP 2Fh)

Before the ASP Program (ASPP) command can be accepted by the device, a Write Enable (WREN) command must be issued. After the Write Enable (WREN) command has been decoded, the device will set the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The ASPP command is entered by driving CS# to the logic LOW state, followed by the instruction and two data bytes on SI, least significant byte first. The ASP Register is two data bytes in length.

The ASPP command affects the P_ERR and WIP bits of the status and configuration registers in the same manner as any other programming operation.

CS# input must be driven to the logic HIGH state after the sixteenth bit of data has been latched in. If not, the ASPP command is not executed. As soon as CS# is driven to the logic HIGH state, the self-timed ASPP operation is initiated. While the ASPP operation is in progress, the status register may be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is a ‘1’ during the self-timed ASPP operation, and is a ‘0’ when it is completed. When the ASPP operation is completed, the Write Enable Latch (WEL) is set to ‘0’.

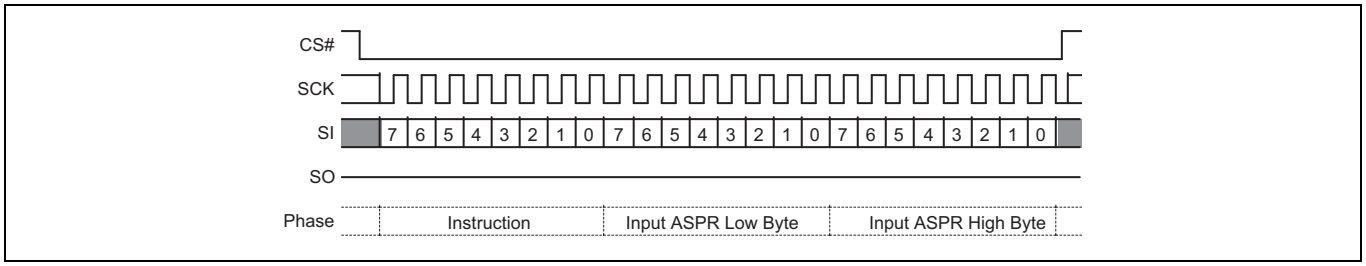


Figure 94 ASPP command

9.8.3 DYB Read (DYBRD FAh or 4DYBRD E0h)

The instruction is latched into SI by the rising edge of the SCK signal. The instruction is followed by the 24- or 32-bit address, depending on the address length configuration CR2V[7], selecting location zero within the desired sector. Note, the high order address bits not used by a particular density device must be zero. Then the 8-bit DYB access register contents are shifted out on the serial output SO. Each bit is shifted out at the SCK frequency by the falling edge of the SCK signal. It is possible to read the same DYB access register continuously by providing multiples of eight clock cycles. The address of the DYB register does not increment so this is not a means to read the entire DYB array. Each location must be read with a separate DYB Read command. The maximum operating clock frequency for READ command is 133 MHz.

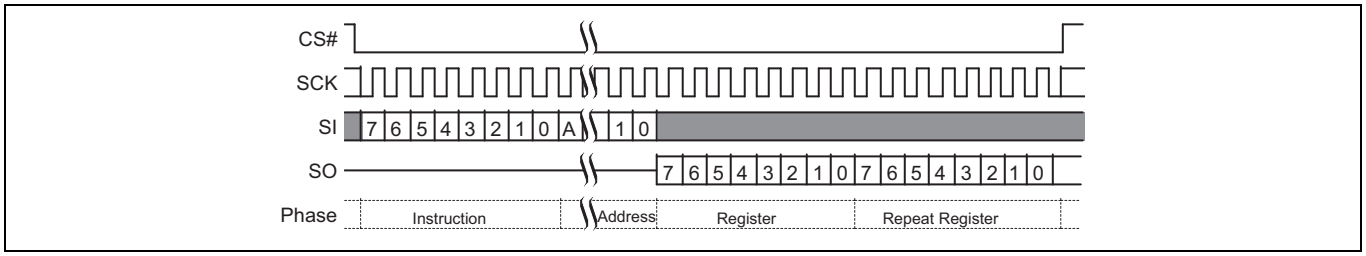


Figure 95 DYBRD command sequence[68, 69]

This command is also supported in QPI mode. In QPI mode, the instruction and address is shifted to IO0-IO3 and returning data is shifted out on IO0-IO3.

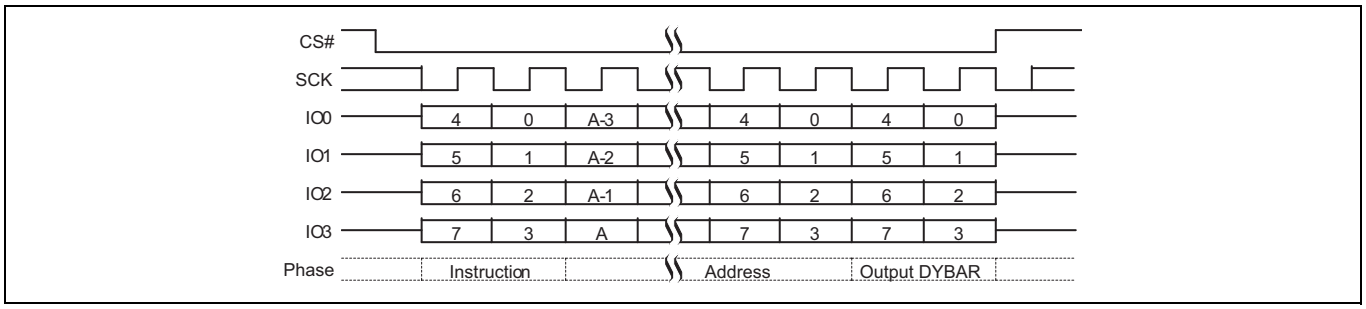


Figure 96 DYBRD QPI mode command sequence[68, 69]

Note
68. A = MSb of address = 23 for Address length (CR2V[7] = 0, or 31 for CR2V[7] = 1 with command FAh.
69. A = MSb of address = 31 with command E0h.

9.8.4 DYB Write (DYBWR FBh or 4DYBWR E1h)

Before the DYB Write (DYBWR) command can be accepted by the device, a Write Enable (WREN) command must be issued. After the Write Enable (WREN) command has been decoded, the device will set the Write Enable Latch (WEL) in the status register to enable any write operations.

The DYBWR command is entered by driving CS# to the logic LOW state, followed by the instruction, followed by the 24- or 32-bit address, depending on the address length configuration CR2V[7], selecting location zero within the desired sector (note, the high order address bits not used by a particular density device must be zero), then the data byte on SI. The DYB Access Register is one data byte in length. The data value must be 00h to protect or FFh to unprotect the selected sector.

The DYBWR command affects the P_ERR and WIP bits of the status and configuration registers in the same manner as any other programming operation. CS# must be driven to the logic HIGH state after the eighth bit of data has been latched in. As soon as CS# is driven to the logic HIGH state, the self-timed DYBWR operation is initiated. While the DYBWR operation is in progress, the status register may be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is a '1' during the self-timed DYBWR operation, and is a '0' when it is completed. When the DYBWR operation is completed, the Write Enable Latch (WEL) is set to '0'.

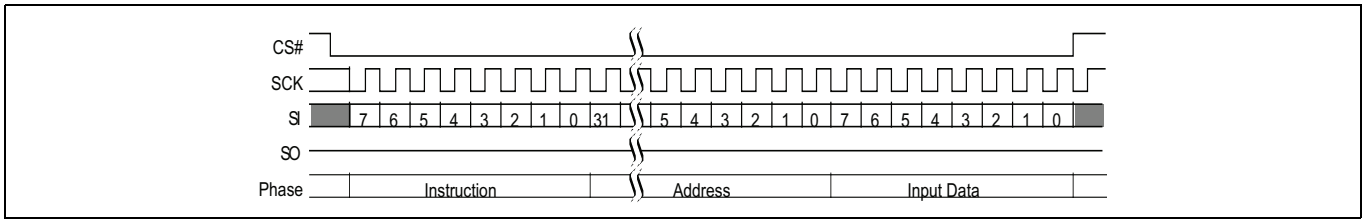


Figure 97 DYBWR command sequence[70, 71]

This command is also supported in QPI mode. In QPI mode, the instruction is shifted to IO0-IO3, two clock cycles per byte.

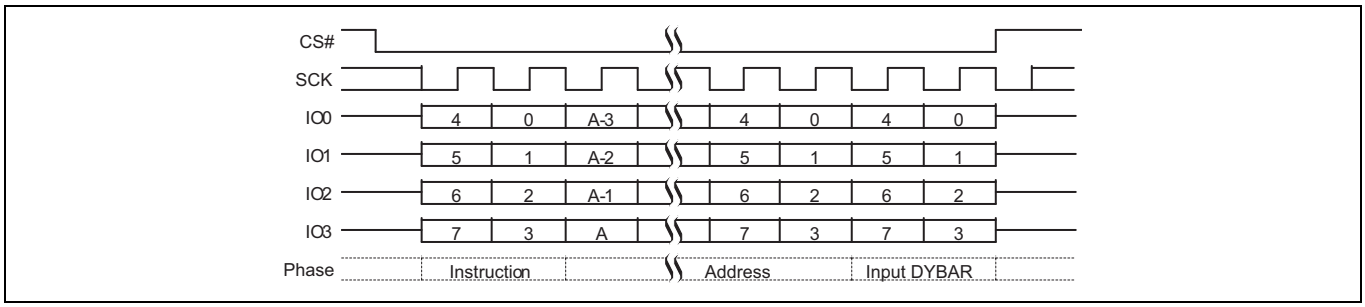


Figure 98 DYBWR QPI mode command sequence[70, 71]

Note
70. A = MSb of address = 23 for Address length (CR2V[7] = 0, or 31 for CR2V[7] = 1 with command FBh.
71. A = MSb of address = 31 with command E1h.

9.8.5 PPB Read (PPBRD FCh or 4PPBRD E2h)

The instruction E2h is shifted into SI by the rising edges of the SCK signal, followed by the 24- or 32-bit address, depending on the address length configuration CR2V[7], selecting location zero within the desired sector (note, the high order address bits not used by a particular density device must be zero). Then the 8-bit PPB access register contents are shifted out on SO.

It is possible to read the same PPB access register continuously by providing multiples of eight clock cycles. The address of the PPB register does not increment so this is not a means to read the entire PPB array. Each location must be read with a separate PPB Read command. The maximum operating clock frequency for the PPB Read command is 133 MHz.

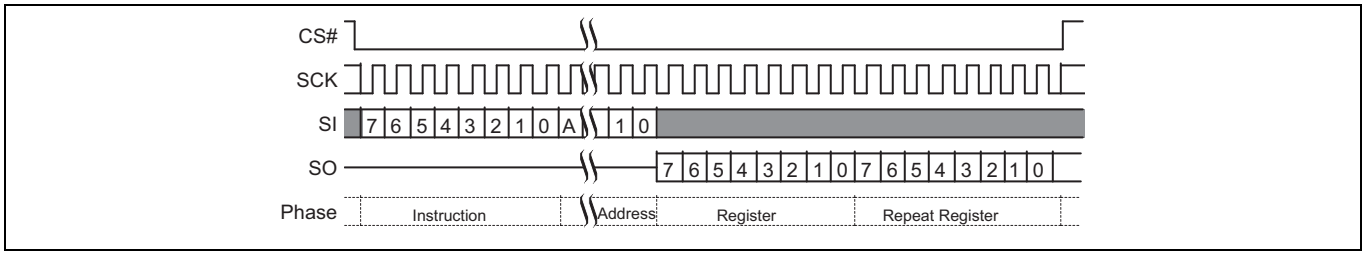


Figure 99 PPBRD command sequence[72, 73]

9.8.6 PPB Program (PPBP FDh or 4PPBP E3h)

Before the PPB Program (PPBP) command can be accepted by the device, a Write Enable (WREN) command must be issued. After the Write Enable (WREN) command has been decoded, the device will set the Write Enable Latch (WEL) in the status register to enable any write operations.

The PPBP command is entered by driving CS# to the logic LOW state, followed by the instruction, followed by the 24 or 32-bit address, depending on the address length configuration CR2V[7], selecting location zero within the desired sector (note, the high order address bits not used by a particular density device must be zero).

The PPBP command affects the P_ERR and WIP bits of the status and configuration registers in the same manner as any other programming operation.

CS# must be driven to the logic HIGH state after the last bit of address has been latched in. If not, the PPBP command is not executed. As soon as CS# is driven to the logic HIGH state, the self-timed PPBP operation is initiated. While the PPBP operation is in progress, the status register may be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is a '1' during the self-timed PPBP operation, and is a '0' when it is completed. When the PPBP operation is completed, the Write Enable Latch (WEL) is set to '0'.

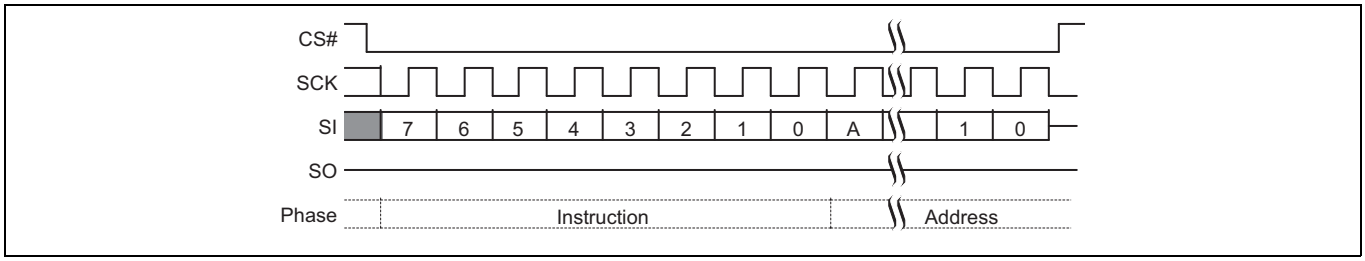


Figure 100 PPBP command sequence[74, 75]

Notes
72. A = MSb of address = 23 for Address length (CR2V[7] = 0, or 31 for CR2V[7] = 1 with command FCh.
73. A = MSb of address = 31 with command E2h.
74. A = MSb of address = 23 for Address length (CR2V[7] = 0, or 31 for CR2V[7] = 1 with command FDh.
75. A = MSb of address = 31 with command E3h.

9.8.7 PPB Erase (PPBE E4h)

The PPB Erase (PPBE) command sets all PPB bits to 1. Before the PPB Erase command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the status register to enable any write operations.

The instruction E4h is shifted into SI by the rising edges of the SCK signal.

CS# must be driven into the logic HIGH state after the eighth bit of the instruction byte has been latched in on SI. This will initiate the beginning of internal erase cycle, which involves the pre-programming and erase of the entire PPB memory array. Without CS# being driven to the logic HIGH state after the eighth bit of the instruction, the PPB erase operation will not be executed.

With the internal erase cycle in progress, the user can read the value of the Write-In Progress (WIP) bit to check if the operation has been completed. The WIP bit will indicate a '1' when the erase cycle is in progress and a '0' when the erase cycle has been completed. The Erase suspend is not allowed during PPB Erase.

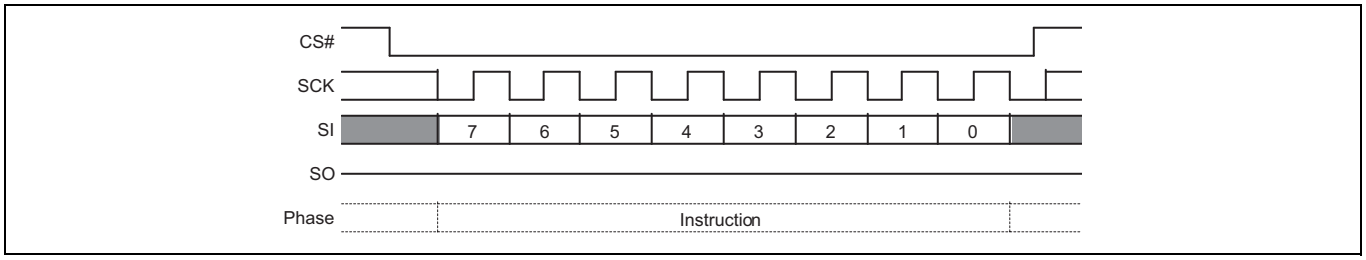


Figure 101 PPB erase command sequence

9.8.8 PPB Lock Bit Read (PLBRD A7h)

The PPB Lock Bit Read (PLBRD) command allows the PPB Lock Register contents to be read out of SO. It is possible to read the PPB lock register continuously by providing multiples of eight clock cycles. The PPB Lock Register contents may only be read when the device is in standby state with no other operation in progress. It is recommended to check the Write-In Progress (WIP) bit of the status register before issuing a new command to the device.

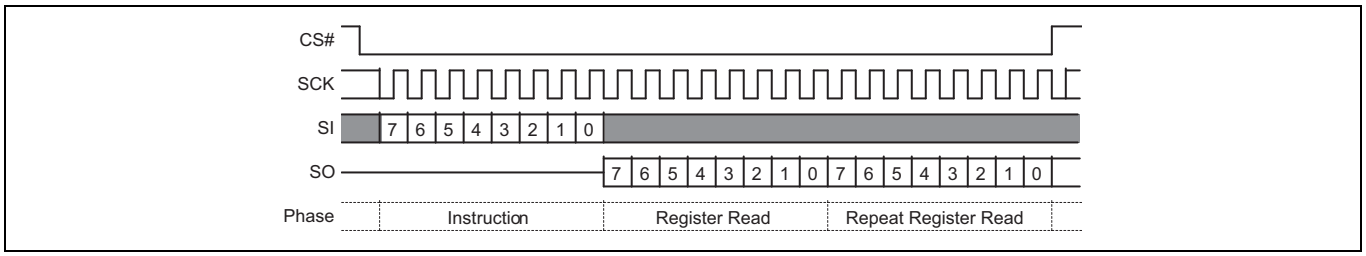


Figure 102 PPB Lock Register Read command sequence

9.8.9 PPB Lock Bit Write (PLBWR A6h)

The PPB Lock Bit Write (PLBWR) command clears the PPB Lock Register to zero. Before the PLBWR command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device, which sets the Write Enable Latch (WEL) in the Status Register to enable any write operations.

The PLBWR command is entered by driving CS# to the logic LOW state, followed by the instruction.

CS# must be driven to the logic HIGH state after the eighth bit of instruction has been latched in. If not, the PLBWR command is not executed. As soon as CS# is driven to the logic HIGH state, the self-timed PLBWR operation is initiated. While the PLBWR operation is in progress, the status register may still be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is a '1' during the self-timed PLBWR operation, and is a '0' when it is completed. When the PLBWR operation is completed, the Write Enable Latch (WEL) is set to '0'. The maximum clock frequency for the PLBWR command is 133 MHz.

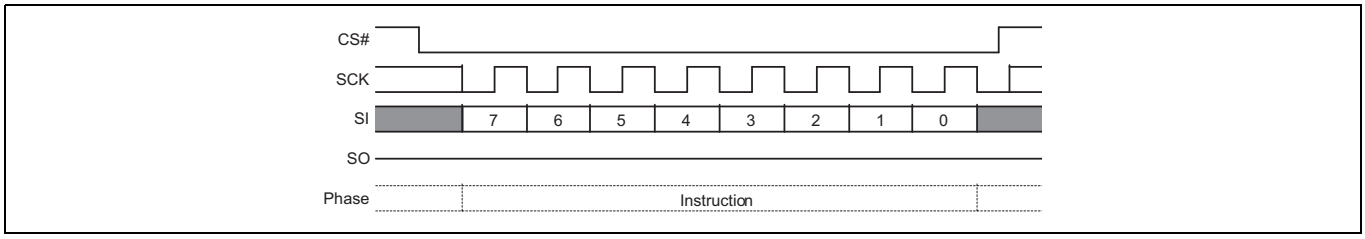


Figure 103 PPB Lock Bit Write command sequence

9.8.10 Password Read (PASSRD E7h)

The correct password value may be read only after it is programmed and before the Password Mode has been selected by programming the Password Protection Mode bit to '0' in the ASP Register (ASP[2]). After the Password Protection mode is selected the password is no longer readable, the PASSRD command will output undefined data.

The PASSRD command is shifted into SI. Then the 64-bit password is shifted out on the serial output SO, least significant byte first, most significant bit of each byte first. Each bit is shifted out at the SCK frequency by the falling edge of the SCK signal. It is possible to read the password continuously by providing multiples of 64 clock cycles. The maximum operating clock frequency for the PASSRD command is 133 MHz.

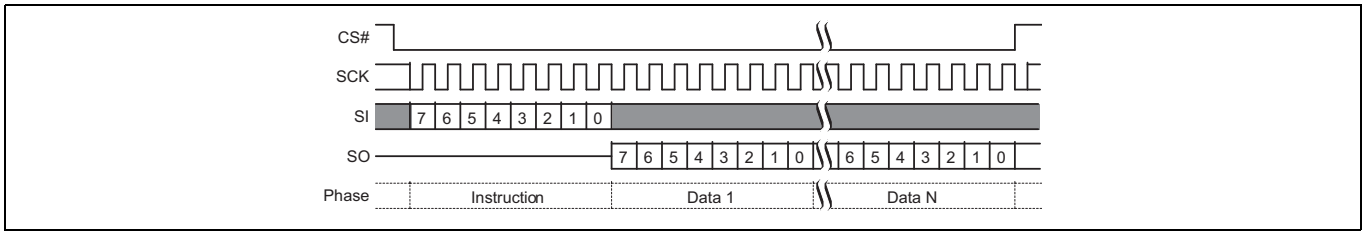


Figure 104 Password Read command sequence

9.8.11 Password Program (PASSP E8h)

Before the Password Program (PASSP) command can be accepted by the device, a Write Enable (WREN) command must be issued and decoded by the device. After the Write Enable (WREN) command has been decoded, the device sets the Write Enable Latch (WEL) to enable the PASSP operation.

The password can only be programmed before the Password Mode is selected by programming the Password Protection Mode bit to '0' in the ASP Register (ASP[2]). After the Password Protection ,ode is selected the PASSP command is ignored.

The PASSP command is entered by driving CS# to the logic LOW state, followed by the instruction and the password data bytes on SI, least significant byte first, most significant bit of each byte first. The password is 64 bits in length.

CS# must be driven to the logic HIGH state after the 64th bit of data has been latched. If not, the PASSP command is not executed. As soon as CS# is driven to the logic HIGH state, the self-timed PASSP operation is initiated. While the PASSP operation is in progress, the status register may be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is a '1' during the self-timed PASSP cycle, and is a '0' when it is completed. The PASSP command can report a program error in the P_ERR bit of the status register. When the PASSP operation is completed, the Write Enable Latch (WEL) is set to '0'. The maximum clock frequency for the PASSP command is 133 MHz.

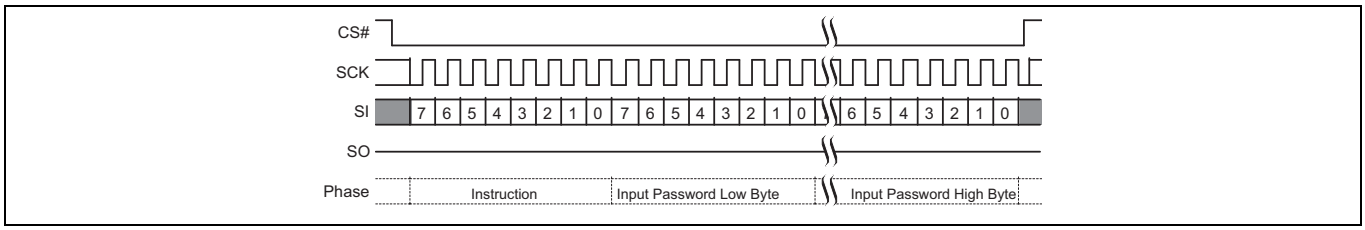


Figure 105 Password Program command sequence

9.8.12 Password Unlock (PASSU E9h)

The PASSU command is entered by driving CS# to the logic LOW state, followed by the instruction and the password data bytes on SI, least significant byte first, most significant bit of each byte first. The password is 64 bits in length.

CS# must be driven to the logic HIGH state after the 64th bit of data has been latched. If not, the PASSU command is not executed. As soon as CS# is driven to the logic HIGH state, the self-timed PASSU operation is initiated. While the PASSU operation is in progress, the status register may be read to check the value of the Write-In Progress (WIP) bit. The Write-In Progress (WIP) bit is a '1' during the self-timed PASSU cycle, and is a '0' when it is completed.

If the PASSU command supplied password does not match the hidden password in the Password Register, an error is reported by setting the P_ERR bit to 1. The WIP bit of the status register also remains set to '1'. It is necessary to use the CLSR command to clear the status register, the RESET command to software reset the device, or drive the RESET# input low to initiate a hardware reset, in order to return the P_ERR and WIP bits to '0'. This returns the device to standby state, ready for new commands such as a retry of the PASSU command.

If the password does match, the PPB Lock bit is set to '1'. The maximum clock frequency for the PASSU command is 133 MHz.

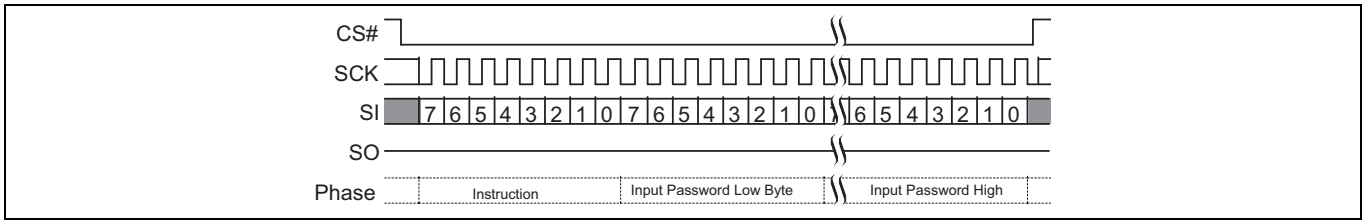


Figure 106 Password Unlock command sequence

9.9 Reset commands

Software controlled Reset commands restore the device to its initial power up state, by reloading volatile registers from non-volatile default values. However, the volatile FREEZE bit in the Configuration Register CR1V[0] and the volatile PPB Lock bit in the PPB Lock Register are not changed by a software reset. The software reset cannot be used to circumvent the FREEZE or PPB Lock bit protection mechanisms for the other security configuration bits.

The Freeze bit and the PPB Lock bit will remain set at their last value prior to the software reset. To clear the FREEZE bit and set the PPB Lock bit to its protection mode selected power on state, a full POR sequence or hardware reset must be done.

The non-volatile bits in the configuration register (CR1NV), TBPROT_O, TBPARM, and BPNV_O, retain their previous state after a Software Reset.

The Block Protection bits BP2, BP1, and BP0, in the status register (SR1V) will only be reset to their default value if FREEZE = 0.

A reset command (RST or RESET) is executed when CS# is brought HIGH at the end of the instruction and requires t_{RPH} time to execute.

In the case of a previous Power-up Reset (POR) failure to complete, a reset command triggers a full power-up sequence requiring t_{PU} to complete.

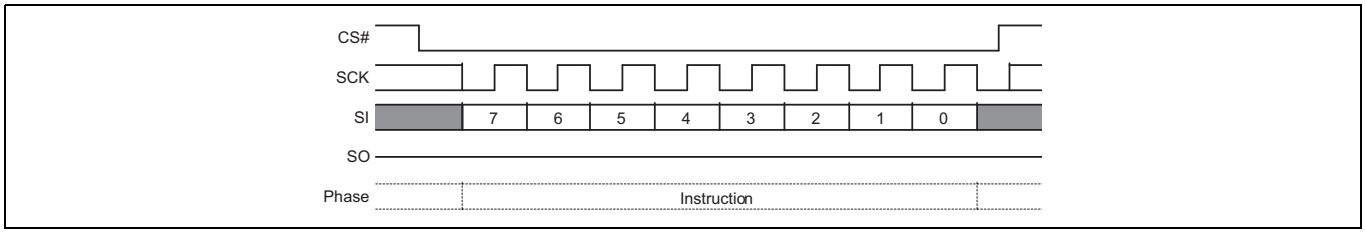


Figure 107 Software Reset command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted ito IO0-IO3, two clock cycles per byte.

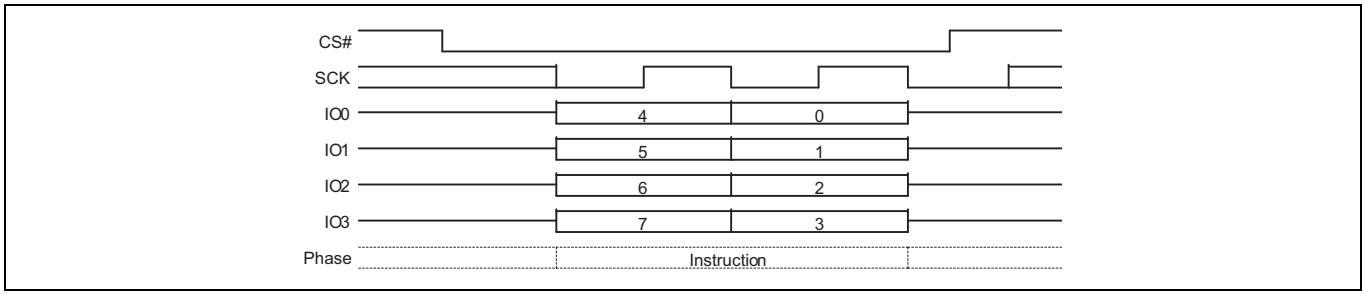


Figure 108 Software Reset command sequence QPI mode

9.9.1 Software Reset Enable (RSTEN 66h)

The Reset Enable (RSTEN) command is required immediately before a Reset command (RST) such that a software reset is a sequence of the two commands. Any command other than RST following the RSTEN command, will clear the reset enable condition and prevent a later RST command from being recognized.

9.9.2 Software Reset (RST 99h)

The Reset (RST) command immediately following a RSTEN command, initiates the software reset process.

9.9.3 Legacy Software Reset (RESET F0h)

The Legacy Software Reset (RESET) is a single command that initiates the software reset process. This command is disabled by default but can be enabled by programming CR3V[0] = 1, for software compatibility with Infineon legacy FL-S devices.

9.9.4 Mode Bit Reset (MBR FFh)

The Mode Bit Reset (MBR) command is used to return the device from continuous high performance read mode back to normal standby awaiting any new command. Because some device packages lack a hardware RESET# input and a device that is in a continuous high performance read mode may not recognize any normal SPI command, a system hardware reset or software reset command may not be recognized by the device. It is recommended to use the MBR command after a system reset when the RESET# signal is not available or, before sending a software reset, to ensure the device is released from continuous High Performance Read mode.

The MBR command sends Ones on SI or IO0 for eight SCK cycles. IO1 to IO3 are ‘don’t care’ during these cycles.

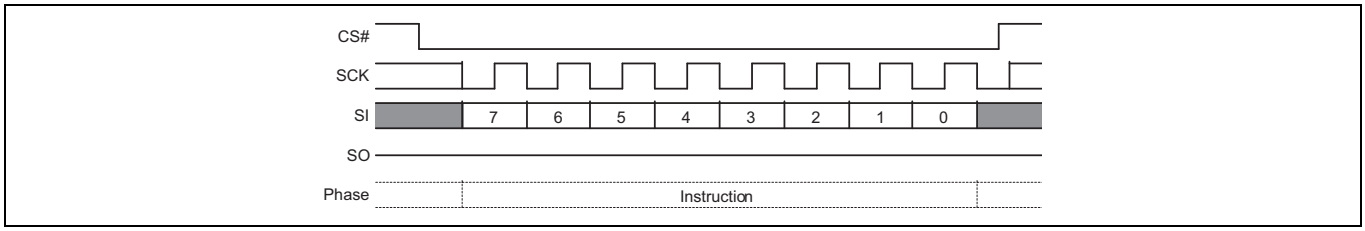


Figure 109 Mode Bit Reset command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted to IO0-IO3, two clock cycles per byte.

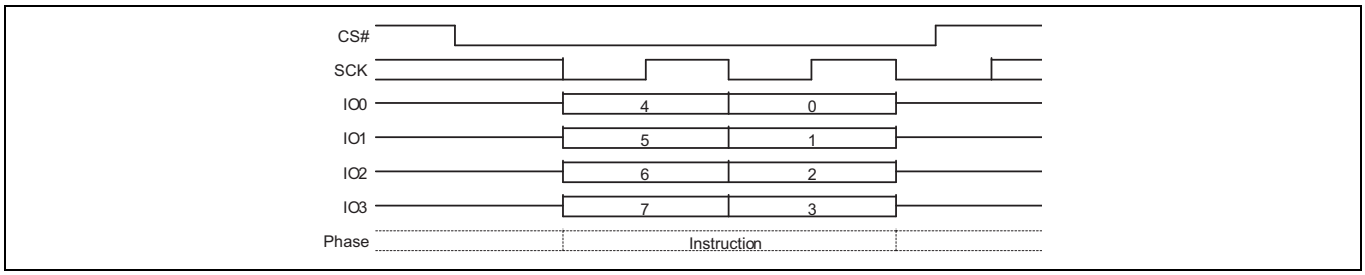


Figure 110 Mode Bit Reset command sequence QPI mode

9.10 DPD commands

9.10.1 Enter Deep Power-Down (DPD B9h)

Although the standby current during normal operation is relatively LOW, standby current can be further reduced with the Deep Power-down command. The lower power consumption makes the Deep Power-Down (DPD) command especially useful for battery powered applications (see I_{DPD} in **"DC characteristics"** on page 34).

The DPD command is accepted only while the device is not performing an embedded algorithm as indicated by the Status Register 1 volatile Write In Progress (WIP) bit being cleared to zero (SR1V[0] = 0).

The command is initiated by driving the CS# pin LOW and shifting the instruction code 'B9h' as shown in **Figure 111**. The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Deep Power-Down command will not be executed. After CS# is driven HIGH, the power-down state will be entered within the time duration of t_{DPD} (refer to **"Timing specifications"** on page 37).

While in the power-down state only the Release from Deep Power-Down command, which restores the device to normal operation, will be recognized. All other commands are ignored. This includes the Read Status Register command, which is always available during normal operation. Ignoring all but one command also makes the Power Down state useful for write protection. The device always powers-up in the interface standby state with the standby current of I_{CC1}.

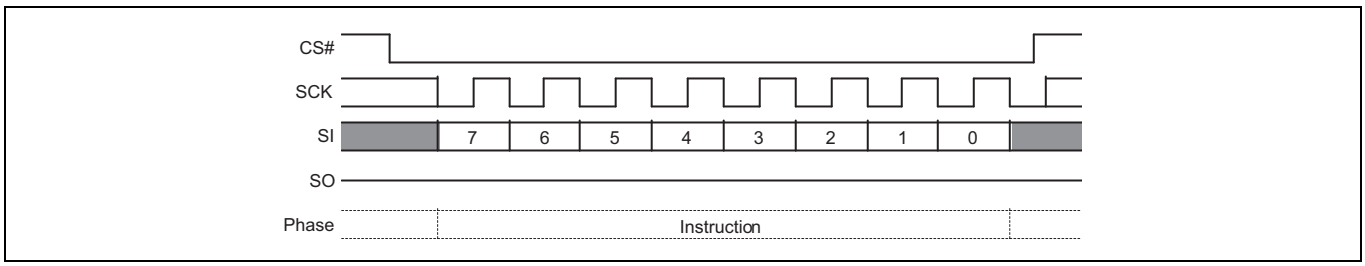


Figure 111 Deep Power-Down command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted to IO0-IO3, two clock cycles per byte.

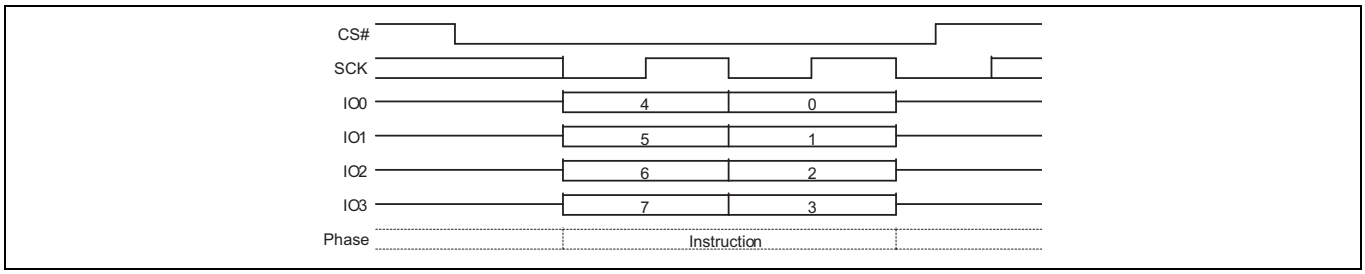


Figure 112 DPD command sequence QPI mode

9.10.2 Release from Deep Power-Down (RES ABh)

The Release from Deep Power-Down command is used to release the device from the deep power-down state. In some legacy SPI devices the RES command could also be used to obtain the device electronic identification (ID) number. However, the device ID function is not supported by the RES command.

To release the device from the deep power-down state, the command is issued by driving the CS# pin LOW, shifting the instruction code 'ABh' and driving CS# HIGH as shown in **Figure 113**. Release from deep power-down will take the time duration of t_{RES} (**"Timing specifications"** on page 37) before the device will resume normal operation and other commands are accepted. The CS# pin must remain HIGH during the t_{RES} time duration.

Hardware Reset will also release the device from the DPD state as part of the hardware reset process.

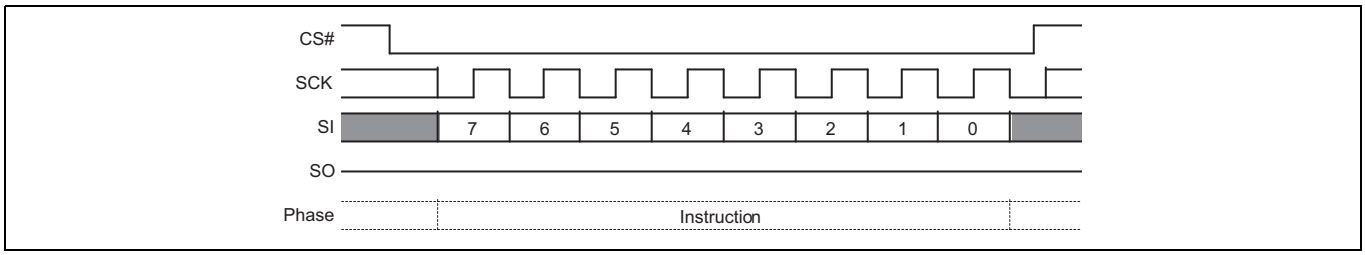


Figure 113 Release from Deep Power-Down command sequence

This command is also supported in QPI mode. In QPI mode, the instruction is shifted to IO0-IO3, two clock cycles per byte.

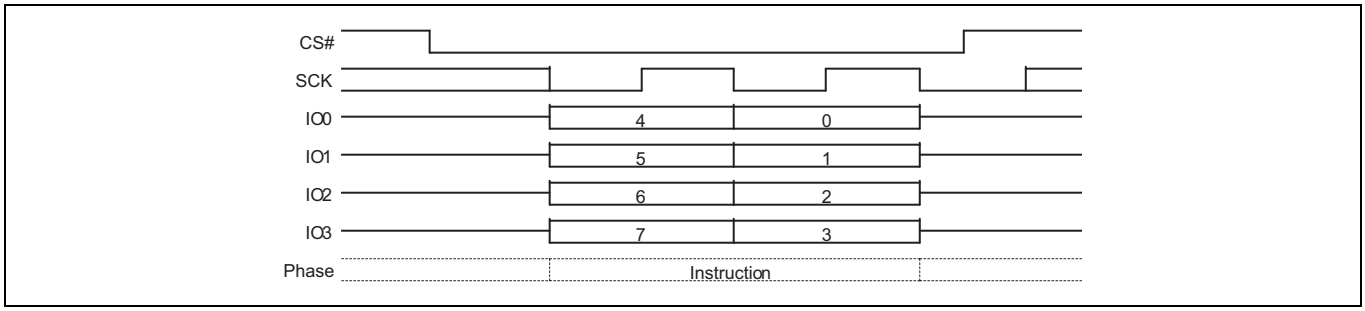


Figure 114 RES command sequence QPI mode

10 Embedded algorithm performance tables

Table 50 Program and erase performance[78, 79, 80]

Symbol	Parameter	Min	Typ[77]	Max	Unit
t_W	Non-volatile Register Write Time	–	240	750	ms
t_{PP}	Page Programming (512 bytes) Page Programming (256 bytes)		475 360	2000 2000	µs
t_{SE}	Sector Erase Time (256 KB physical sectors)		930	2900	ms
	Sector Erase Time (4 KB sectors)		240	725	
t_{BE}[76]	Bulk Erase Time (S25FS512S)		220	720	sec
tEES	Evaluate Erase Status Time (64-KB or 4-KB physical sectors)		20	25	µs
	Evaluate Erase Status Time (256-KB physical or logical sectors)		80	100	

Notes
76. Not 100% tested.
77. Typical program and erase times assume the following conditions: 25°C, V_{CC} = 1.8 V; random data pattern.
78. The programming time for any OTP programming command is the same as t_{PP}. This includes OTPP 42h, PNVDLR 43h, ASPP 2Fh, and PASSP E8h.
79. The programming time for the PPBP E3h command is the same as t_{PP}. The erase time for PPBE E4h command is the same as t_{SE}.
80. Data retention of 20 years is based on 1k erase cycles or less.

Table 51 Program or erase suspend AC parameters

Parameter	Typ	Max	Unit	Comments
Suspend latency (t_{SL})	–	50	µs	The time from Suspend command until the WIP bit is ‘0’.
Resume to next Program Suspend (t_{RS})	100	–		Minimum is the time needed to issue the next Suspend command but ≥ typical periods are needed for Program or Erase to progress to completion.

11 Data integrity

11.1 Erase endurance

Table 52 Erase endurance

Parameter	Minimum	Unit
Program/erase cycles per main flash array sectors	100k	P/E cycle
Program/erase cycles per PPB array or non-volatile register array [81]		

Note
81. Each write command to a non-volatile register causes a P/ E cycle on the entire non-volatile register array. OTP bits and registers internally reside in a separate array that is not P/E cycled.

11.2 Data retention

Table 53 Data retention

Parameter	Test conditions	Minimum time	Unit
Data retention time	10k program/erase cycles	20	Years
	100k program/erase cycles	2	

Contact Infineon Sales or an FAE representative for additional information on data integrity. An application note is available at: **www.infineon.com/appnotes**.

12 Device identification

12.1 Serial flash discoverable parameters (SFDP) address map

The SFDP address space has a header starting at address zero that identifies the SFDP data structure and provides a pointer to each parameter. One parameter is mandated by the JEDEC JESD216 standard. Cypress provides an additional parameter by pointing to the ID-CFI address space, i.e. the ID-CFI address space is a sub-set of the SFDP address space. The JEDEC parameter is located within the ID-CFI address space and is thus both a CFI parameter and an SFDP parameter. In this way both SFDP and ID-CFI information can be accessed by either the RSFDP or RDID commands.

Table 54 SFDP overview map

Byte address	Description
0000h	Location zero within JEDEC JESD216B SFDP space – start of SFDP header
,,,	Remainder of SFDP header followed by undefined space
1000h	Location zero within ID-CFI space – start of ID-CFI parameter tables
...	ID-CFI parameters
1090h	Start of SFDP parameter tables which are also grouped as one of the CFI parameter tables (the CFI parameter itself starts at 108Eh, the SFDP parameter table data is double word aligned starting at 1090h)
...	Remainder of SFDP parameter tables followed by either more CFI parameters or undefined space

12.2 SFDP header table

Table 55 SFDP header

SFDP byte address	SFDP Dword name	Data	Description
00h	SFDP Header 1st DWORD	53h	This is the entry point for Read SFDP (5Ah) command i.e. location zero within SFDP space ASCII “S”.
01h		46h	ASCII “F”
02h		44h	ASCII “D”
03h		50h	ASCII “P”
04h	SFDP Header 2nd DWORD	06h	SFDP Minor Revision (06h = JEDEC JESD216 Revision B). This revision is backward compatible with all prior minor revisions. Minor revisions are changes that define previously reserved fields, add fields to the end, or that clarify definitions of existing fields. Increments of the minor revision value indicate that previously reserved parameter fields may have been assigned a new definition or entire Dwords may have been added to the parameter table. However, the definition of previously existing fields is unchanged and therefore remain backward compatible with earlier SFDP parameter table revisions. Software can safely ignore increments of the minor revision number, as long as only those parameters the software was designed to support are used i.e. previously reserved fields and additional Dwords must be masked or ignored . Do not do a simple compare on the minor revision number, looking only for a match with the revision number that the software is designed to handle. There is no problem with using a higher number minor revision.
05h		01h	SFDP Major Revision This is the original major revision. This major revision is compatible with all SFDP reading and parsing software.
06h		05h	Number of Parameter Headers (zero based, 05h = 6 parameters)
07h		FFh	Unused
08h	Parameter Header 0 1st DWORD	00h	Parameter ID LSB (00h = JEDEC SFDP Basic SPI Flash Parameter)
09h		00h	Parameter Minor Revision (00h = JESD216) - This older revision parameter header is provided for any legacy SFDP reading and parsing software that requires seeing a minor revision 0 parameter header. SFDP software designed to handle later minor revisions should continue reading parameter headers looking for a higher numbered minor revision that contains additional parameters for that software revision.
0Ah		01h	Parameter Major Revision (01h = The original major revision - all SFDP software is compatible with this major revision.
0Bh		09h	Parameter Table Length (in double words = Dwords = 4 byte units) 09h = 9 Dwords
0Ch	Parameter Header 0 2nd DWORD	90h	Parameter Table Pointer Byte 0 (Dword = 4-byte aligned) JEDEC Basic SPI Flash parameter byte offset = 1090h
0Dh		10h	Parameter Table Pointer Byte 1
0Eh		00h	Parameter Table Pointer Byte 2
0Fh		FFh	Parameter ID MSB (FFh = JEDEC defined legacy Parameter ID)

Table 55 SFDP header *(continued)*

SFDP byte address	SFDP Dword name	Data	Description
10h	Parameter Header 1 1st DWORD	00h	Parameter ID LSB (00h = JEDEC SFDP Basic SPI Flash Parameter)
11h		05h	Parameter Minor Revision (05h = JESD216 Revision A) - This older revision parameter header is provided for any legacy SFDP reading and parsing software that requires seeing a minor revision 5 parameter header. SFDP software designed to handle later minor revisions should continue reading parameter headers looking for a later minor revision that contains additional parameters.
12h		01h	Parameter Major Revision (01h = The original major revision - all SFDP software is compatible with this major revision.
13h		10h	Parameter Table Length (in double words = Dwords = 4 byte units) 10h = 16 Dwords
14h	Parameter Header 1 2nd DWORD	90h	Parameter Table Pointer Byte 0 (Dword = 4 byte aligned) JEDEC Basic SPI Flash parameter byte offset = 1090h address
15h		10h	Parameter Table Pointer Byte 1
16h		00h	Parameter Table Pointer Byte 2
17h		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)
18h	Parameter Header 2 1st DWORD	00h	Parameter ID LSB (00h = JEDEC SFDP Basic SPI Flash Parameter)
19h		06h	Parameter Minor Revision (06h = JESD216 Revision B)
1Ah		01h	Parameter Major Revision (01h = The original major revision - all SFDP software is compatible with this major revision.
1Bh		10h	Parameter Table Length (in double words = Dwords = 4 byte units) 10h = 16 Dwords
1Ch	Parameter Header 2 2nd DWORD	90h	Parameter Table Pointer Byte 0 (Dword = 4 byte aligned) JEDEC Basic SPI Flash parameter byte offset = 1090h address
1Dh		10h	Parameter Table Pointer Byte 1
1Eh		00h	Parameter Table Pointer Byte 2
1Fh		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)
20h	Parameter Header 3 1st DWORD	81h	Parameter ID LSB (81h = SFDP Sector Map Parameter)
21h		00h	Parameter Minor Revision (00h = Initial version as defined in JESD216 Revision B)
22h		01h	Parameter Major Revision (01h = The original major revision - all SFDP software that recognizes this parameter's ID is compatible with this major revision.
23h		10h (512 Mb)	Parameter Table Length (in double words = Dwords = 4 byte units) OPN Dependent 16 = 10h (512 Mb)
24h	Parameter Header 3 2nd DWORD	D8h	Parameter Table Pointer Byte 0 (Dword = 4 byte aligned) JEDEC parameter byte offset = 10D8h
25h		10h	Parameter Table Pointer Byte 1
26h		00h	Parameter Table Pointer Byte 2
27h		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)
28h	Parameter Header 4 1st DWORD	84h	Parameter ID LSB (00h = SFDP 4 Byte Address Instructions Parameter)
29h		00h	Parameter Minor Revision (00h = Initial version as defined in JESD216 Revision B)
2Ah		01h	Parameter Major Revision (01h = The original major revision - all SFDP software that recognizes this parameter's ID is compatible with this major revision.
2Bh		02h	Parameter Table Length (in double words = Dwords = 4 byte units) (2h = 2 Dwords)

Table 55 SFDP header *(continued)*

SFDP byte address	SFDP Dword name	Data	Description
2Ch	Parameter Header 4 2nd DWORD	D0h	Parameter Table Pointer Byte 0 (Dword = 4 byte aligned) JEDEC parameter byte offset = 10D0h
2Dh		10h	Parameter Table Pointer Byte 1
2Eh		00h	Parameter Table Pointer Byte 2
2Fh		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)
30h	Parameter Header 5 1st DWORD	01h	Parameter ID LSB (Cypress Vendor Specific ID-CFI parameter) Legacy Manufacturer ID 01h = AMD / Cypress
31h			Parameter Minor Revision (01h = ID-CFI updated with SFDP Rev B table)
32h			Parameter Major Revision (01h = The original major revision - all SFDP software that recognizes this parameter's ID is compatible with this major revision.
33h		47h (512 Mb)	Parameter Table Length (in double words = Dwords = 4 byte units) Parameter Table Length (in double words = Dwords = 4 byte units)
34h	Parameter Header 5 2nd DWORD	00h	Parameter Table Pointer Byte 0 (Dword = 4 byte aligned) Entry point for ID-CFI parameter is byte offset = 1000h relative to SFDP location zero.
35h		10h	Parameter Table Pointer Byte 1
36h		00h	Parameter Table Pointer Byte 2
37h		01h	Parameter ID MSB (01h = JEDEC JEP106 Bank Number 1)

12.3 Device ID and common flash interface (ID-CFI) address map

12.3.1 Device ID

Table 56 Manufacturer and Device ID

Byte address	Data	Description
00h	01h	Manufacturer ID for Cypress
01h	02h (512 Mb)	Device ID Most Significant Byte — Memory Interface Type
02h	20h (512 Mb)	Device ID Least Significant Byte — Density
03h	4Dh	ID-CFI Length - Number bytes following. Adding this value to the current location of 03h gives the address of the last valid location in the ID-CFI legacy address map. The legacy CFI address map ends with the Primary Vendor-Specific Extended Query. The original legacy length is maintained for backward software compatibility. However, the CFI Query Identification String also includes a pointer to the Alternate Vendor-Specific Extended Query that contains additional information related to the FS-S family.
04h	00h (Uniform 256-KB physical sectors)	Physical Sector Architecture The S25FS512S may be configured with or without 4-KB parameter sectors in addition to the uniform sectors.
05h	81h (S25FS512S)	Family ID
06h	xxh	ASCII characters for Model. Refer to **"Ordering part number"** on page 161 for the model number definitions.
07h		
08h		Reserved
09h		
0Ah		
0Bh		
0Ch		
0Dh		
0Eh		
0Fh		

Table 57 CFI query identification string

Byte address	Data	Description
10h 11h 12h	51h 52h 59h	Query Unique ASCII string "QRY"
13h 14h	02h 00h	Primary OEM Command Set FL-P backward compatible command set ID
15h 16h	40h 00h	Address for Primary Extended Table
17h 18h	53h 46h	Alternate OEM Command Set ASCII characters "FS" for SPI (F) interface, S Technology
19h 1Ah	51h 00h	Address for Alternate OEM Extended Table

Table 58 CFI system interface string

Byte address	Data	Description
1Bh	17h	V_{CC} Min. (erase / program): 100 millivolts BCD)
1Ch	19h	V_{CC} Max. (erase / program): 100 millivolts BCD)
1Dh	00h	V_{PP} Min. voltage (00h = no V_{PP} present)
1Eh		V_{PP} Max. voltage (00h = no V_{PP} present)
1Fh	09h	Typical timeout per single byte program 2^N µs
20h		Typical timeout for Min. size Page program 2^N µs (00h = not supported)
21h	0Ah (256 KB)	Typical timeout per individual sector erase 2^N ms
22h	11h (512 Mb)	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	02h	Max. timeout for byte program 2^N times typical
24h		Max. timeout for page program 2^N times typical
25h	03h	Max. timeout per individual sector erase 2^N times typical
26h		Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 59 Device geometry definition for bottom boot initial delivery state

Byte address	Data	Description
27h	1Ah (512 Mb)	Device Size = 2^N bytes
28h	02h	Flash Device Interface Description: 0000h = x8 only 0001h = x16 only 0002h = x8/x16 capable 0003h = x32 only 0004h = Single I/O SPI, 3-byte address 0005h = Multi I/O SPI, 3-byte address 0102h = Multi I/O SPI, 3- or 4-byte address
29h	01h	
2Ah	08h	Max. number of bytes in multi-byte write = 2^N 0000h = Not supported 0008h = 256B page 0009h = 512B page
2Bh	00h	
2Ch	03h	Number of Erase Block Regions within device 1 = Uniform Device, >1 = Boot Device
2Dh	07h	Erase Block Region 1 Information (refer to JEDEC JEP137) 8 sectors = 8-1 = 0007h 4-KB sectors = 256 bytes x 0010h
2Eh	00h	
2Fh	10h	
30h	00h	Erase Block Region 2 Information (refer to JEDEC JEP137) 512 Mb: 1 sectors = 1-1 = 0000h 224-KB sector = 256 bytes x 0380h
31h		
32h		
33h	80h	
34h	00h (128 Mb) 00h (256 Mb) 03h (512 Mb)	

Table 59 Device geometry definition for bottom boot initial delivery state *(continued)*

Byte address	Data	Description
35h	FEh	Erase Block Region 3 Information 512 Mb: 255 sectors = 255-1 = 00FEh 256-KB sectors = 0400h x 256 bytes
36h	00h (128 Mb) 01h (256 Mb) 00h (512 Mb) 01h (1 Gb	
37h	00h	
38h	01h (128 Mb) 01h (256 Mb) 04h (512 Mb) 04h (1 Gb)	
39h thru 3Fh	FFh	RFU

Table 60 CFI primary vendor-specific extended query

Byte address	Data	Description
40h	50h	Query-unique ASCII string “PRI”
41h	52h	
42h	49h	
43h	31h	Major version number = 1, ASCII
44h	33h	Minor version number = 3, ASCII
45h	21h	Address Sensitive Unlock (Bits 1-0) 00b = Required, 01b = Not Required Process Technology (Bits 5-2) 0000b = 0.23 µm Floating Gate 0001b = 0.17 µm Floating Gate 0010b = 0.23 µm MirrorBit 0011b = 0.11 µm Floating Gate 0100b = 0.11 µm MirrorBit 0101b = 0.09 µm MirrorBit 1000b = 0.065 µm MirrorBit
46h	02h	Erase Suspend 0 = Not Supported, 1 = Read Only, 2 = Read and Program
47h	01h	Sector Protect 00 = Not Supported, X = Number of sectors in group
48h	00h	Temporary Sector Unprotect 00 = Not Supported, 01 = Supported
49h	08h	Sector Protect/Unprotect Scheme 04 = High Voltage Method 05 = Software Command Locking Method 08 = Advanced Sector Protection Method
4Ah	00h	Simultaneous Operation 00 = Not Supported, X = Number of Sectors
4Bh	01h	Burst Mode (Synchronous sequential read) support 00 = Not Supported, 01 = Supported
4Ch	03h	Page Mode Type, initial delivery configuration, user configurable for 512B page 00 = Not Supported, 01 = 4 Word Read Page, 02 = 8 Read Word Page, 03 = 256 Byte Program Page, 04 = 512 Byte Program Page
4Dh	00h	ACC (Acceleration) Supply Minimum 00 = Not Supported, 100 mV
4Eh		ACC (Acceleration) Supply Maximum 00 = Not Supported, 100 mV
4Fh	07h	WP# Protection 01 = Whole Chip 04 = Uniform Device with Bottom WP Protect 05 = Uniform Device with Top WP Protect 07 = Uniform Device with Top or Bottom Write Protect (user configurable)
50h	01h	Program Suspend 00 = Not Supported, 01 = Supported

Note

82. FS512S devices are user configurable to have either a hybrid sector architecture (with eight 4-KB sectors / one 224-KB sector and all remaining sectors are uniform 256 KB) or a uniform sector architecture with all sectors uniform 256 KB. FS-S devices are also user configurable to have the 4-KB parameter sectors at the top of memory address space. The CFI geometry information of the above table is relevant only to the initial delivery state. All devices are initially shipped from Cypress with the hybrid sector architecture with the 4-KB sectors located at the bottom of the array address map. However, the device configuration TBPARM bit CR1NV[2] may be programed to invert the sector map to place the 4-KB sectors at the top of the array address map. The 20h_NV bit (CR3NV[3} may be programmed to remove the 4-KB sectors from the address map. The flash device driver software must examine the TBPARM and 20h_NV bits to determine if the sector map was inverted or hybrid sectors removed at a later time.

The alternate vendor-specific extended query provides information related to the expanded command set provided by the FS-S family. The alternate query parameters use a format in which each parameter begins with an identifier byte and a parameter length byte. The driver software can check each parameter ID and can use the length value to skip to the next parameter if the parameter is not needed or not recognized by the software.

Table 61 CFI alternate vendor-specific extended query header

Byte address	Data	Description
51h	41h	Query-unique ASCII string “ALT”
52h	4Ch	
53h	54h	
54h	32h	Major version number = 2, ASCII
55h	30h	Minor version number = 0, ASCII

Table 62 CFI alternate vendor-specific extended query parameter 0

Parameter relative byte address offset	Data	Description
00h	00h	Parameter ID (Ordering Part Number)
01h	10h	Parameter Length (The number of following bytes in this parameter. Adding this value to the current location value +1 = the first byte of the next parameter).
02h	53h	ASCII “S” for manufacturer (Infineon)
03h	32h	ASCII “25” for Product Characters (Single Die SPI)
04h	35h	
05h	46h	ASCII “FS” for Interface Characters (SPI 1.8V)
06h	53h	
07h	35h (512 Mb)	ASCII characters for density
08h	31h (512 Mb)	
09h	32h (512 Mb)	
0Ah	53h	ASCII “S” for Technology (65-nm MIRRORBIT™)
0Bh	FFh	Reserved for Future Use
0Ch	FFh	
0Dh	FFh	
0Eh	FFh	
0Fh	FFh	
10h	xxh	ASCII characters for Model. Refer to **“Ordering part number”** on page 161 for the model number definitions.
11h	xxh	

Table 63 CFI alternate vendor-Specific extended query parameter 80h address options

Parameter relative byte address offset	Data	Description
00h	80h	Parameter ID (Ordering Part Number)
01h	01h	Parameter Length (The number of following bytes in this parameter. Adding this value to the current location value +1 = the first byte of the next parameter)
02h	EBh	Bits 7:5 – Reserved = 111b Bit 4 – Address Length Bit in CR2V[7] – Yes= 0b Bit 3 – AutoBoot support – No = 1b Bit 2 – 4 byte address instructions supported – Yes= 0b Bit 1 – Bank address + 3 byte address instructions supported –No = 1b Bit 0 - 3 byte address instructions supported – No = 1b

Table 64 CFI alternate vendor-specific extended query parameter 84h suspend commands

Parameter relative byte address offset	Data	Description
00h	84h	Parameter ID (Suspend Commands)
01h	08h	Parameter Length (The number of following bytes in this parameter. Adding this value to the current location value +1 = the first byte of the next parameter)
02h	75h	Program suspend instruction code
03h	32h	Program suspend latency maximum (µs)
04h	7Ah	Program resume instruction code
05h	64h	Program resume to next suspend typical (µs)
06h	75h	Erase suspend instruction code
07h	32h	Erase suspend latency maximum (µs)
08h	7Ah	Erase resume instruction code
09h	64h	Erase resume to next suspend typical (µs)

Table 65 CFI alternate vendor-specific extended query parameter 88h data protection

Parameter relative byte address offset	Data	Description
00h	88h	Parameter ID (Data Protection)
01h	04h	Parameter Length (The number of following bytes in this parameter. Adding this value to the current location value +1 = the first byte of the next parameter)
02h	0Ah	OTP size 2^N bytes, FFh = Not supported
03h	01h	OTP address map format, 01h = FL-S and FS-S format, FFh = not supported
04h	xxh	Block Protect Type, model dependent 00h = FL-P, FL-S, FS-S FFh = Not supported
05h	xxh	Advanced Sector Protection type, model dependent 01h = FL-S and FS-S ASP

Table 66 CFI alternate vendor-specific extended query parameter 8Ch reset timing

Parameter relative byte address offset	Data	Description
00h	8Ch	Parameter ID (Reset Timing)
01h	06h	Parameter Length (The number of following bytes in this parameter. Adding this value to the current location value +1 = the first byte of the next parameter).
02h	96h	POR maximum value
03h	01h	POR maximum exponent 2^N µs
04h	23h	Hardware Reset maximum value, FFh = not supported (the initial delivery state has hardware reset disabled but it may be enabled by the user at a later time)
05h	00h	Hardware Reset maximum exponent 2^N µs
06h	23h	Software Reset maximum value, FFh = Not supported
07h	00h	Software Reset maximum exponent 2^N µs

Table 67 CFI alternate vendor-Specific extended query parameter 94h ECC

Parameter relative byte address offset	Data	Description
00h	94h	Parameter ID (ECC)
01h	01h	Parameter Length (The number of following bytes in this parameter. Adding this value to the current location value +1 = the first byte of the next parameter).
02h	10h	ECC unit size byte, FFh = ECC disabled

Table 68 CFI alternate vendor-Specific extended query parameter F0h RFU

Parameter relative byte address offset	Data	Description
00h	F0h	Parameter ID (RFU)
01h	09h	Parameter Length (The number of following bytes in this parameter. Adding this value to the current location value +1 = the first byte of the next parameter).
02h	FFh	RFU
...	FFh	
0Ah	FFh	

This parameter type (Parameter ID F0h) may appear multiple times and have a different length each time. The parameter is used to reserve space in the ID-CFI map or to force space (pad) to align a following parameter to a required boundary.

12.4 JEDEC SFDP Rev B parameter tables

From the view point of the CFI data structure, all of the SFDP parameter tables are combined into a single CFI Parameter as a contiguous byte sequence.

From the viewpoint of the SFDP data structure, there are three independent parameter tables. Two of the tables have a fixed length and one table has a variable structure and length depending on the device density ordering part number (OPN). The basic flash parameter table and the 4-byte address instructions parameter table have a fixed length and are presented below as a single table. This table is **Table 69** of the overall CFI parameter.

The JEDEC Sector Map Parameter table structure and length depends on the density OPN and is presented as a set of tables, one for each device density. The appropriate table for the OPN is Section 2(should it be linked to section 2) of the overall CFI parameter and is appended to Section 1.

Table 69 CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, section 1, basic flash parameter and 4-byte address instructions parameter

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
00h	--	N/A	A5h	CFI Parameter ID (JEDEC SFDP)
01h	--	N/A	88h (512 Mb)	CFI Parameter Length (The number of following bytes in this parameter. Adding this value to the current location value +1 = the first byte of the next parameter). OPN dependent: 18Dw + 16Dw = 34Dw * 4B = 136B = 88h B (512 Mb)
02h	00h	JEDEC Basic Flash Parameter Dword-1	E7h	Start of SFDP JEDEC parameter, located at 1090h in the overall SFDP address space. Bits 7:5 = unused = 111b Bit 4:3 = 06h is status register write instruction and status register is default nonvolatile= 00b Bit 2 = Program Buffer > 64 bytes = 1 Bits 1:0 = Uniform 4-KB erase unavailable = 11b
03h	01h		FFh	Bits 15:8 = Uniform 4-KB erase opcode = not supported = FFh
04h	02h		B2h (FSxxxSAG) BAh (FSxxxSDS)	Bit 23 = Unused = 1b Bit 22 = Supports Quad Out Read = No = 0b Bit 21 = Supports Quad I/O Read = Yes =1b Bit 20 = Supports Dual I/O Read = Yes = 1b Bit19 = Supports DDR 0= No, 1 = Yes; FS-SAG = 0b, FS-SDS = 1b Bit 18:17 = Number of Address Bytes, 3 or 4 = 01b Bit 16 = Supports Dual Out Read = No = 0b
05h	03h		FFh	Bits 31:24 = Unused = FFh
06h	04h	JEDEC Basic Flash Parameter Dword-2	FFh	Density in bits, zero based, 512 Mb = 1FFFFFFFh
07h	05h		FFh	
08h	06h		FFh	
09h	07h		1Fh (512 Mb)	
0Ah	08h	JEDEC Basic Flash Parameter Dword-3	48h	Bits 7:5 = number of Quad I/O (1-4-4) Mode cycles = 010b Bits 4:0 = number of Quad I/O Dummy cycles = 01000b (Initial Delivery State)
0Bh	09h		EBh	Quad I/O instruction code
0Ch	0Ah		FFh	Bits 23:21 = number of Quad Out (1-1-4) Mode cycles = 111b Bits 20:16 = number of Quad Out Dummy cycles = 11111b
0Dh	0Bh		FFh	Quad Out instruction code
0Eh	0Ch	JEDEC Basic Flash Parameter Dword-4	FFh	Bits 7:5 = number of Dual Out (1-1-2) Mode cycles = 111b Bits 4:0 = number of Dual Out Dummy cycles = 11111b
0Fh	0Dh		FFh	Dual Out instruction code
10h	0Eh		88h	Bits 23:21 = number of Dual I/O (1-2-2) Mode cycles = 100b Bits 20:16 = number of Dual I/O Dummy cycles = 01000b (Initial Delivery State)
11h	0Fh		BBh	Dual I/O instruction code

Table 69 CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, section 1, basic flash parameter and 4-byte address instructions parameter *(continued)*

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
12h	10h	JEDEC Basic Flash Parameter Dword-5	FEh	Bits 7:5 RFU = 111b Bit 4 = QPI supported = Yes = 1b Bits 3:1 RFU = 111b Bit 0 = Dual All not supported = 0b
13h	11h		FFh	Bits 15:8 = RFU = FFh
14h	12h		FFh	Bits 23:16 = RFU = FFh
15h	13h		FFh	Bits 31:24 = RFU = FFh
16h	14h	JEDEC Basic Flash Parameter Dword-6	FFh	Bits 7:0 = RFU = FFh
17h	15h		FFh	Bits 15:8 = RFU = FFh
18h	16h		FFh	Bits 23:21 = number of Dual All Mode cycles = 111b Bits 20:16 = number of Dual All Dummy cycles = 11111b
19h	17h		FFh	Dual All instruction code
1Ah	18h	JEDEC Basic Flash Parameter Dword-7	FFh	Bits 7:0 = RFU = FFh
1Bh	19h		FFh	Bits 15:8 = RFU = FFh
1Ch	1Ah		48h	Bits 23:21 = number of QPI Mode cycles = 010b Bits 20:16 = number of QPI Dummy cycles = 01000b
1Dh	1Bh		EBh	QPI mode Quad I/O (4-4-4) instruction code
1Eh	1Ch	JEDEC Basic Flash Parameter Dword-8	0Ch	Erase type 1 size 2^N bytes = 4 KB = 0Ch for Hybrid (Initial Delivery State)
1Fh	1Dh		20h	Erase type 1 instruction
20h	1Eh		10h	Erase type 2 size 2^N bytes = 64 KB = 10h
21h	1Fh		D8h	Erase type 2 instruction
22h	20h	JEDEC Basic Flash Parameter Dword-9	12h	Erase type 3 size 2^N bytes = 256 KB = 12h
23h	21h		D8h	Erase type 3 instruction
24h	22h		00h	Erase type 4 size 2^N bytes = not supported = 00h
25h	23h		FFh	Erase type 4 instruction = not supported = FFh

Table 69 CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, section 1, basic flash parameter and 4-byte address instructions parameter *(continued)*

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
26h	24h	JEDEC Basic Flash Parameter Dword-10	82h	Bits 31:30 = Erase type 4 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 1S = 11b (RFU) Bits 29:25 = Erase type 4 Erase, Typical time count = 11111b (RFU) Bits 24:23 = Erase type 3 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 128mS = 10b Bits 22:18 = Erase type 3 Erase, Typical time count = 00100b (typ erase time = count +1 * units = 5*128mS = 640mS) Bits 17:16 = Erase type 2 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 16mS = 01b Bits 15:11 = Erase type 2 Erase, Typical time count = 01000b (typ erase time = count +1 * units = 9*16mS = 144mS) Bits 10:9 = Erase type 1 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 16mS = 01b Bits 8:4 = Erase type 1 Erase, Typical time count = 01000b (typ erase time = count +1 * units = 9*16mS = 144mS) Bits 3:0 = Multiplier from typical erase time to maximum erase time = 2*(N+1), N=2h = 6x multiplier Binary Fields: 11-11111-10-00100-01-01000-01-01000-0010 Nibble Format: 1111_1111_0001_0001_0100_0010_1000_0010 Hex Format: FF_11_42_82
27h	25h		42h	
28h	26h		11h	
29h	27h		FFh	

Table 69 CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, section 1, basic flash parameter and 4-byte address instructions parameter *(continued)*

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
2Ah	28h	JEDEC Basic Flash Parameter Dword-11	91h	Bit 31 Reserved = 1b Bits 30:29 = Chip Erase, Typical time units (00b: 16 ms, 01b: 256 ms, 10b: 4 s, 11b: 64 s) = 512 Mb = 64s = 11b Bits 28:24 = Chip Erase, Typical time count, (count+1)*units, 512 Mb = 00010b = 2+1*64uS = 192s Bits 23 = Byte Program Typical time, additional byte units (0b:1uS, 1b:8uS) = 1uS = 0b Bits 22:19 = Byte Program Typical time, additional byte count, (count+1)*units, count = 0000b, (typ Program time = count +1 * units = 1*1uS = 1uS Bits 18 = Byte Program Typical time, first byte units (0b:1uS, 1b:8uS) = 8uS = 1b Bits 17:14 = Byte Program Typical time, first byte count, (count+1)*units, count = 1100b, (typ Program time = count +1 * units = 13*8uS = 104uS Bits 13 = Page Program Typical time units (0b:8uS, 1b:64uS) = 64uS = 1b Bits 12:8 = Page Program Typical time count, (count+1)*units, count = 00110b, (typ Program time = count +1 * units = 7*64uS = 448uS) Bits 7:4 = Page size 2^N, N=9h, = 512B page Bits 3:0 = Multiplier from typical time to maximum for Page or Byte program = 2*(N+1), N=1h = 4x multiplier 128 Mb Binary Fields: 1-10-01000-0-0000-1-1100-1-00110-1001-0001 Nibble Format: 1100_1000_0000_0111_0010_0110_1001_0001 Hex Format: C8_07_26_91 256 Mb Binary Fields: 1-10-10001-0-0000-1-1100-1-00110-1001-0001 Nibble Format: 1101_0001_0000_0111_0010_0110_1001_0001 Hex Format: D1_07_26_91 512 Mb Binary Fields: 1-11-00010-0-0000-1-1100-1-00110-1001-0001 Nibble Format: 1110_0010_0000_0111_0010_0110_1001_0001 Hex Format: E2_07_26_91
2Bh	29h		26h	
2Ch	2Ah		07h	
2Dh	2Bh		E2h (512 Mb)	

Table 69 CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, section 1, basic flash parameter and 4-byte address instructions parameter *(continued)*

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
2Eh	2Ch	JEDEC Basic Flash Parameter Dword-12	ECh	Bit 31 = Suspend and Resume supported = 0b Bits 30:29 = Suspend in-progress erase max latency units (00b: 128ns, 01b: 1us, 10b: 8us, 11b: 64us) = 8us= 10b Bits 28:24 = Suspend in-progress erase max latency count = 00100b, max erase suspend latency = count +1 * units = 5*8uS = 40uS Bits 23:20 = Erase resume to suspend interval count = 0001b, interval = count +1 * 64us = 2 * 64us = 128us Bits 19:18 = Suspend in-progress program max latency units (00b: 128ns, 01b: 1us, 10b: 8us, 11b: 64us) = 8us= 10b Bits 17:13 = Suspend in-progress program max latency count = 00100b, max erase suspend latency = count +1 * units = 5*8uS = 40uS Bits 12:9 = Program resume to suspend interval count = 0001b, interval = count +1 * 64us = 2 * 64us = 128us Bit 8 = RFU = 1b Bits 7:4 = Prohibited operations during erase suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) + xx1xb: May not initiate a page program in the erase suspended sector size + x1xxb: May not initiate a read in the erase suspended sector size + 1xxxb: The erase and program restrictions in bits 5:4 are sufficient = 1110b Bits 3:0 = Prohibited Operations During Program Suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) + xx0xb: May not initiate a new page program anywhere (program nesting not permitted) + x1xxb: May not initiate a read in the program suspended page size + 1xxxb: The erase and program restrictions in bits 1:0 are sufficient = 1100b Binary Fields: 0-10-00100-0001-10-00100-0001-1-1110-1100 Nibble Format: 0100_0100_0001_1000_1000_0011_1110_1100 Hex Format: 44_18_83_EC
2Fh	2Dh		83h	
30h	2Eh		18h	
31h	2Fh		44h	
32h	30h	JEDEC Basic Flash Parameter Dword-13	8Ah	Bits 31:24 = Erase Suspend Instruction = 75h Bits 23:16 = Erase Resume Instruction = 7Ah Bits 15:8 = Program Suspend Instruction = 85h Bits 7:0 = Program Resume Instruction = 8Ah
33h	31h		85h	
34h	32h		7Ah	
35h	33h		75h	

Table 69 CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, section 1, basic flash parameter and 4-byte address instructions parameter *(continued)*

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
36h	34h	JEDEC Basic Flash Parameter Dword-14	F7h	Bit 31 = Deep Power Down Supported = supported = 0 Bits 30:23 = Enter Deep Power Down Instruction = B9h Bits 22:15 = Exit Deep Power Down Instruction = ABh Bits 14:13 = Exit Deep Power Down to next operation delay units = (00b: 128ns, 01b: 1us, 10b: 8us, 11b: 64us) = 1us = 01b Bits 12:8 = Exit Deep Power Down to next operation delay count = 11101b, Exit Deep Power Down to next operation delay = (count+1)*units = 29+1 *1us = 30us Bits 7:4 = RFU = Fh Bit 3:2 = Status Register Polling Device Busy = 01b: Legacy status polling supported = Use legacy polling by reading the Status Register with 05h instruction and checking WIP bit[0] (0=ready; 1=busy). = 01b Bits 1:0 = RFU = 11b Binary Fields: 0-10111001-10101011-01-11101-1111-01-11 Nibble Format: 0101_1100_1101_0101_1011_1101_1111_0111 Hex Format: 5C_D5_BD_F7
37h	35h		BDh	
38h	36h		D5h	
39h	37h		5Ch	

Table 69 CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, section 1, basic flash parameter and 4-byte address instructions parameter *(continued)*

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
3Ah	38h	JEDEC Basic Flash Parameter Dword-15	8Ch	Bits 31:24 = RFU = FFh Bit 23 = Hold and WP Disable = not supported = 0b Bits 22:20 = Quad Enable Requirements = 101b: QE is bit 1 of the Status Register 2. Status register 1 is read using Read Status instruction 05h. Status register 2 is read using instruction 35h. QE is set via Write Status instruction 01h with two data bytes where bit 1 of the second byte is one. It is cleared via Write Status with two data bytes where bit 1 of the second byte is zero. Bits 19:16 0-4-4 Mode Entry Method = xxx1b: Mode Bits[7:0] = A5h Note: QE must be set prior to using this mode + x1xxb: Mode Bit[7:0]=Axh + 1xxxb: RFU = 1101b Bits 15:10 0-4-4 Mode Exit Method = xx_xxx1b: Mode Bits[7:0] = 00h will terminate this mode at the end of the current read operation + xx_1xxxb: Input Fh (mode bit reset) on DQ0-DQ3 for 8 clocks. This will terminate the mode prior to the next read operation. + x1_xxxxb: Mode Bit[7:0] != Axh + 1x_x1xx: RFU = 11_1101 Bit 9 = 0-4-4 mode supported = 1 Bits 8:4 = 4-4-4 mode enable sequences = x_1xxxb: device uses a read-modify-write sequence of operations: read configuration using instruction 65h followed by address 800003h, set bit 6, write configuration using instruction 71h followed by address 800003h. This configuration is volatile. = 01000b Bits 3:0 = 4-4-4 mode disable sequences = x1xxb: device uses a read-modify-write sequence of operations: read configuration using instruction 65h followed by address 800003h, clear bit 6, write configuration using instruction 71h followed by address 800003h.. This configuration is volatile. + 1xxxb: issue the Soft Reset 66/99 sequence = 1100b Binary Fields: 11111111-0-101-1101-111101-1-01000-1100 Nibble Format: 1111_1111_0101_1101_1111_0110_1000-1100 Hex Format: FF_5D_F6_8C
3Bh	39h		F6h	
3Ch	3Ah		5Dh	
3Dh	3Bh		FFh	

Table 69 CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, section 1, basic flash parameter and 4-byte address instructions parameter *(continued)*

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
3Eh	3Ch	JEDEC Basic Flash Parameter Dword-16	F0h	Bits 31:24 = Enter 4-Byte Addressing = xxxx_xxx1b: issue instruction B7h (preceding write enable not required) + xx1x_xxxxb: Supports dedicated 4-Byte address instruction set. Consult vendor data sheet for the instruction set definition. + 1xxx_xxxxb: Reserved = 10100001b Bits 23:14 = Exit 4-Byte Addressing = xx_xx1x_xxxxb: Hardware reset + xx_x1xx_xxxxb: Software reset (see bits 13:8 in this DWORD) + xx_1xxx_xxxxb: Power cycle + x1_xxxx_xxxxb: Reserved + 1x_xxxx_xxxxb: Reserved = 11_1110_0000b Bits 13:8 = Soft Reset and Rescue Sequence Support = x1_xxxxb: issue reset enable instruction 66h, then issue reset instruction 99h. The reset enable, reset sequence may be issued on 1, 2, or 4 wires depending on the device operating mode. + 1x_xxxxb: exit 0-4-4 mode is required prior to other reset sequences above if the device may be operating in this mode. = 110000b Bit 7 = RFU = 1 Bits 6:0 = Volatile or Nonvolatile Register and Write Enable Instruction for Status Register 1 = + xx1_xxxxb: Status Register 1 contains a mix of volatile and nonvolatile bits. The 06h instruction is used to enable writing of the register. + x1x_xxxxb: Reserved + 1xx_xxxxb: Reserved = 1110000b Binary Fields: 10100001-1111100000-110000-1-1110000 Nibble Format: 1010_0001_1111_1000_0011_0000_1111_0000 Hex Format: A1_F8_30_F0
3Fh	3Dh		30h	
40h	3Eh		F8h	
41h	3Fh		A1h	

Table 69 CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, section 1, basic flash parameter and 4-byte address instructions parameter *(continued)*

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP Dword name	Data	Description
42h nonvolatile	40h	JEDEC 4 Byte Address Instructions Parameter Dword-1	6Bh	Supported = 1, Not Supported = 0 Bits 31:20 = RFU = FFFh Bit 19 = Support for nonvolatile individual sector lock write command, Instruction=E3h = 1 Bit 18 = Support for nonvolatile individual sector lock read command, Instruction=E2h = 1 Bit 17 = Support for volatile individual sector lock Write command, Instruction=E1h = 1 Bit 16 = Support for volatile individual sector lock Read command, Instruction=E0h = 1 Bit 15 = Support for (1-4-4) DTR_Read Command, Instruction=EEh = 1 Bit 14 = Support for (1-2-2) DTR_Read Command, Instruction=BEh = 0 Bit 13 = Support for (1-1-1) DTR_Read Command, Instruction=0Eh = 0 Bit 12 = Support for Erase Command – Type 4 = 0 Bit 11 = Support for Erase Command – Type 3 = 1 Bit 10 = Support for Erase Command – Type 2 = 1 Bit 9 = Support for Erase Command – Type 1 = 1 Bit 8 = Support for (1-4-4) Page Program Command, Instruction=3Eh =0 Bit 7 = Support for (1-1-4) Page Program Command, Instruction=34h = 0 Bit 6 = Support for (1-1-1) Page Program Command, Instruction=12h = 1 Bit 5 = Support for (1-4-4) FAST_READ Command, Instruction=ECh = 1 Bit 4 = Support for (1-1-4) FAST_READ Command, Instruction=6Ch = 0 Bit 3 = Support for (1-2-2) FAST_READ Command, Instruction=BCh = 1 Bit 2 = Support for (1-1-2) FAST_READ Command, Instruction=3Ch = 0 Bit 1 = Support for (1-1-1) FAST_READ Command, Instruction=0Ch = 1 Bit 0 = Support for (1-1-1) READ Command, Instruction=13h = 1
43h	41h		8Eh	
44h	42h		FFh	
45h	43h		FFh	
46h	44h	JEDEC 4 Byte Address Instructions Parameter Dword-2	21h	Bits 31:24 = FFh = Instruction for Erase Type 4: RFU Bits 23:16 = DCh = Instruction for Erase Type 3 Bits 15:8 = DCh = Instruction for Erase Type 2 Bits 7:0 = 21h = Instruction for Erase Type 1
47h	45h		DCh	
48h	46h		DCh	
49h	47h		FFh	

Sector Map parameter table notes:

Table 70 provides a means to identify how the device address map is configured and provides a sector map for each supported configuration. This is done by defining a sequence of commands to read out the relevant configuration register bits that affect the selection of an address map. When more than one configuration bit must be read, all the bits are concatenated into an index value that is used to select the current address map.

To identify the sector map configuration in FS512S the following configuration bits are read in the following MSb to LSb order to form the configuration map index value:

- CR3NV[3] — 0 = Hybrid Architecture, 1 = Uniform Architecture
- CR1NV[2] — 0 = 4 KB parameter sectors at bottom, 1 = 4 KB sectors at top

The value of some configuration bits may make other configuration bit values not relevant (don’t care), hence not all possible combinations of the index value define valid address maps. Only selected configuration bit

combinations are supported by the SFDP Sector Map Parameter Table. Other combinations must not be used in configuring the sector address map when using this SFDP parameter table to determine the sector map. The following index value combinations are supported.

Table 70 Sector map parameter

Device	CR3NV[3]	CR1NV[2]	Index Value	Description
FS512S	0	0	01h	4 KB sectors at bottom with remainder 256 KB sectors
	0	1	03h	4 KB sectors at top with remainder 256 KB sectors
	1	0	05h	Uniform 256 KB sectors

Table 71 CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, section 2, sector map parameter table, 512 Mb

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP D word name	Data	Description
4Ah	48h	JEDEC Sector Map Parameter Dword-1 Config. Detect-1	FCh	Bits 31:24 = Read data mask = 0000_1000b: Select bit 3 of the data byte for 20h_NV value 0= Hybrid map with 4-KB parameter sectors 1= Uniform map Bits 23:22 = Configuration detection command address length = 11b: Variable length Bits 21:20 = RFU = 11b Bits 19:16 = Configuration detection command latency = 1111b: variable latency Bits 15:8 = Configuration detection instruction = 65h: Read any register Bits 7:2 = RFU = 111111b Bit 1 = Command Descriptor = 0 Bit 0 = not the end descriptor = 0
4Bh	49h		65h	
4Ch	4Ah		FFh	
4Dh	4Bh		08h	
4Eh	4Ch	JEDEC Sector Map Parameter Dword-2 Config. Detect-1	04h	Bits 31:0 = Sector map configuration detection command address = 00_00_00_04h: address of CR3NV
4Fh	4Dh		00h	
50h	4Eh		00h	
51h	4Fh		00h	
52h	50h	JEDEC Sector Map Parameter Dword-3 Config. Detect-2	FCh	Bits 31:24 = Read data mask = 0000_0100b: Select bit 2 of the data byte for TBPARM_O value 0= 4-KB parameter sectors at bottom 1= 4-KB parameter sectors at top Bits 23:22 = Configuration detection command address length = 11b: Variable length Bits 21:20 = RFU = 11b Bits 19:16 = Configuration detection command latency = 1111b: variable latency Bits 15:8 = Configuration detection instruction = 65h: Read any register Bits 7:2 = RFU = 111111b Bit 1 = Command Descriptor = 0 Bit 0 = not the end descriptor = 0
53h	51h		65h	
54h	52h		FFh	
55h	53h		04h	
56h	54h	JEDEC Sector Map Parameter Dword-4 Config. Detect-2	02h	Bits 31:0 = Sector map configuration detection command address = 00_00_00_02h: address of CR1NV
57h	55h		00h	
58h	56h		00h	
59h	57h		00h	

Table 71 CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, section 2, sector map parameter table, 512 Mb *(continued)*

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP D word name	Data	Description
5Ah	58h	JEDEC Sector Map Parameter Dword-5 Config. Detect-3	FDh	Bits 31:24 = Read data mask = 0000_0010b: Select bit 1 of the data byte for D8h_NV value 0= 64-KB uniform sectors 1= 256-KB uniform sectors Bits 23:22 = Configuration detection command address length = 11b: Variable length Bits 21:20 = RFU = 11b Bits 19:16 = Configuration detection command latency = 1111b: variable latency Bits 15:8 = Configuration detection instruction = 65h: Read any register Bits 7:2 = RFU = 111111b Bit 1 = Command Descriptor = 0 Bit 0 = The end descriptor = 1
5Bh	59h		65h	
5Ch	5Ah		FFh	
5Dh	5Bh		02h	
5Eh	5Ch	JEDEC Sector Map Parameter Dword-6 Config. Detect-3	04h	Bits 31:0 = Sector map configuration detection command address = 00_00_00_04h: address of CR3NV
5Fh	5Dh		00h	
60h	5Eh		00h	
61h	5Fh		00h	
62h	60h	JEDEC Sector Map Parameter Dword-7 Config-1 Header	FEh	Bits 31:24 = RFU = FFh Bits 23:16 = Region count (Dwords -1) = 02h: Three regions Bits 15:8 = Configuration ID = 01h: 4-KB sectors at bottom with remainder 256-KB sectors Bits 7:2 = RFU = 111111b Bit 1 = Map Descriptor = 1 Bit 0 = not the end descriptor = 0
63h	61h		01h	
64h	62h		02h	
65h	63h		FFh	
66h	64h	JEDEC Sector Map Parameter Dword-8 Config-1 Region-0	F1h	Bits 31:8 = Region size = 00007Fh: Region size as count-1 of 256 Byte units = 8 x 4 KB sectors = 32 KB Count = 32 KB/256 = 128, value = count -1 = 128 -1 = 127 = 7Fh Bits 7:4 = RFU = Fh Erase Type not supported = 0/ supported = 1 Bit 3 = Erase Type 4 support = 0b --- Erase Type 4 is not defined Bit 2 = Erase Type 3 support = 0b --- Erase Type 3 is 256-KB erase and is supported in the 4-KB sector region Bit 1 = Erase Type 2 support = 0b --- Erase Type 2 is 64-KB erase and is not supported in the 4-KB sector region Bit 0 = Erase Type 1 support = 1b --- Erase Type 1 is 4-KB erase and is supported in the 4-KB sector region
67h	65h		7Fh	
68h	66h		00h	
69h	67h		00h	

Table 71 CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, section 2, sector map parameter table, 512 Mb *(continued)*

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP D word name	Data	Description
6Ah	68h	JEDEC Sector Map Parameter Dword-9 Config-1 Region-1	F4h	Bits 31:8 = Region size = 00037Fh: Region size as count-1 of 256 Byte units = 1 x 224 KB sectors = 224 KB Count = 224 KB/256 = 896, value = count -1 = 896 -1 = 895 = 37Fh Bits 7:4 = RFU = Fh Erase Type not supported = 0/ supported = 1 Bit 3 = Erase Type 4 support = 0b --- Erase Type 4 is not defined Bit 2 = Erase Type 3 support = 1b --- Erase Type 3 is 256-KB erase and is supported in the 32-KB sector region Bit 1 = Erase Type 2 support = 0b --- Erase Type 2 is 64-KB erase and is not supported in the 32-KB sector region Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4-KB erase and is not supported in the 32-KB sector region
6Bh	69h		7Fh	
6Ch	6Ah		03h	
6Dh	6Bh		00h	
6Eh	6Ch	JEDEC Sector Map Parameter Dword-10 Config-1 Region-2	F4h	Bits 31:8 = 512 Mb device Region size = 03FBFFh: Region size as count-1 of 256 Byte units = 255 x 256 KB sectors = 65280 KB Count = 65280 KB/256 = 261120, value = count -1 = 261120 -1 = 261119 = 3FBFFh Bits 7:4 = RFU = Fh Erase Type not supported = 0/ supported = 1 Bit 3 = Erase Type 4 support = 0b --- Erase Type 4 is not defined Bit 2 = Erase Type 3 support = 1b --- Erase Type 3 is 256-KB erase and is supported in the 64-KB sector region Bit 1 = Erase Type 2 support = 0b --- Erase Type 2 is 64-KB erase and is not supported in the 64-KB sector region Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4-KB erase and is not supported in the 64-KB sector region
6Fh	6Dh		FFh	
70h	6Eh		FBh	
71h	6Fh		03h (512 Mb	
72h	70h	JEDEC Sector Map Parameter Dword-11 Config-3 Header	FEh	Bits 31:24 = RFU = FFh Bits 23:16 = Region count (Dwords -1) = 02h: Three regions Bits 15:8 = Configuration ID = 03h: 4 KB sectors at top with remainder 256 KB sectors Bits 7:2 = RFU = 111111b Bit 1 = Map Descriptor = 1 Bit 0 = not the end descriptor = 0
73h	71h		03h	
74h	72h		02h	
75h	73h		FFh	

Table 71 CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, section 2, sector map parameter table, 512 Mb *(continued)*

CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP D word name	Data	Description
76h	74h	JEDEC Sector Map Parameter Dword-12 Config-3 Region-0	F4h	Bits 31:8 = 512 Mb device Region size = 03FBFFh: Region size as count-1 of 256 Byte units = 255 x 256 KB sectors = 65280 KB Count = 65280 KB/256 = 261120, value = count -1 = 261120 -1 = 261119 = 3FBFFh Bits 7:4 = RFU = Fh Erase Type not supported = 0/ supported = 1 Bit 3 = Erase Type 4 support = 0b --- Erase Type 4 is not defined Bit 2 = Erase Type 3 support = 1b --- Erase Type 3 is 256-KB erase and is supported in the 64-KB sector region Bit 1 = Erase Type 2 support = 0b --- Erase Type 2 is 64-KB erase and is not supported in the 64-KB sector region Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4-KB erase and is not supported in the 64-KB sector region
77h	75h		FFh	
78h	76h		FBh	
79h	77h		03h (512 Mb	
7Ah	78h	JEDEC Sector Map Parameter Dword-13 Config-3 Region-1	F4h	Bits 31:8 = Region size = 00037Fh: Region size as count-1 of 256 Byte units = 1 x 224 KB sectors = 224 KB Count = 224 KB/256 = 896, value = count -1 = 896 -1 = 895 = 37Fh Bits 7:4 = RFU = Fh Erase Type not supported = 0/ supported = 1 Bit 3 = Erase Type 4 support = 0b --- Erase Type 4 is not defined Bit 2 = Erase Type 3 support = 1b --- Erase Type 3 is 256-KB erase and is supported in the 224-KB sector region Bit 1 = Erase Type 2 support = 0b --- Erase Type 2 is 64-KB erase and is not supported in the 224-KB sector region Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4-KB erase and is not supported in the 224-KB sector region
7Bh	79h		7Fh	
7Ch	7Ah		03h	
7Dh	7Bh		00h	
7Eh	7C	JEDEC Sector Map Parameter Dword-14 Config-3 Region-2	F1h	Bits 31:8 = Region size = 00007Fh: Region size as count-1 of 256 Byte units = 8 x 4 KB sectors = 32 KB Count = 32 KB/256 = 128, value = count -1 = 128 -1 = 127 = 7Fh Bits 7:4 = RFU = Fh Erase Type not supported = 0/ supported = 1 Bit 3 = Erase Type 4 support = 0b --- Erase Type 4 is not defined Bit 2 = Erase Type 3 support = 0b --- Erase Type 3 is 256-KB erase and is not supported in the 4-KB sector region Bit 1 = Erase Type 2 support = 0b --- Erase Type 2 is 64-KB erase and is not supported in the 4-KB sector region Bit 0 = Erase Type 1 support = 1b --- Erase Type 1 is 4-KB erase and is supported in the 4-KB sector region
7Fh	7D		7Fh	
80h	7E		00h	
81h	7F		00h	

Table 71 CFI alternate vendor-specific extended query parameter A5h, JEDEC SFDP Rev B, section 2, sector map parameter table, 512 Mb *(continued)*

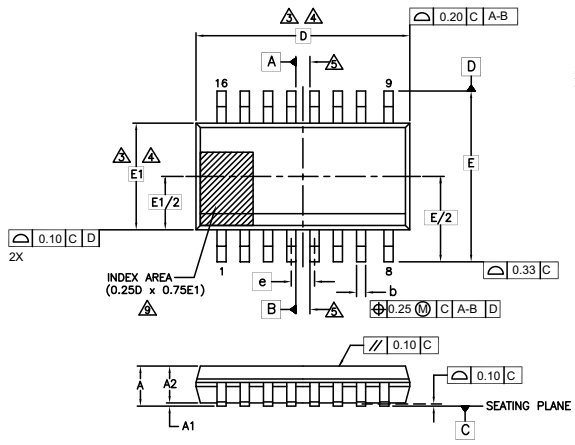
CFI parameter relative byte address offset	SFDP parameter relative byte address offset	SFDP D word name	Data	Description
82h	80h	JEDEC Sector Map Parameter Dword-15 Config-4 Header	FFh	Bits 31:24 = RFU = FFh Bits 23:16 = Region count (Dwords -1) = 00h: One region Bits 15:8 = Configuration ID = 05h: Uniform 256-KB sectors Bits 7:2 = RFU = 111111b Bit 1 = Map Descriptor = 1 Bit 0 = The end descriptor = 1
83h	81h		05h	
84h	82h		00h	
85h	83h		FFh	
86h	84h	JEDEC Sector Map Parameter Dword-16 Config-4 Region-0	F4h	Bits 31:8 = 512 Mb device Region size = 03FFFFh: Region size as count-1 of 256 Byte units = 256 x 256 KB sectors = 65536 KB Count = 65536 KB/256 = 262144, value = count -1 = 262144 -1 = 262143 = 3FFFFh Bits 7:4 = RFU = Fh Erase Type not supported = 0/ supported = 1 Bit 3 = Erase Type 4 support = 0b --- Erase Type 4 is not defined Bit 2 = Erase Type 3 support = 1b --- Erase Type 3 is 256-KB erase and is supported in the 256-KB sector region Bit 1 = Erase Type 2 support = 0b --- Erase Type 2 is 64-KB erase and is not supported in the 256-KB sector region Bit 0 = Erase Type 1 support = 0b --- Erase Type 1 is 4-KB erase and is not supported in the 256-KB sector region
87h	85h		FFh	
88h	86h		FFh	
89h	87h		03h	

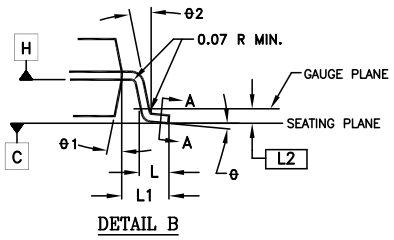
13 Initial delivery state

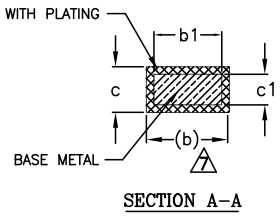
The device is shipped from Infineon with non-volatile bits set as follows:

- The entire memory array is erased: i.e., all bits are set to '1' (each byte contains FFh).
- The OTP address space has the first 16 bytes programmed to a random number. All other bytes are erased to FFh.
- The SFDP address space contains the values as defined in the description of the SFDP address space.
- The ID-CFI address space contains the values as defined in the description of the ID-CFI address space.
- The Status Register 1 non-volatile contains 00h (all SR1NV bits are cleared to 0's).
- The Configuration Register 1 non-volatile contains 00h.
- The Configuration Register 2 non-volatile contains 08h.
- The Configuration Register 3 non-volatile contains 00h.
- The Configuration Register 4 non-volatile contains 10h.
- The Password Register contains FFFFFFFF-FFFFFFFFh.
- All PPB bits are 1.
- The ASP Register bits are FFFFh.

14 Package diagrams







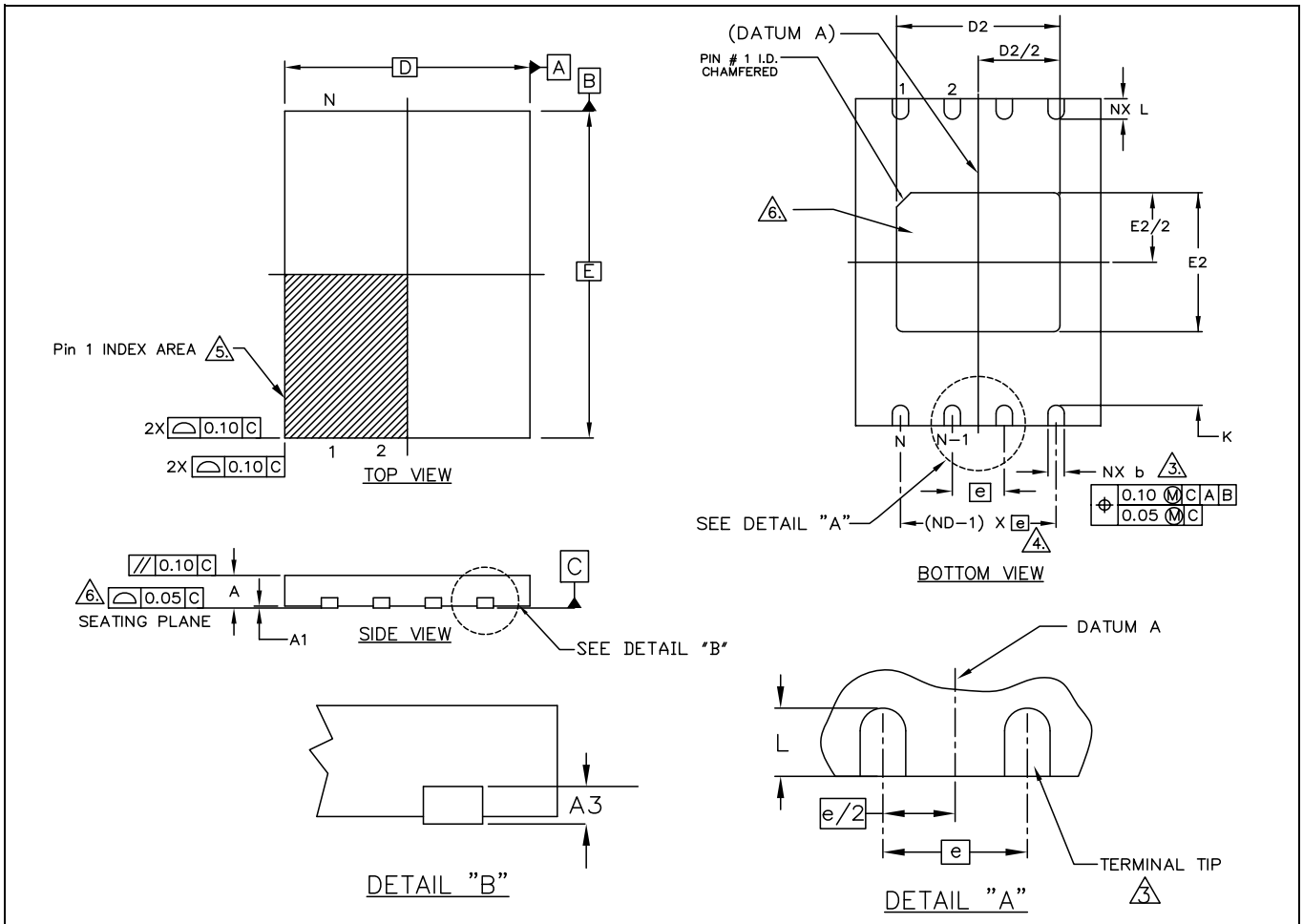
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	2.35	-	2.65
A1	0.10	-	0.30
A2	2.05	-	2.55
b	0.31	-	0.51
b1	0.27	-	0.48
c	0.20	-	0.33
c1	0.20	-	0.30
D	10.30 BSC		
E	10.30 BSC		
E1	7.50 BSC		
e	1.27 BSC		
L	0.40	-	1.27
L1	1.40 REF		
L2	0.25 BSC		
N	16		
h	0.25	-	0.75
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 1994.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. D AND E1 DIMENSIONS ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUSIVE OF ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A AND B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10 mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE LEAD FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED.
10. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.

002-15547 *A

Figure 115 SOIC 16-lead, 10.30 × 7.50 × 2.65 mm (SO3016) (PG-DSO-16)



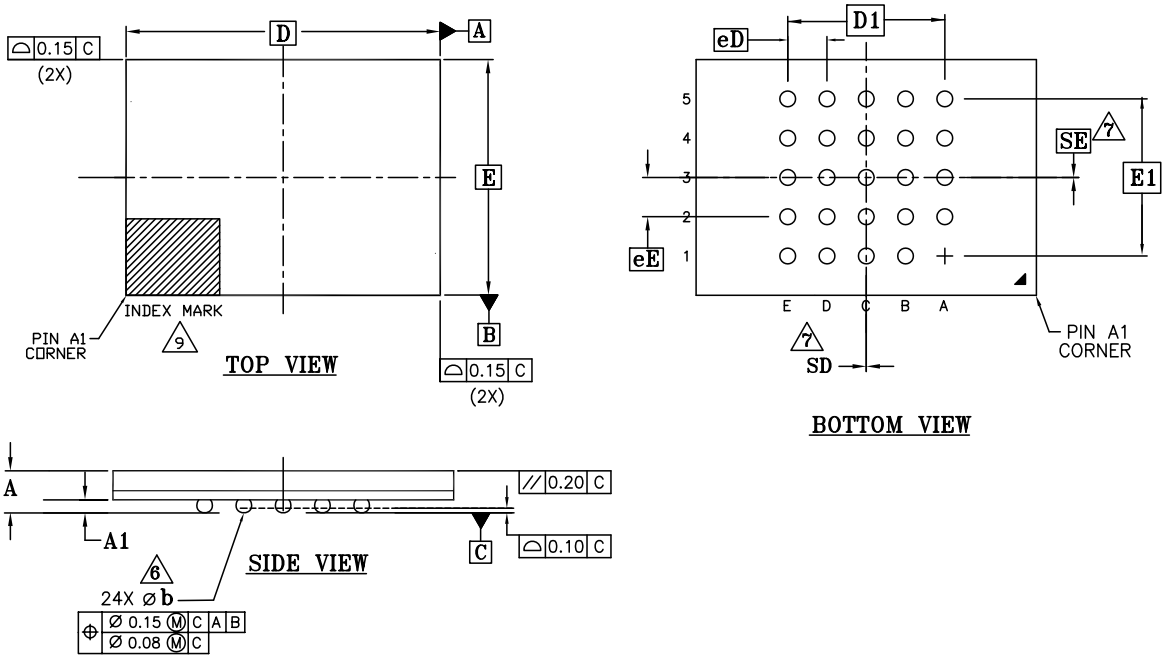
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		1.27 BSC.	
N		8	
ND		4	
L	0.45	0.50	0.55
b	0.35	0.40	0.45
D2	3.90	4.00	4.10
E2	3.30	3.40	3.50
D		6.00 BSC	
E		8.00 BSC	
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3		0.20 REF	
K	0.20	-	-

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A

002-15552 *A

Figure 116 WSON 8-lead DFN 6.0 × 8.0 × 0.8 mm (WNH008) WNH008 4.0 × 3.4 mm E-Pad (SAWN)(PG-WSON-8)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.20	-	-
D		8.00 BSC	
E		6.00 BSC	
D1		4.00 BSC	
E1		4.00 BSC	
MD		5	
ME		5	
N		24	
Ø b	0.35	0.40	0.45
eE		1.00 BSC	
eD		1.00 BSC	
SD		0.00 BSC	
SE		0.00 BSC	

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7 "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

002-15534 **

Figure 117 Ball grid array 24-ball FBGA 8.0 × 6.0 × 1.2 mm (FAB024) (PG-TFBGA-24)

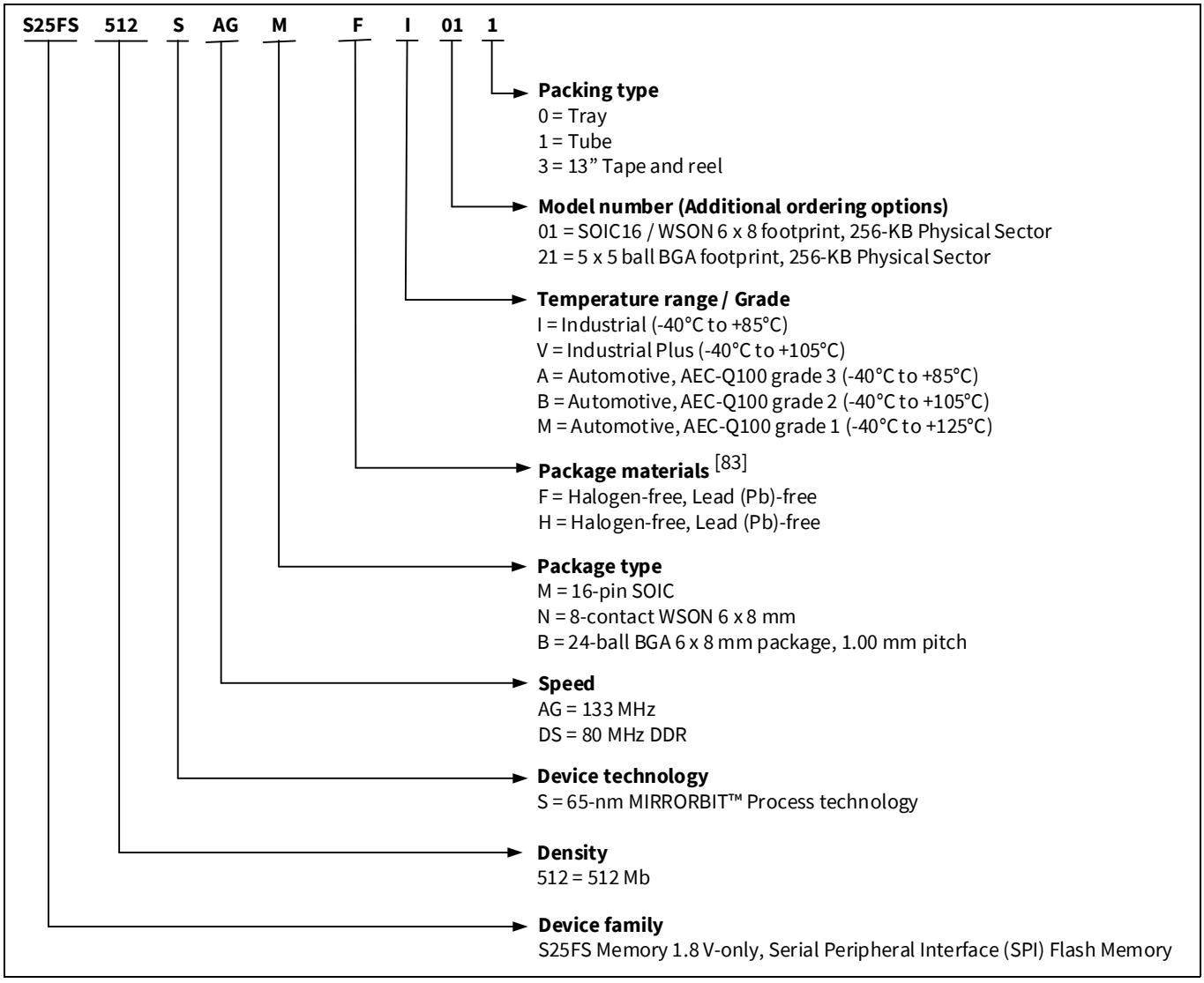
14.1 Special handling instructions for FBGA packages

Flash memory devices in BGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

15 Ordering information

15.1 Ordering part number

The ordering part number is formed by a valid combination of the following:



Note
83. Halogen free definition is in accordance with IE 61249-2-21 specification.

15.2 Valid combinations — standard

Valid combinations list configurations planned to be supported in volume for this device. Contact the local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 72 Valid combinations — standard

Base ordering part number	Speed option	Package and temperature	Model number	Packing type	Package marking
S25FS512S	AG	MFI, MFV	01	0, 1, 3	FS512S + A +(Temp) + F + (Model Number)
		NFI, NFV			
		BHI, BHV	21	0, 3	FS512S + A +(Temp) + H + (Model Number)
	DS	MFI, MFV	01	0, 1, 3	FS512S + D +(Temp) + F + (Model Number)
		NFI, NFV			
		BHI, BHV	21	0, 3	FS512S + D +(Temp) + H + (Model Number)

15.3 Valid combinations — automotive grade / AEC-Q100

Table 73 lists configurations that are automotive grade / AEC-Q100 qualified and are planned to be available in volume. The table will be updated as new combinations are released. Consult your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Production Part Approval Process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non–AEC-Q100 grade products are not manufactured or documented in full compliance with
ISO/TS-16949 requirements.

AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

Table 73 Valid combinations — automotive grade / AEC-Q100

Base ordering part number	Speed option	Package and temperature	Model number	Packing type	Package marking
S25FS512S	AG	MFA, MFB, MFM	01	0, 1, 3	FS512S + A + (Temp) + F + (Model Number)
		NFA, NFB, NFM			
		BHA, BHB, BHM	21	0, 3	FS512S + A + (Temp) + H + (Model Number)
	DS	MFA, MFB, MFM	01	0, 1, 3	FS512S + D + (Temp) + F + (Model Number)
		NFA, NFB, NFM			
		BHA, BHB, BHM	21	0, 3	FS512S + D + (Temp) + H + (Model Number)

Revision history

Document version	Date of release	Description of changes
*N	2021-05-02	Publish to Web.
*O	2023-10-03	**Table 31**: Updated the default state for “WRAP ENABLE” bit to 1. Updated the package title in **Figure 117**. **Table 53**: Updated the test conditions 100k program cycles for 2 years.

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