

CY14MB064Q2A-SXQ

[Follow](#)
[Buy online](#)

- Overview**
- [Parametrics](#)
- [Documents](#)
- [Order](#)
- [Support](#)

Parametrics

Parametrics	CY14MB064Q2A-SXQ
Density	64 kBit
Frequency	40 MHz
Interfaces	SPI
Lead Ball Finish	Pure Sn
Operating Temperature min max	-40 °C 105 °C
Operating Voltage min max	2.7 V 3.6 V
Operating Voltage (VCCQ) max	3.6 V
Organization (X x Y)	8Kb x 8
Peak Reflow Temp	260 °C
Publish in NPSG	Y
Publish in PSG	Y
Qualification	Industrial(Q)
Speed	-

Documents

> [Login to myInfineon](#) to see all documents available

Product Qualification Report

[QTP 102204: 1Meg Serial Non-Volatile SRAM Product Family S8 Technology CMI \(Feb 4\) 08_00 | 2021-11-11 | pdf | 153 KB](#) > EN [Share](#)

Order

Sales Product Name	CY14MB064Q2A-SXQ
OPN Info	CY14MB064Q2A-SXQ
Product Status	active and preferred
Infineon Package name	PG-DSO-8
Standard Package name	
Order online	Buy online
Completely lead free	yes
Halogen free	yes
RoHS compliant	yes
Packing Size	485
Packing Type	TUBE
Moisture Level	
Moisture Packing	DRY

Support

Search the FAQs! Enter your search terms...



Top 6 FAQs. Use the search bar above to show more!

<p>Async SRAMs: Interchangeability of Data & Address pins</p> <p>In Asynchronous SRAMs, the address pins (Ax) can be assigned in any bit order. For instance, pin A15 of CPU can be connected to A0 of SRAM, A10 of CPU to A1 of SRAM etc. Address assignment can be made a...</p> <p>+ Read more</p>	<p>Byte Power Down Feature in MOBL™ SRAMs</p> <p>The Byte Power Down (BPD) function, available in certain MOBL™ SRAMs, makes the BHE#-BLE# combination act as chip enable when disabled together. This means that when BHE# and BLE# are...</p> <p>+ Read more</p>	<p>MPWR SRAMs: Time to write when device wakes up from standby</p> <p>The minimum /WE pulse required to write the data into a memory cell is called the write pulse width (TPWE). This parameter is determined by how fast the write enabling circuit connects the data input...</p> <p>+ Read more</p>
<p>Is CY7C1041DV33 an interleaved part?</p> <p>The device is an interleaved part. Two adjacent bits of a logical word are separated by 7 other bits. This design scheme significantly reduces the susceptibility of the device to multi-bit...</p> <p>+ Read more</p>	<p>Load Capacitance of Tri-State data bus of many SRAMs connected together</p> <p>Eventhough only one SRAM will be using the data bus at a time, it will see the load capacitance due to all other data busses from idle SRAMs. If the pin capaticance of one SRAM's Tri-State Data bus is 15pF a...</p> <p>+ Read more</p>	<p>Technical Support</p> <p>In order to enable us to process your inquiry as efficiently as possible and ensure your case is duly reported, we kindly ask you to submit your request via the support form:...</p> <p>+ Read more</p>

Ask for technical support	Call us toll-free or request a call back	Live chat with our Support Center	Ask our community for support
---------------------------	------------------------------------------	-----------------------------------	-------------------------------



TOP

Follow us



© 1999 - 2022 Infineon Technologies AG > Usage of this website is subject to our Usage Terms > Imprint > Contact > Privacy Policy > Glossary

苏CP备15016286号-1 | 苏公网安备 32021402001016号 | 营业执照

