IRHNS9A7064
JANSR2N7652U2A

RADIATION HARDENED POWER MOSFET SURFACE MOUNT (SupIR-SMD)

60V, N-CHANNEL
REF: MIL-PRF-19500/777
R9 TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	I_D	QPL Part Number
IRHNS9A7064	100 kRads (Si)	4.0mΩ	100A*	JANSR2N7652U2A
IRHNS9A3064	300 kRads (Si)	4.0mΩ	100A*	JANSF2N7652U2A


SupIR-SMD

Description

IR HiRel R9 technology provides superior power MOSFETs for space applications. These devices have improved immunity to Single Event Effect (SEE) and have been characterized for useful performance with Linear Energy Transfer (LET) up to 90MeV/(mg/cm^2). Their combination of low RDS(on) and faster switching times reduces the power losses and increases power density in today's high speed switching applications such as DC-DC converters and motor controllers. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching temperature stability of electrical parameters.

Features

- Low RDS(on)
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Ceramic Package
- Light Weight
- Surface Mount
- ESD Rating: Class 3B per MIL-STD-750, Method 1020

Absolute Maximum Ratings — Pre-Irradiation

Symbol	Parameter	Value	Units
I_{D1} @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	100*	A
I_{D2} @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	100*	
I_{DM} @ T_C = 25°C	Pulsed Drain Current ①	400	
P_D @ T_C = 25°C	Maximum Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	4000	mJ
I_{AR}	Avalanche Current ①	100	A
E_{AR}	Repetitive Avalanche Energy ①	25	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.8	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (for 5s)	
	Weight	3.3 (Typical)	g

* Current is limited by package

For Footnotes, refer to the page 2.

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.06	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	4.0	mΩ	V_{GS} = 12V, I_{D2} = 100A* ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 6.0mA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-7.2	—	mV/°C	
Gfs	Forward Transconductance	50	—	—	S	V_{DS} = 15V, I_{D2} = 100A* ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	µA	V_{DS} = 48V, V_{GS} = 0V
		—	—	25		V_{DS} = 48V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_G	Total Gate Charge	—	—	194	nC	I_{D1} = 100A*
Q_{GS}	Gate-to-Source Charge	—	—	50		V_{DS} = 30V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	69		V_{GS} = 12V
$t_{d(on)}$	Turn-On Delay Time	—	—	30	ns	V_{DD} = 30V
tr	Rise Time	—	—	180		I_{D1} = 100A
$t_{d(off)}$	Turn-Off Delay Time	—	—	113		R_G = 2.35Ω
t_f	Fall Time	—	—	66		V_{GS} = 12V
Ls +L_D	Total Inductance	—	12	—	nH	Measured from center of Drain pad to center of Source pad
C_{iss}	Input Capacitance	—	9100	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	3700	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	30	—		f = 1.0MHz
R_G	Gate Resistance	—	1.5	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	100*	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	400		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_J = 25°C,I_S =100A*, V_{GS} = 0V④
t_{rr}	Reverse Recovery Time	—	130	165	ns	T_J = 25°C, I_F =100A*
Q_{rr}	Reverse Recovery Charge	—	775	—	nC	V_{DD} ≤ 25V, di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

* Current is limited by package

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.50	°C/W
$R_{\theta J\text{-}PCB}$	Junction-to-PC Board (Soldered to 2" sq.inch copper clad board)	—	1.6	—	

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.
② V_{DD} = 60V, starting T_J = 25°C, L = 0.8mH, Peak I_L = 100A, V_{GS} = 20V
③ I_{SD} ≤ 100A, di/dt ≤ 1155A/µs, V_{DD} ≤ 60V, T_J ≤ 150°C
④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%
⑤ Total Dose Irradiation with V_{GS} Bias. 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
⑥ Total Dose Irradiation with V_{DS} Bias. 48 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

Symbol	Parameter	Up to 300 kRads (Si) [1]		Units	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	——	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	V	V_{DS} = V_{GS}, I_D = 6.0mA
I_{GSS}	Gate-to-Source Leakage Forward	——	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	——	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	——	1.0	µA	V_{DS} = 48V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	——	6.0	mΩ	V_{GS} = 12V, I_{D2} = 75A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (SupIR-SMD)	——	4.0	mΩ	V_{GS} = 12V, I_{D2} = 100A
V_{SD}	Diode Forward Voltage	——	1.2	V	V_{GS} = 0V, I_S = 75A

1. Part numbers IRHNS9A7064 (JANSR2N7652U2A) and IRHNS9A3064 (JANSF2N7652U2A)

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm²))	Energy (MeV)	Range (µm)	VDS (V)			
			@ VGS = 0V	@ VGS = -1V	@ VGS = -5V	@ VGS = -10V
38 ± 5%	355 ± 7.5%	43 ± 7.5%	60	60	60	60
60 ± 5%	753 ± 7.5%	60 ± 10%	60	60	60	60
90 ± 5%	1515 ± 7.5%	82 ± 7.5%	60	60	——	——

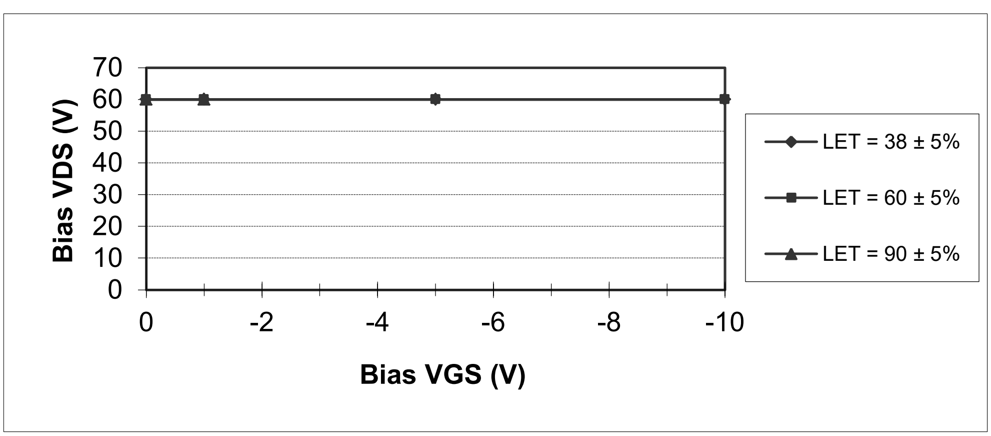


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

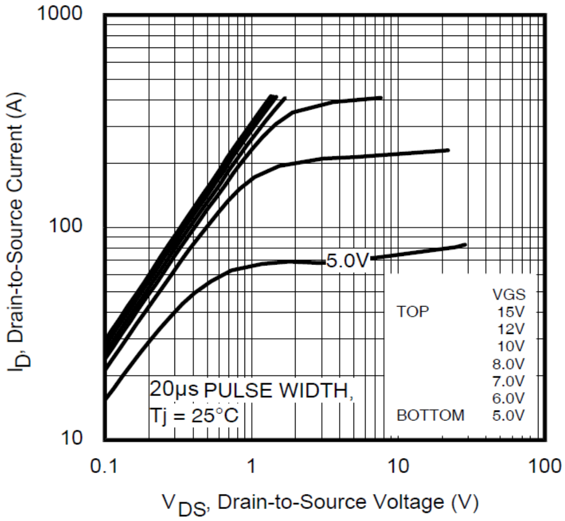


Fig 1. Typical Output Characteristics

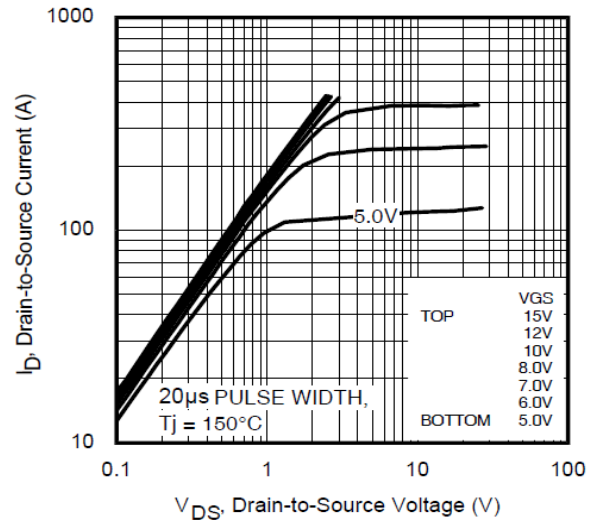


Fig 2. Typical Output Characteristics

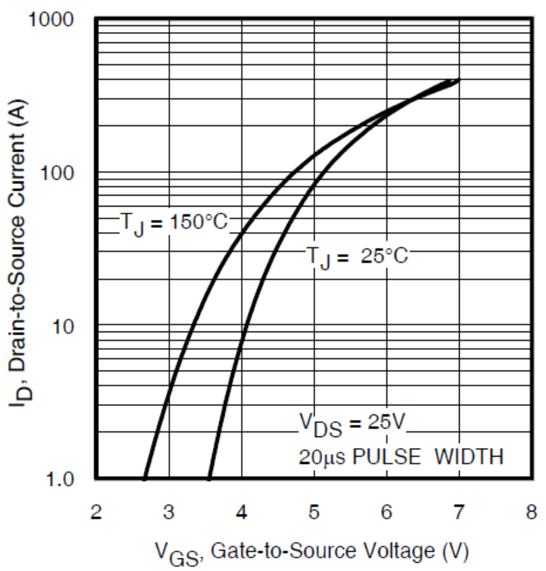


Fig 3. Typical Transfer Characteristics

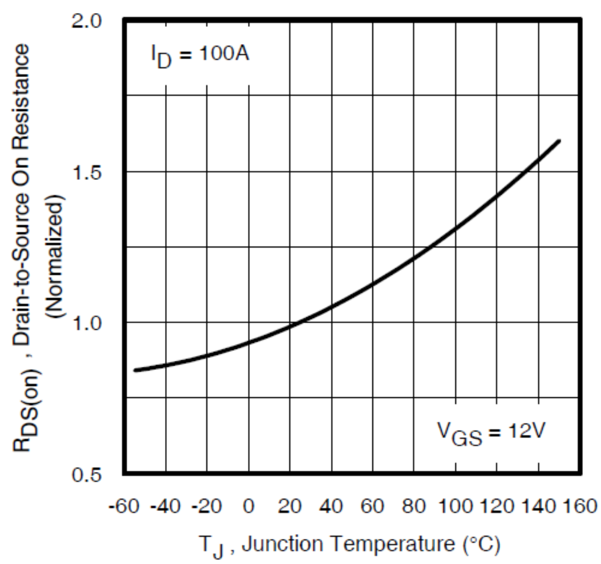


Fig 4. Normalized On-Resistance Vs. Temperature

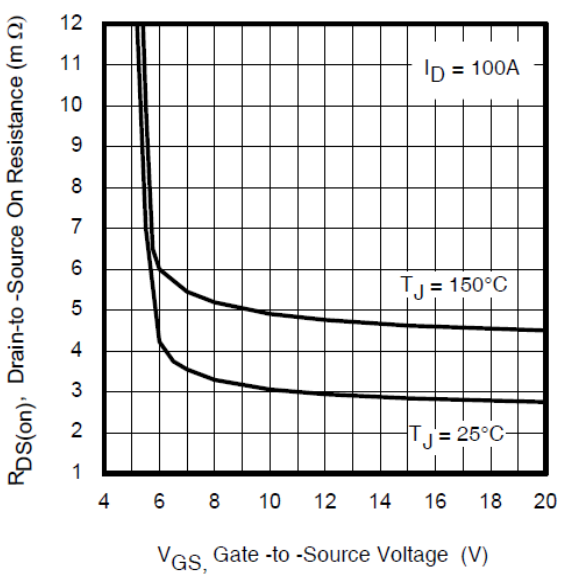


Fig 5. Typical On-Resistance Vs Gate Voltage

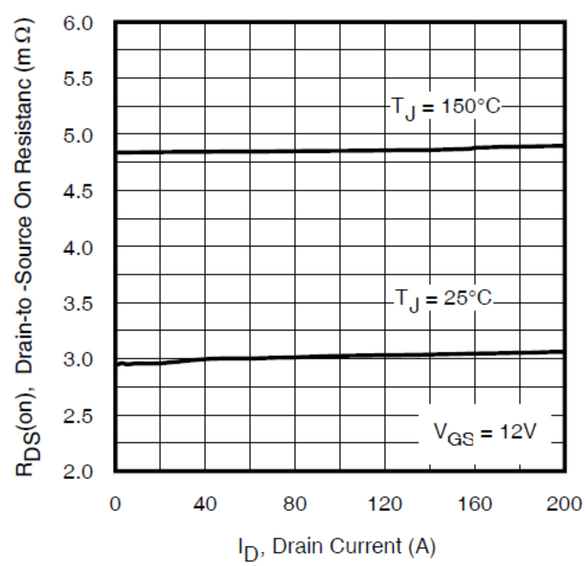


Fig 6. Typical On-Resistance Vs Drain Current

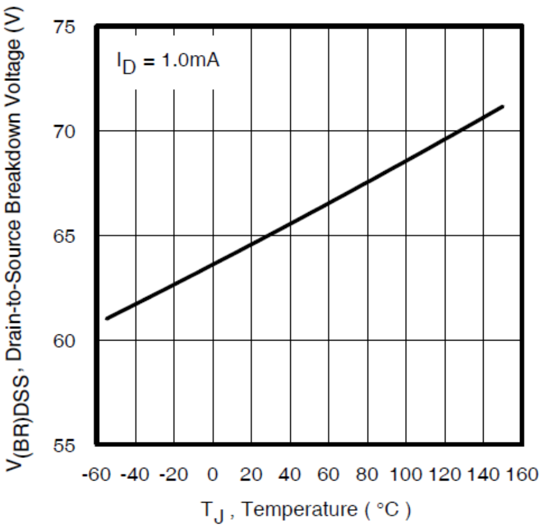


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

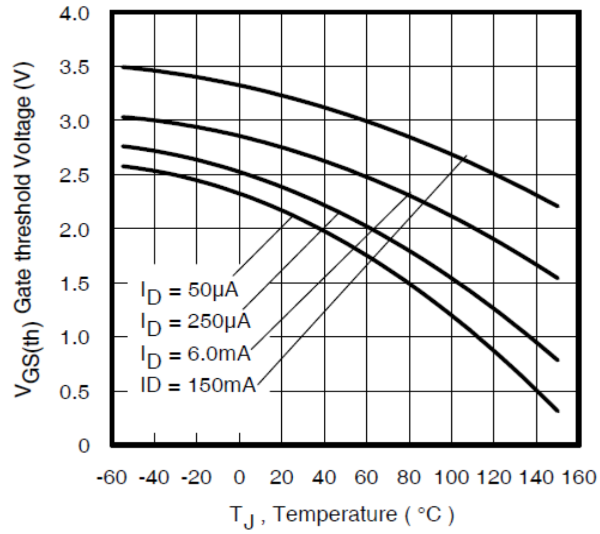


Fig 8. Typical Threshold Voltage Vs Temperature

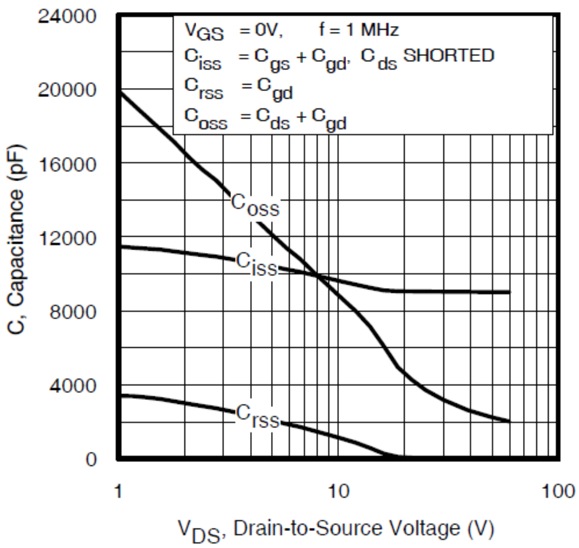


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

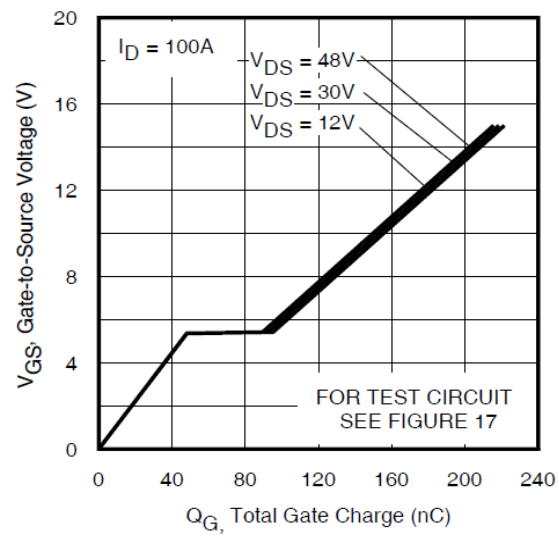


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

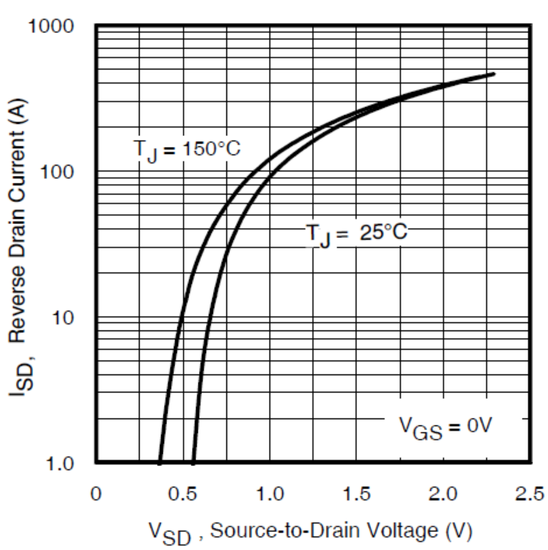


Fig 11. Typical Source-Drain Diode Forward Voltage

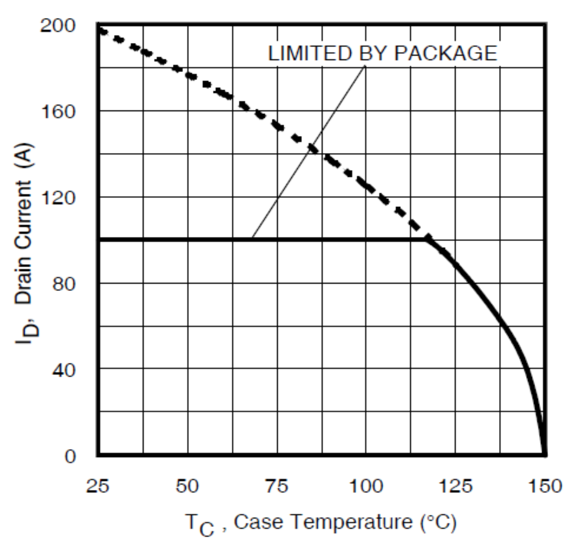


Fig 12. Maximum Drain Current Vs.Case Temperature

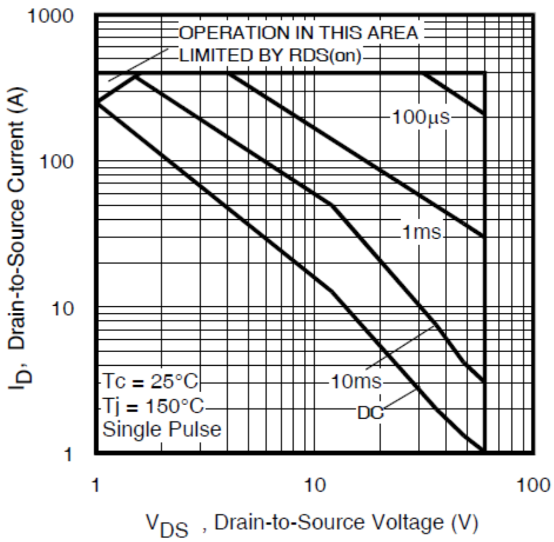


Fig 13. Maximum Safe Operating Area

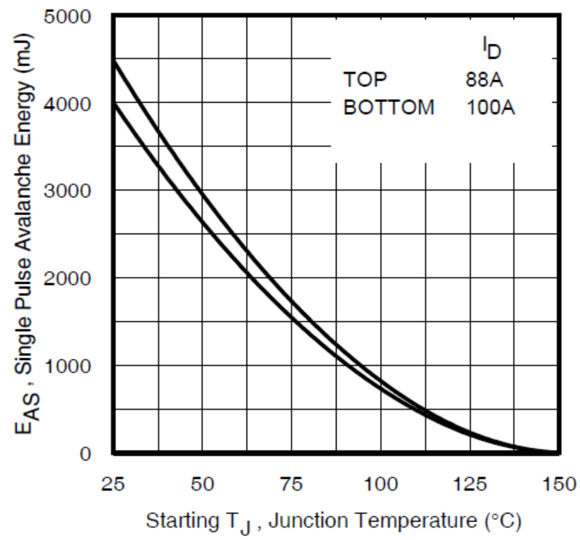


Fig 14. Maximum Avalanche Energy Vs. Drain Current

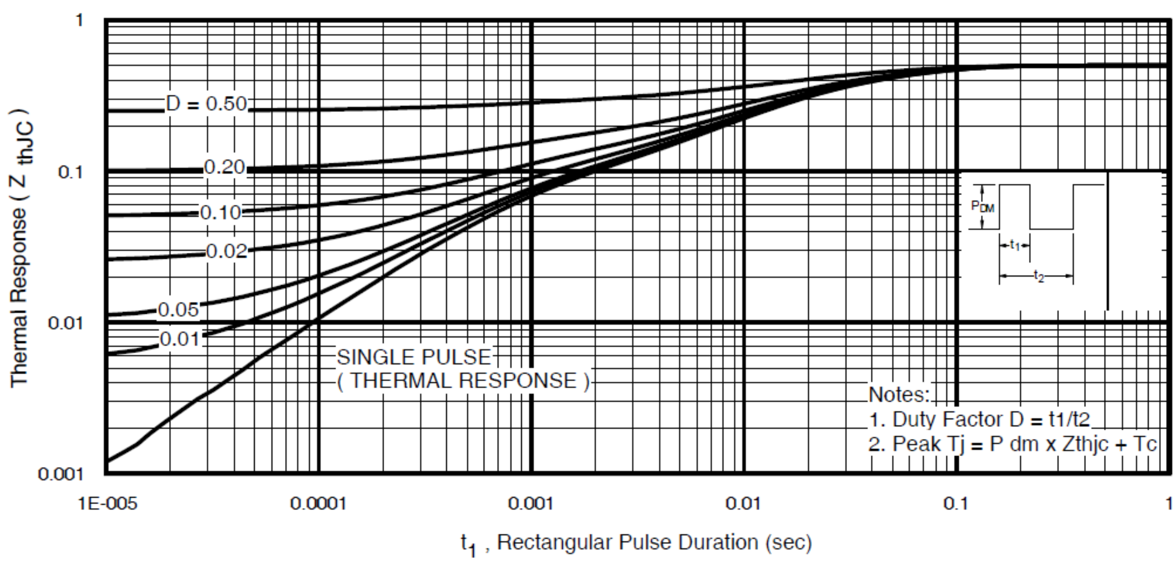


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

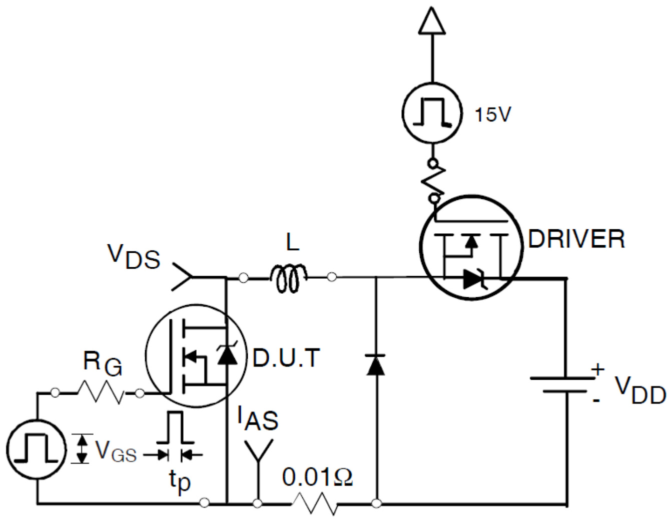


Fig 16a. Unclamped Inductive Test Circuit

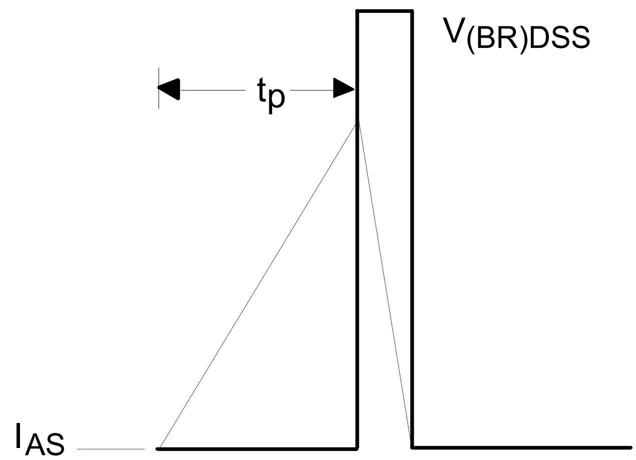


Fig 16b. Unclamped Inductive Waveforms

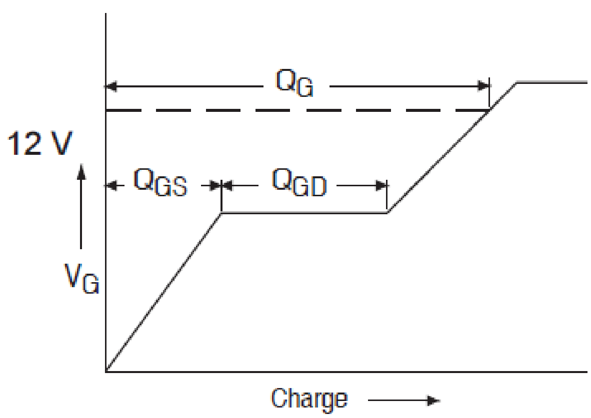


Fig 17a. Gate Charge Waveform

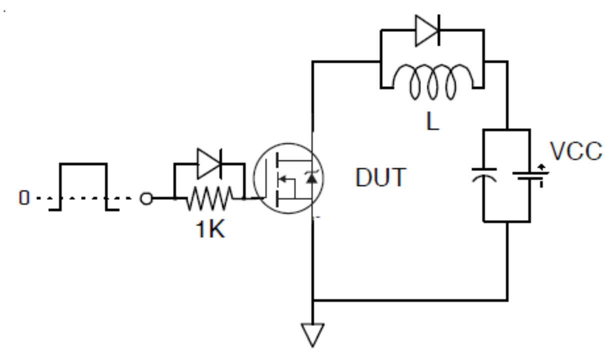


Fig 17b. Gate Charge Test Circuit

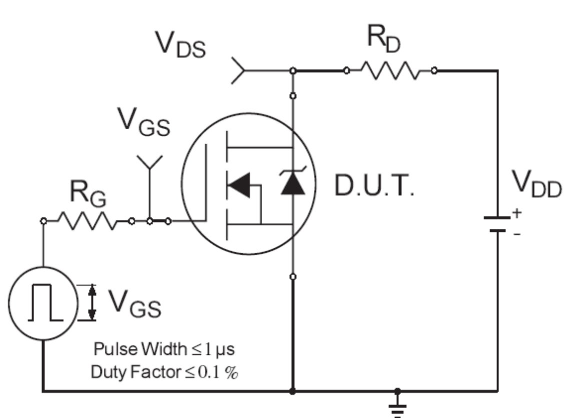


Fig 18a. Switching Time Test Circuit

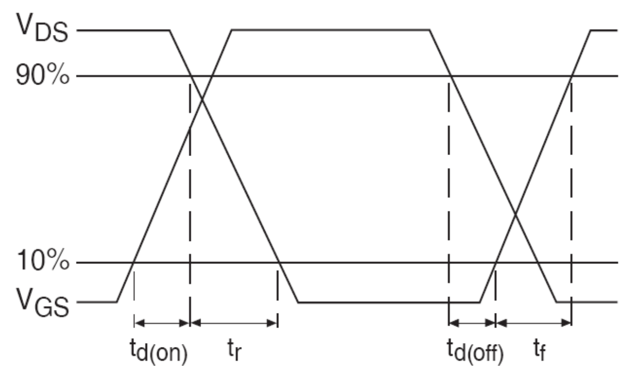
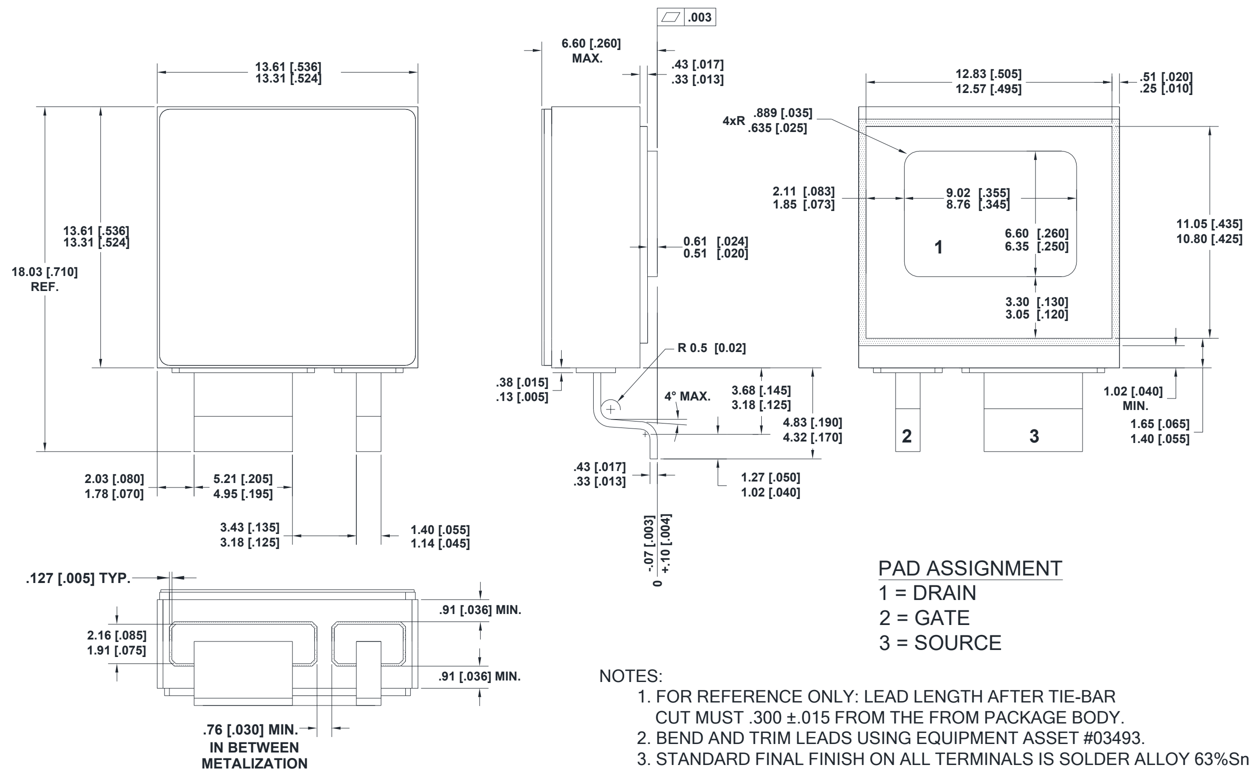


Fig 18b. Switching Time Waveforms

Note: For the most updated package outline, please see the website: [SupIR-SMD]()

Case Outline and Dimensions — SupIR-SMD

REV.	DESCRIPTION	ECN	DATE
E	INITIAL RELEASE	1120_ER6904	4-3-20



PAD ASSIGNMENT
1 = DRAIN
2 = GATE
3 = SOURCE

NOTES:
1. FOR REFERENCE ONLY: LEAD LENGTH AFTER TIE-BAR CUT MUST .300 ±.015 FROM THE FROM PACKAGE BODY.
2. BEND AND TRIM LEADS USING EQUIPMENT ASSET #03493.
3. STANDARD FINAL FINISH ON ALL TERMINALS IS SOLDER ALLOY 63%Sn 37%Pb.

IR HiRel
An Infineon Technologies Company

TITLE: CASE OUTLINE STD SUPSMD2, LF	
DRAWING NO. D101003G-WEB	REV E

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