

# BFR380L3

## Low profile linear silicon NPN RF bipolar transistor



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## Product description

The BFR380L3 is a low noise device based on Si that is part of Infineon's established third generation RF bipolar transistor family. Its high transition frequency and low current and low noise characteristics make the device suitable for a broad range of applications as high as 3.5 GHz. It remains cost competitive without compromising on ease of use.



## Feature list

- Minimum noise figure  $NF_{min} = 1.1$  dB at 1.8 GHz, 3 V, 8 mA
- High gain  $G_{ma} = 14$  dB at 1.8 GHz, 3 V, 40 mA
- $OIP_3 = 29.5$  dBm at 1.8 GHz, 3 V, 40 mA

## Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

## Potential applications

- Low noise amplifiers (LNAs) for DVB-T/H
- LNAs for TV white space application
- Low noise, high linearity amplifiers for sub-1 GHz ISM band applications

## Device information

**Table 1** Part information

Product name / Ordering code	Package	Pin configuration			Marking	Pieces / Reel
BFR380L3 / BFR380L3E6327XTMA1	TSLP-3-1	1 = B	2 = E	3 = C	FC	15000

**Attention:** ESD (Electrostatic discharge) sensitive device, observe handling precautions

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**Absolute maximum ratings**

**1 Absolute maximum ratings**

**Table 2 Absolute maximum ratings at  $T_A = 25\text{ °C}$  (unless otherwise specified)**

Parameter	Symbol	Values		Unit	Note or test condition
		Min.	Max.		
Collector emitter voltage	$V_{CEO}$	-	6	V	Open base
Collector emitter voltage	$V_{CES}$		15		E-B short circuited
Collector base voltage	$V_{CBO}$		15		Open emitter
Emitter base voltage	$V_{EBO}$		2		Open collector
Base current	$I_B$		14	mA	-
Collector current	$I_C$		80		
Total power dissipation <sup>1)</sup>	$P_{tot}$		380	mW	$T_S \leq 96\text{ °C}$
Junction temperature	$T_J$		150	°C	-
Storage temperature	$T_{Stg}$	-55			

**Attention:** *Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding only one of these values may cause irreversible damage to the integrated circuit.*

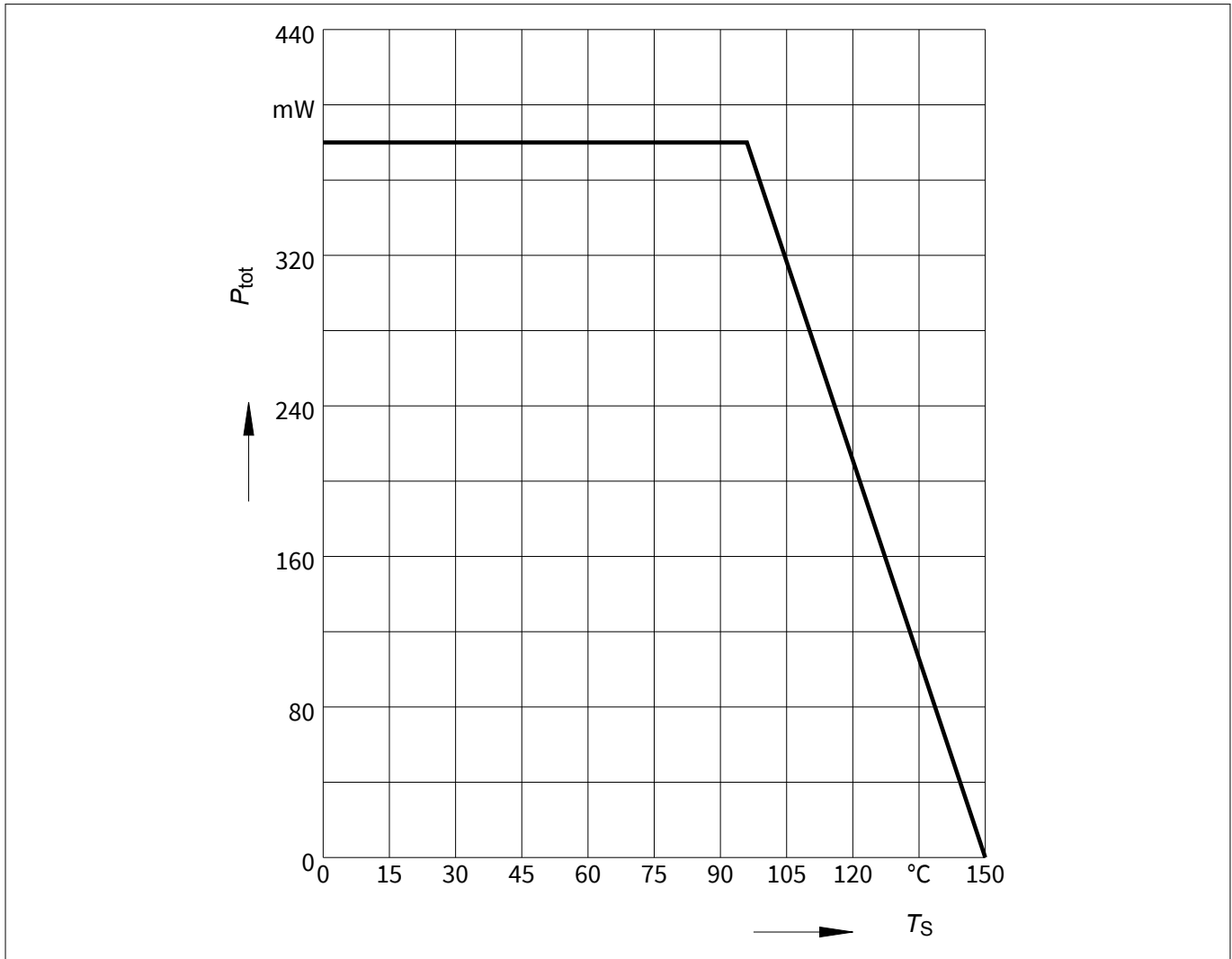
<sup>1</sup>  $T_S$  is the soldering point temperature.  $T_S$  is measured on the emitter lead at the soldering point of the PCB.

**Thermal characteristics**

**2 Thermal characteristics**

**Table 3 Thermal resistance**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Junction - soldering point	$R_{thJS}$	-	140	-	K/W	-



**Figure 1 Total power dissipation  $P_{tot} = f(T_s)$**

**Electrical characteristics**

**3 Electrical characteristics**

**3.1 DC characteristics**

**Table 4 DC characteristics at  $T_A = 25\text{ °C}$  (unless otherwise specified)**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Collector emitter breakdown voltage	$V_{(BR)CEO}$	6	9	–	V	$I_C = 1\text{ mA}$ , $I_B = 0$ , open base
Collector emitter leakage current	$I_{CES}$	–	1	30 <sup>2)</sup>	nA	$V_{CE} = 5\text{ V}$ , $V_{BE} = 0$ , E-B short circuited
			–	1000 <sup>2)</sup>		$V_{CE} = 15\text{ V}$ , $V_{BE} = 0$ , E-B short circuited
Collector base leakage current	$I_{CBO}$			30 <sup>2)</sup>		$V_{CB} = 5\text{ V}$ , $I_E = 0$ , open emitter
Emitter base leakage current	$I_{EBO}$		10	500 <sup>2)</sup>		$V_{EB} = 1\text{ V}$ , $I_C = 0$ , open collector
DC current gain	$h_{FE}$	90	120	160		$V_{CE} = 3\text{ V}$ , $I_C = 40\text{ mA}$ , pulse measured

**3.2 General AC characteristics**

**Table 5 General AC characteristics at  $T_A = 25\text{ °C}$**

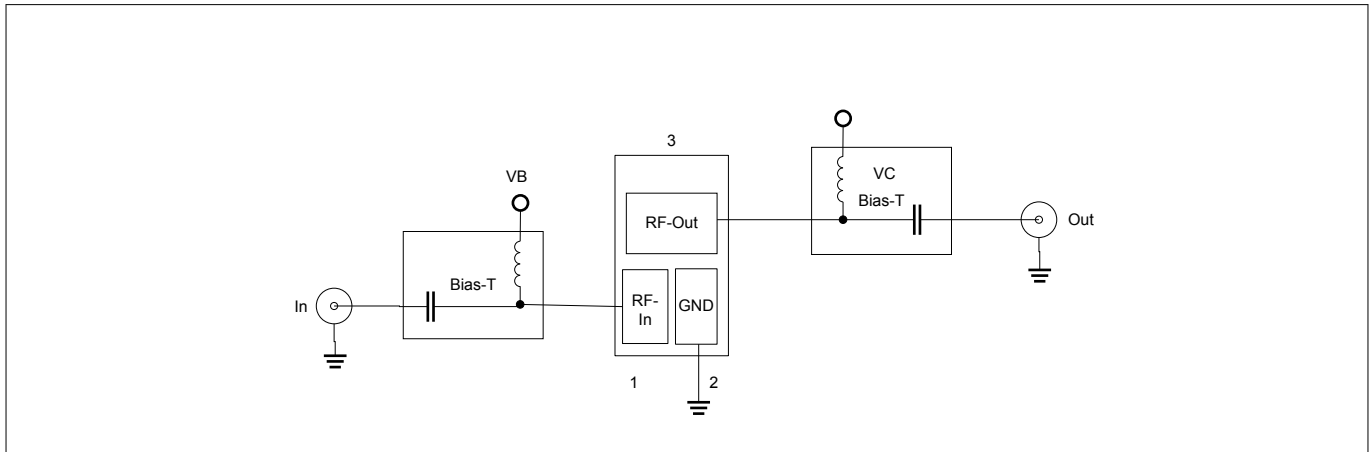
Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Transition frequency	$f_T$	11	14	–	GHz	$V_{CE} = 3\text{ V}$ , $I_C = 40\text{ mA}$ , $f = 1\text{ GHz}$
Collector base capacitance	$C_{CB}$	–	0.45	0.8	pF	$V_{CB} = 5\text{ V}$ , $V_{BE} = 0$ , $f = 1\text{ MHz}$ , emitter grounded
Collector emitter capacitance	$C_{CE}$		0.18	–		$V_{CE} = 5\text{ V}$ , $V_{BE} = 0$ , $f = 1\text{ MHz}$ , base grounded
Emitter base capacitance	$C_{EB}$		1			$V_{EB} = 0.5\text{ V}$ , $V_{CB} = 0$ , $f = 1\text{ MHz}$ , collector grounded

<sup>2</sup> Maximum values not limited by the device but by the short cycle time of the 100% test.

**Electrical characteristics**

**3.3 Frequency dependent AC characteristics**

Measurement setup is a test fixture with Bias-T's in a 50 Ω system,  $T_A = 25\text{ }^\circ\text{C}$ .



**Figure 2 Testing circuit**

**Table 6 AC characteristics,  $V_{CE} = 3\text{ V}$ ,  $f = 1.8\text{ GHz}$**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Power gain					dB	$I_C = 40\text{ mA}$
<ul style="list-style-type: none"> <li>Maximum power gain</li> <li>Transducer gain</li> </ul>	$G_{ma}$ $ S_{21} ^2$	11.5 9.5	14 11.5	16.5 13.5		
Noise figure					dBm	$I_C = 8\text{ mA}$
<ul style="list-style-type: none"> <li>Minimum noise figure</li> </ul>	$NF_{min}$	0.5	1.1	2.1		
Linearity					dBm	$I_C = 40\text{ mA}$ , $Z_S = Z_L = 50\text{ }\Omega$ , $Z_S = Z_{S,opt}$ , $Z_L = Z_{L,opt}$
<ul style="list-style-type: none"> <li>3rd order intercept point at output</li> </ul>	$OIP_3$	–	29.5	–		
<ul style="list-style-type: none"> <li>1 dB gain compression point at output</li> </ul>	$OP_{1dB}$ $OP_{1dB}$		16 19.5			

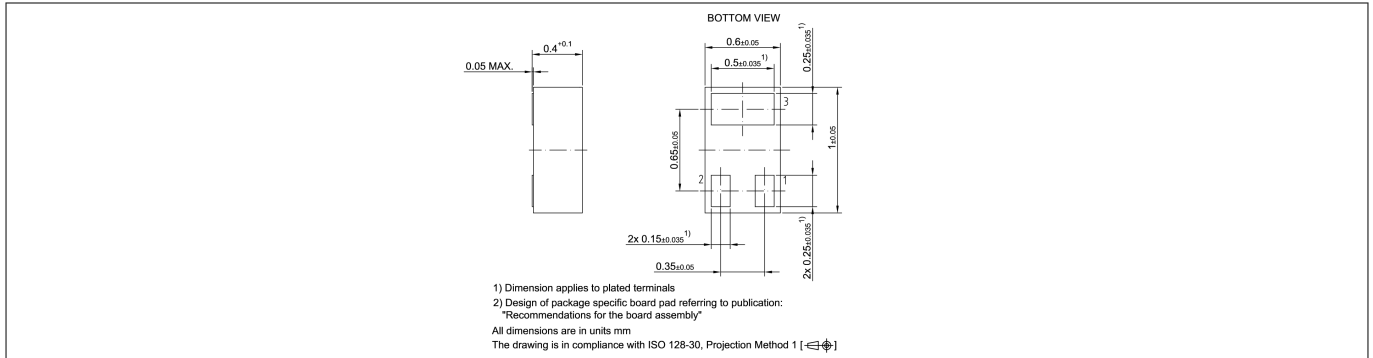
**Table 7 AC characteristics,  $V_{CE} = 3\text{ V}$ ,  $f = 3\text{ GHz}$**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Power gain					dB	$I_C = 40\text{ mA}$
<ul style="list-style-type: none"> <li>Maximum power gain</li> <li>Transducer gain</li> </ul>	$G_{ma}$ $ S_{21} ^2$	7.5 5.5	10 7.5	12.5 9.5		

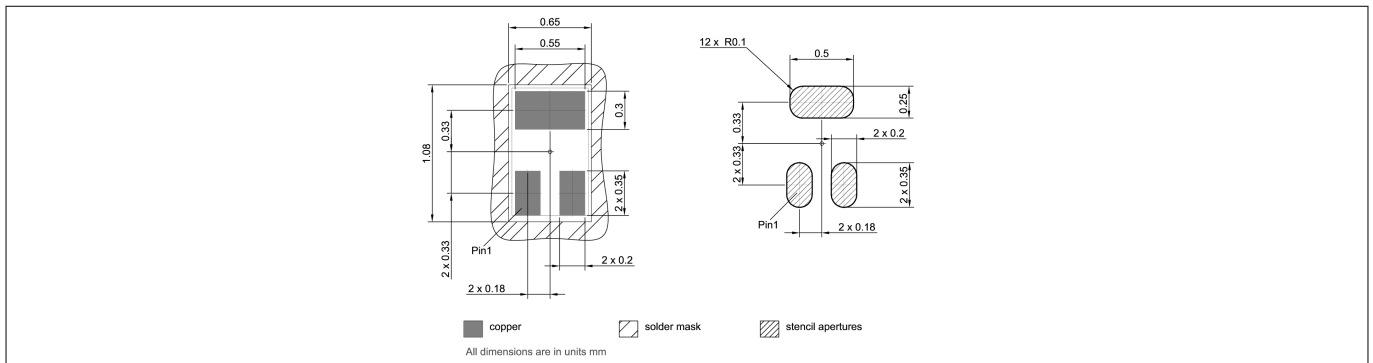
Note:  $G_{ms} = |S_{21} / S_{12}|$  for  $k < 1$ ;  $G_{ma} = |S_{21} / S_{12}| (k - (k^2 - 1)^{1/2})$  for  $k > 1$ . In order to get the  $NF_{min}$  values stated in this chapter, the test fixture losses have been subtracted from all measured results.  $OIP_3$  value depends on termination of all intermodulation frequency components. Termination used for this measurement is 50 Ω from 0.1 MHz to 6 GHz.

**Package information TSLP-3-1**

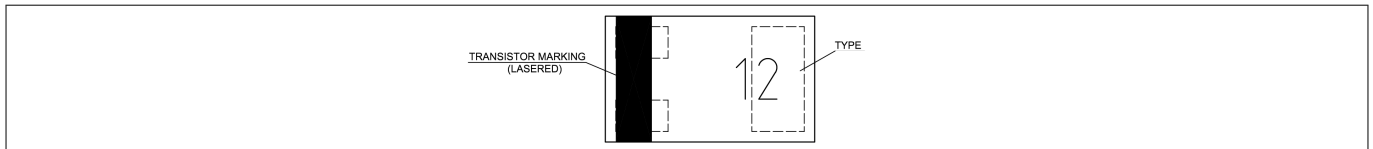
**4 Package information TSLP-3-1**



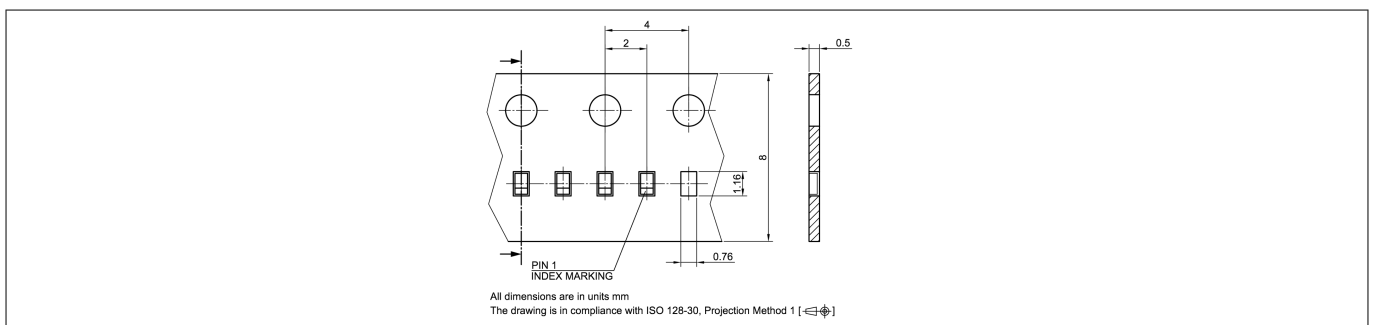
**Figure 3 Package outline**



**Figure 4 Foot print**



**Figure 5 Marking layout example**



**Figure 6 Tape information**

*Note:* See our [Recommendations for Printed Circuit Board Assembly of TSLP/TSSLP/TSNP Packages](#). The marking layout is an example. For the real marking code refer to the device information on the first page. The number of characters shown in the layout example is not necessarily the real one. The marking layout can consist of less characters.

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Revision history

## Revision history

Document version	Date of release	Description of changes
Revision 2.0	2019-01-25	New datasheet layout.



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