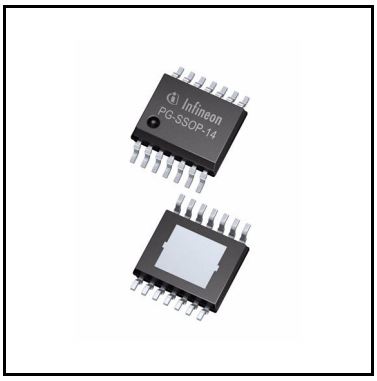
LITIX™ Power

TLD5095EL - Multitopology LITIX™Power DC/DC Controller IC

AEC Qualified RoHS



1 Overview

Description

The TLD5095EL is a smart multitopology LED controller with built in protection and diagnostic features. The main function of this device is to regulate a constant LED current. The constant current regulation is especially beneficial for LED color accuracy and longer lifetime. The controller concept of the TLD5095EL allows a multi-purpose usage such as Boost, Buck, Buck-Boost, SEPIC and Flyback configuration with various load current levels by simply adjusting the external components. The TLD5095EL has a PWM output for dimming a LED load. The diagnostics are communicated on a status output (pin ST) to indicate a fault condition such as an LED open circuit. The switching frequency is adjustable in the range of 100 kHz to 500 kHz and can be synchronized to an external clock source. The TLD5095EL features an enable function reducing the shut-down current consumption to < 10 µA. The current mode regulation scheme of this device provides a stable regulation loop maintained by small external compensation components. The integrated soft-start feature limits the current peak as well as voltage overshoot at start-up. This IC is suited for use in the harsh automotive environments and provides protection functions such as output overvoltage protection and overtemperature shutdown.

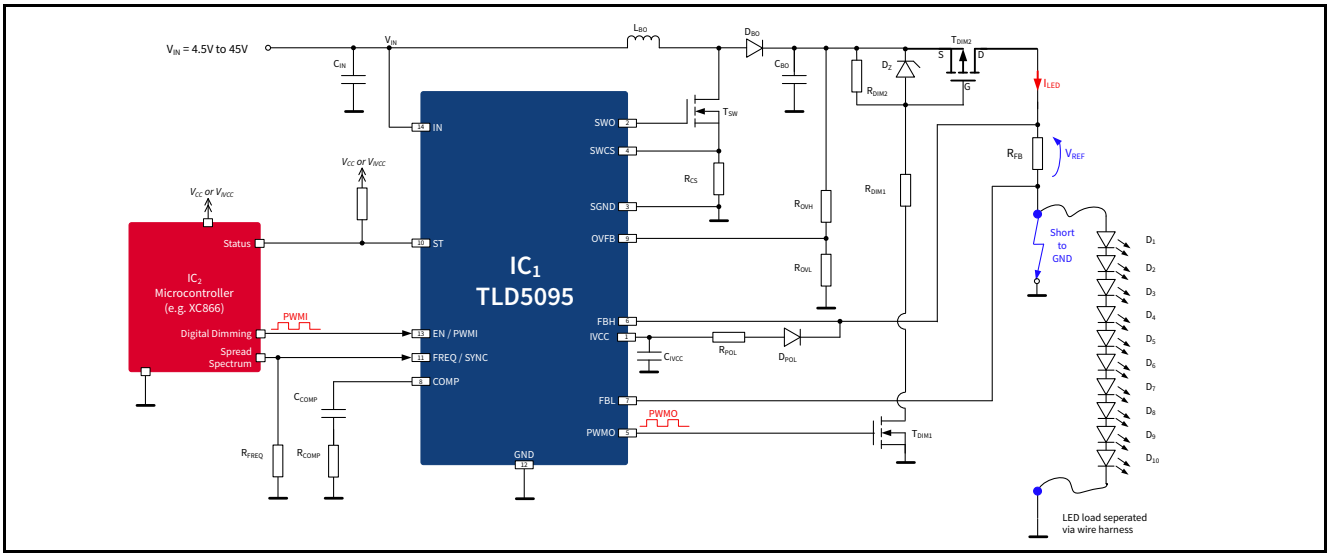


Figure 1 Simplified typical application

Type	Package	Marking
TLD5095EL	PG-SSOP-14	TLD5095

Potential applications

- Automotive exterior and interior lighting

Features

- Wide input voltage range from 4.75 V to 45 V
- Constant current or constant voltage regulation
- Drives LEDs in Boost, Buck, Buck-Boost, SEPIC and Flyback topology
- Very low shutdown current: I_Q < 10 µA
- Flexible switching frequency range, 100 kHz to 500 kHz
- Synchronization with external clock source
- Output open circuit diagnostic
- PWM dimming
- Internal soft start
- 300 mV high-side current sense to ensure highest flexibility and LED current accuracy
- Internal 5 V low drop out voltage regulator
- Wide LED current range via simple adaptation of external components
- Available in a small thermally enhanced PG-SSOP-14 package
- Output overvoltage protection
- Overtemperature shutdown
- Green product (RoHS) compliant

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

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2 Block diagram

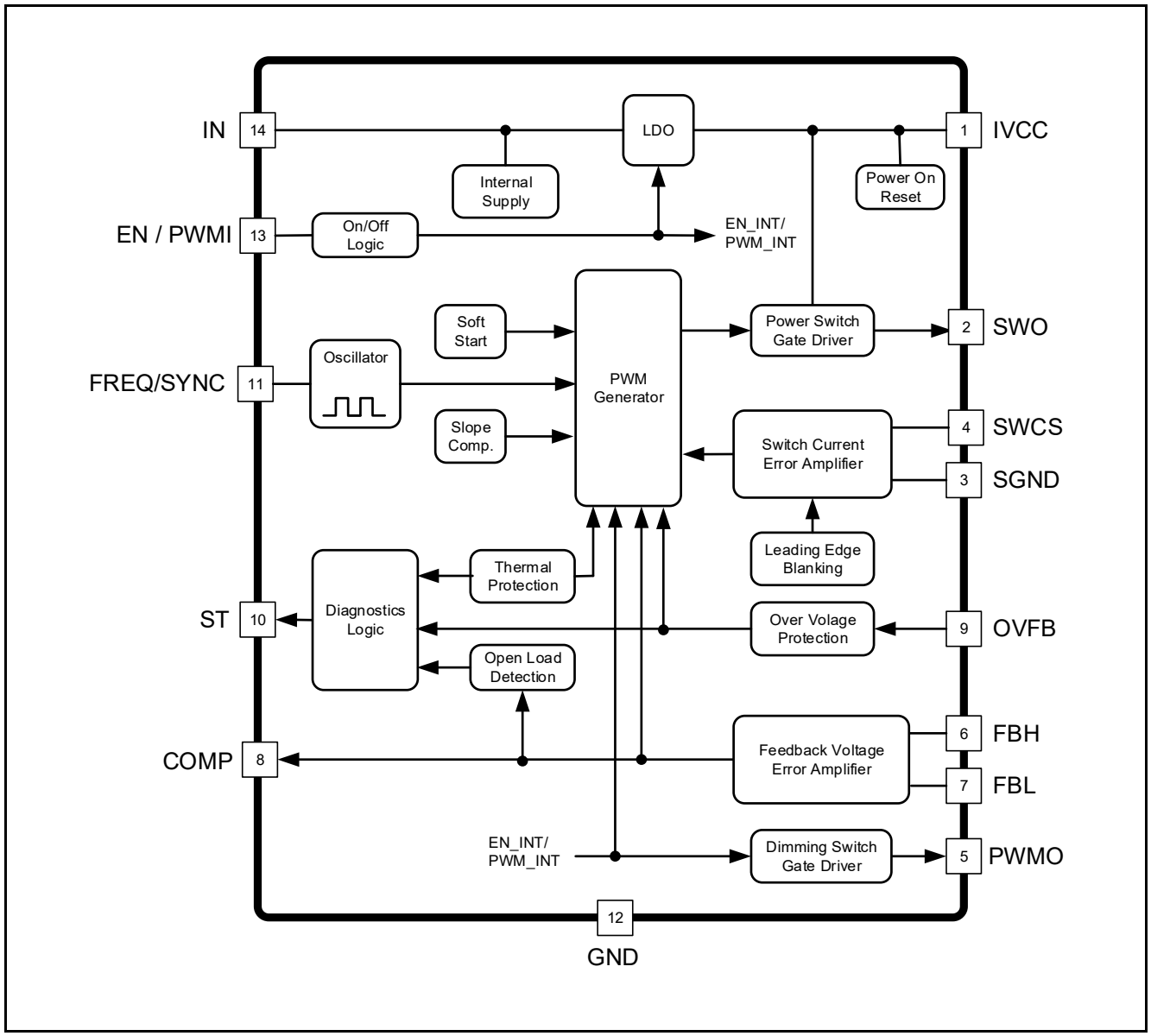


Figure 2 Block diagram TLD5095EL

3 Pin configuration

3.1 Pin assignment

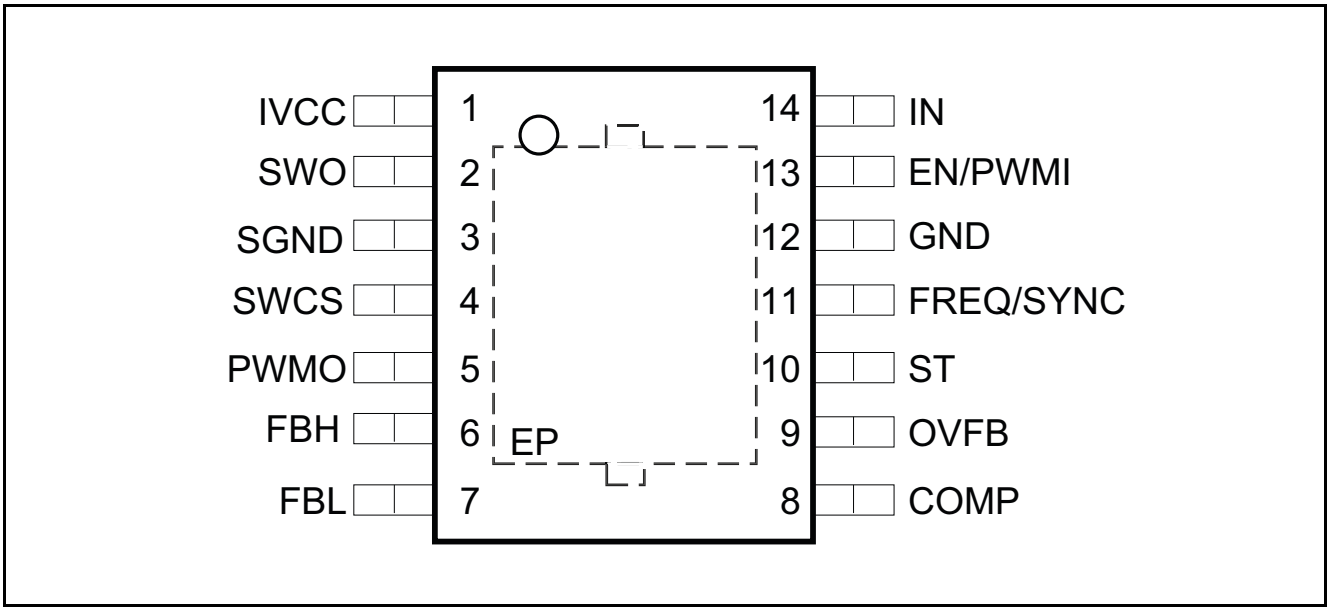


Figure 3 Pin configuration TLD5095EL

3.2 Pin definitions and functions

Table 1 Pin definition and function

#	Symbol	Direction	Function
1	IVCC	Output	**Internal LDO** Used for internal biasing and gate drive. Bypass with external capacitor. Pin must not be left open
2	SWO	Output	**Switch gate driver** Connect to gate of external switching MOSFET
3	SGND	–	**Current sense ground** Ground return for current sense switch
4	SWCS	Input	**Current sense** Detects the peak current through switch
5	PWMO	Output	**PWM dimming gate driver** Connect to gate of external MOSFET
6	FBH	Input	**Voltage feedback positive** Non inverting Input (+)
7	FBL	Input	**Voltage feedback negative** Inverting Input (-)
8	COMP	Input	**Compensation** Connect R and C network to pin for stability

Pin configuration

Table 1 Pin definition and function

#	Symbol	Direction	Function
9	OVFB	Input	**Overvoltage protection feedback** Connect to resistive voltage divider to set overvoltage threshold
10	ST	Output	**Status** Open drain diagnostic output to indicate fault condition. Connect pull up resistor to pin
11	FREQ / SYNC	Input	**Frequency select or synchronization input** Connect external resistor to GND to set frequency or apply external clock signal for synchronization within frequency capture range
12	GND	–	**Ground** Connect to system ground
13	EN / PWMI	Input	**Enable or PWM** Apply logic high signal to enable device or PWM signal for dimming LED
14	IN	Input	**Supply** Supply for internal biasing
15	EP	–	**Exposed pad** Connect to external heat spreading Cu area with electrically GND (e.g. inner GND layer of multilayer PCB with thermal vias)

4 General product characteristics

4.1 Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground (unless otherwise specified)

Table 2 Absolute maximum ratings[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage							
IN Supply input	V_{IN}	-0.3	–	45	V	–	P_4.1.1
EN / PWMI Enable or PWM input	V_{EN}	-40	–	45	V	–	P_4.1.2
FBH-FBL Feedback error amplifier differential	V_{FBH} - V_{FBL}	-5.5	–	5.5	V	Differential signal (not referred to GND)	P_4.1.3
FBH Feedback error amplifier positive input	V_{FBH}	-0.3	–	45	V	–	P_4.1.4
FBL Feedback error amplifier negative input	V_{FBL}	-0.3	–	45	V	–	P_4.1.5
OVFB Overvoltage feedback input	V_{OVP}	-0.3	–	5.5	V	–	P_4.1.6
OVFB Overvoltage feedback input	V_{OVP}	-0.3	–	6.2	V	t < 10 s	P_4.1.7
SWCS Switch current sense input	V_{SWCS}	-0.3	–	5.5	V	–	P_4.1.8
SWCS Switch current sense input	V_{SWCS}	-0.3	–	6.2	V	t < 10 s	P_4.1.9
SWO Switch gate drive output	V_{SWO}	-0.3	–	5.5	V	–	P_4.1.10
SWO Switch gate drive output	V_{SWO}	-0.3	–	6.2	V	t < 10 s	P_4.1.11
SGND Current sense switch GND	V_{SGND}	-0.3	–	0.3	V	–	P_4.1.12
COMP Compensation input	V_{COMP}	-0.3	–	5.5	V	–	P_4.1.13
COMP Compensation input	V_{COMP}	-0.3	–	6.2	V	t < 10s	P_4.1.14

Table 2 Absolute maximum ratings[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
FREQ / SYNC Frequency and synchronization input	$V_{FREQ/SYNC}$	-0.3	–	5.5	V	–	P_4.1.15
FREQ / SYNC Frequency and synchronization input	$V_{FREQ/SYNC}$	-0.3	–	6.2	V	t < 10 s	P_4.1.16
PWMO PWM dimming output	V_{PWMO}	-0.3	–	5.5	V	–	P_4.1.17
PWMO PWM dimming output	V_{PWMO}	-0.3	–	6.2	V	t < 10 s	P_4.1.18
ST Diagnostic status output	V_{ST}	-0.3	–	45	V	–	P_4.1.19
ST Diagnostic status output	I_{ST}	-5	–	5	mA	–	P_4.1.20
IVCC Internal linear voltage regulator output	V_{IVCC}	-0.3	–	5.5	V	–	P_4.1.21
IVCC Internal linear voltage regulator output	V_{IVCC}	-0.3	–	6.2	V	t < 10 s	P_4.1.22
Temperature							
Junction temperature	T_J	-40	–	150	°C	–	P_4.1.23
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.24
ESD susceptibility							
ESD resistivity to GND	$V_{ESD,HBM}$	-2	–	2	kV	HBM[2)]	P_4.1.25
ESD resistivity to GND	$V_{ESD,CDM}$	-500	–	500	V	CDM[3)]	P_4.1.26
ESD resistivity pin 1,7,8,14 (corner pins) to GND	$V_{ESD,CDM,C}$	-750	–	750	V	CDM[3)]	P_4.1.27

1) Not subject to production test, specified by design
2) ESD susceptibility, Human Body Model “HBM” according to ANSI/ESDA/JEDEC JS-001 (1.5 kW, 100 pF)
3) ESD susceptibility, Charged Device Model “CDM” ESDA STM5.3.1 or ANSI/ESD S.5.3.1

Note:

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage	V_{IN}	4.75	–	45	V	$V_{IVCC} > V_{IVCC,RTH,d}$	P_4.2.1
Feedback voltage input	V_{FBH}; V_{FBL}	4.5	–	45	V	–	P_4.2.2
Junction temperature	T_J	-40	–	150	°C	–	P_4.2.3

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table

4.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org***

Table 4 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	10	–	K/W	1)2)	P_4.3.1
Junction to ambient	R_{thJA}	–	47	–	K/W	1)3) 2s2p	P_4.3.2
Junction to ambient	R_{thJA}	–	54	–	K/W	1) 1s0p + 600 mm^2	P_4.3.3
Junction to ambient	R_{thJA}	–	64	–	K/W	1)1s0p + 300 mm^2	P_4.3.4

1) Not subject to production test, specified by design

2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins and the exposed pad are fixed to ambient temperature). T_A = 25°C dissipates 1 W

3) Specified R_{thJA} value is according to JEDEC 2s2p (JESD 51-7) + (JESD 51-5) and JEDEC 1s0p (JESD 51-3) + heatsink area at natural convection on FR4 board; the device was simulated on a 76.2 x 114.3 x 1.5 mm board. The 2s2p board has 2 outer copper layers (2 x 70 µm Cu) and 2 inner copper layers (2 x 35 µm Cu), A thermal via (diameter = 0.3 mm and 25 µm plating) array was applied under the exposed pad and connected the first outer layer (top) to the first inner layer and second outer layer (bottom) of the JEDEC PCB. T_A=25°C, IC dissipates 1 W

5 Regulator

5.1 Description

The TLD5095 regulator is suitable for Boost, Buck, Buck-Boost, SEPIC and Flyback configurations. The constant output current is especially useful for light emitting diode (LED) applications. The regulator function is implemented by a pulse width modulated (PWM) current mode controller.

The PWM current mode controller uses the peak current through the external power switch and error in the output current to determine the appropriate pulse width duty cycle (on time) for constant output current. The current mode controller provides a PWM signal to an internal gate driver which then outputs the same PWM signal to external n-channel enhancement mode metal oxide field effect transistor (MOSFET) power switch.

The current mode controller also has a built-in slope compensation to prevent sub-harmonic oscillations which is a characteristic of current mode controllers operating at high duty cycles (>50% duty).

An additional built-in feature is an integrated soft start that limits the current through the inductor and external power switch during initialization. The soft start function gradually increases the inductor and switch current over 1 ms (typical) to minimize potential overvoltage at the output.

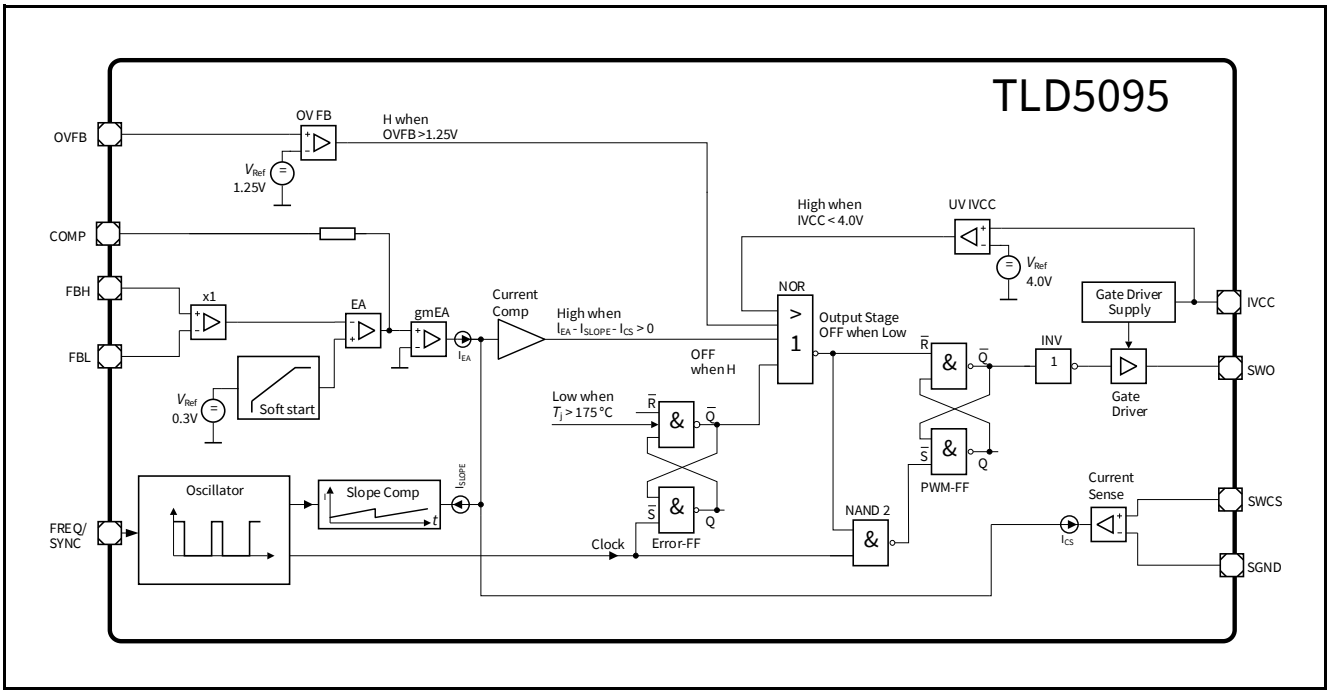


Figure 4 Block diagram boost regulator

5.2 Electrical characteristics

V_{IN} = 6 V to 40 V, 4.5 V ≤ V_{FBH} ≤ 40 V, 4.5 V ≤ V_{FBL} ≤ 40 V, -5.5 V ≤ V_{FBH} - V_{FBL} ≤ 5.5 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 5 Electrical characteristics: Boost regulator

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Regulator							
Feedback reference voltage	V_{REF}	0.28	0.30	0.32	V	V_{IN} = 19 V; V_{REF} = V_{FBH} - V_{FBL}	P_5.2.1
Voltage line regulation	$\Delta V_{REF}/\Delta V_{IN}$	–	–	0.15	%/V	V_{IN} = 6 to 19 V; V_{BO}= 30 V; I_{BO} = 500 mA **Figure 26**	P_5.2.2
Voltage load regulation	$(\Delta V_{REF}/V_{REF})$ $/\Delta I_{BO}$	–	–	5	%/A	V_{IN} = 6 V; V_{BO}= 30 V; I_{BO} = 100 to 500 mA **Figure 26**	P_5.2.3
Switch peak overcurrent threshold	V_{SWCS}	130	150	170	mV	V_{IN} = 6 V V_{FBH} = V_{FBL} = 5 V V_{COMP} = 3.5 V	P_5.2.4
Maximum duty cycle	$D_{MAX,fixed}$	90	93	95	%	Fixed frequency mode	P_5.2.5
Maximum duty cycle	$D_{MAX,sync}$	88	–	–	%	Synchronization mode	P_5.2.6
Soft start ramp	t_{SS}	350	1000	1500	µs	V_{FB} rising from 5% to 95% of V_{FB}, typ.	P_5.2.7
Feedback input current	I_{FBx}	-10	-50	-100	µA	V_{FBH} - V_{FBL} = 0.3 V	P_5.2.8
Switch current sense input current	I_{SWCS}	10	50	100	µA	V_{SWCS} = 150 mV	P_5.2.9
Input undervoltage shutdown	$V_{IN,off}$	3.75	–	–	V	V_{IN} decreasing	P_5.2.10
Input voltage startup	$V_{IN,on}$	–	–	4.75	V	V_{IN} increasing	P_5.2.11
Gate driver for external switch							
Gate driver peak sourcing current	$I_{SWO,SRC}$	–	380	–	mA	[1] V_{SWO} = 3.5 V Current flows out of pin	P_5.2.12
Gate driver peak sinking current	$I_{SWO,SNK}$	–	550	–	mA	[1] V_{SWO} = 1.5 V	P_5.2.13
Gate driver output rise time	$t_{R,SWO}$	–	30	60	ns	$C_{L,SWO}$ = 3.3 nF; V_{SWO} = 1 V to 4 V	P_5.2.14

Table 5 Electrical characteristics: Boost regulator

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Gate driver output fall time	$t_{F,SWO}$	–	20	40	ns	$C_{L,SWO}$ = 3.3 nF; V_{SWO} = 1 V to 4 V	P_5.2.15
Gate driver output voltage	V_{SWO}	4.5	–	5.5	V	1) $C_{L,SWO}$ = 3.3 nF	P_5.2.16

1) Not subject to production test, specified by design

6 Oscillator and synchronization

6.1 Description

R_{FREQ} vs. switching frequency

The internal oscillator is used to determine the switching frequency of the multitopology regulator. The switching frequency can be selected from 100 kHz to 500 kHz with an external resistor to GND. To set the switching frequency with an external resistor the following formula can be applied.

(6.1)

$$R_{FREQ} = \frac{1}{(141 \cdot 10^{-12}\left[\frac{s}{\Omega}\right]) \cdot \left(f_{FREQ}\left[\frac{1}{s}\right]\right)} - (3.5 \cdot 10^{3}\,[\Omega])[\Omega]$$

In addition, the oscillator is capable of changing from the frequency set by the external resistor to a synchronized frequency from an external clock source. If an external clock source is provided on the pin FREQ/SYNC, then the internal oscillator synchronizes to this external clock frequency and the multitopology regulator switches at the synchronized frequency. The synchronization frequency capture range is 250 kHz to 500 kHz.

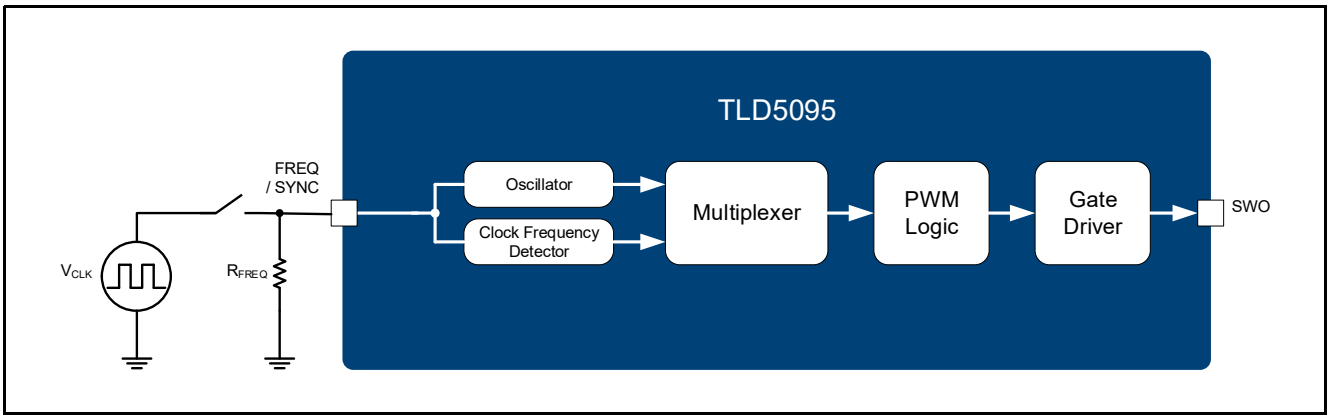


Figure 5 Oscillator and synchronization block diagram and simplified application circuit

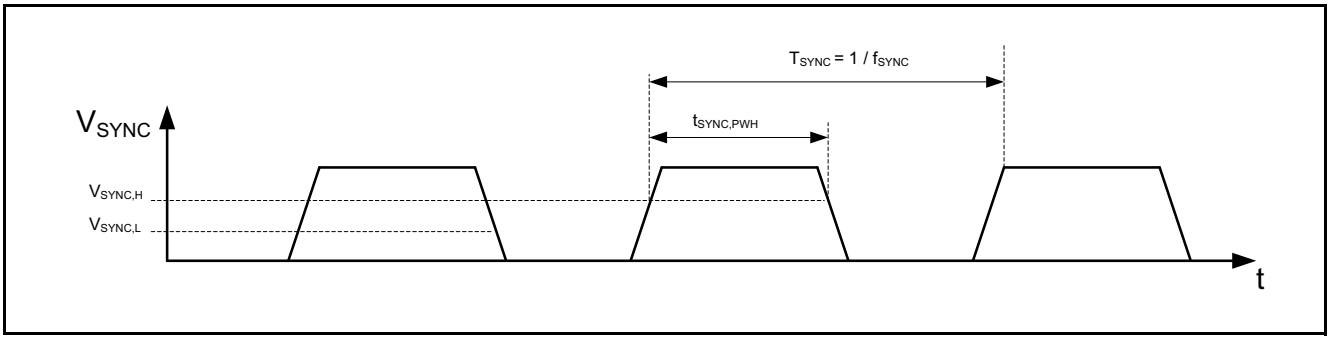


Figure 6 Synchronization timing diagram

6.2 Electrical characteristics oscillator

V_{IN} = 6 V to 40 V, 4.5 V ≤ V_{FBH} ≤ 40 V, 4.5 V ≤ V_{FBL} ≤ 40 V, -5.5 V ≤ V_{FBH} - V_{FBL} ≤ 5.5 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 6 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Oscillator							
Oscillator frequency	f_{FREQ}	250	300	350	kHz	R_{FREQ} = 20 kΩ	P_6.1.1
Oscillator frequency adjustment range	f_{FREQ}	100	–	500	kHz	17% internal tolerance + external resistor tolerance	P_6.1.2
FREQ / SYNC supply current	I_{FREQ}	–	–	-700	µA	V_{FREQ} = 0 V	P_6.1.3
Frequency voltage	V_{FREQ}	1.16	1.24	1.32	V	f_{FREQ} = 100 kHz	P_6.1.4
Synchronization							
Synchronization frequency capture range	f_{SYNC}	250	–	500	kHz	–	P_6.1.5
Synchronization signal high logic level valid	$V_{SYNC,H}$	3.0	–	–	V	1)	P_6.1.6
Synchronization signal low logic level valid	$V_{SYNC,L}$	–	–	0.8	V	1)	P_6.1.7
Synchronization signal logic high pulse width	$t_{SYNC,PWH}$	200	–	–	ns	1)	P_6.1.8

1) Synchronization of external PWM ON signal to falling edge

6.3 Typical performance characteristics of oscillator

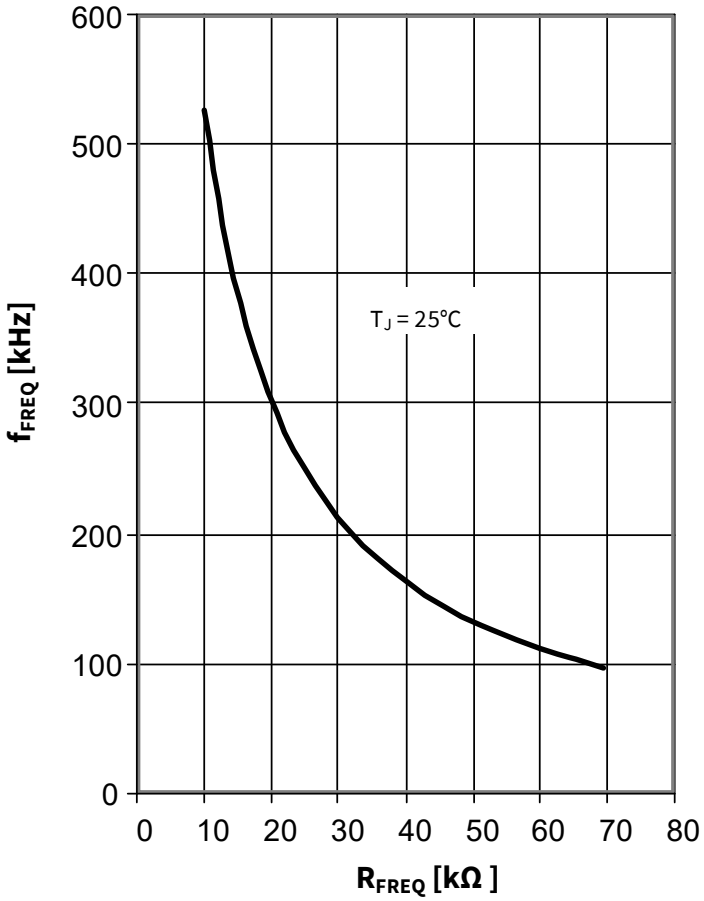


Figure 7 Switching frequency f_{SW} versus frequency select resistor to GND R_{FREQ}

7 Enable and dimming function

7.1 Description

The enable function powers the device on or off. A valid logic low signal on enable pin EN/PWMI powers off the device and current consumption is less than 10 µA. A valid logic high enable signal on enable pin EN/PWMI powers on the device. The enable function features an integrated pull down resistor which ensures that the IC is shut down and the power switch is off in case the enable pin EN is left open.

In addition to the enable function described above, the EN/PWMI pin detects a pulse width modulated (PWM) input signal that is fed through to an internal gate driver. The internal gate driver outputs the same PWM signal on the PWMO pin to an external n-channel enhancement mode MOSFET for PWM dimming an LED load. PWM dimming an LED is a commonly practiced dimming method to prevent color shift in an LED light source. Moreover the PWM output function may also be used for to drive other types of loads besides LED.

The enable and PWM input function share the same pin. Therefore a valid logic low signal at the EN/PWMI pin needs to differentiate between an enable power off signal or an PWM low signal. The device differentiates between an enable off command and PWM dimming signal by requiring the signal at the EN/PWMI pin to stay low for a minimum of 8 ms.

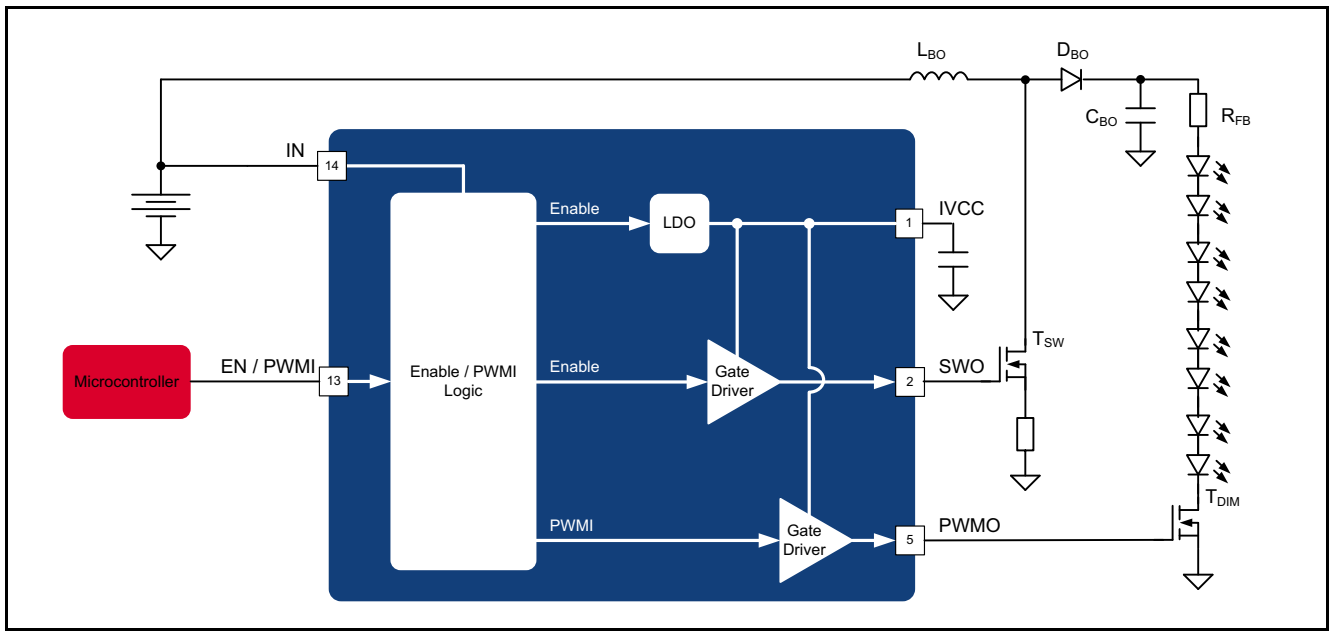


Figure 8 Block diagram and simplified application circuit enable and LED dimming

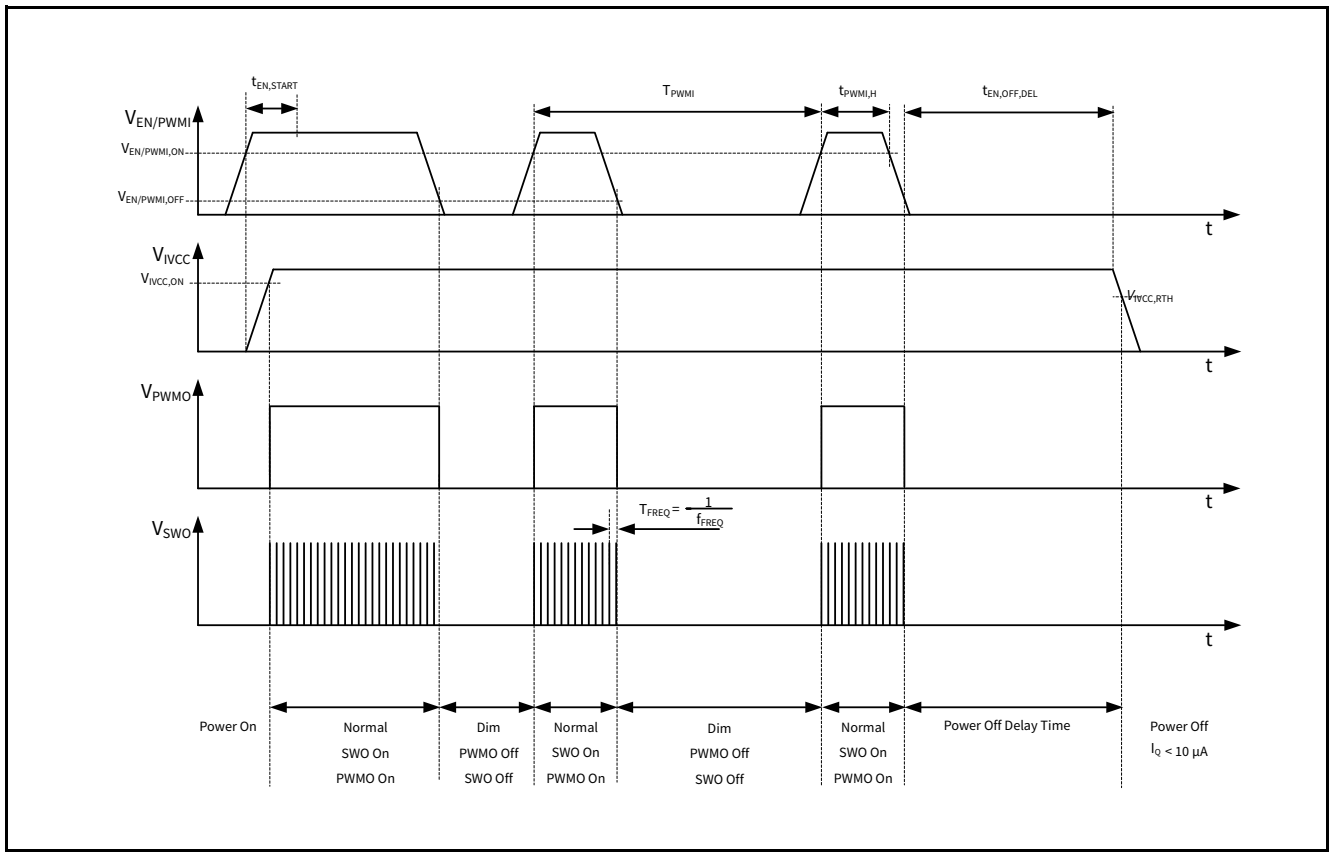


Figure 9 Timing diagram enable and LED dimming

7.2 Electrical characteristics

V_{IN} = 6 V to 40 V, 4.5 V ≤ V_{FBH} ≤ 40 V, -5.5 V ≤ V_{FBH} - V_{FBL} ≤ 5.5 V, T_J = -40°C to +150°C, all voltages with respect to ground positive current flowing into pin; (unless otherwise specified)

Table 7 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Enable / PWM Input							
Enable/PWMI turn on threshold	$V_{EN/PWMI,ON}$	3.0	–	–	V	–	P_7.1.1
Enable/PWMI turn off threshold	$V_{EN/PWMI,OFF}$	–	–	0.8	V	–	P_7.1.2
Enable/PWMI hysteresis	$V_{EN/PWMI,HYS}$	50	200	400	mV	–	P_7.1.3
Enable/PWMI high input current	$I_{EN/PWMI,H}$	–	–	30	µA	$V_{EN/PWMI}$ = 16.0 V	P_7.1.4
Enable/PWMI low input current	$I_{EN/PWMI,L}$	–	0.1	1	µA	$V_{EN/PWMI}$ = 0.5 V	P_7.1.5
Enable turn off delay time	$t_{EN,OFF,DEL}$	8	10	12	ms	–	P_7.1.6
PWMI min duty time	$t_{PWMI,H}$	4	–	–	µs	–	P_7.1.7

Enable and dimming function

Table 7 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Enable startup time	$t_{EN,START}$	100	–	–	µs	–	P_7.1.8
Gate driver for dimming switch							
PWMO gate driver peak sourcing current	$I_{PWMO,SRC}$	–	230	–	mA	V_{PWMO} = 3.5 V Current flows out of pin	P_7.1.9
PWMO gate driver peak sinking current	$I_{PWMO,SNK}$	–	370	–	mA	V_{PWMO} = 1.5 V	P_7.1.10
PWMO gate driver output rise time	$t_{R,PWMO}$	–	50	100	ns	$C_{L,PWMO}$ = 3.3 nF; V_{PWMO} = 1 V to 4 V	P_7.1.11
PWMO gate driver output fall time	$t_{F,PWMO}$	–	30	60	ns	$C_{L,PWMO}$ = 3.3 nF; V_{PWMO} = 1 V to 4 V	P_7.1.12
PWMO gate driver output voltage	V_{PWMO}	4.5	–	5.5	V	[1] $C_{L,PWMO}$ = 3.3 nF	P_7.1.13
Current consumption							
Current consumption, shutdown mode	I_{Q_OFF}	–	–	10	µA	$V_{EN/PWMI}$ = 0.8 V; $T_J \leq$ 105°C; V_{IN} = 16 V	P_7.1.14
Current consumption, active mode	I_{Q_ON}	–	–	7	mA	[2] $V_{EN/PWMI} \geq$ 4.75 V; I_{BO} = 0 mA; V_{IN} = 16 V V_{SWO} = 0% Duty	P_7.1.15

1) Not subject to production test, specified by design

2) Dependency on switching frequency and gate charge of external switches

8 Linear Regulator

8.1 Description

The internal linear voltage regulator supplies the internal gate drivers with a typical voltage of 5 V and current up to $I_{LIM,min}$ (P_8.1.2). An external output capacitor with ESR lower than $R_{IVCC,ESR}$ (P_8.1.5) is required on pin IVCC for stability and buffering transient load currents. During normal operation the external MOSFET switches will draw transient currents from the linear regulator and its output capacitor. Proper sizing of the output capacitor must be considered to supply sufficient peak current to the gate of the external MOSFET switches.

Integrated undervoltage protection for the external switching MOSFET

An integrated undervoltage reset threshold circuit monitors the linear regulator output voltage (V_{IVCC}) and resets the device in case the output voltage falls below the IVCC undervoltage reset switch OFF threshold ($V_{IVCC,RTH,d}$). The undervoltage reset threshold for the IVCC pin helps to protect the external switches from excessive power dissipation by ensuring the gate drive voltage is sufficient to enhance the gate of an external logic level n-channel MOSFET.

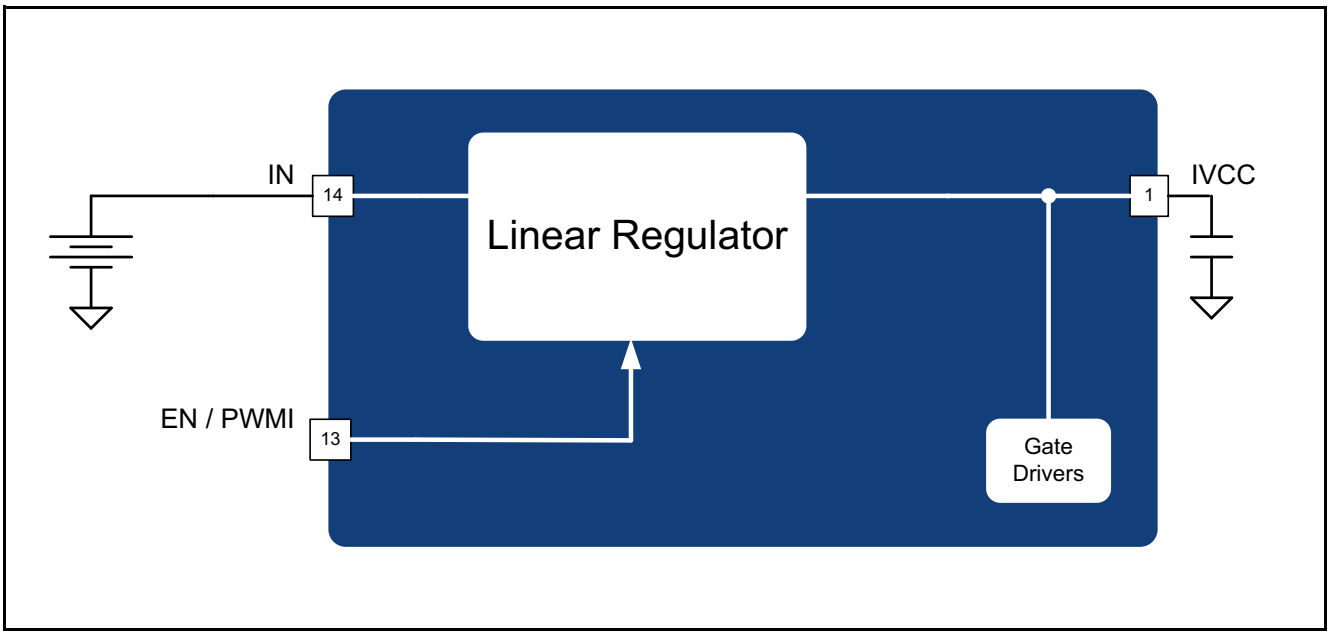


Figure 10 Voltage regulator block diagram and simplified application circuit

8.2 Electrical characteristics

V_{IN} = 6 V to 40 V, 4.5V ≤ V_{FBH} ≤ 40V, 4.5V ≤ V_{FBL} ≤ 40V, -5.5 V ≤ V_{FBH} - V_{FBL} ≤ 5.5 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 8 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage	V_{IVCC}	4.6	5	5.4	V	6 V ≤ V_{IN} ≤ 45 V 0.1 mA ≤ I_{IVCC} ≤ 35 mA	P_8.1.1
Output current limitation	I_{LIM}	51		90	mA	V_{IN} = 13.5 V V_{IVCC} = 4.5V Current flows out of pin	P_8.1.2
Drop out voltage	V_{DR}	–		1.4	V	1) I_{IVCC} = 50 mA	P_8.1.3
Output capacitor	C_{IVCC}	0.47		–	µF	2)3)	P_8.1.4
Output capacitor ESR	$R_{IVCC,ESR}$			0.5	Ω	3) f = 10 kHz	P_8.1.5
Undervoltage reset headroom	$V_{IVCC,HDRM}$	100	–	–	mV	V_{IVCC} decreasing V_{IVCC} - $V_{IVCC,RTH,d}$	P_8.1.6
Undervoltage reset threshold	$V_{IVCC,RTH,d}$	4.0	–	–	V	V_{IVCC} decreasing	P_8.1.7
Undervoltage reset threshold	$V_{IVCC,RTH,i}$	–	–	4.5	V	V_{IVCC} increasing	P_8.1.8

1) Measured when the output voltage VCC has dropped 100 mV from its nominal value
2) Minimum value given is needed for regulator stability; application might need higher capacitance than the minimum
3) Not subject to production test, specified by design

9 Protection and diagnostic functions

9.1 Description

The TLD5095EL has integrated circuits to diagnose and protect against output overvoltage, open load, open feedback and overtemperature faults. In case any of the four fault conditions occur the Status output ST will output an active logic low signal to communicate that a fault has occurred. During an overvoltage or open load condition the gate driver outputs SWO and PWMO will turn off. **Figure 12** illustrates the various open load and open feedback conditions. In the event of an overtemperature condition (**Figure 15**) the integrated thermal shutdown function turns off the gate drivers and internal linear voltage regulator. The typical junction shutdown temperature is 175°C. After cooling down the IC will automatically restart operation. Thermal shutdown is an integrated protection function designed to prevent immediate IC destruction and is not intended for continuous use in normal operation.

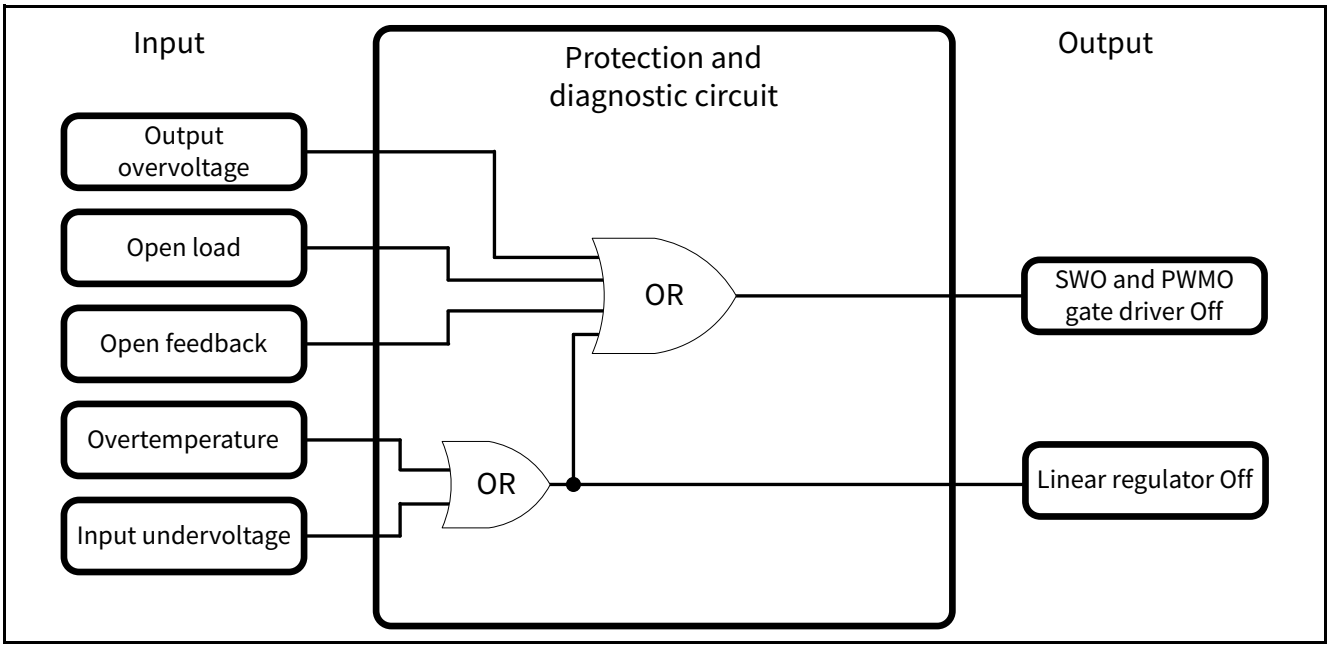
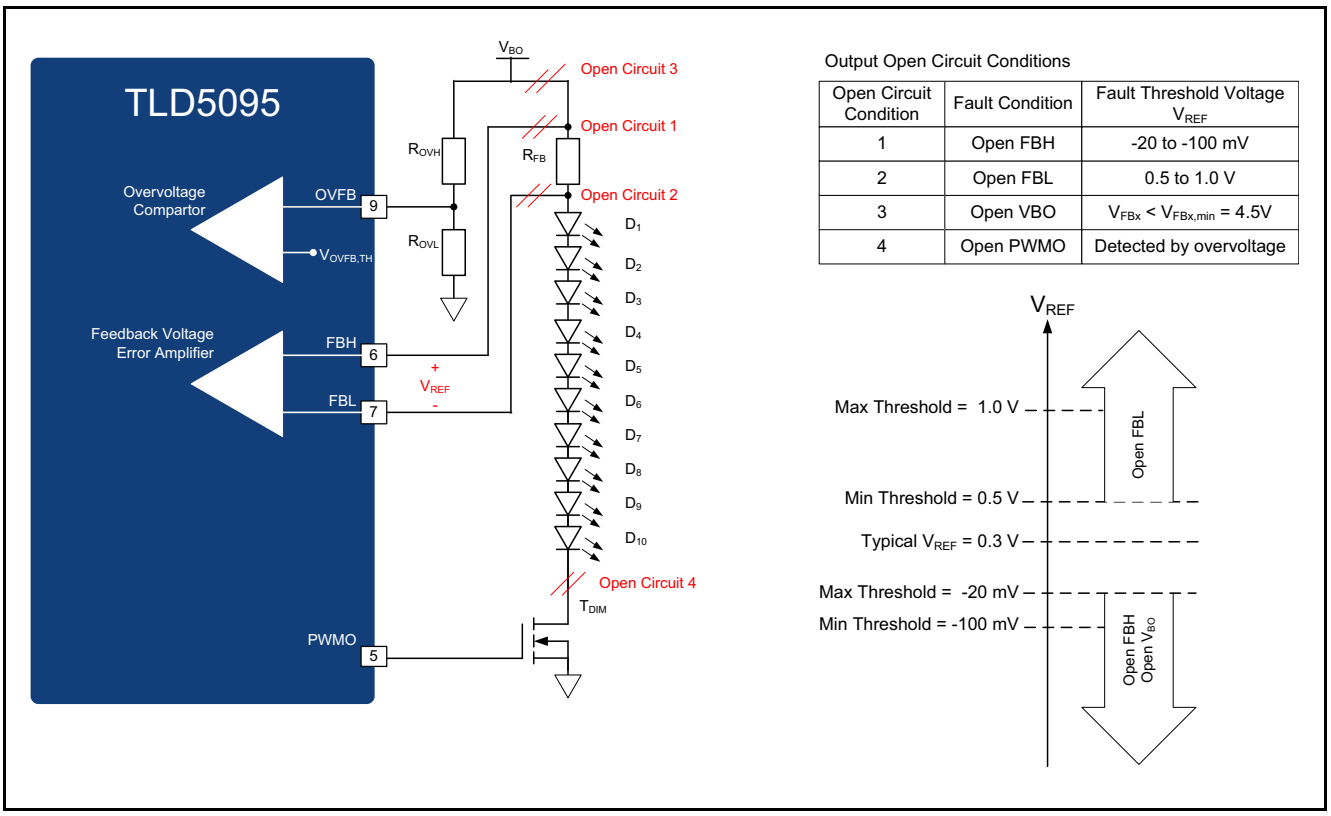


Figure 11 Protection and diagnostic function block diagram

Table 9 Status output truth table

Input		Output			
Condition	**Level**[1)]	**ST**	**SWO**	**PWMO**	**IVCC**
Overvoltage	False	H	Sw[1)]	H or Sw[1)]	Active
	True	L	L	L	Active
Open load	False	H	Sw[1)]	H or Sw[1)]	Active
	True	L	L	L	Active
Open feedback	False	H	Sw[1)]	H or Sw[1)]	Active
	True	L	L	L	Active
Overtemperature	False	H	Sw[1)]	H or Sw[1)]	Active
	True	L	L	L	Shutdown

1) Sw = Switching; False = Condition does NOT exist; True = Condition does exist



Output Open Circuit Conditions

Open Circuit Condition	Fault Condition	Fault Threshold Voltage V_{REF}
1	Open FBH	-20 to -100 mV
2	Open FBL	0.5 to 1.0 V
3	Open VBO	$V_{FBx} < V_{FBx,min}$ = 4.5V
4	Open PWMO	Detected by overvoltage

Figure 12 Open load and open feedback conditions

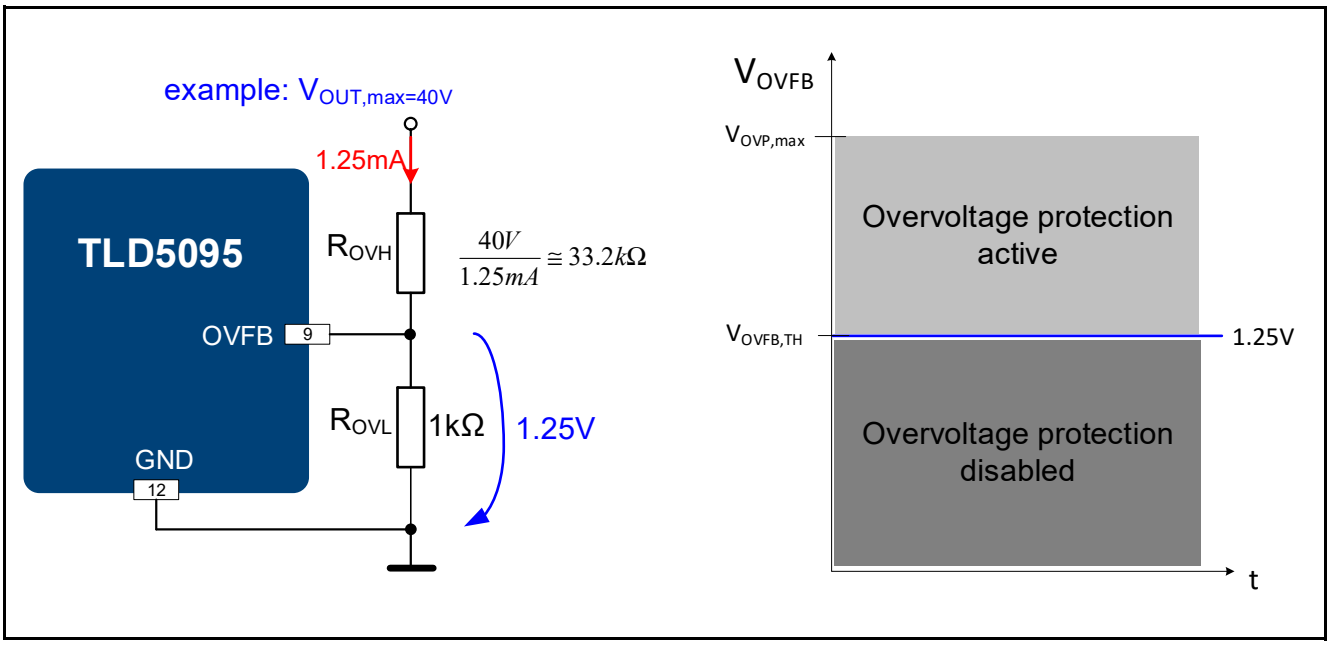


Figure 13 Overvoltage protection description

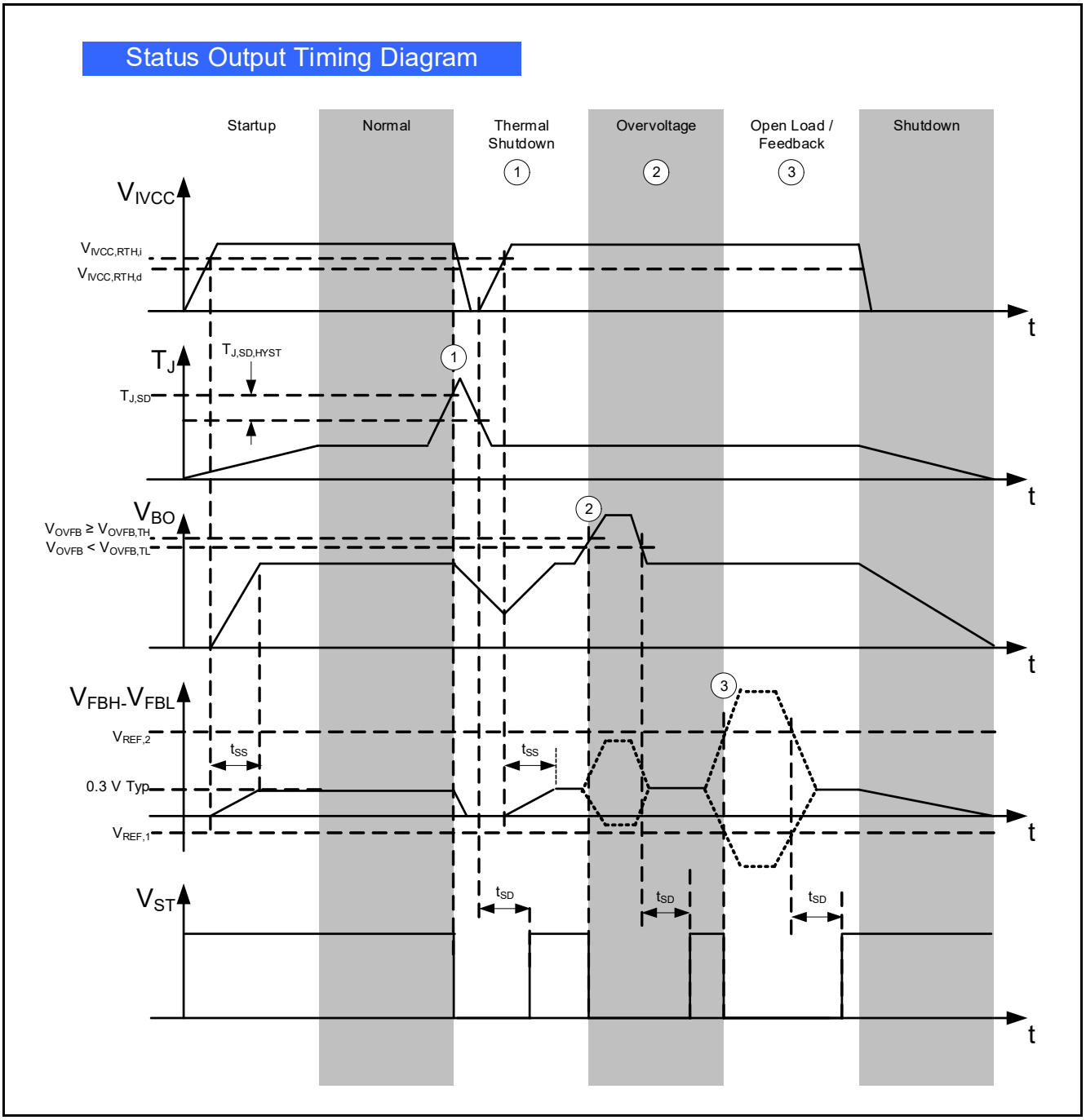


Figure 14 Status output timing diagram

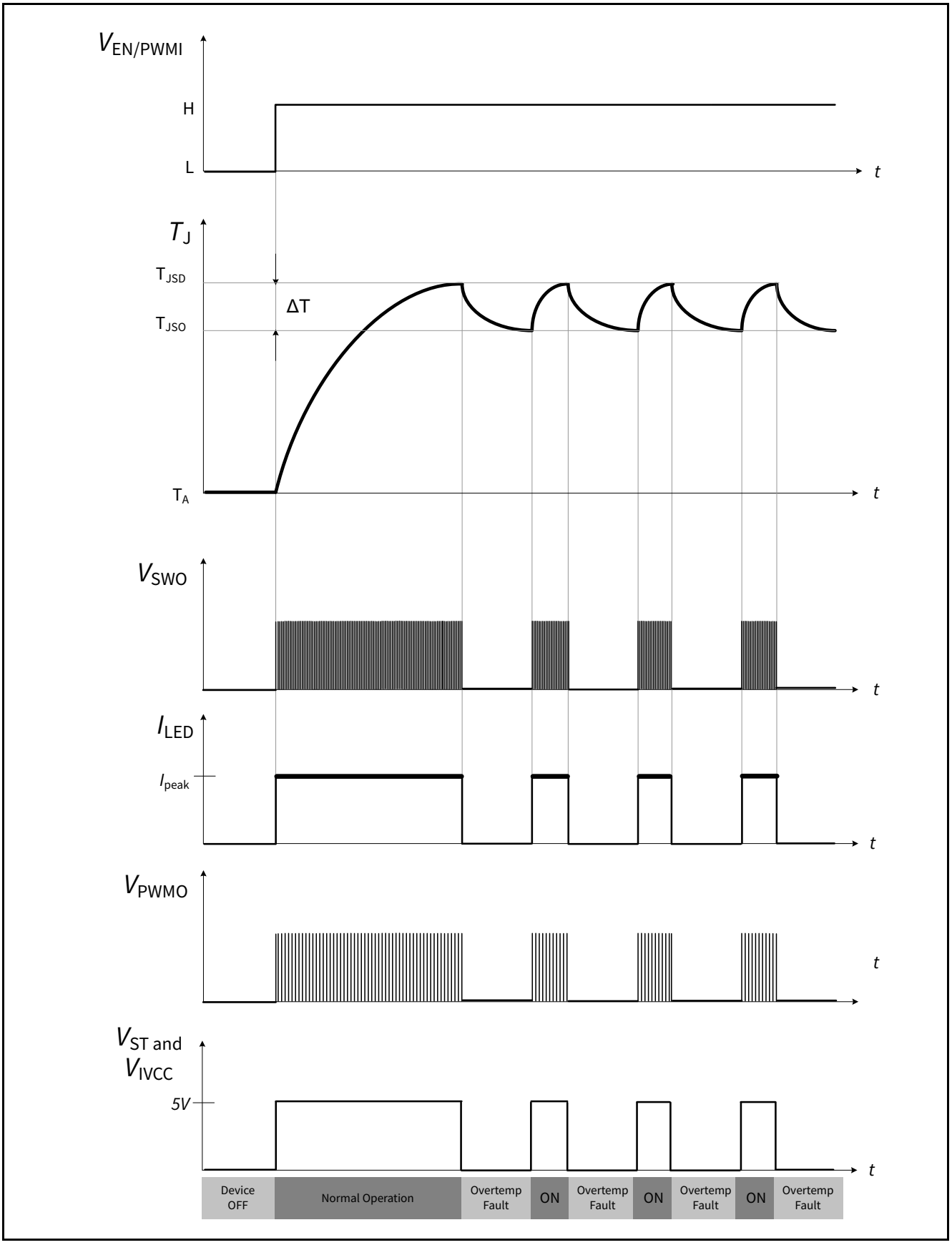


Figure 15 Device overtemperature protection behavior

9.2 Electrical Characteristics

V_{IN} = 6 V to 40 V, 4.5 V ≤ V_{FBH} ≤ 40 V, 4.5 V ≤ V_{FBL} ≤ 40 V, -5.5 V ≤ V_{FBH} - V_{FBL} ≤ 5.5 V, T_J = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin; (unless otherwise specified)

Table 10 Electrical Characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Status output							
Status output voltage low	$V_{ST,LOW}$	–	–	0.4	V	I_{ST} = 1 mA	P_9.2.1
Status sink current limit	$I_{ST,MAX}$	2	–	–	mA	V_{ST} = 1 V	P_9.2.2
Status output current	$I_{ST,HIGH}$	–	–	1	µA	V_{ST} = 5 V	P_9.2.3
Status delay time	t_{SD}	8	10	12	ms	–	P_9.2.4
Temperature protection							
Overtemperature shutdown	$T_{J,SD}$	160	175	190	°C	1)	P_9.2.5
Overtemperature shutdown hystereses	$T_{J,SD,HYST}$	–	15	–	°C	1)	P_9.2.6
Overvoltage protection							
Output overvoltage feedback threshold increasing	$V_{OVFB,TH}$	1.21	1.25	1.29	V	–	P_9.2.7
Output overvoltage feedback hysteresis	$V_{OVFB,HYS}$	50	–	150	mV	Output voltage decreasing	P_9.2.8
Overvoltage reaction time	t_{OVPRR}	2	–	10	µs	Output voltage decreasing	P_9.2.9
Overvoltage feedback input current	I_{OVFB}	-1	0.1	1	µA	V_{OVFB} = 1.25 V	P_9.2.10
Open load and open feedback diagnostics							
Open load/feedback threshold	$V_{REF,1,3}$	-100	–	-20	mV	V_{REF} = V_{FBH} - V_{FBL} Open circuit 1 or 3 (see **Figure 12**)	P_9.2.11
Open feedback threshold	$V_{REF,2}$	0.5	–	1	V	V_{REF} = V_{FBH} - V_{FBL} Open circuit 2 (see **Figure 12**)	P_9.2.12

1) Not subject to production test, specified by design

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

10 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device

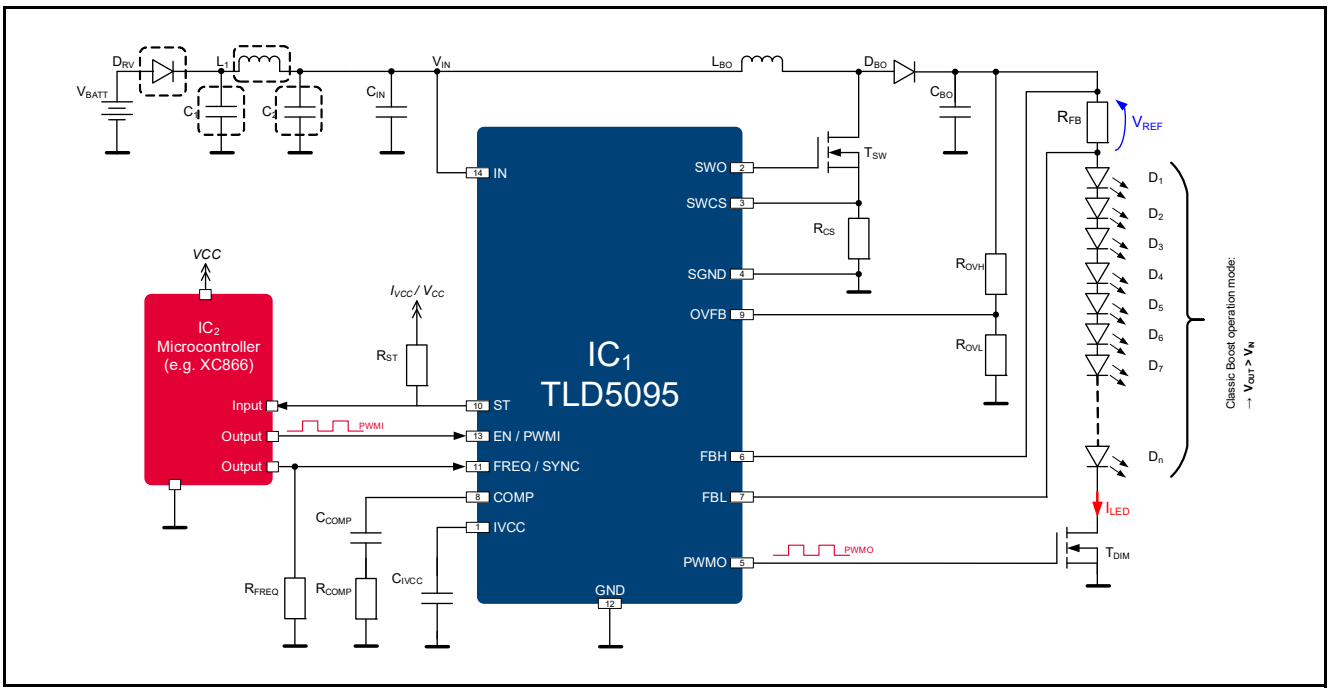


Figure 16 Boost to Ground application circuit - B2G (Boost configuration)

Reference Designator	Value	Manufacturer	Part Number	Type	Quantity
D_{1-10}	White	Osram	LUW H9GP	LED	10
D_{BO}	Schottky, 3 A, 100 V_R	Vishay	SS3H10	Diode	1
C_{IN}, C_{BO}	100 uF, 50V	Panasonic	EEEFK1H101GP	Capacitor	2
C_{COMP}	10 nF	EPCOS	X7R	Capacitor	1
C_{IVCC}	1uF , 6.3V	EPCOS	MLCC CCNPZC105KBW X7R	Capacitor	1
IC_1	--	Infineon	TLD5095	IC	1
IC_2	--	Infineon	XC866	IC	1
L_{BO}	100 uH	Coilcraft	MSS1278T-104ML	Inductor	1
R_{COMP}	10 kΩ, 1%	Panasonic	ERJ3EKF1002V	Resistor	1
R_{FB}	820 mΩ, 1%	Panasonic	ERJ14BQFR82U	Resistor	1
R_{FREQ}, R_{ST}	20 kΩ, 1%	Panasonic	ERJ3EKF2002V	Resistor	2
R_{OVH}	33.2 kΩ, 1%	Panasonic	ERJ3EKF3322V	Resistor	1
R_{OVL}	1 kΩ, 1%	Panasonic	ERJ3EKF1001V	Resistor	1
R_{CS}	50 mΩ, 1%	Panasonic	ERJB1CFR05U	Resistor	1
T_{DIM}, T_{SW}	Dual N-ch enh. (60V, 20A)	Infineon	IPG20N06S4L-26	Transistor	1
	alternativ: 100V N-ch, 35A	Infineon	IPG20N10S4L-22	Transistor	2
	alternativ: 60V N-ch, 2.6A	Infineon	BSP318S	Transistor	2

Figure 17 Bill of Materials for B2G application circuit

Application information

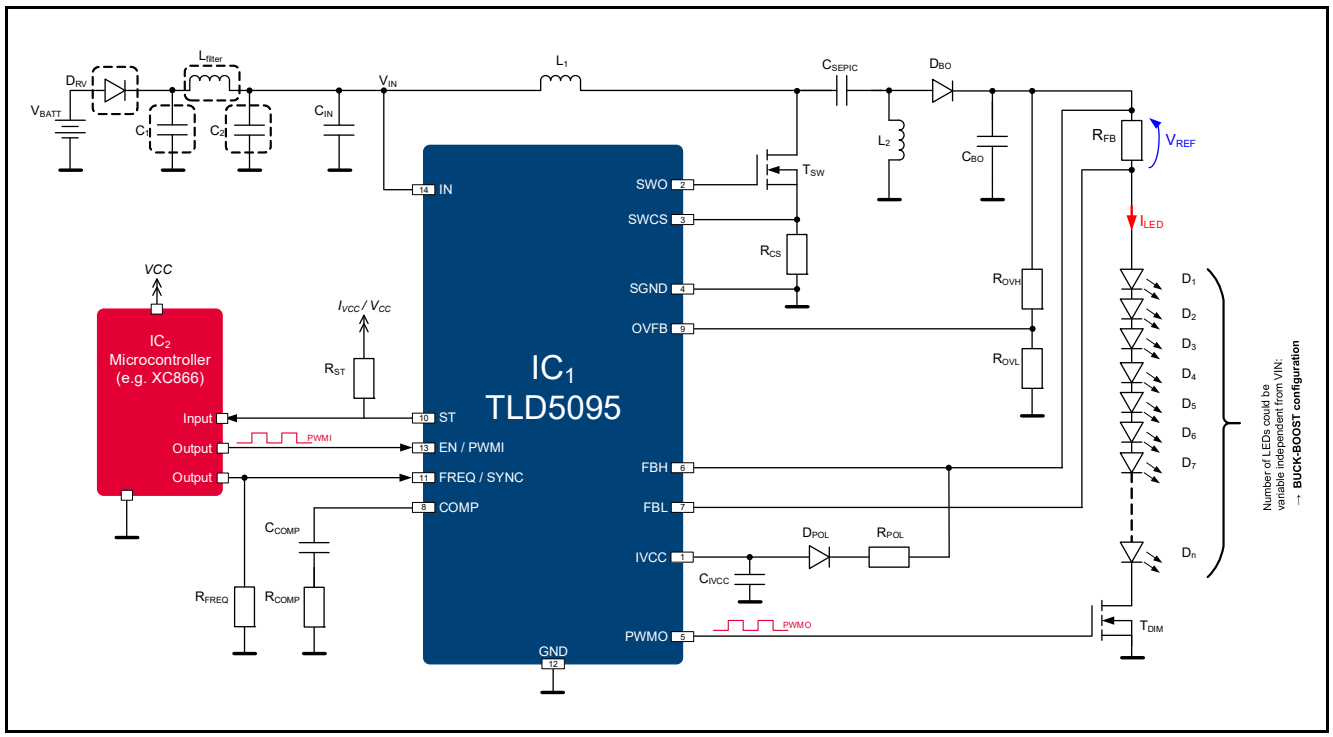


Figure 18 SEPIC application circuit (Buck - Boost configuration)

Reference Designator	Value	Manufacturer	Part Number	Type	Quantity
$D_{1 - n}$	White	Osram	LUW H9GP	LED	variable
D_{BO}	Schottky, 3 A, 100 V_R	Vishay	SS3H10	Diode	1
D_{POL}	80V Diode	Infineon	BAS1603W	Diode	1
C_{SEPIC}	3.3 uF, 20V	EPCOS	X7R, Low ESR	Capacitor	1
C_{IN}, C_{BO}	100 uF, 50V	Panasonic	EEEFK1H101GP	Capacitor	2
C_{COMP}	10 nF	EPCOS	X7R	Capacitor	1
C_{IVCC}	1uF , 6.3V	EPCOS	X7R	Capacitor	1
IC_1	--	Infineon	TLD5095	IC	1
IC_2	--	Infineon	XC866	IC	1
L_1 , L_2	47 uH	Coilcraft	MSS1278T-473ML	Inductor	2
	alternativ: 22uH coupled inductor	Coilcraft	MSD1278-223MLD	Inductor	1
R_{COMP}, R_{POL}	10 kΩ, 1%	Panasonic	ERJ3EKF1002V	Resistor	2
R_{FB}	820 mΩ, 1%	Panasonic	ERJ14BQFR82U	Resistor	1
R_{FREQ}, R_{ST}	20 kΩ, 1%	Panasonic	ERJ3EKF2002V	Resistor	2
R_{OVH}	33.2 kΩ, 1%	Panasonic	ERJ3EKF3322V	Resistor	1
R_{OVL}	1 kΩ, 1%	Panasonic	ERJ3EKF1001V	Resistor	1
R_{CS}	50 mΩ, 1%	Panasonic	ERJB1CFR05U	Resistor	1
T_{DIM}, T_{SW}	Dual N-ch enh. (60V, 20A)	Infineon	IPG20N06S4L-26	Transistor	1
	alternativ: 100V N-ch, 35A	Infineon	IPD35N10S3L-26	Transistor	2
	alternativ: 60V N-ch, 2.6A	Infineon	BSP318S	Transistor	2

Figure 19 Bill of Materials for SEPIC application circuit

Application information

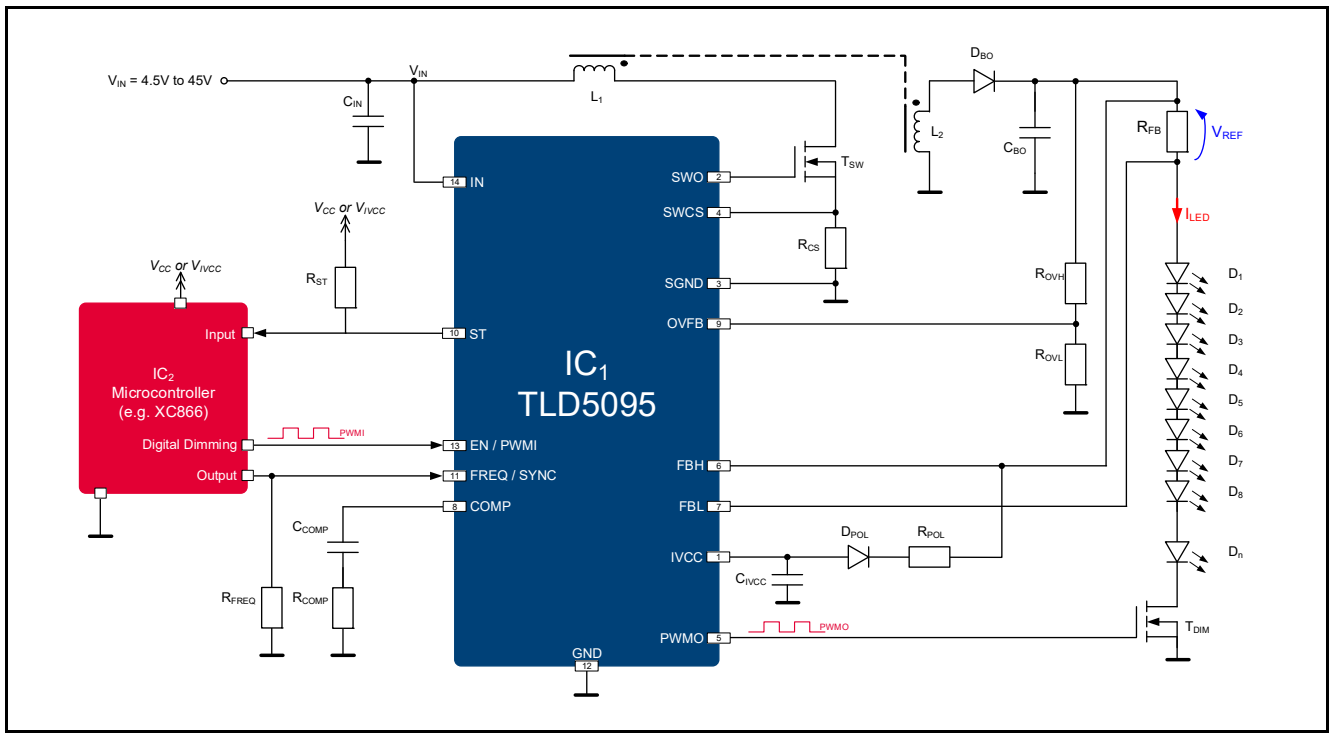


Figure 20 Flyback application circuit (Buck - Boost configuration)

Reference Designator	Value	Manufacturer	Part Number	Type	Quantity
D_{1-n}	White	Osram	LUW H9GP	LED	variable
D_{BO}	Schottky, 3 A, 100 V_R	Vishay	SS3H10	Diode	1
C_{BO}	3.3 uF, 50V (100V)	EPCOS	X7R, Low ESR	Capacitor	1
C_{IN}	100 uF, 50V	Panasonic	EEEFK1H101GP	Capacitor	1
C_{COMP}	47 nF	EPCOS	X7R	Capacitor	1
C_{IVCC}	1 uF , 6.3V	EPCOS	X7R	Capacitor	1
IC_1	--	Infineon	TLD5095	IC	1
IC_2	--	Infineon	XC866	IC	1
L_1 , L_2	1 µH / 9 uH	EPCOS	Transformer EHP 16	Inductor	1
R_{COMP}, R_{POL}	10 kΩ, 1%	Panasonic	ERJ3EKF1002V	Resistor	2
D_{POL}	80 V Diode	Infineon	BAS1603W	Diode	1
R_{FB}	820 mΩ, 1%	Isabellenhütte	SMS – Power Resistor	Resistor	1
R_{FREQ}, R_{ST}	10 kΩ, 1%	Panasonic	ERJ3EKF1002V	Resistor	2
R_{OVH}	56.2 kΩ, 1%	Panasonic	ERJ3EKF5622V	Resistor	1
R_{OVL}	1.24 kΩ, 1%	Panasonic	ERJ3EKF1241V	Resistor	1
R_{CS}	5 mΩ, 1%	Isabellenhütte	SMS - Power Resistor	Resistor	1
T_{DIM}, T_{SW}	Dual N-ch enh. (60V, 20A)	Infineon	IPG20N06S4L-26	Transistor	1
	alternativ: 100V N-ch, 35A	Infineon	IPG20N10S4L-22	Transistor	2
	alternativ: 60V N-ch, 2.6A	Infineon	BSP318S	Transistor	2

Figure 21 Bill of Materials for Flyback application circuit

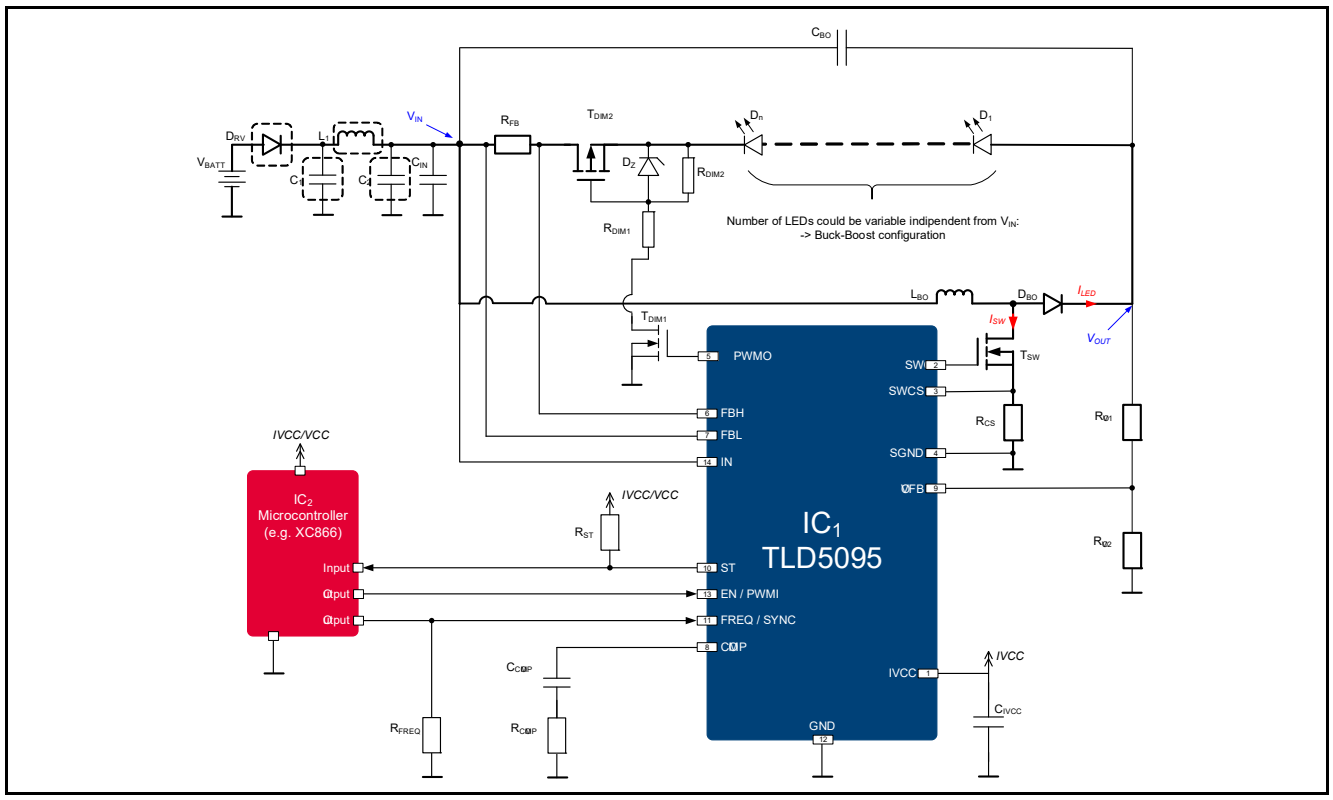


Figure 22 Boost to Battery application circuit - B2B (Buck - Boost configuration)

Reference Designator	Value	Manufacturer	Part Number	Type	Quantity
D_{1-n}	White	Osram	LUW H9GP	Diode	variable
D_{BO}	Schottky, 3 A, 100 V_R	Vishay	SS3H10	Diode	1
D_Z	5V	Vishay	Zener	Diode	1
C_{BO}	100 uF, 80V	Panasonic	EEVFK1K101Q	Capacitor	1
C_{IN}	100 uF, 50V	Panasonic	EEEFK1H101GP	Capacitor	1
C_{COMP}	10 nF	EPCOS	X7R	Capacitor	1
C_{IVCC}	1 uF, 6.3V	EPCOS	MLCC CCNPZC105KBW X7R	Capacitor	1
IC_1	--	Infineon	TLD5095	IC	1
IC_2	--	Infineon	XC866	IC	1
L_{BO}	100 uH	Coilcraft	MSS1278T-104ML_	Inductor	1
R_{COMP}, R_{DIM1}, R_{DIM2}	10 kΩ, 1%	Panasonic	ERJ3EKF1002V	Resistor	3
R_{FB}	820 mΩ, 1%	Panasonic	ERJ14BQFR82U	Resistor	1
R_{FREQ}, R_{ST}	20 kΩ, 1%	Panasonic	ERJ3EKF2002V	Resistor	2
R_{OVH}	33.2 kΩ, 1%	Panasonic	ERJP06F5102V	Resistor	1
R_{OVL}	1 kΩ, 1%	Panasonic	ERJ3EKF1001V	Resistor	1
R_{CS}	50 mΩ, 1%	Panasonic	ERJB1CFR05U	Resistor	1
T_{DIM1}, T_{DIM2}	60V Dual N-ch (3.1A) and P-ch. enh. (2A)	Infineon	BSO615CG	Transistor	1
	alternativ: 100V N-ch (0.37A),	Infineon	BSP123	Transistor	1
	alternativ: 60V P-ch (1.9A)	Infineon	BSP171P	Transistor	1
T_{SW}	N-ch, OptiMOS-T2 100V, 35A	Infineon	IPD35N10S3L-26	Transistor	1
	alternativ: 60V N-ch, 30A	Infineon	IPD30N06S4L-23	Transistor	1
	alternativ: 60V N-ch, 2.6A	Infineon	BSP318S	Transistor	1

Figure 23 Bill of Materials for B2B application circuit

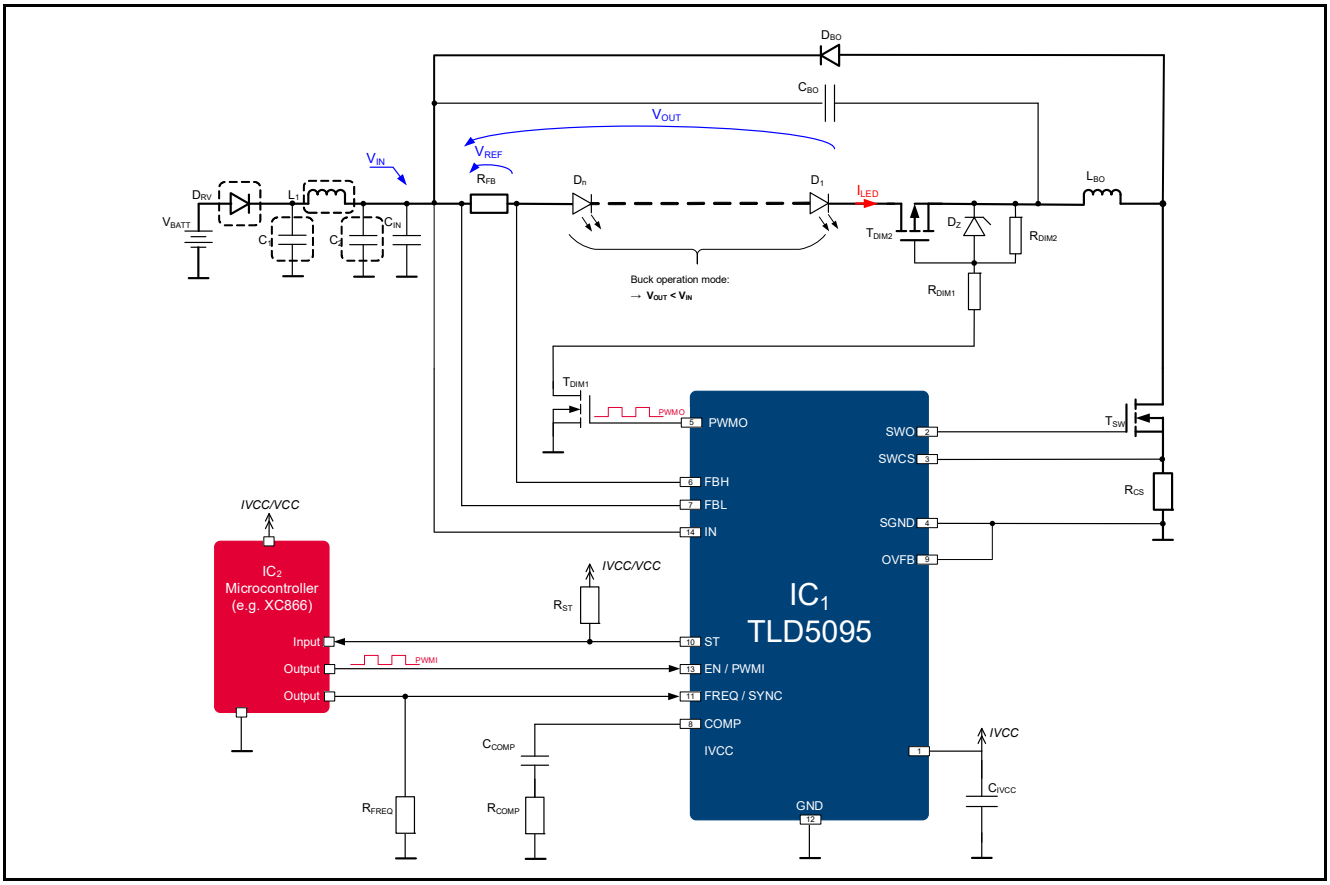


Figure 24 Buck application circuit

Reference Designator	Value	Manufacturer	Part Number	Type	Quantity
D_{1-2}	White	Osram	LE UW Q9WP	LED	2
D_{BO}	Schottky, 3 A, 100 V_R	Vishay	SS3H10	Diode	1
C_{BO}	4.7 uF, 50V	EPCOS	X7R	Capacitor	1
C_{IN}	100 uF, 50V	Panasonic	EEEFK1H101GP	Capacitor	1
C_{COMP}	47 nF	EPCOS	X7R	Capacitor	1
C_{IVCC}	1 uF , 6.3V	EPCOS	MLCC CCNPZC105KBW X7R	Capacitor	1
IC_1	--	Infineon	TLD5095	IC	1
IC_2	--	Infineon	XC866	IC	1
L_1	22 µH	Coilcraft	MSS1278T	Inductor	1
R_{COMP}	10 kΩ, 1%	Panasonic	ERJ3EKF1002V	Resistor	1
R_{FB}	820 mΩ, 1%	Isabellenhütte	SMS – Power Resistor	Resistor	1
R_{FREQ}, R_{ST}	20 kΩ, 1%	Panasonic	ERJ3EKF2002V	Resistor	2
R_{CS}	50 mΩ, 1%	Isabellenhütte	SMS - Power Resistor	Resistor	1
T_{SW}	100V, N-ch, 35A	Infineon	IPG20N10S4L-22	Transistor	1
	alternativ: 60V N-ch, 30A	Infineon	IPD30N06S4L-23	Transistor	1

Figure 25 Bill of Materials for Buck application circuit

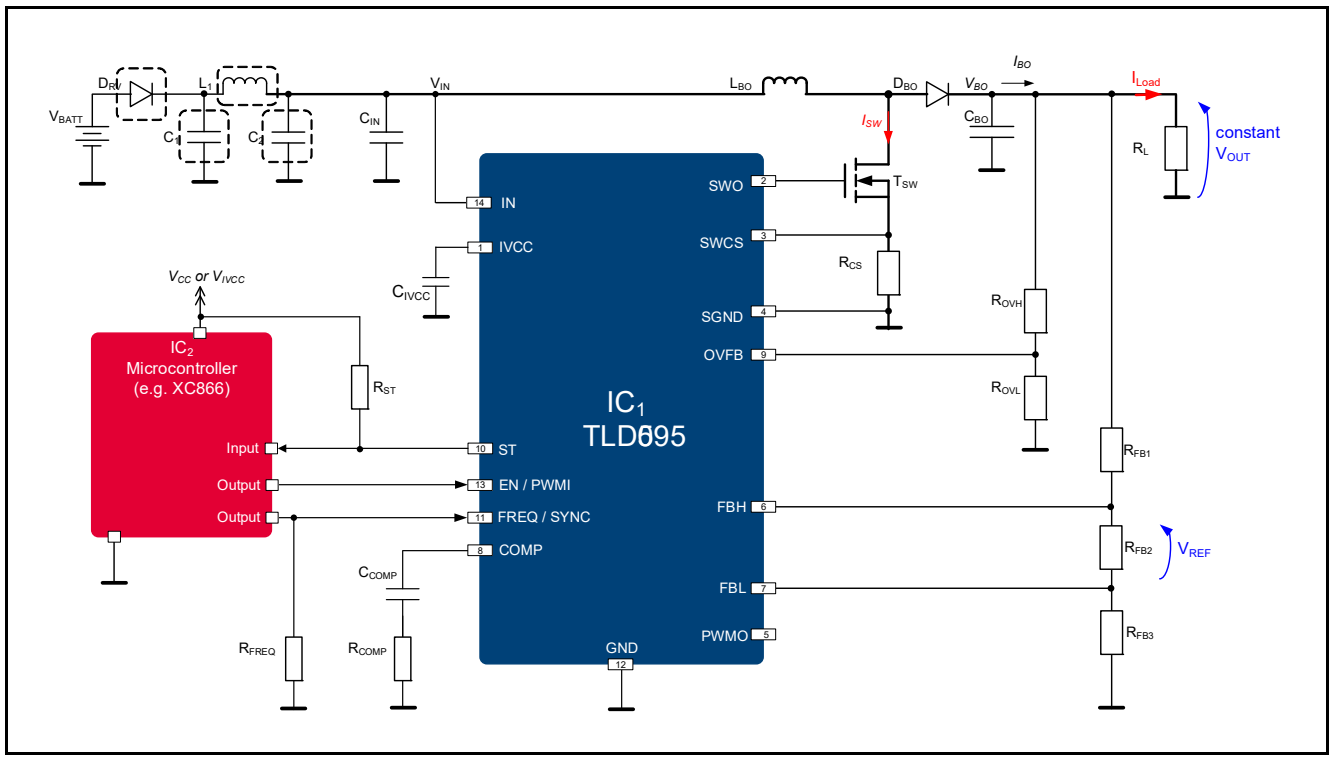


Figure 26 Boost voltage application circuit

Reference Designator	Value	Manufacturer	Part Number	Type	Quantity
D_{BO}	Schottky, 3 A, 100 V_R	Vishay	SS3H10	Diode	1
C_{BO}	100 uF, 80V	Panasonic	EEVFK1K101Q	Capacitor	1
C_{IN}	100 uF, 50V	Panasonic	EEEFK1H101GP	Capacitor	1
C_{COMP}	10 nF, 16V	EPCOS	X7R	Capacitor	1
C_{IVCC}	1 uF, 6.3V	Panasonic	X7R	Capacitor	1
IC_1	--	Infineon	TLD5095	IC	1
IC_2	--	Infineon	XC866	IC	1
L_{BO}	100 uH	Coilcraft	MSS1278T-104ML_	Inductor	1
R_{COMP}	10 kohms, 1%	Panasonic	ERJ3EKF1002V	Resistor	1
R_{FB1},R_{FB3}	51 kohms, 1%	Panasonic	ERJ3EKF5102V	Resistor	1
R_{FB2}	1 kohms, 1%	Panasonic	ERJ3EKF1001V	Resistor	1
R_{FREQ}, R_{ST}	20 kohms, 1%	Panasonic	ERJ3EKF2002V	Resistor	2
R_{OVH}	33.2 kohms, 1%	Panasonic	ERJ3EKF3322V	Resistor	1
R_{OVL}	1 kohms, 1%	Panasonic	ERJ3EKF1001V	Resistor	1
R_{CS}	50 mohms, 1%	Panasonic	ERJB1CFR05U	Resistor	1
T_{SW}	N-ch, OptiMOS-T2 100V	Infineon	IPD35N10S3L-26	Transistor	1

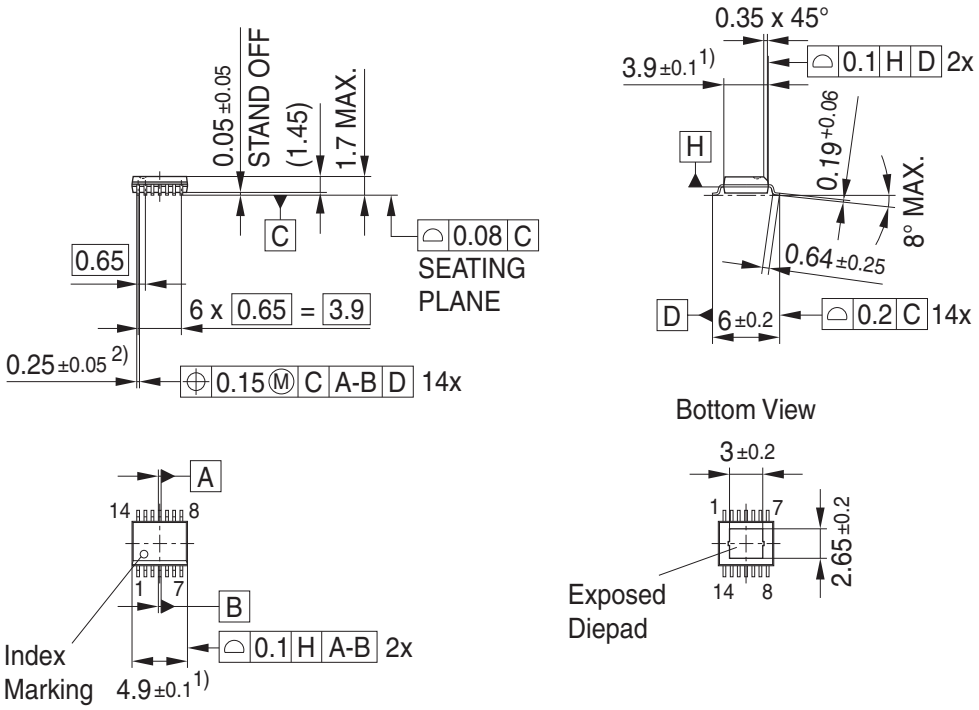
Figure 27 Bill of Materials for Boost voltage application circuit

Note: The application drawings and corresponding bill of materials are simplified examples. Optimization of the external components must be done accordingly to specific application requirements

10.1 Further application information

- For further information you may contact **http://www.infineon.com/**
- Application Note: TLD509x DC-DC Multitopology Controller IC “Dimensioning and Stability Guideline - Theory and Practice”

11 Package outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Lead width can be 0.61 max. in dambar area

Figure 28 Outline PG-SSOP-14 dimensions in mm

Green Product (RoHS Compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

12 Revision history

Revision	Date	Changes
1.5	2018-09-19	**Table 1** update
		P_4.1.7 updated (max 45 → 6.2)
		Table 2 update
		P_4.3.2 to P_4.3.4 added footnote
		P_5.2.12; P_5.2.13 added footnote
		P_5.2.12 added note current direction
		Table 7 inserted test conditions:
		P_7.1.9 added note current direction
		P_7.1.13 added footnote
		P_8.1.2 added note current direction
		P_9.2.5 added footnote
		P_9.2.6 added footnote
1.4	2015-03-11	Brand name change to LITIX™ Power

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