TPMS

Tire Pressure Monitoring Sensor

SP37T

High integrated single-chip TPMS sensor with a low power embedded micro-controller and wireless FSK/ASK UHF transmitter

SP37T Version A4

1300kPa

Datasheet

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SP37T High integrated single-chip TPMS sensor with a low power embedded micro-controller and wireless FSK/ASK UHF transmitter

Revision History: 2012-04-03, Revision 1.1

Previous Revision: Revision 1.0

Page	Subjects (major changes since last revision)
Page 78	Update LF Receiver Input Select
Page 148	Update Pressure Measurement Error
Page 156	Temperature Conditions Updated
Page 158	Temperature Conditions Updated

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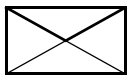

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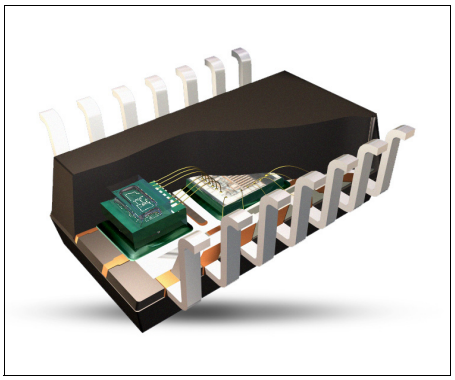
SP37T

1 Introduction



1.1 Overview

The SP37T is a sensor for air pressure measurements designed for TPMS applications. With its microcontroller and integrated peripherals, the SP37T offers a single package solution for TPMS applications. It requires only few external components. The SP37T features

- Pressure sensor for ambient pressure measurement
- Z-axis acceleration sensor for motion detection
- Temperature and supply voltage sensor
- 8051 based microcontroller
- Advanced system controller to minimize power consumption
- RF Transmitter
- LF Receiver

Measurements of pressure, acceleration, temperature, and battery voltage are performed under software control, and the data can be formatted and prepared for RF transmission by the microcontroller.

An intelligent wakeup mechanism is available to reduce power consumption. An Interval Timer controls the timing of measurements and transmissions. The circuitry can be programmed to wakeup at regular intervals or it can be woken up by the integrated LF Receiver, which furthermore enables SP37T to receive data. Additionally, wakeup is possible by an external wakeup source connected to a General Purpose Input/Output (GPIO).

The integrated microcontroller is instruction set compatible to the standard 8051 processor. It is equipped with various peripherals (e.g. a hardware Manchester/BiPhase Encoder/Decoder and CRC Generator/Checker) enabling an easy implementation of customer-specific applications.

The low power consumption RF Transmitter for 315 and 434 MHz contains a fully integrated PLL synthesizer, an ASK/FSK modulator and an efficient power amplifier. Fine tuning of the center frequency can be done either using the on-chip capacitors bank or adding external capacitors.

On-chip FLASH memory is integrated to store:

- The customer specific application program code
- A unique ID-Number
- The calibration data for the sensors

Additional on-chip ROM memory is available that holds the ROM library functions (developed by Infineon) which covers standard tasks used by the application. The available ROM Library functions are described in a separate document (see **[1]**).

Product Name	Product Type	Ordering Code	Package
SP37T	Tire Pressure Monitoring Sensor	SP370-23-156-0	PG-DSOSP-14-6

1.2 Features

Main features:

- Supply voltage range from 1.9 V up to 3.6 V
- Operating temperature range -40 to +125 °C
- Low supply current
- Pressure sensor for 1300kPa range
- Z-axis acceleration sensor for motion detection
- Temperature sensor
- THERMAL SHUTDOWN mode for device protection at high temperatures
- Battery voltage sensor
- Integrated RF Transmitter for ISM Band 315/434 MHz
- Selectable output power 5 or 8 dBm (transformed into 50 Ohm load)
- Configurable RF transmission data rates up to 10 kbit/s Manchester coded (20 kchips/s)
- ASK/FSK modulation capability
- Frequency deviation up to 50 kHz in FSK mode
- Fully integrated VCO and PLL Synthesizer
- On chip crystal oscillator tuning
- LF Receiver with very high input sensitivity
- LF Receiver data rate 3.9 kbit/s
- 8051 instruction set compatible microcontroller (cycle-optimized)
- 6 kByte FLASH memory (for application code)
- 16 kByte ROM (for ROM library functions)
- 256 Bytes RAM
- Wakeup from POWER DOWN state using the Interval Timer, the LF Receiver or an external wakeup source connected via a GPIO pin
- I^2C programming/debugging interface
- Hardware Manchester/BiPhase Encoder for RF Transmitter
- Hardware Manchester Decoder for LF Receiver
- 16 Bit Hardware CRC generator
- 8 Bit Pseudo Random Number Generator
- Watchdog timer
- 3 bidirectional GPIO pins

2 Functional Description

2.1 General

2.2 Pin Configuration

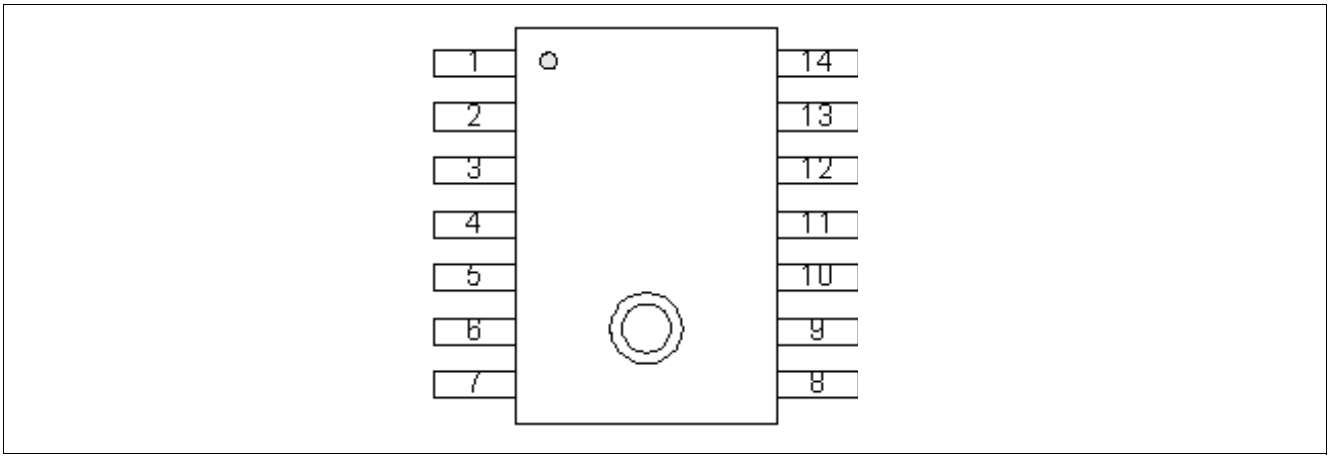


Figure 1 Pin Configuration PG-DSOSP-14-6 (Top View, Figure not to Scale)

2.3 Pin Description

Table 1 IPin Description

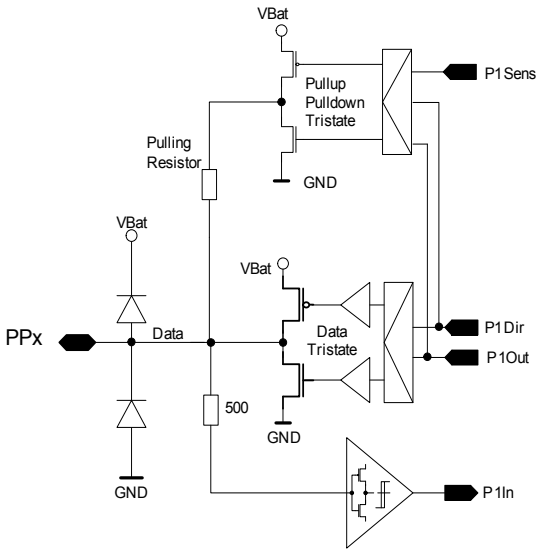
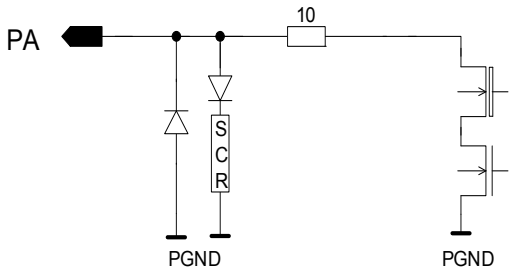
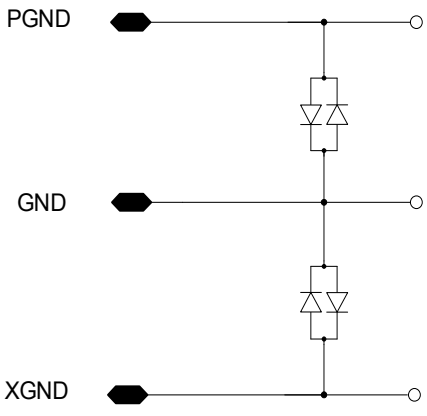
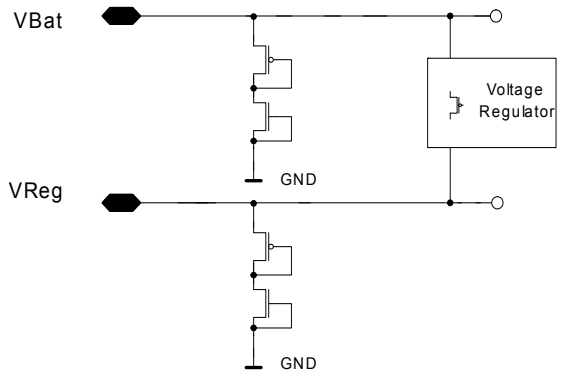
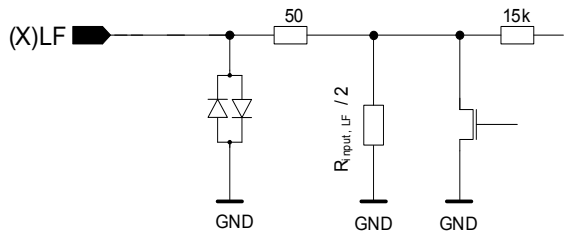
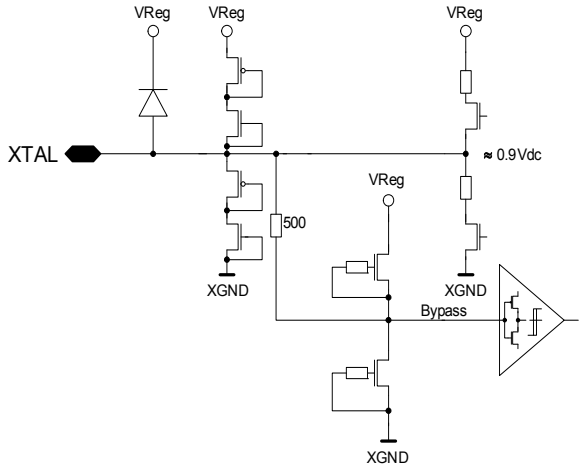
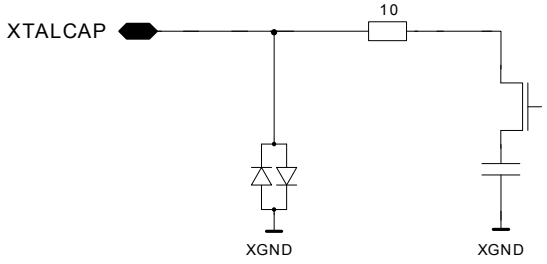
Pin No.	Name	Pin Type	Buffer Type	Function
1	PP0	Digital I/0		GPIO PP0 / I2C Clock / OpMode0 *Note: Internal pull-up/pull-down switchable*
2	PP1	Digital I/0		GPIO PP1 / I2C Data / OpMode1 *Note: Internal pull-up/pull-down switchable*
3	PP2	Digital I/0		GPIO PP2 / TxData *Note: Internal pull-up/pull-down switchable*
4	PA	Analog		RF Transmitter Output
5	PGND	Supply		RF Transmitter Ground
7	GND	Supply		**Ground**
8	GND	Supply		**Ground**
12	XGND	Supply		**Crystal Oscillator Ground**

Table 1 IPin Description (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
6	VBAT	Supply		**Battery Supply Voltage**
9	VREG	Supply		**Internal voltage regulator output** *Note: Connect to decoupling capacitor (CBCAP=100nF)*
10	LF	Analog		**Differential LF Receiver Input 1**
11	XLF	Analog		**Differential LF Receiver Input 2**
13	XTAL	Analog		**Crystal Oscillator Input**
14	XTALCAP	Analog		**Crystal Oscillator Load Capacitance**

2.4 Block Diagram

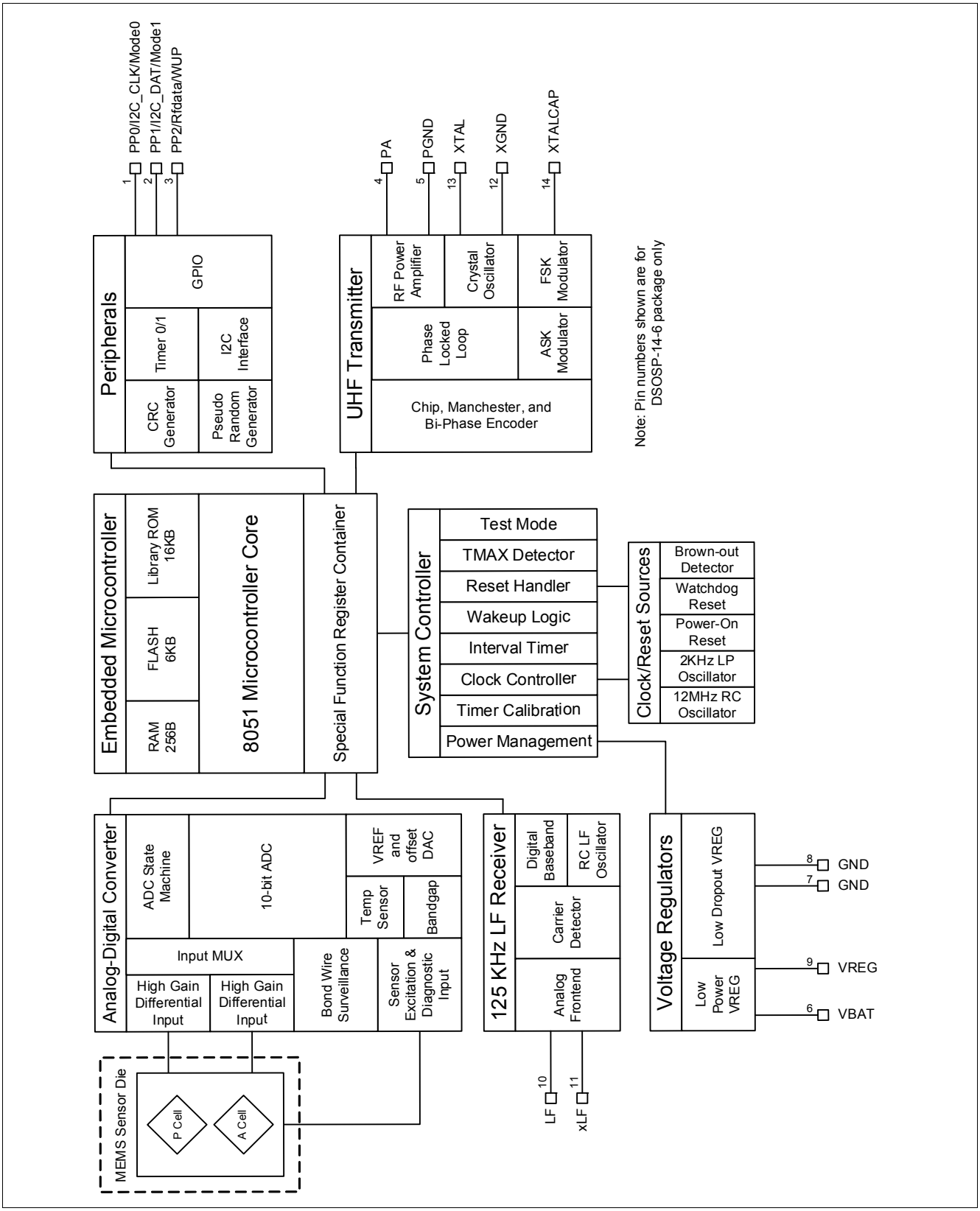


Figure 2 SP37T Block Diagram

2.5 Operating Modes and States

The SP37T can be operated in four different operating modes.

- NORMAL mode
- PROGRAMMING mode
- DEBUG mode
- (internal production TEST mode)

The operating mode selection is done at Power On Reset by setting the GPIO pins PP0 and PP1 according to the following table:

Table 2 SP37T - Operating Modes

PP0	PP1	Operating mode	Device controlled by
1	1	NORMAL mode	FLASH Program at 4000_H
0	1	PROGRAMMING mode	ROM firmware / external I^2C Master
1	0	DEBUG mode	ROM firmware / external I^2C Master
0	0	Internal production test mode[1)]	ROM firmware / external I^2C Master

1) IMPORTANT: Do not enter this mode since unpredictable behavior of the device might result

Note: Since PP0 and PP1 have their internal pull-up resistors enabled at Power On Reset, the default startup mode is NORMAL mode if the PP0 and PP1 pins are left unconnected.

2.5.1 Operating Modes

The operating modes depend on the setting of Lockbyte 2, which protects the FLASH Sector 0 (Code Sector) against overwriting, erasing and read-out to prevent reverse engineering of the application code. **Figure 3** shows the mode diagram if the Lockbyte 2 is not set.

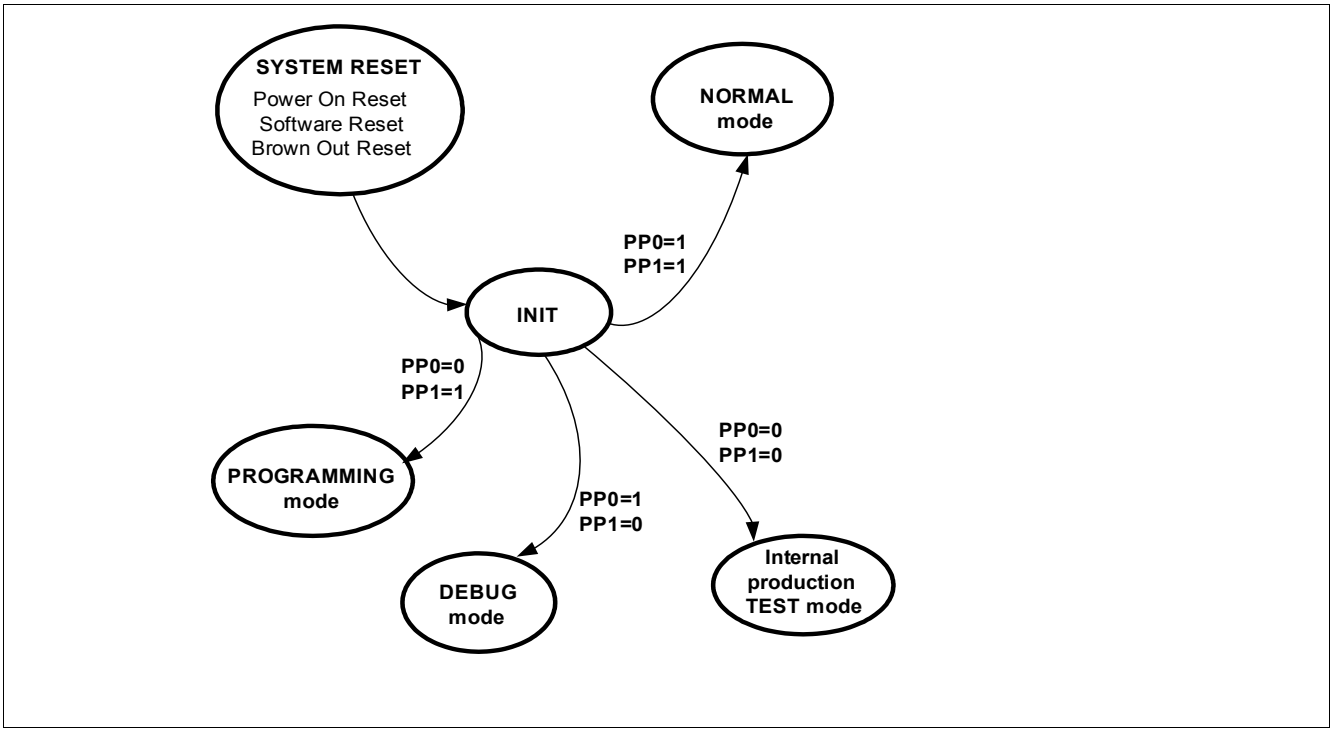


Figure 3 Available Operating Modes if Lockbyte 2 is not Set

For security reasons some operating modes are not accessible anymore after the Lockbyte 2 (see **"FLASH" on Page 29**) is set. **Figure 4** shows the behavior of the SP37T once the Lockbyte 2 is set. All mode selections (except the internal production TEST mode) lead to NORMAL mode.

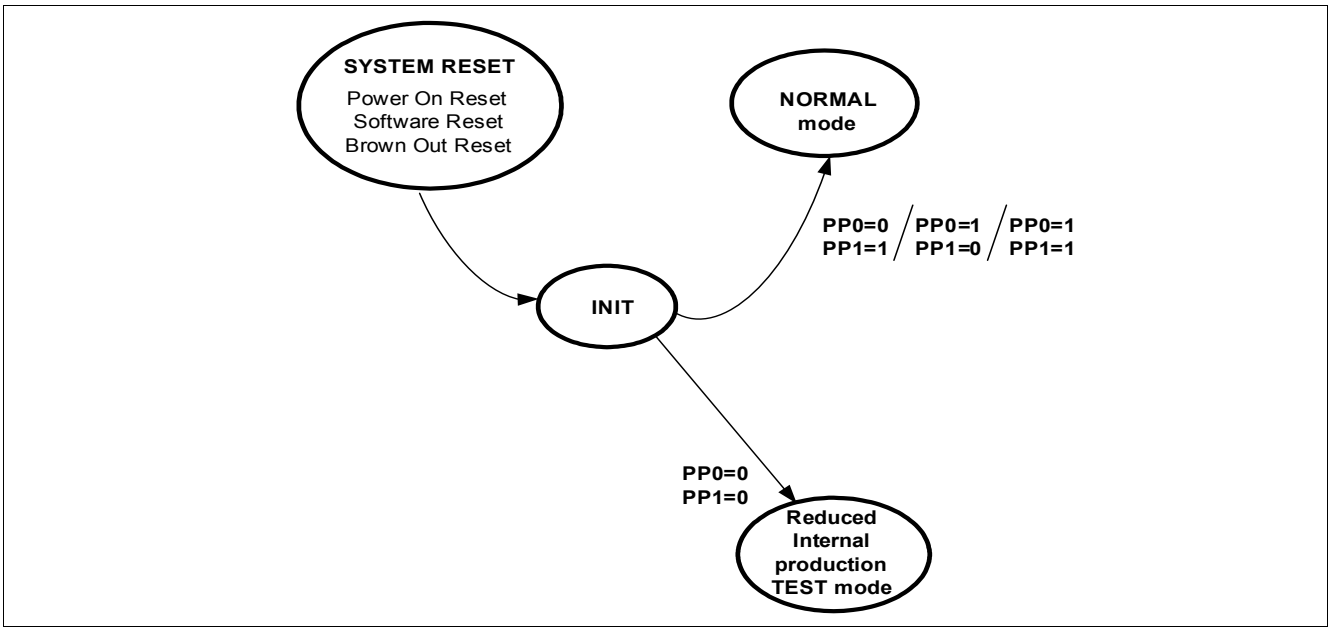


Figure 4 Available Operating Modes if Lockbyte 2 is Set

2.5.2 Resets and Operating Mode Selection

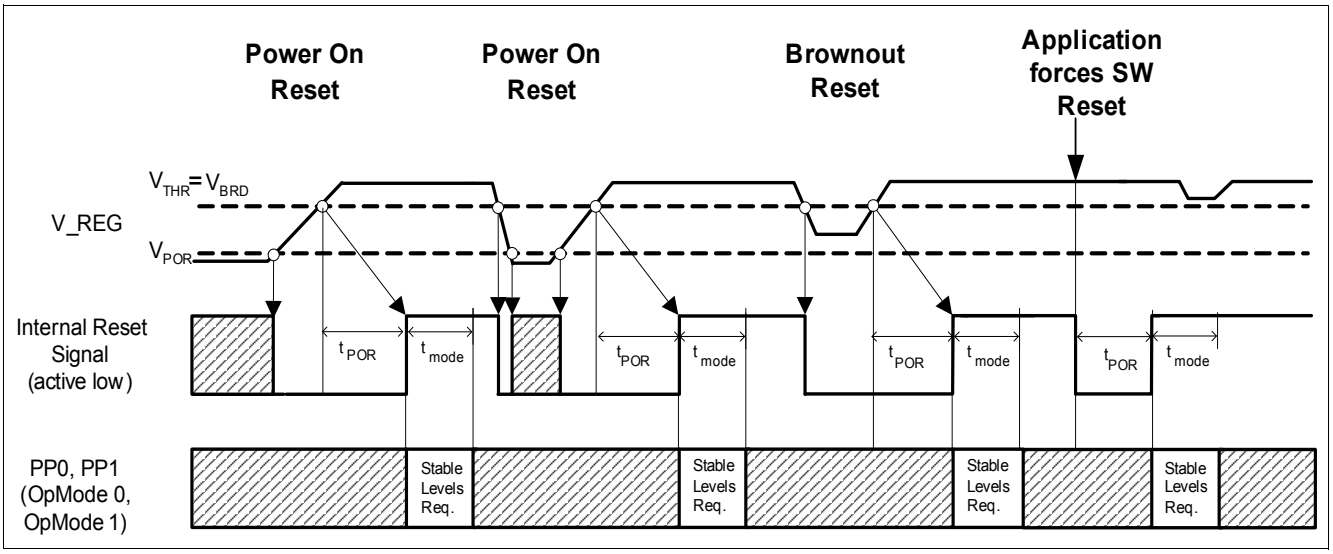


Figure 5 Power On Reset / Brown Out Reset / Operating Mode Selection

Three kinds of resets can occur which cause an operating mode selection:

- The Power On Reset circuit is activated if V_{REG} rises above V_{POR}. The internal blocks are held in RESET state until V_{REG} has risen above V_{THR}.
- The Brown Out Reset circuit is activated if V_{REG} drops below V_{BRD}. The internal blocks are held in RESET state until V_{REG} has risen above V_{BRD} again.
- The SP37T's Software Reset can be forced by SP37T setting SRF bit CFG2.0[RESET].

When the Internal Reset state is released (after t_{POR} is elapsed), a further period t_{MODE} is required for reading the states applied to PP0 and PP1 to determine the operation mode of the device according to **Table 2 "SP37T - Operating Modes" on Page 18**. The levels on these pins must be stable during the whole t_{MODE} period. After t_{MODE} has elapsed, the device starts operation in the selected mode.

The Watchdog Reset is a special case and it does not result in a mode selection. The Watchdog Reset affects only the CPU core and forces a program restart.

2.5.3 NORMAL Mode Operation

After a startup in NORMAL mode the system controller handles the different states as shown in the state transition diagram below.

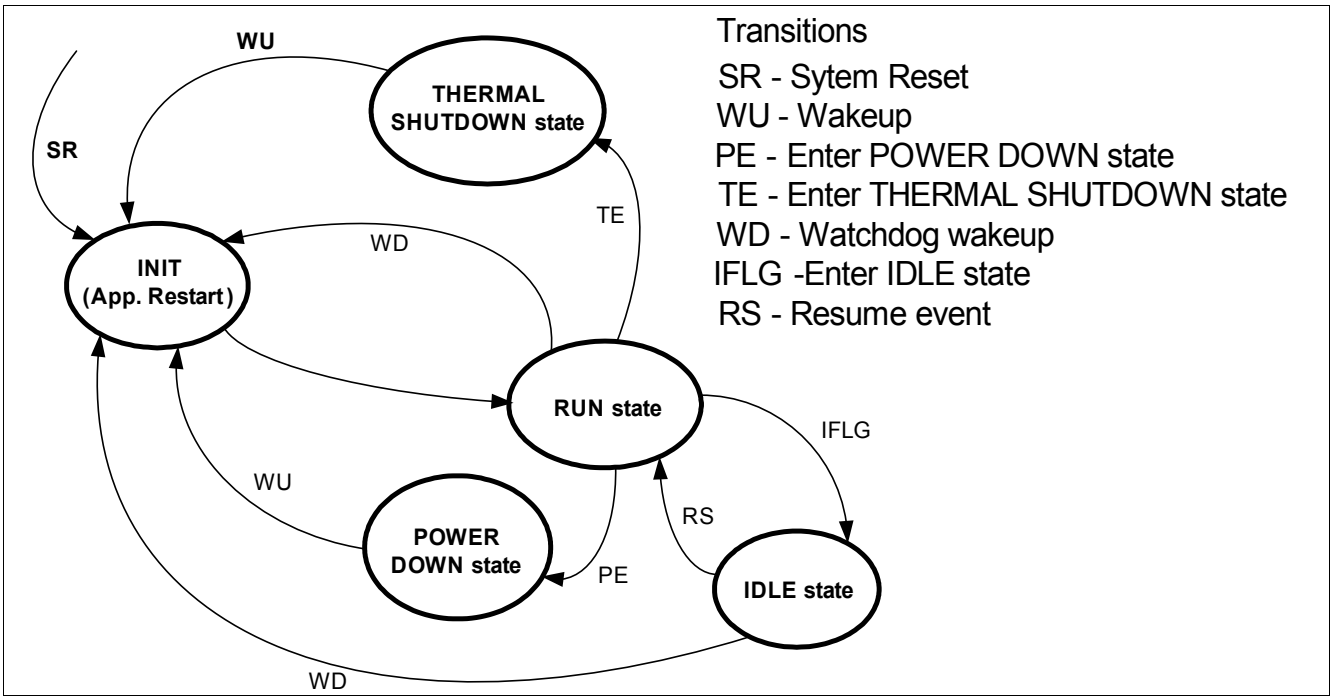


Figure 6 NORMAL Mode State Diagram

2.5.3.1 INIT State

The INIT state is entered after every System Reset (either Power On Reset, Brown Out Reset or Software Reset) to determine the desired operation mode (see **“Operating Modes” on Page 19**) and to initialize the SP37T. The INIT state is entered as well if a wakeup or watchdog timeout occurs, but no operation mode selection is done after a wakeup and RUN state is entered immediately.

2.5.3.2 RUN State

In RUN state, the microcontroller is executing the application program from the FLASH. In this state the watchdog is active to prevent software-deadlocks. The microcontroller (CPU) clock source is always based on the 12MHz RC HF Oscillator.

2.5.3.3 IDLE State

In IDLE state the microcontroller clock is stopped to reduce the current consumption, while the peripherals Timer 0, ADC, RF Transmitter and LF Receiver can continue normal operation.

After a resume event is triggered by one of the enabled peripherals, the microcontroller continues the operation where it was interrupted. The resume event source can be identified by reading SFR REF (see **“Resume Event Flag Register” on Page 50**).

2.5.3.4 POWER DOWN State

In POWER DOWN state, the system controller takes control of the SP37T microcontroller and most peripherals are switched off.

In POWER DOWN state the active peripherals (Interval Timer, LF On/Off timer,...) are clocked by the 2kHz RC LP Oscillator.

After a wakeup occurred, the wakeup source can be identified by reading SFR WUF (see **"Wakeup Flag Register" on Page 48**).

2.5.3.5 THERMAL SHUTDOWN State

The application can enter THERMAL SHUTDOWN state if the temperature is above the TMAX threshold temperature. Once the device is in THERMAL SHUTDOWN state, only the TMAX circuit can provide a wakeup event. All other wakeup sources are disabled. The device will remain in this state until the temperature falls below the T_{REL} threshold (see **"TMAX Detector" on Page 24** for details).

2.5.3.6 State Transitions

With reference to **Figure 6 "NORMAL Mode State Diagram" on Page 21**, the following state transitions can occur:

Table 3 State Transitions in NORMAL Mode

State transition	Description
RUN state => IDLE state	The application program can set SFR bit CFG0.5 [IDLE] to enter IDLE state. (see **"Configuration Register 0" on Page 41**) Note: If no peripheral that can create a RESUME event is active, IDLE state will not be entered and the application will continue un-interrupted.
IDLE state => RUN state	A peripheral unit (Timer 0, ADC, RF Transmitter, LF Receiver) creates a resume event. The application automatically resumes where it was interrupted when entering IDLE state (see **"Resume Event Flag Register" on Page 50**)
IDLE state => INIT state RUN state => INIT state	Overflow of the watchdog timer. The application will restart. The watchdog wakeup is indicated in the SFR WUF. **"Wakeup Flag Register" on Page 48**
RUN state => THERMAL SHUDOWN state	The application program can call a ROM Library function to enter THERMAL SHUTDOWN state.
RUN state => POWER DOWN state	The application program can call a ROM Library function to enter POWER DOWN state.
POWER DOWN state => RUN state THERMAL SHUTDOWN state => RUN state	A wakeup event will restart the application, and set the SFR WUF accordingly. (see **"Wakeup Flag Register" on Page 48**)
INIT state => RUN state	This state change is initiated automatically by the system controller as soon as the initialization is finished.

2.5.3.7 Status of SP37T Blocks in Different States

Depending on the current state in NORMAL mode the internal blocks of the SP37T are active, inactive or are not supplied with supply voltage to minimize the current consumption. The following table gives an overview over of the individual blocks in the different states.

Table 4 Status of SP37T Blocks in Different States

Unit	Run state	IDLE state	POWER DOWN state	THERMAL SHUT-DOWN state
Power On Reset	Active[1)]	Active	Active	Active
Brown Out Detector	Active	Active	Inactive	Inactive
TMAX Detector	Handled by ROM Library functions[2)]	Inactive[3)]	Inactive	Active
Voltage Regulator (V_{REG})	Active	Active	Active	Active
System controller	Active	Active	Active	Active
Microcontroller	Active	Inactive	No supply[4)]	No supply
Manchester/ BiPhase encoder, Timer	Active	Active	No supply	No supply
Peripheral modules CRC, I2C, Pseudo Random Number Generator	Selectable inactive or active	Inactive	No supply	No supply
Watchdog timer	Active	Active	No supply	No supply
Upper 128Bytes RAM	Active	Inactive	No supply	No supply
Lower 128Bytes RAM	Active	Inactive	Selectable No supply or inactive	Selectable No supply or inactive
FLASH	Active	Inactive	No supply	No supply
ROM	Active	Inactive	No supply	No supply
Crystal oscillator	Selectable inactive or active	Selectable inactive or active	No supply	No supply
2kHz RC LP Oscillator	Active	Active	Active	Inactive
12MHz RC HF Oscillator	Active	Active	No supply	No supply
Interval Timer	Active	Active	Active	Inactive
LF Receiver	Selectable inactive or active	Selectable inactive or active	Selectable inactive or active	Inactive
RF Transmitter	Selectable inactive or active	Selectable inactive or active	Inactive	Inactive
Sensor	Handled by ROM Library functions	Handled by ROM Library functions	No supply	No supply

1) Active: block is powered, active and keeps its register contents.
2) The ADC, the Sensor and VMIN Detector are controlled by ROM Library functions described in [1].
3) Inactive: block is powered, cannot be used, but keeps its register contents.
4) No supply: block is not powered, cannot be used and all register content is lost.

2.6 Fault Protection

The SP37T features multiple fault protections which prevent the application from unexpected behavior and deadlocks. This chapter gives a brief overview of the available fault protections. Detailed explanation of the usage can be found later in this document and in **[1]**.

2.6.1 Watchdog Timer

For operation security a watchdog timer is available to avoid application software deadlocks. The watchdog timer is only active in NORMAL mode and DEBUG mode and must be reset periodically by the application, otherwise the timer generates a wakeup and forces a restart of SP37T application program. Setting SFR bit CFG2.1[WDRES] resets the watchdog timer (see **"Configuration Register 2" on Page 43**)

The watchdog timeout period is fixed (see **Table 51 "Watchdog Timer" on Page 166**). The accuracy depends on the accuracy of the 2kHz RC LP Oscillator which is used to clock the watchdog timer.

Upon wakeup the watchdog timer is automatically reset. The watchdog timer is not, however, automatically reset upon entry into IDLE state. Therefore care must be taken so that the application does not remain in IDLE state longer than the minimum watchdog timeout period.

2.6.2 VMIN Detector

This circuit will detect if the supply voltage is very close to the minimum required value. The ROM library functions which perform measurements will return the VMIN status in a status byte with the measurement result (see **[1]**).

2.6.3 ADC Measurement Overflow & Underflow

The ROM Library functions which perform measurements will return the over/underflow status in a status byte with the measurement result. (see **[1]**)

2.6.4 ADC Selftest

A dedicated ROM Library function is able to perform a selftest of the ADC (see **[1]**).

2.6.5 Bond Wire Surveillance

The continuity of the bond wire connection between the ASIC die and the sensor die is checked as part of every pressure and acceleration measurement. The ROM library routines which perform the measurements will return the bond wire status in a status byte with the measurement result (see **[1]**).

2.6.6 Sensor Integrity Check

An integrity check of the acceleration sensor is performed as part of every measurement. The ROM library routine which performs acceleration measurements will return the integrity status in the status byte with the measurement result (see **[1]**).

2.6.7 TMAX Detector

The TMAX detector is used to wakeup the SP37T from THERMAL SHUTDOWN state if the ambient temperature falls below the release trigger level T_{REL}.
Entering THERMAL SHUTDOWN state is initiated by a ROM Library function described in **[1]**.

2.7 Functional Block Description

2.7.1 Sensors and Data Acquisition

The SP37T has four sensors to acquire environmental data:

2.7.1.1 Pressure Sensor

The pressure sensor consists of a single-crystal silicon, bulk micro machined membrane with an integrated full Wheatstone piezo-resistive bridge. The piezo-resistors are placed inside a vacuum reference chamber, whilst the pressure media to be measured in the application is applied to the opposite side of the membrane. This gives good long-term properties as the measurement bridge is protected from the environment. Pressure measurement is performed by a dedicated ROM library function (see **[1]**).

2.7.1.2 Acceleration Sensor

The acceleration sensor consists of a single-crystal silicon, bulk micro machined beam and mass with an integrated full Wheatstone piezo-resistive bridge. The whole beam and mass are placed inside a hermetically sealed chamber and are therefore well protected from the environment. A diagnostic resistor is integrated along the edge of the beam to be used to check the mechanical integrity of the beam. Acceleration measurement is performed by a dedicated library ROM library function (see **[1]**). **Figure 7** shows the direction of the sensitive axis for the accelerometer. If the SP37T is mounted on the wheel as shown in **Figure 7**, it will measure a positive acceleration when the wheel rotates.

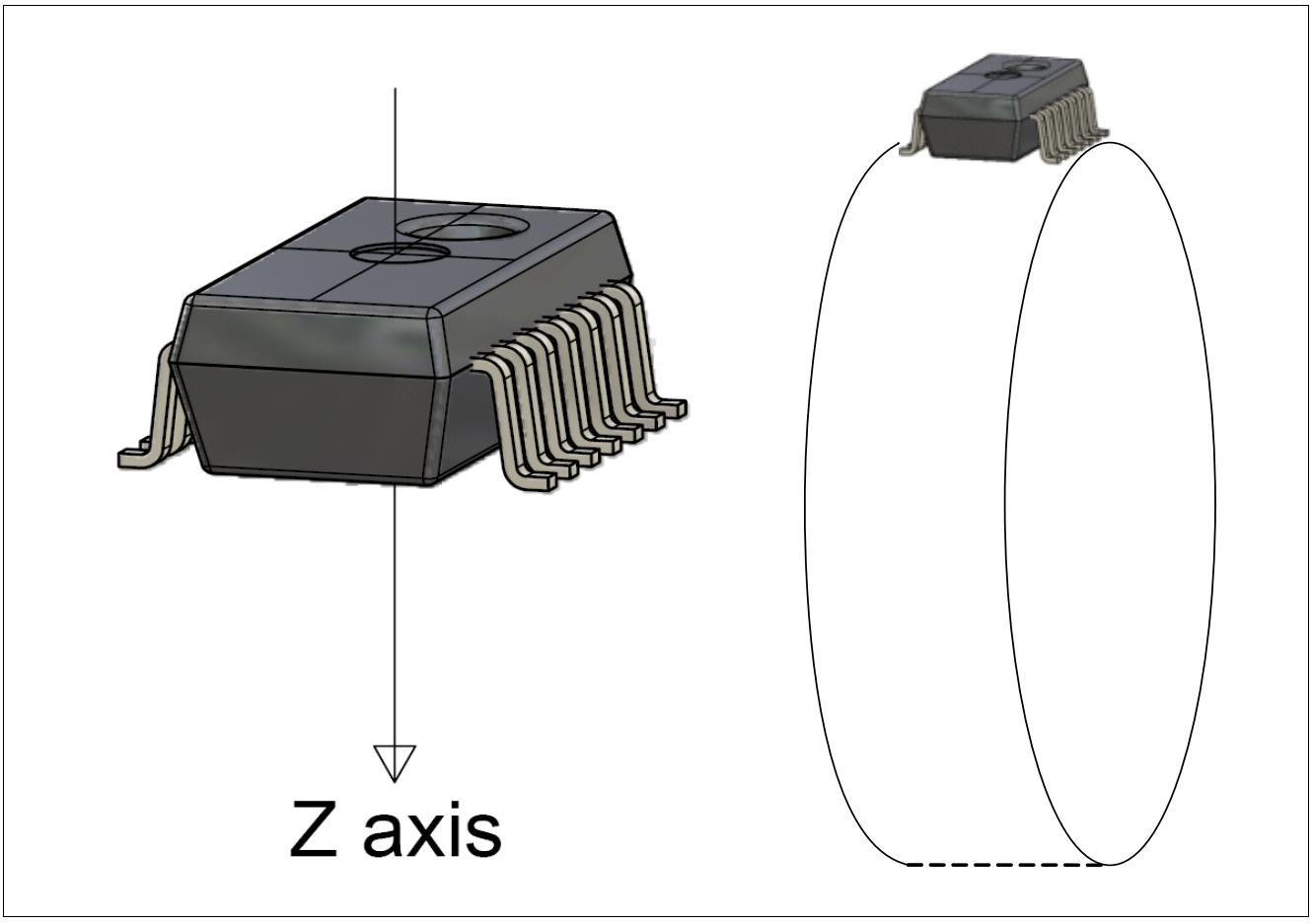


Figure 7 Device Orientation

2.7.1.3 Temperature Sensor

The temperature sensor is placed on the ASIC. This is read by the ADC referenced to a fixed (band gap) voltage. Temperature measurement is performed by a dedicated ROM library function (see **[1]**).

2.7.1.4 Battery Voltage Sensor

The battery voltage sensor is a circuit which provides a signal proportional to the supply voltage. The voltage is read by the ADC referenced to a fixed (band gap) voltage. Supply Voltage measurement is performed by a dedicated ROM library function (see **[1]**).

2.7.1.5 Data Acquisition

The analog data is acquired and digitized by the internal 10 Bit ADC.

Measurement routines for acquiring the environmental data are available within the ROM library functions that are described in **[1]**.

Characteristic of the individual sensors can be found in **“Characteristics” on Page 148**.

2.7.2 Memory Organization

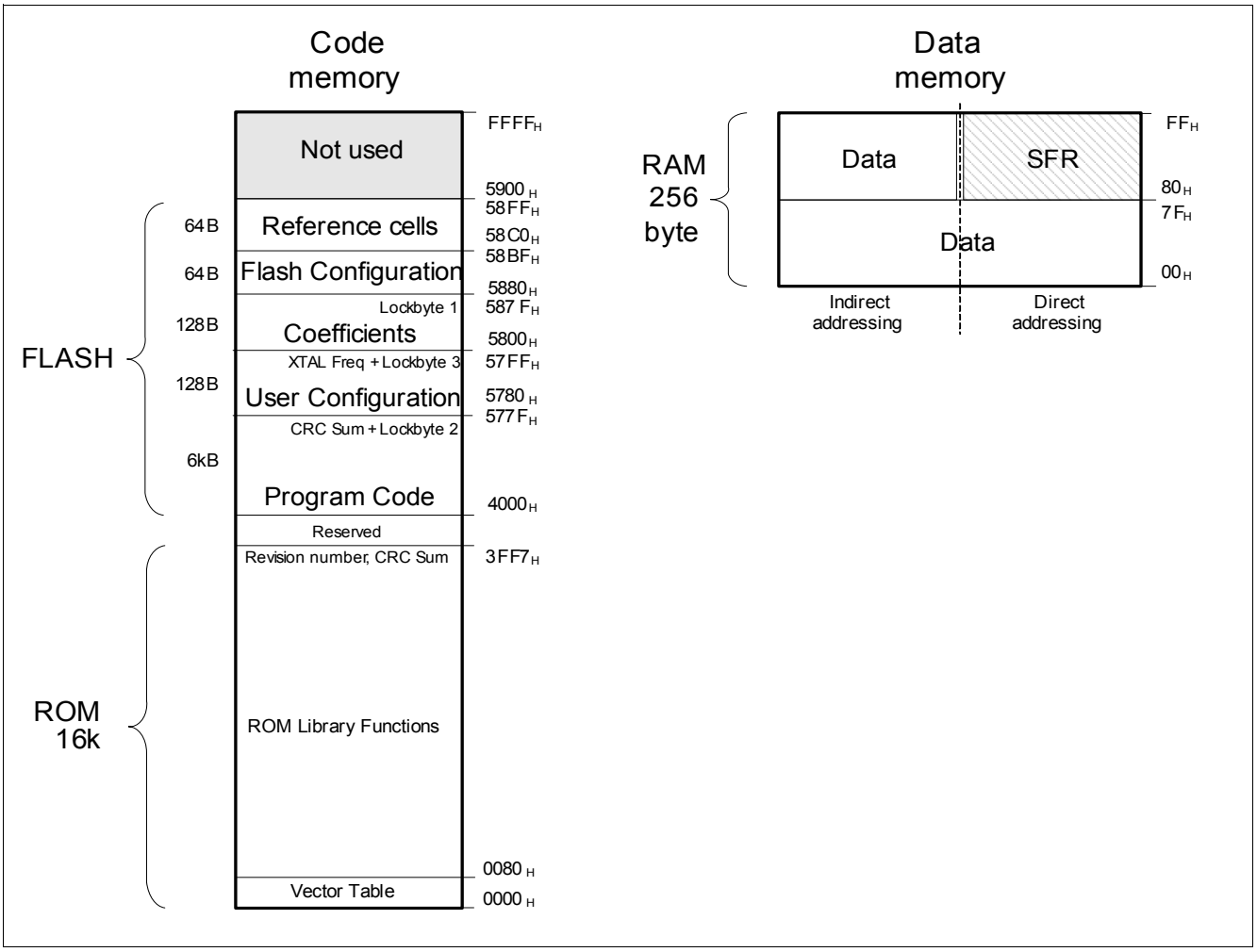


Figure 8 Memory Map

The following memory blocks are implemented:

- 16 kByte ROM memory
- 6 kByte FLASH memory
- 256 Byte RAM memory
- 128 Byte SFR register

2.7.2.1 ROM

A 16 kB ROM memory is located in the address range 0000_H to $3FF7_H$.

2.7.2.1.1 ROM Library Functions and Reset/Wakeup Handlers

The ROM contains the reset handler, operation mode handler, wakeup handler, internal test and debug routines and the ROM Library functions (see in [1]).

2.7.2.1.2 ROM Protections

To protect the ROM code against readout a hardware mechanism is implemented, thus no read operations can be performed on the ROM.

Direct jumping into the ROM area is prevented by a hardware mechanism, thus access to the ROM library functions is granted only via a vector table at the bottom of the ROM address space.

2.7.2.2 FLASH

2.7.2.2.1 FLASH Organization

The FLASH is divided into five sectors. Each sector can be erased and written individually.

Sectors 0 and 1 are accessible for customer usage.

Sectors 2, 3 and 4 are written in the Infineon production site and cannot be erased or re-written by the customer.

- **4000_H -- $577F_H$ (6016 Bytes) Code sector (0):** The code sector contains the application software including a CRC16 Checksum (to be written to $577D_H$ -- $577E_H$) and the Lockbyte 2 (to be written to $577F_H$).
- **5780_H -- $57FF_H$ (128 Bytes) User Configuration sector (1):**The User Configuration sector can store individual device configuration data. It also contains the crystal frequency which is needed as a timebase for ROM Library functions (to be written to $57FA_H$ -- $57FC_H$) and the Lockbyte 3 (to be written to $57FF_H$).
- **5800_H -- $587F_H$ (128 Bytes) Coefficients sector (2):** This sector is written during the sensor calibration process and contains calibration coefficients, the unique Sensor ID and Lockbyte 1 (to be written to $587F_H$).
- **5880_H -- $58BF_H$ (64 Bytes) FLASH Configuration sector (3):** This sector contains the FLASH driver parameters and other device configuration parameters.
- **$58C0_H$ -- $58FF_H$ (64 Bytes) Reference Cell sector (4):** This sector contains the reference cells for FLASH reading.

2.7.2.2.2 FLASH Protection

To protect the FLASH against unauthorized access three FLASH Lockbytes are available.

Note: The Lockbytes are set, if the value in the appropriate FLASH address is programmed to $D1_H$. Setting the Lockbyte to 00_H will result in a unlocked FLASH area. Any other value must not be written to these locations. After programming a Lockbyte, the SP37T has to be reset before the FLASH lock takes effect.

- **Lockbyte 1** ($587F_H$)

This Lockbyte protects the FLASH sectors 2, 3 and 4 against overwriting and erasing. This Lockbyte is programmed at the Infineon production site.

- **Lockbyte 2** ($577F_H$)

This Lockbyte protects the FLASH sector 0 (Code Sector) against overwriting, erasing (except reduced internal production test mode) and read-out to prevent reverse engineering of the application code.

This Lockbyte has to be set at the end of the programming sequence of the Code Sector via the I^2C Interface (when writing the highest FLASH Line starting at 5760_H). Once it is set, the available operating modes are reduced according to **Figure 4 “Available Operating Modes if Lockbyte 2 is Set” on Page 19**.

- **Lockbyte 3** ($57FF_H$)

This Lockbyte protects the FLASH sector 1 (User Configuration Sector) against overwriting and erasing (except reduced internal production test mode).

The Lockbyte can be set either via I^2C in PROGRAMMING mode in the same programming sequence as Lockbyte 2 is set, or by using a dedicated ROM Library function in NORMAL mode by the application software (see **[1]**).

2.7.2.3 RAM

The RAM is available as volatile data storage for the application program. Some RAM locations are required by the ROM Library Functions and therefore not freely available for use by the application program. For more details please refer to the ROM Library function guide **[1]**.

The upper 128 bytes of RAM are switched off in POWER DOWN state and THERMAL SHUTDOWN state and lose their contents.
The lower 128 bytes of RAM can be powered during POWER DOWN state and THERMAL SHUTDOWN state. This is selectable using SFR bit CFG2.4[PDLMB].

If not powered in these states, this RAM loses the content, otherwise it can be used as battery buffered storage like the General Purpose Registers (see **“General Purpose Registers” on Page 39**).

Note: The RAM is not reset at a System Reset or watchdog timeout.
After a Brown Out Reset this feature may be used to possibly recover data.
After Power On Reset the application has to initialize the RAM if needed.

3 Special Function Registers

Special Function Registers (SFR) are used to control and monitor the state of the SP37T and its peripherals.

The following table shows the naming convention for the SFR descriptions that are used throughout this document

Table 5 Register Naming Convention Wakeup / Reset Value

State	Symbol	Description
Low	0	Register value is 0_B
High	1	Register value is 1_B
Undefined	X	Register value is undefined
Unchanged	U	Register value is unchanged

Table 6 provides links within this document to detailed description of the application relevant SFRs. In addition to register names and offset addresses, this table indicates how each SFR behaves after wakeup and reset events. The Wakeup Value column applies in the case of a wakeup event, which includes a watchdog timeout. The Reset Value column applies in the case of a Power On Reset, Brownout Reset or Software Reset event.

Table 6 Registers Overview

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Reset Value
Microcontroller				
ACC	Accumulator	$E0_H$	00_H	00_H
B	Register B	$F0_H$	00_H	00_H
DPH	Data Pointer (high)	83_H	00_H	00_H
DPL	Data Pointer (low)	82_H	00_H	00_H
PSW	Program Status Word	$D0_H$	00_H	00_H
SP	Stack Pointer	81_H	07_H	07_H
General Purpose Registers[1)]				
GPR0	General Purpose Register 0	$B8_H$	UU_H	XX_H
GPR1	General Purpose Register 1	$B0_H$	UU_H	XX_H
GPR2	General Purpose Register 2	$A8_H$	UU_H	XX_H
GPR3	General Purpose Register 3	$F1_H$	UU_H	XX_H
GPR4	General Purpose Register 4	$F2_H$	UU_H	XX_H
GPR5	General Purpose Register 5	$F3_H$	UU_H	XX_H
GPR6	General Purpose Register 6	$F5_H$	UU_H	XX_H
GPR7	General Purpose Register 7	$F6_H$	UU_H	XX_H
GPR8	General Purpose Register 8	$F7_H$	UU_H	XX_H
GPR9	General Purpose Register 9	$F9_H$	UU_H	XX_H
GPRA	General Purpose Register 10	FA_H	UU_H	XX_H
GPRB	General Purpose Register 11	FB_H	UU_H	XX_H

Table 6 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Reset Value
GPRC	General Purpose Register 12	FC_H	UU_H	XX_H
GPRD	General Purpose Register 13	FD_H	UU_H	XX_H
GPRE	General Purpose Register 14	FE_H	UU_H	XX_H
GPRF	General Purpose Register 15	FF_H	UU_H	XX_H
System Configuration Registers				
CFG0	Configuration Register 0	$F8_H$	$0000U000_B$	00_H
CFG1	Configuration Register 1	$E8_H$	$000U000U_B$	00_H
CFG2	Configuration Register 2	$D8_H$	$000U1000_B$	18_H
DSR	Diagnosis and Status Register	$D9_H$	$0XUU00XU_B$	$0XXX0000_B$
System Controller				
WUF	Wakeup Flag Register	$C0_H$	XX_H	00_H
WUM	Wakeup Mask Register	$C1_H$	UU_H	FF_H
REF	Resume Event Flag Register	$D1_H$	00_H	00_H
Interval Timer				
ITPR	Interval Timer Period Register	BC_H	UU_H	01_H
Interval Timer Precounter / Calibration				
ITPH	Interval Timer Precounter Register (High Byte)	BB_H	$0000UUUU_B$	03_H
ITPL	Interval Timer Precounter Register (Low Byte)	BA_H	UU_H	$E8_H$
Clock Controller				
DIVIC	Internal Clock Divider	$B9_H$	$000000UU_B$	00_H
Crystal Pulling				
XTAL0	XTAL Frequency Register (FSKLOW)	$C4_H$	UU_H	FF_H
XTAL1	XTAL Frequency Register (FSKHIGH/ASK)	$C3_H$	UU_H	FF_H
RF 315/434 MHz FSK/ASK Transmitter				
RFC	RF-Transmitter Control Register	$C8_H$	00_H	00_H
RFTX	RF-Transmitter Configuration Register	AE_H	$UUU0UUUU_B$	87_H
Manchester/BiPhase Encoder				
RFENC	RF-Encoder Tx Control Register	CA_H	$E0_H$	$E0_H$
RFD	RF-Encoder Tx Data Register	$C9_H$	00_H	00_H
RFS	RF-Encoder Tx Status Register	CB_H	02_H	02_H
LF Receiver				
LFRXC	LF Receiver Control Register	98_H	$0UUUUU00_B$	00_H
LF Receiver Analog Front End				
LFRX0	LF Receiver Configuration Register 0	$B7_H$	UU_H	38_H
LF Attenuator (AGC)				
LFRX1	LF Receiver Configuration Register 1	$B6_H$	UU_H	00_H

Table 6 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Reset Value
LFRX2	LF Receiver Configuration Register 2	AF_H	UU_H	77_H
LF Carrier Detector				
LFCDFLT	LF Carrier Detect Filtering	$B2_H$	UU_H	00_H
LFCDM0	LF Carrier Detector Mode Register 0	$B5_H$	$UUUUUUU0_B$	00_H
LF Receiver On/Off Timer				
LFOOT	LF On/Off Timer Configuration Register	$C6_H$	UU_H	00_H
LFOOTP	LF OnOff Timer Precounter	$C5_H$	UU_H	64_H
LF Receiver Baseband				
LFDIV	LF Bitrate Divider Factor	$B4_H$	$00UUUUUU_B$	17_H
Wakeup Pattern Detector				
LFPCFG	LF Pattern Detection Configuration Register	$C7_H$	$00UU00UU_B$	00_H
LFP0H	LF Pattern 0 Detector Sequence Data MSB	CD_H	UU_H	FF_H
LFP0L	LF Pattern 0 Detector Sequence Data LSB	CC_H	UU_H	FF_H
LFP1H	LF Pattern 1 Detector Sequence Data MSB	CF_H	UU_H	FF_H
LFP1L	LF Pattern 1 Detector Sequence Data LSB	CE_H	UU_H	FF_H
LF Receiver Data Interface				
LFRXD	LF Receiver Data Register	$A5_H$	UU_H	00_H
LFRXS	LF Receiver Status Register	$A4_H$	$XUXUUUUU_B$	$X0X00000_B$
16 Bit CRC (Cyclic Redundancy Check) Generator/Checker				
CRCC	CRC Control Register	$A9_H$	02_H	02_H
CRCD	CRC Data Register	AA_H	00_H	00_H
CRC0	CRC Preload/Result Register 0 (low byte)	AC_H	00_H	00_H
CRC1	CRC Preload/Result Register 1 (high byte)	AD_H	00_H	00_H
Pseudo Random Number Generator				
RNGD	Random Number Generator Data Register	AB_H	UU_H	55_H
Timer Unit				
TCON	Timer Control Register	88_H	00_H	00_H
TMOD	Timer Mode Register	89_H	00_H	00_H
TH0	Timer 0 Register High Byte	$8C_H$	00_H	00_H
TL0	Timer 0 Register Low Byte	$8A_H$	00_H	00_H
TH1	Timer 1 Register High Byte	$8D_H$	00_H	00_H
TL1	Timer 1 Register Low Byte	$8B_H$	00_H	00_H
General Purpose Input/Output (GPIO)				
P1DIR	IO-Port 1 Direction Register	91_H	UU_H	FF_H
P1IN	IO-Port 1 Data In Register	92_H	$00000XXX_B$	$00000XXX_B$
P1OUT	IO-Port 1 Data Out Register	90_H	UU_H	FF_H
P1SENS	IO-Port 1 Sensitivity Register	93_H	$00000UUU_B$	00_H
I2C Interface				

Table 6 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Reset Value
I2CD	I2C Data Register	$9A_H$	00_H	00_H
I2CS	I2C Status Register	$9B_H$	00_H	00_H
Debug Special Function Register				
DBCH0	Debug Compare Register 0 (high byte)	95_H	00_H	00_H
DBCL0	Debug Compare Register 0 (low byte)	94_H	00_H	00_H
DBCH1	Debug Compare Register 1 (high byte)	$9D_H$	00_H	00_H
DBCL1	Debug Compare Register 1 (low byte)	$9C_H$	00_H	00_H
DBTH0	Debug Target Register 0 (high byte)	97_H	00_H	00_H
DBTL0	Debug Target Register 0 (low byte)	96_H	00_H	00_H
DBTH1	Debug Target Register 1 (high byte)	$9F_H$	00_H	00_H
DBTL1	Debug Target Register 1 (low byte)	$9E_H$	00_H	00_H

1) Reset Value for GRP0 - GPRF is typically undefined (X) except in the case of Software Reset, which leaves the GPR content unchanged (U).

The register is addressed bytewise.

Table 7 Registers Access Types

Mode	Symbol	Description Hardware (HW)	Description Software (SW)
Basic Access Types			
write/read	wr	Register is used as input for the HW	Register is read and writable by SW
read only	r	Register is written by HW	Value written by SW is ignored by HW; that is, SW may write any value to this field without affecting HW behavior
write only	w	Register is written by software and affects hardware behavior with every write by software.	Register is writable by SW. When read, the register does not return the value that has been written previously, but the reset value instead.
UNUSED	-	Register is not used by HW.	Value written by SW is ignored by HW; that is, SW may write any value to this field without affecting HW behavior.
Reserved		Register is used as input for internal HW; Access Type is not documented.	Value must be kept by SW. SW read or write any value to this field affecting HW behavior.
Special Access Types[1)]			
Read self clearing	rc	Register is used as input for the HW, the register will be cleared due to a HW mechanism.	Reading from the register generates a strobe signal for the HW. Register is readable by SW.
Write self clearing	wc	Register is used as input for the HW, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW. Register is writable by SW.

1) Optional types

3.1 Microcontroller

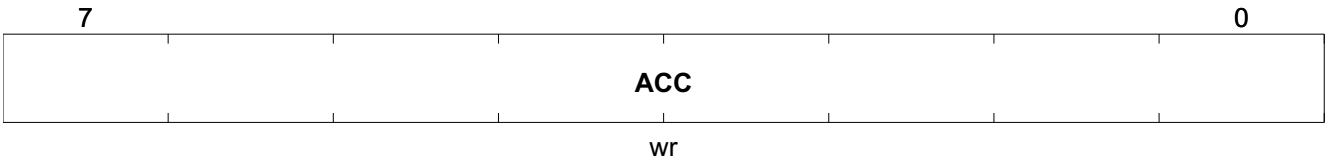
The SP37T incorporates an 8051 instruction set compatible microcontroller. It offers an 8-bit data path, several addressing modes (direct, register, register indirect, immediate, index), and accesses the built-in peripherals through SFRs. To handle the sequential nature of TPMS applications efficiently, wakeup and resume mechanisms are implemented instead of an interrupt controller.

The microcontroller incorporates the following basic SFRs: Accumulator (ACC), Register B (B) and Program Status Word (PSW) are bit addressable registers used to perform arithmetical and logical operations. The Stack Pointer (SP) and Data Pointer (DPTR) are included to allow basic programming structures. The Data Pointer (DPTR) is determined by SFR DPH and SFR DPL.

SFR PSW holds the status of basic arithmetic operations.

Accumulator

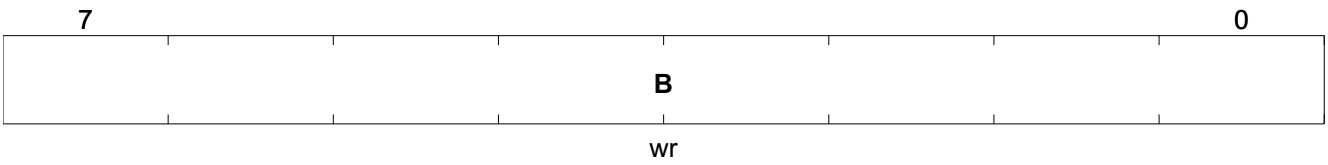
ACC	Offset	Wakeup Value	Reset Value
Accumulator	**$E0_H$**	**00_H**	**00_H**



Field	Bits	Type	Description
ACC	7:0	wr	**Accumulator** Reset: 00_H

Register B

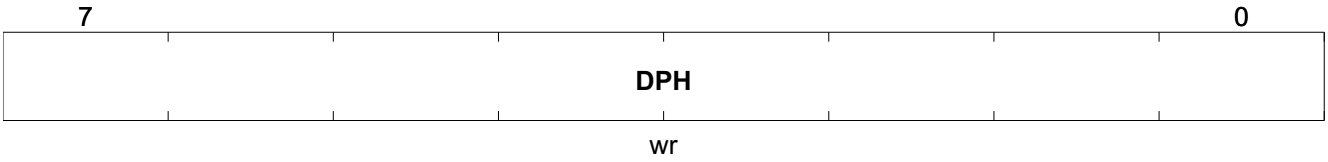
B	Offset	Wakeup Value	Reset Value
Register B	**$F0_H$**	**00_H**	**00_H**



Field	Bits	Type	Description
B	7:0	wr	**Register B 7-0** Reset: 00_H

Data Pointer (high)

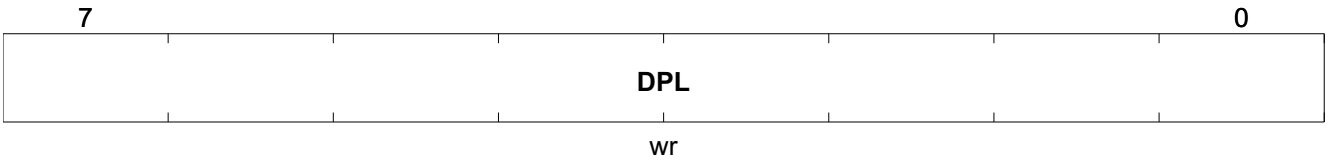
DPH	Offset	Wakeup Value	Reset Value
Data Pointer (high)	**83_H**	**00_H**	**00_H**



Field	Bits	Type	Description
DPH	7:0	wr	**Data Pointer (high)** Reset: 00_H

Data Pointer (low)

DPL	Offset	Wakeup Value	Reset Value
Data Pointer (low)	**82_H**	**00_H**	**00_H**



Field	Bits	Type	Description
DPL	7:0	wr	**Data Pointer (low)** Reset: 00_H

Program Status Word

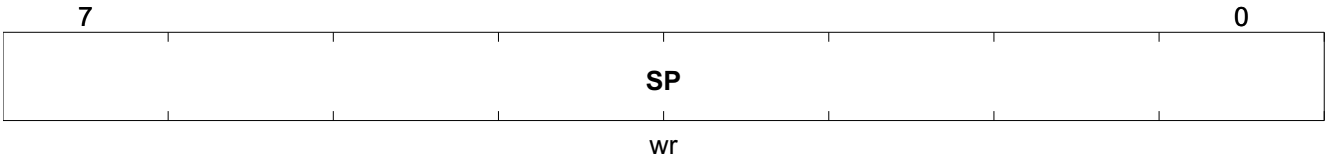
PSW	Offset	Wakeup Value	Reset Value
Program Status Word	**$D0_H$**	**00_H**	**00_H**

7	6	5	4	3	2	1	0
CY	**AC**	**F0**	**RS**		**OV**	**F1**	**P**
wr	wr	wr	wr		wr	wr	r

Field	Bits	Type	Description
CY	7	wr	**Carry** Reset: 0_H
AC	6	wr	**Auxiliary Carry** Carry-out for BCD operations Reset: 0_H
F0	5	wr	**Flag 0** Available for general purpose use. Reset: 0_H
RS	4:3	wr	**Register Bank Select** 00_B Bank 0 (00_H - 07_H) 01_B Bank 1(08_H - $0F_H$) 10_B Bank 2(10_H - 17_H) 11_B Bank 3(18_H - $1F_H$) Reset: 0_H
OV	2	wr	**Overflow** Reset: 0_H
F1	1	wr	**Flag 1** Available for general purpose use. Reset: 0_H
P	0	r	**Parity** Set or cleared each instruction cycle to indicate an odd or even number of 1 bits in the accumulator Reset: 0_H

Stack Pointer

SP	Offset	Wakeup Value	Reset Value
Stack Pointer	81_H	07_H	07_H



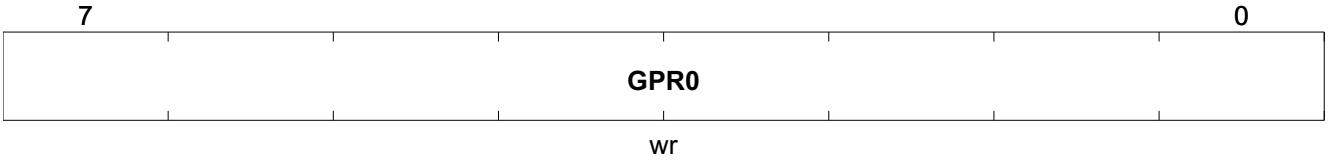
Field	Bits	Type	Description
SP	7:0	wr	**Stack Pointer (SP)** SP is incremented before data is pushed and decremented after data is popped. SP always points to the last valid stack byte. Reset: 07_H

3.2 General Purpose Registers

The SP37T incorporates 16 general purpose registers that can be used by the application to store data beyond a POWER DOWN state / THERMAL SHUTDOWN state period. The GPR Registers are not cleared after a System Reset. After a Power On Reset, the GPR contents will be undefined.

General Purpose Register 0

GPR0	Offset	Wakeup Value	Reset Value
General Purpose Register 0	$B8_H$	UU_H	XX_H



Field	Bits	Type	Description
GPR0	7:0	wr	**General Purpose** Reset: XX_H

General Purpose Registers 0 - F are freely available for application program use. GPR0, GPR1, GPR2 are located at Offset Addresses that make them well suited for bit manipulation. Placing bit variables in these GPRs will result in more efficient CPU operation.

Table 8 Register 0 to F[1)]

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Reset Value
GPR0	General Purpose Register 0	$B8_H$	UU_H	XX_H
GPR1	General Purpose Register 1	$B0_H$	UU_H	XX_H
GPR2	General Purpose Register 2	$A8_H$	UU_H	XX_H
GPR3	General Purpose Register 3	$F1_H$	UU_H	XX_H
GPR4	General Purpose Register 4	$F2_H$	UU_H	XX_H
GPR5	General Purpose Register 5	$F3_H$	UU_H	XX_H
GPR6	General Purpose Register 6	$F5_H$	UU_H	XX_H
GPR7	General Purpose Register 7	$F6_H$	UU_H	XX_H
GPR8	General Purpose Register 8	$F7_H$	UU_H	XX_H
GPR9	General Purpose Register 9	$F9_H$	UU_H	XX_H
GPRA	General Purpose Register 10	FA_H	UU_H	XX_H
GPRB	General Purpose Register 11	FB_H	UU_H	XX_H
GPRC	General Purpose Register 12	FC_H	UU_H	XX_H
GPRD	General Purpose Register 13	FD_H	UU_H	XX_H

Table 8 Register 0 to F[1)] (cont'd)

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Reset Value
GPRE	General Purpose Register 14	FE_H	UU_H	XX_H
GPRF	General Purpose Register 15	FF_H	UU_H	XX_H

1) Reset Value for GRP0 - GPRF is typically undefined (X) except in the case of Software Reset, which leaves the GPR content unchanged (U).

3.3 System Configuration Registers

The system configuration registers can be used for:

- Initiating state transitions (SFR CFG0)
- Enabling or disabling peripherals (SFR CFG1 and SFR CFG2)
- Monitoring the operation mode, the system state and peripherals (SFR DSR)

Configuration Register 0

CFG0	Offset	Wakeup Value	Reset Value
Configuration Register 0	**$F8_H$**	**$0000U000_B$**	**00_H**

7	6	5	4	3	2	1	0
PDWN	**TSHDWN**	**IDLE**	**ENXOSC**	**FTM**	Res	**UNUSED**	Res
wr	wr	wr	wr	wr		-	

Field	Bits	Type	Description
PDWN	7	wr	**Enter POWER DOWN State** If set to 1 by software the POWER DOWN state is entered; This bit is automatically reset to 0 by the system controller after a wakeup. Entering POWER DOWN state is handled by a ROM Library function. It is not recommended to set this bit manually. Reset: 0_H
TSHDWN	6	wr	**Enter THERMAL SHUTDOWN State** If set to 1 by software the THERMAL SHUTDOWN state is entered; This bit is automatically reset to 0 by the system controller after wakeup. Entering THERMAL SHUTDOWN state is handled by a ROM Library function. It is not recommended to set this bit manually. Reset: 0_H
IDLE	5	wr	**Enter IDLE State** If set to 1 by software the IDLE state is entered; This bit is automatically reset to 0 by the system controller after a resume event occurs. Reset: 0_H
ENXOSC	4	wr	**Enable XTAL Oscillator** Control of XTAL oscillator enable is handled by a ROM Library function. It is not recommended to change this bit manually. 0_B XTAL oscillator disable 1_B XTAL oscillator enable Reset: 0_H
FTM	3	wr	**Enable Functional Test Mode** This mode is used only during internal device testing. 0_B FTM disabled 1_B FTM enable Reset: 0_H

Field	Bits	Type	Description
Res	2		**Reserved** This bit must be set to 0_B. Reset: 0_H
UNUSED	1	-	**UNUSED** Reset: 0_H
Res	0		**Reserved** This bit must be set to 0_B. Reset: 0_H

Configuration Register 1

CFG1	Offset	Wakeup Value	Reset Value
Configuration Register 1	**$E8_H$**	**$000U000U_B$**	**00_H**

7	6	5	4	3	2	1	0
Res	**I2CEN**	**RNGEN**	**RFTXPEN**	Res	**ITRD**	**ITINIT**	**ITEN**
	wr	wc	wr		wr	r	wr

Field	Bits	Type	Description
Res	7		**Reserved** This bit must be set to 0_B. Reset: 0_H
I2CEN	6	wr	**I2C Enable** 0_B Standard I/O Port functionality 1_B I2C functionality on Pins PP0/SCL and PP1/SDA Reset: 0_H
RNGEN	5	wc	**Random Number Generator Enable** 0_B Cleared automatically after random number is generated 1_B Initiates generation of a new pseudo random number Reset: 0_H
RFTXPEN	4	wr	**Transmitter Data Port Output Enable** If this bit is set the RF transmission baseband data is made available on PP2, and the RF Manchester/BiPhase Encoder does not turn on the PA. If RF transmission in parallel with PP2 mirroring is desired , the PA must be enabled by the application prior to RF transmission (RFC.0 = 1). 0_B Standard I/O Port functionality 1_B Echoes RF transmission baseband data on port PP2/TXData Reset: 0_H
Res	3		**Reserved** This bit must be set to 0_B. Reset: 0_H

Field	Bits	Type	Description
ITRD	2	wr	**Interval Timer Read Enable** To safely read SFR ITPR, this bit should be set to 1 prior to reading ITPR. After the ITPR contents are read, this bit should be checked. 0_B SFR ITPR read result is not valid 1_B SFR ITPR read result is valid Reset: 0_H
ITINIT	1	r	**Interval Timer Initialization** When the wakeup interval is changed by programming ITPR, ITPL or ITPH with a new value, this bit is set to 1 until the new value has taken effect. The application should not leave RUN state while this bit is 1 otherwise the ITPR setting does not take effect. This bit is automatically cleared after initialization is complete. 0_B Interval Timer Initialization complete 1_B Interval Timer Initialization in progress Reset: 0_H
ITEN	0	wr	**Interval Timer Enable** Interval Timer is always enabled in NORMAL mode, setting or clearing ITEN bit has no effect. 0_B Disable Interval Timer (TEST/DEBUG mode only) 1_B Enable Interval Timer Reset: 0_H

Configuration Register 2

CFG2	Offset	Wakeup Value	Reset Value
Configuration Register 2	**$D8_H$**	**$000U1000_B$**	**18_H**

7	6	5	4	3	2	1	0
UNUSED	**I2CGCEN**	**UNUSED**	**PDLMB**	Res	**UNUSED**	**WDRES**	**RESET**
-	wr	-	wr		-	wc	wc

Field	Bits	Type	Description
UNUSED	7	-	**UNUSED** Reset: 0_H
I2CGCEN	6	wr	**I2C General Call Enable** 0_B Disabled 1_B Enabled Reset: 0_H
UNUSED	5	-	**UNUSED** Reset: 0_H

Field	Bits	Type	Description
PDLMB	4	wr	**Lower RAM Memory Block (00_H-$7F_H$) Power Control** 0_B Lower RAM retains power in POWER DOWN and THERMAL SHUTDOWN states 1_B Lower RAM is not powered in POWER DOWN and THERMAL SHUTDOWN states Reset: 1_H
Res	3		**Reserved** This bit must be set to 1_B. Reset: 1_H
UNUSED	2	-	**UNUSED** Reset: 0_H
WDRES	1	wc	**Reset Watchdog Counter** 0_B Cleared automatically after reset of watchdog counter 1_B Watchdog counter is reset Reset: 0_H
RESET	0	wc	**System Reset** 0_B Cleared automatically after software reset is performed 1_B A software reset is performed Reset: 0_H

Diagnosis and Status Register

DSR	Offset	Wakeup Value	Reset Value
Diagnosis and Status Register	$D9_H$	$0XUU00XU_B$	$0XXX0000_B$

7	6	5	4	3	2	1	0
Res	**TGOOD**	**OPMODE**		Res		**WUPEND**	Res
	r	r				r	

Field	Bits	Type	Description
Res	7		**Reserved** This bit must be set to 0_B. Reset: 0_H
TGOOD	6	r	**TMAX Detector Status** Entering THERMAL SHUTDOWN state is handled by a ROM Library function. 0_B Temperature > TMAX 1_B Temperature < TMAX Reset: X_B
OPMODE	5:4	r	**Operating Mode** 00_B TEST Mode 01_B DEBUG Mode 10_B PROGRAMMING Mode 11_B NORMAL Mode Reset: XX_B
Res	3:2		**Reserved** These bits must be set to 00_B. Reset: 0_H
WUPEND	1	r	**Wakeup Pending in SFR WUF** 0_B SFR WUF contents have not changed since the last read 1_B SFR WUF contents have changed since the last read Reset: 0_H
Res	0		**Reserved** This bit must be set to 0_B. Reset: 0_H

3.4 System Controller

While the microcontroller controls the SP37T in RUN state, the system controller takes over control in POWER DOWN state, IDLE state and THERMAL SHUTDOWN state.

The system controller handles wakeup / resume events and system resets. It is clocked by the 2kHz RC LP Oscillator.

Difference between System Reset and Wakeup:

- **System Reset** - The digital circuit is reset. Program execution starts at address 0000_H to perform reset initialization routines (including operation mode selection) and will jump to the FLASH at address 4000_H to execute the application program.
- **Wakeup** - Only the program counter of the microcontroller and its peripheral units are reset. Program Execution starts at address 0000_H to perform wakeup initialization routines and jumps to the FLASH at 4000_H to execute the application program.

Wakeup Event Handling

Whenever a wakeup occurs, the SP37T leaves POWER DOWN state and enters RUN state to execute the application program. This transition can be initiated from various sources. The wakeup source can be identified by reading SFR WUF.

The wakeup sources can be enabled or disabled by setting the appropriate bits in SFR WUM. The bits WDOG, TMAX and ITIM are always enabled. Setting these bits have no effect in NORMAL/DEBUG modes.

The bits in SFR WUF are cleared upon read (read-clear). If subsequent wakeup source activity is detected, the SFR DSR.WUPEND bit and the corresponding SFR WUF bit(s) will be set. Note that wakeup sources that have a mask bit set (disabled) in SFR WUM will always be cleared (inactive) in SFR WUF.

The SFR WUF is not automatically cleared when entering the POWER DOWN state. For this reason it is a good practice to have the application software read WUF and handle any pending wakeup events before entering POWER DOWN. Otherwise, any flags in SFR WUF will remain marked as pending upon the next device wakeup. Note that only new wakeup source activity, occurring after entering POWER DOWN, will cause a device wakeup to occur.

Watchdog Wakeup

A watchdog wakeup occurs after the watchdog timer has elapsed.
See **“Watchdog Timer” on Page 24** for details about the watchdog timer.

TMAX Wakeup

A TMAX wakeup occurs only if the device was in THERMAL SHUTDOWN state and the temperature falls below the threshold release temperature T_{REL}.
See **“TMAX Detector” on Page 24** for details about the TMAX wakeup.

LF Receiver Wakeup Event

The LF Receiver wakeup can be enabled by setting one of following bits:

- SFR bit WUM.5 [LFCD] or
- SFR bit WUM.4 [LFSY] or
- SFR bit WUM.3[LFPM1] and/or SFR bitWUM.2 [LFPM0]

The wakeup source can be read in the SFR WUF.

The LF Receiver has to be configured appropriate for the particular wakeup modes. See **“LF Receiver” on Page 74** for details.

External PP2 Wakeup Event

I/O Port PP2 can be configured to wakeup the SP37T from POWER DOWN state by an external source.

PP2 has to be configured according to **“External Wakeup on PP2” on Page 118** for this feature.

Interval Timer Wakeup Event

When the Interval Timer elapses, a wakeup event is generated and POWER DOWN state is left. The wakeup can be identified by the application software reading SFR bit WUF.0[ITIM].
The Interval Timer is reloaded automatically with the actual value from SFR ITPR and immediately restarted. The Interval Timer is also counting during RUN state which leads to accurate wakeup intervals even if RUN state periods vary in execution time.

Wakeup Flag Register

WUF	Offset	Wakeup Value	Reset Value
Wakeup Flag Register	$C0_H$	XX_H	00_H

7	6	5	4	3	2	1	0
WDOG_FLAG	TMAX_FLAG	LFCD_FLAG	LFSY_FLAG	LFPM1_FLAG	LFPM0_FLAG	EXT_FLAG	ITIM_FLAG
rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
WDOG_FLAG	7	rc	**Watchdog Wakeup** Reset: 0_H
TMAX_FLAG	6	rc	**Thermal Shutdown (TMAX) Release Wakeup** Reset: 0_H
LFCD_FLAG	5	rc	**LF Carrier Wakeup** Reset: 0_H
LFSY_FLAG	4	rc	**LF Sync Match Wakeup** Reset: 0_H
LFPM1_FLAG	3	rc	**LF Pattern 1 Match Wakeup** Reset: 0_H
LFPM0_FLAG	2	rc	**LF Pattern 0 Match Wakeup** Reset: 0_H
EXT_FLAG	1	rc	**I/O-Port PP2 External Wakeup** Reset: 0_H
ITIM_FLAG	0	rc	**Interval Timer Wakeup** Reset: 0_H

Wakeup Mask Register

WUM	Offset	Wakeup Value	Reset Value
Wakeup Mask Register	$C1_H$	UU_H	FF_H

7	6	5	4	3	2	1	0
WDOG_MASK	TMAX_MASK	LFCD_MASK	LFSY_MASK	LFPM1_MASK	LFPM0_MASK	EXT_MASK	ITIM_MASK
wr	wr	wr	wr	wr	wr	wr	wr

Field	Bits	Type	Description
WDOG_MASK	7	wr	**Disable Watchdog Reset** Watchdog is always enabled, setting this bit has no effect in NORMAL/DEBUG modes. Reset: 1_H
TMAX_MASK	6	wr	**Disable Thermal Shutdown (TMAX) Release Wakeup** TMAX Wakeup is handled by ROM Library Functions, setting this bit has no effect in NORMAL/DEBUG modes. Reset: 1_H
LFCD_MASK	5	wr	**Disable LF Carrier Wakeup** 0_B Enable LF Carrier wakeup 1_B Disable LF Carrier wakeup Reset: 1_H
LFSY_MASK	4	wr	**Disable LF Sync Match Wakeup** 0_B Enable LF Sync Match wakeup 1_B Disable LF Sync Match wakeup Reset: 1_H
LFPM1_MASK	3	wr	**Disable LF Pattern 1 Match Wakeup** 0_B Enable LF Pattern 1 Match wakeup 1_B Disable LF Pattern 1 Match wakeup Reset: 1_H
LFPM0_MASK	2	wr	**Disable LF Pattern 0 Match Wakeup** 0_B Enable LF Pattern 0 Match wakeup 1_B Disable LF Pattern 0 Match wakeup Reset: 1_H
EXT_MASK	1	wr	**Disable I/O-Port PP2 External Wakeup** 0_B Enable I/O-Port PP2 wakeup 1_B Disable I/O-Port PP2 wakeup Reset: 1_H
ITIM_MASK	0	wr	**Disable Interval Timer Wakeup** Interval Timer Wakeup is always enabled in NORMAL mode, setting this bit has no effect in NORMAL/DEBUG modes. Reset: 1_H

Resume Event Flag Register

Note: SFR DIVIC must be 00b in order to reliably read SFR REF

REF	Offset	Wakeup Value	Reset Value
Resume Event Flag Register	**$D1_H$**	**00_H**	**00_H**

7	6	5	4	3	2	1	0
UNUSED		**READC**	**RELFO**	**RERFF**	**RERFU**	**UNUSED**	**RET0**
-		rc	rc	rc	rc	-	rc

Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
READC	5	rc	**A/D Conversion complete** This bit is for use by ROM Library functions. Reset: 0_H
RELFO	4	rc	**LF Receive Buffer full** Data can be read by the application software. Reset: 0_H
RERFF	3	rc	**RF Transmission complete** All bits in the transmitter shift register have been transmitted. Reset: 0_H
RERFU	2	rc	**RF Transmit Buffer empty** Next byte to be transmitted may be loaded to SFR RFD. Reset: 0_H
UNUSED	1	-	**UNUSED** Reset: 0_H
RET0	0	rc	**Timer 0 Underflow** Reset: 0_H

3.5 Interval Timer

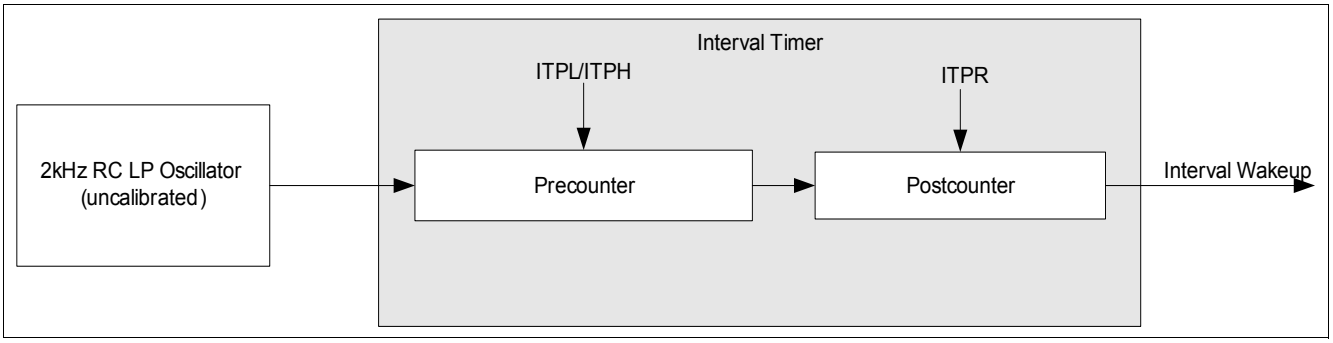


Figure 9 Interval Timer Block Diagram

The Interval Timer is responsible to wakeup the SP37T from the POWER DOWN state after a predefined time interval. It is clocked by the 2kHz RC LP Oscillator and incorporates two dividers:

- Precounter: can be calibrated and represents the timebase; please refer to **"Interval Timer Precounter / Calibration" on Page 53**
- Postcounter: configures the Interval Timer duration in multiples of the timebase.

The Precounter (ITPH/L) is a 16 bit register with 12 significant bits. The precounter values 0001_H up to $0FFF_H$ corresponds to 1_{dec} up to 4095_{dec}. The maximum precounter value 0000_H corresponds to 4096_D.

To increase the timer accuracy, it is recommended to use a ROM library function which calibrates the precounter dependent on the actual frequency of the 2kHz RC LP Oscillator. See **[1]** for details.

The Postcounter (ITPR) is an 8 bit register. 01_H up to FF_H corresponds to a multiplication of the timebase with 1_{dec} up to 255_{dec}. The maximum postcounter value 00_H corresponds to 256_D.

The Interval Timer duration is determined by the SFR ITPR. The desired value can be calculated by using the following equation

$$Intervaltimerperiod[s] = timebase[s] \bullet postcounter[ITPR] \quad (1)$$

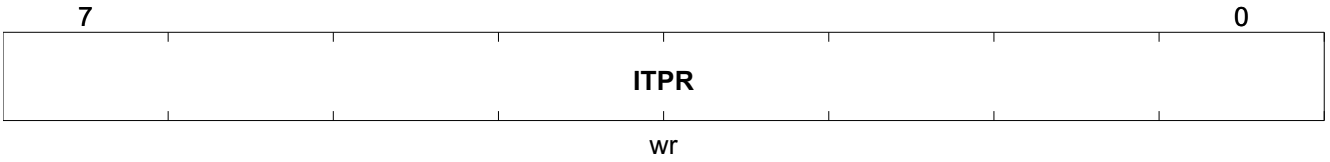
$$timebase[s] = \frac{precounter[ITPL/H]}{f_{2kHzRCLPOscillator}\left[\frac{1}{s}\right]} \quad (2)$$

Writing to the Postcounter (ITPR) establishes the counter reload value.

Reading from the Postcounter (ITPR) returns the counter value, not the counter reload value. The Interval Timer is asynchronous from the CPU, so care must be taken when reading its contents. To safely read the ITPR, the SFR CFG1 ITRd bit should be set to one prior to reading ITPR. After the ITPR contents are read, the SFR CFG1 ITRd bit should be checked: If the ITPR read result is valid, the SFR CFG ITRd bit will still be set. If the SFR CFG1 ITRd bit is cleared during ITPR read, the ITPR read result is not valid.

Interval Timer Period Register

ITPR	Offset	Wakeup Value	Reset Value
Interval Timer Period Register	BC_H	UU_H	01_H



Field	Bits	Type	Description
ITPR	7:0	wr	**Interval Timer Period Register** To safely read ITPR, SFR CFG1.2 should be set to 1 prior to reading ITPR. If the ITPR read was successful, SFR CFG1.2 will remain set to 1. Reset: 01_H

3.6 Interval Timer Precounter / Calibration

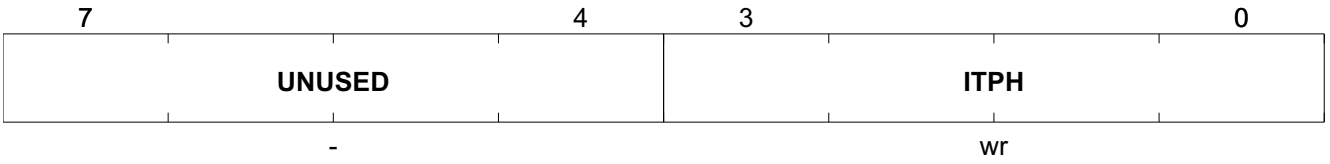
Calibration is done by counting clock cycles from the crystal oscillator during one 2kHz RC LP Oscillator period. In the case that the crystal oscillator is not available (not running), the 12 MHz RC HF Oscillator is used instead. The calibration is performed automatically by a ROM library function (see **[1]**).

Notes

1. *SFR ITPL and SFR ITPH can be modified manually for using other (uncalibrated) precounter values than the ones determined by the ROM Library function.*
2. *After writing SFR ITPR, SFR ITPL or SFR ITPH some time is needed to activate the new setting. SFR bit CFG1.1[ITInit] is cleared automatically when the new setting takes effect.*
3. *Reading SFR ITPL or SFR ITPH returns the low byte or the high byte of the Precounter reload value, respectively.*

Interval Timer Precounter Register (High Byte)

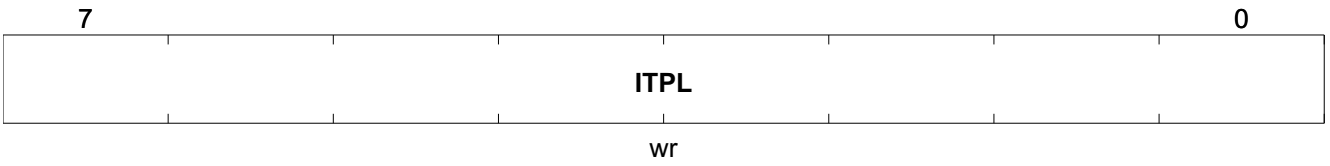
ITPH	Offset	Wakeup Value	Reset Value
Interval Timer Precounter Register (High Byte)	**BB_H**	**$0000UUUU_B$**	**03_H**



Field	Bits	Type	Description
UNUSED	7:4	-	**UNUSED** Reset: 0_H
ITPH	3:0	wr	**Interval Timer Precounter Register (High Byte)** Reset: 3_H

Interval Timer Precounter Register (Low Byte)

ITPL	Offset	Wakeup Value	Reset Value
Interval Timer Precounter Register (Low Byte)	BA_H	UU_H	$E8_H$



Field	Bits	Type	Description
ITPL	7:0	wr	**Interval Timer Precounter Register (Low Byte);** Reset: $E8_H$

3.7 Clock Controller

The Clock Controller for internal clock management is part of the system controller.

In SP37T the microcontroller (CPU) clock source is always based on the 12 MHz RC HF Oscillator (system clock). to provide minimum current consumption. The internal clock divider (SFR DIVIC) may be used to slow down the speed of the microcontroller and to reduce the current consumption further. The crystal is used as clock source for the RF Transmitter and for the Timer Unit (e.g. for oscillator calibrations). The start up of the crystal (e.g. for RF Transmission) can be performed automatically by a ROM library function (see **[1]**). **Figure 10** shows the clocking scheme for the different SP37T blocks.

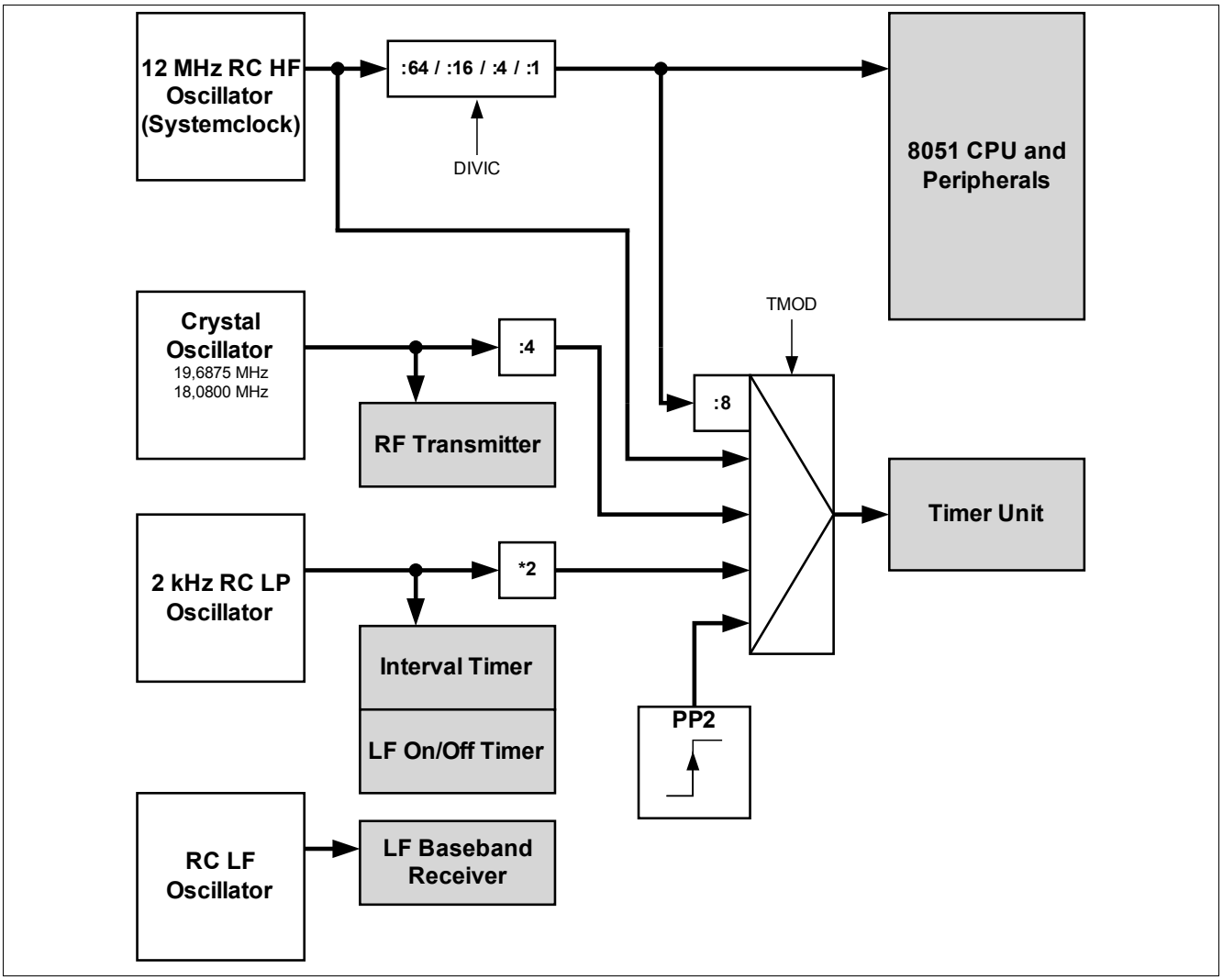


Figure 10 SP37T Clock Concept

2kHz RC LP Oscillator (Low Power)

The 2 kHz RC LP Oscillator stays active throughout all operating states except THERMAL SHUTDOWN state. The typical oscillator frequency is 2kHz. Characteristics can be found in **Table 44 “2 kHz RC LP Oscillator” on Page 161**.

12MHz RC HF Oscillator (High Frequency)

The 12 MHz RC HF Oscillator runs at typical 12 MHz and is used as system clock for the SP37T in RUN state. Characteristics can be found in **Table 43 “12 MHz RC HF Oscillator” on Page 161**.

Crystal Oscillator

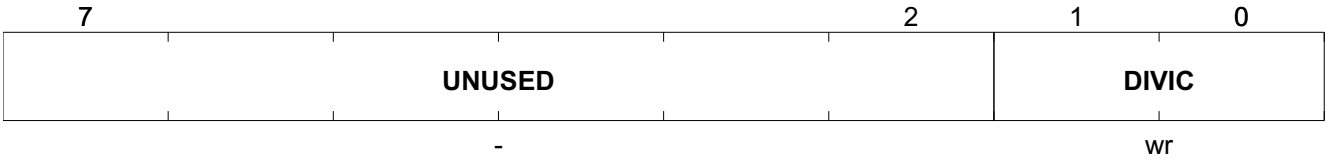
The crystal oscillator is a Negative Impedance Converter (NIC) oscillator with a crystal operating in series resonance. Characteristics can be found in **Table 42 “Crystal Oscillator, fCrystal = 18 MHz...20 MHz” on Page 160**.

RC LF Oscillator

The RC LF Oscillator is part of the LF Receiver and only used as clock for the LF Receiver Baseband.

Internal Clock Divider

DIVIC	Offset	Wakeup Value	Reset Value
Internal Clock Divider	**$B9_H$**	**$000000UU_B$**	**00_H**



Field	Bits	Type	Description
UNUSED	7:2	-	**UNUSED** Reset: 00_H
DIVIC	1:0	wr	**SystemClock Divider** 00_B Duvide by 1 01_B Divide by 4 10_B Divide by 16 11_B Divide by 64 Reset: 0_H

3.8 Crystal Pulling

To achieve FSK transmission, the reference frequency of the NIC crystal oscillator is detuned by switching between two different capacitances (one for the low and one for the high FSK frequency). These capacitance values are achieved with embedded switchable capacitors and/or with external capacitors, mounted in series to the crystal. For ASK transmission, the capacitance can be used to tune the center frequency.

The SP37T offers the possibility to use either internal capacitors and/or external capacitors for pulling the crystal frequency. This is determined by the SFR bit RFTX.FSKSWITCH.

*Note: $C_{parasitic}$ used in **Figure 11**, **Figure 13** and **Figure 14** is the overall parasitic capacitance between the pins XGND an XCAP (switch, bond wires, pad parasitics,...). The formulas for calculating the resulting capacitance for ASK/FSK (C_{ASK}, $C_{FSKHIGH}$, C_{FSKLOW}) only take into account the dominating factor of $C_{Switch, OFF}$.. Specification for the parasitic capacitance can be found in **Table 42 "Crystal Oscillator, fCrystal = 18 MHz...20 MHz" on Page 160**.*

The following pages show the configurations for ASK/FSK using internal or external capacitors.

FSK with internal capacitors

- In the configuration shown in **Figure 11** the internal capacitors are used. The desired capacitor values must be selected by using SFR XTAL1 and SFR XTAL0. The exact values used should be verified by module level testing.
- During FSK transmission the output of the Manchester/Biphase Encoder determines which capacitor value is used. The capacitor value in SFR XTAL0 is applied when the output of the Manchester/Bi-phase Encoder is 0; SFR XTAL1 is applied when the output is 1.

Note: SFR bit RFTX.FSKSWITCH must be set to 0 for this configuration

$$C_{FSKHIGH} \cong C_{XTAL1} + C_{Switch,OFF} \quad (3)$$

$$C_{FSKLOW} \cong C_{XTAL0} + C_{Switch,OFF} \quad (4)$$

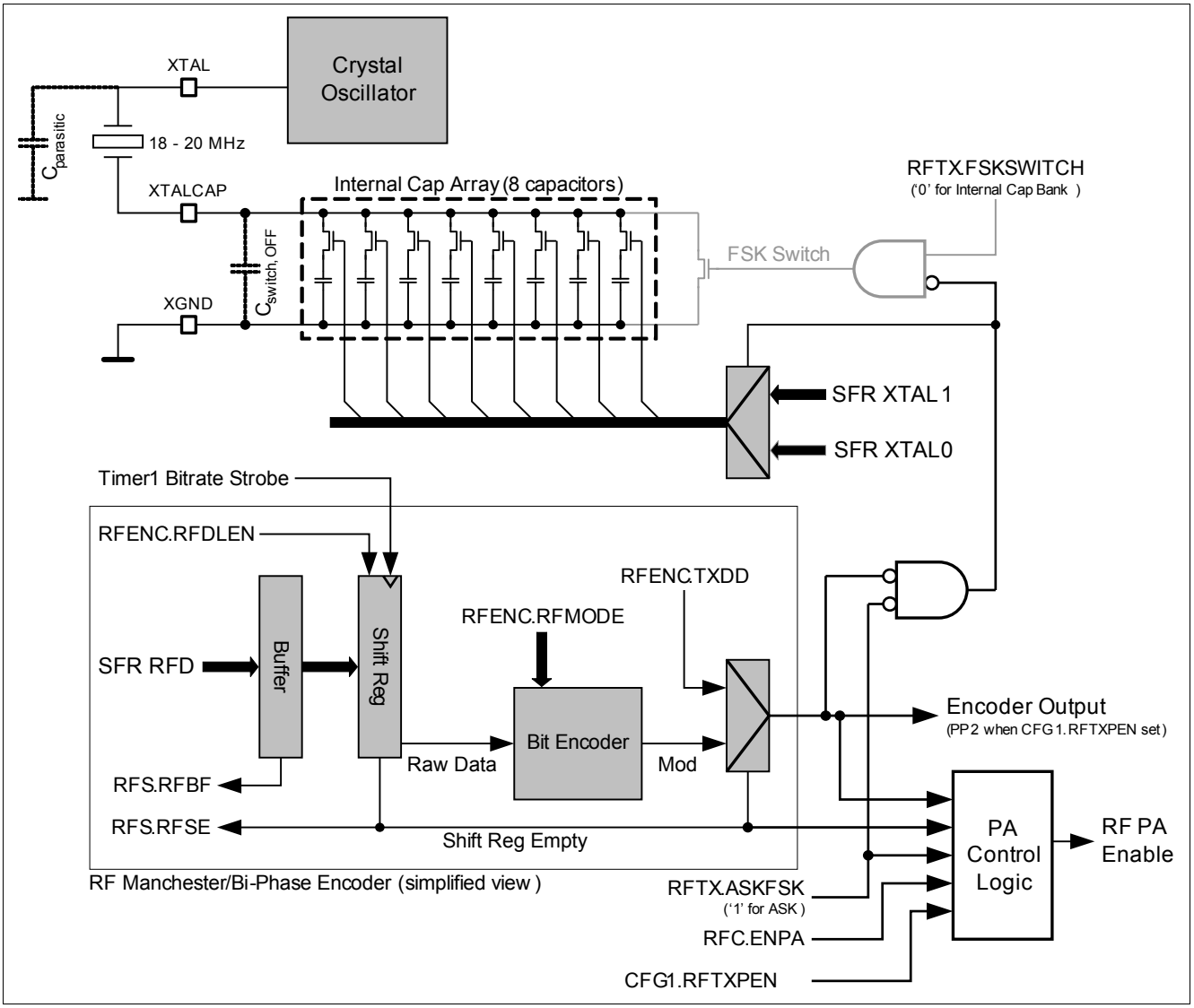


Figure 11 FSK using the internal capacitors

ASK with internal capacitor

- In the configuration shown in **Figure 12** the internal capacitor array is used. The desired capacitor value must be selected by using SFR XTAL1 to establish the RF carrier frequency. The exact value used should be verified by module level testing.
- During ASK transmission the output of the Manchester/Biphase Encoder controls the RF Power Amplifier. The PA is enabled when the output of the Manchester/Bi-phase Encoder is 1; disabled when the output is 0.

$$C_{ASK} \cong C_{XTAL1} + C_{Switch,OFF} \quad (5)$$

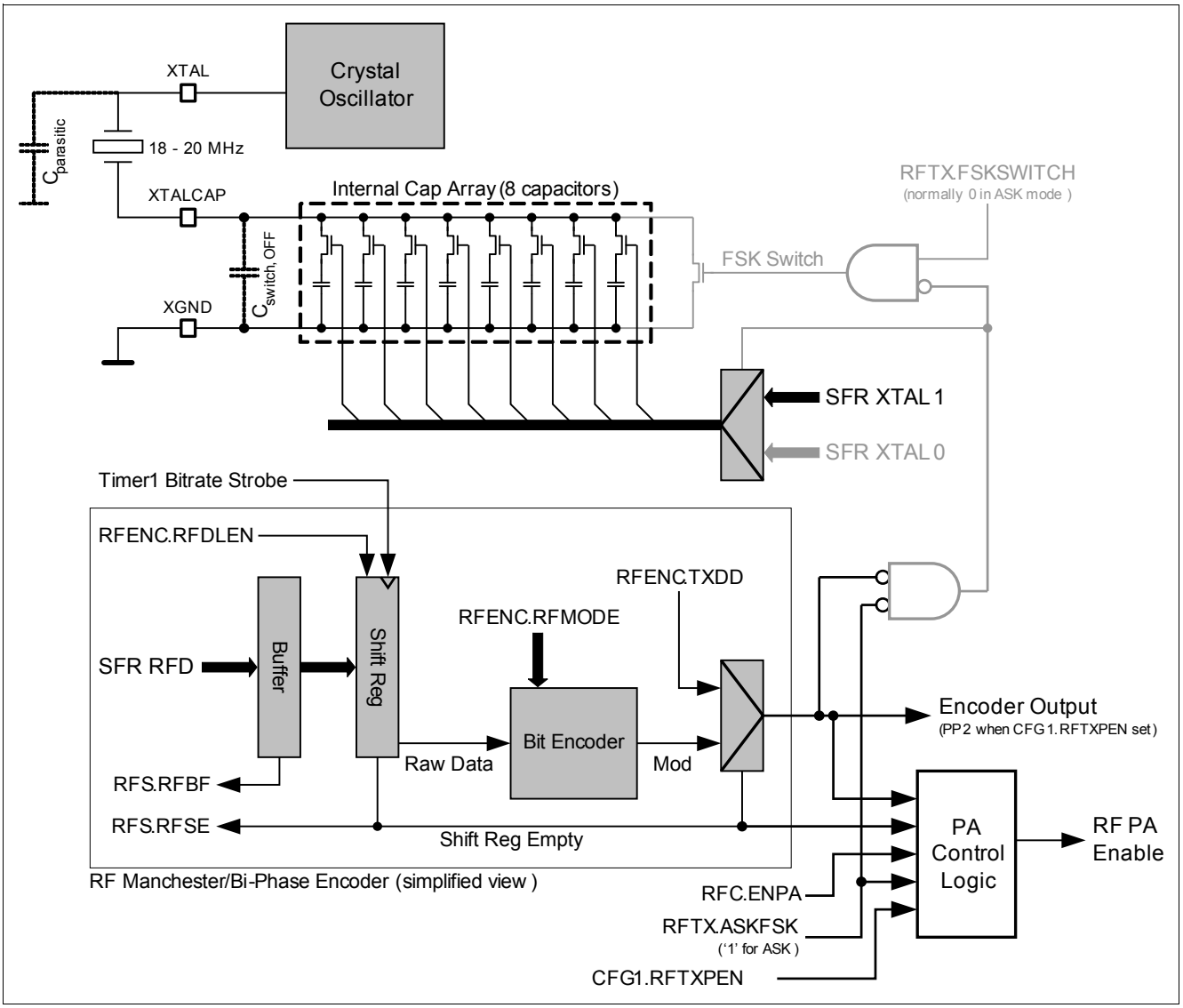


Figure 12 ASK using the internal capacitor

FSK with external capacitors

- In the configuration shown in **Figure 13** the FSK switch is used in conjunction with external capacitors. Guidelines for determining the external capacitor values are **Equation (6)** and **Equation (7)**. The exact values used should be verified by module level testing.
- During FSK transmission the output of the Manchester/Biphase Encoder opens and closes the FSK switch. The FSK switch is closed when the output of the Manchester/Bi-phase Encoder is 0; opened when the output is 1.

Note: SFR bit RFTX.FSKSWITCH must be set to 1 for this configuration

$$C_{FSKHIGH} \cong \frac{C_1 \cdot (C_2 + C_{Switch,OFF})}{C_1 + (C_2 + C_{Switch,OFF})} \quad (6)$$

$$C_{FSKLOW} \cong C_1 \quad (7)$$

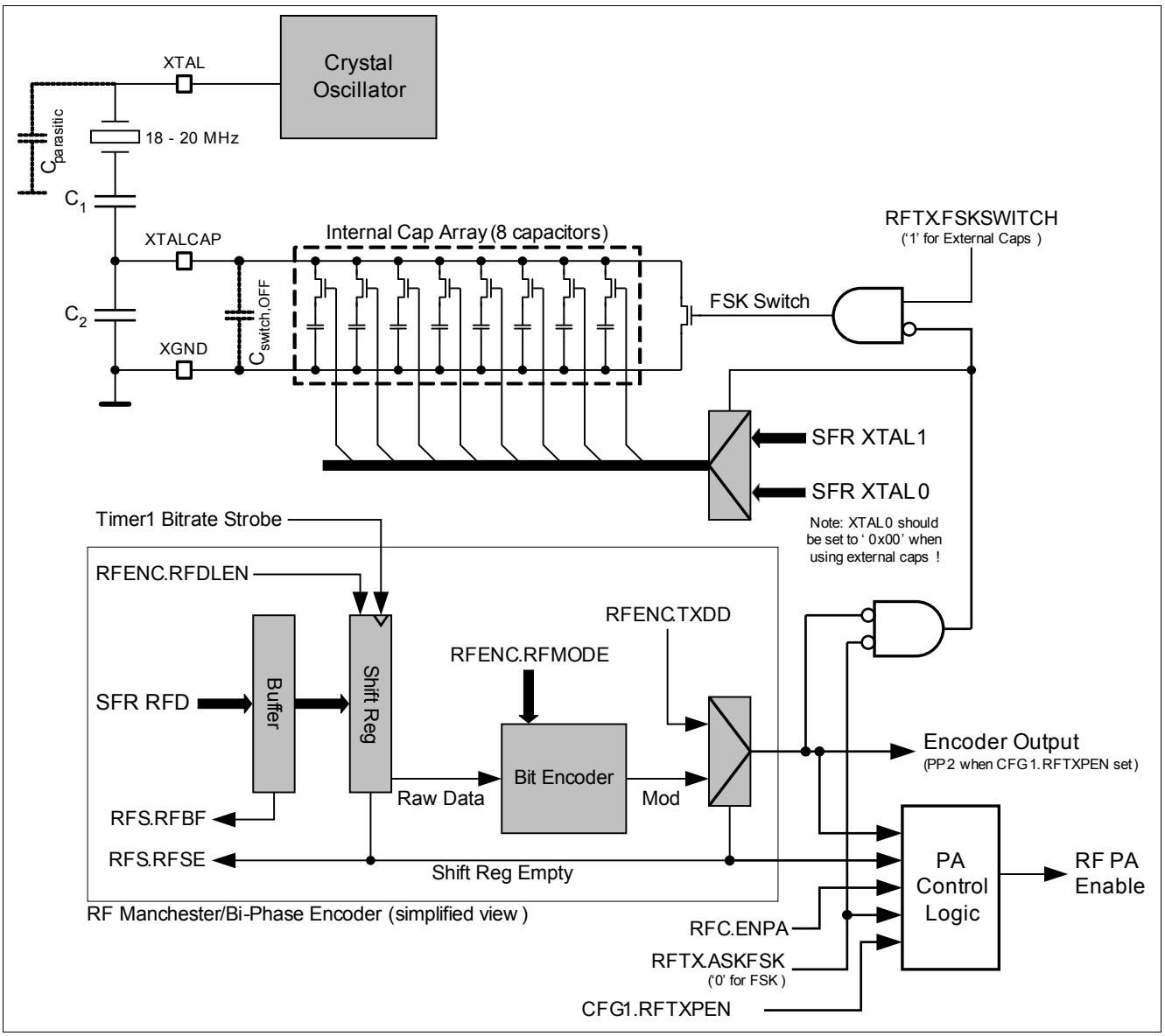


Figure 13 FSK using only external capacitors

ASK with external capacitor

- In the configuration shown in **Figure 14** an external capacitor is used to establish the RF carrier frequency. A guideline for determining the external capacitor value is **Equation (8)**. The exact value used should be verified by module level testing.
- During ASK transmission the output of the Manchester/Biphase Encoder controls the RF Power Amplifier. The PA is enabled when the output of the Manchester/Bi-phase Encoder is 1; disabled when the output is 0.

Note: SFR XTAL1 is typically set to 00_H for this configuration.

$$C_{ASK} \cong C_{XTAL1} + C_{Switch,OFF} + C_1 \quad (8)$$

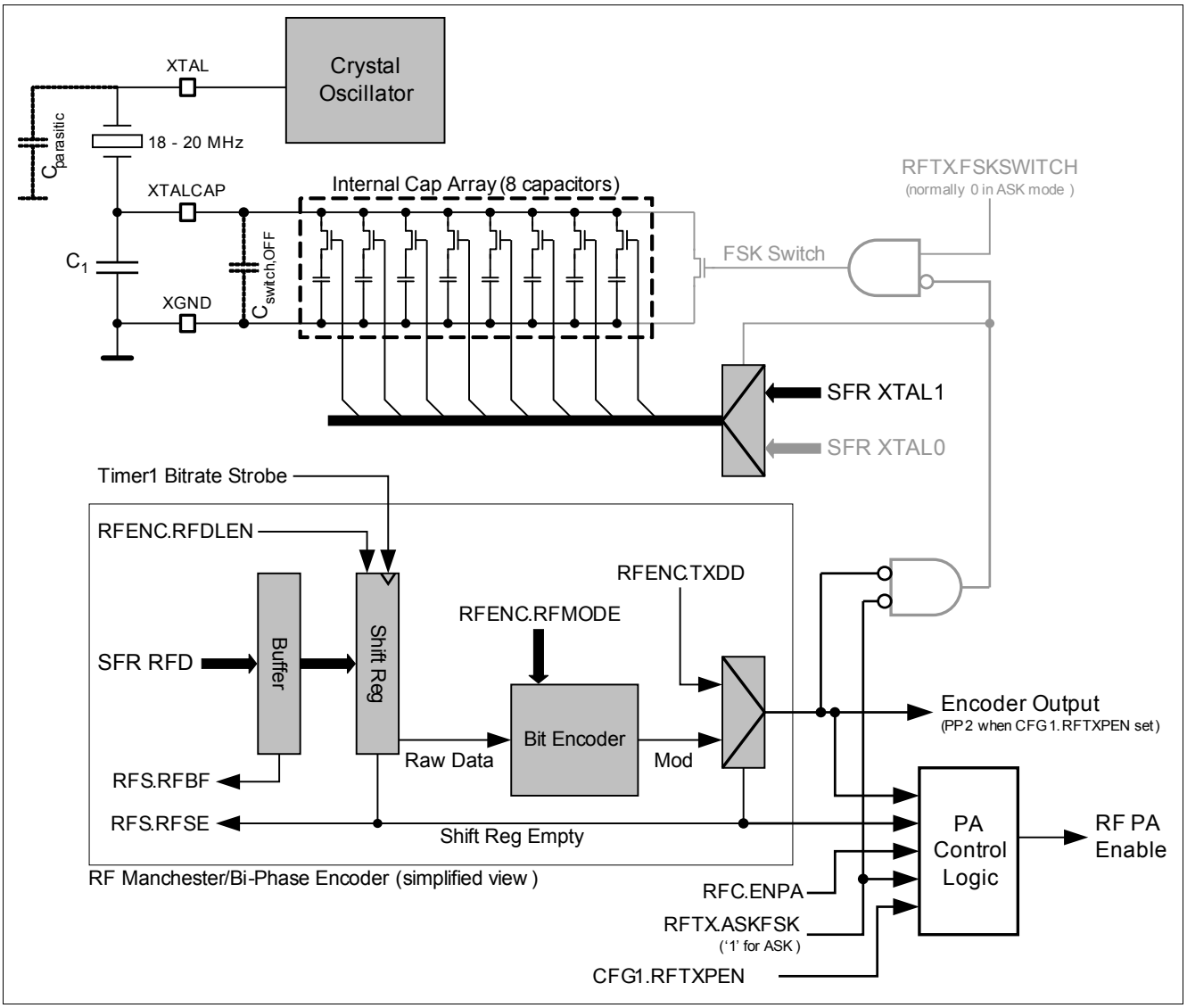
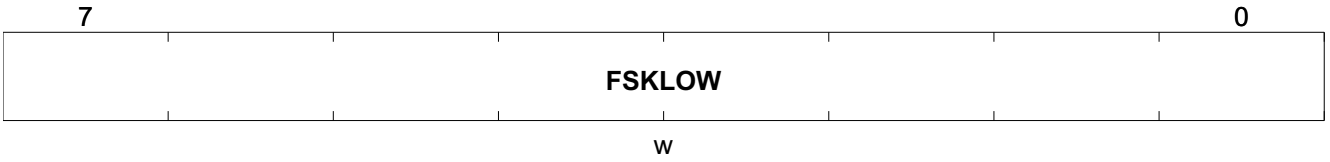


Figure 14 ASK using only an external capacitor

XTAL Frequency Register (FSKLOW)

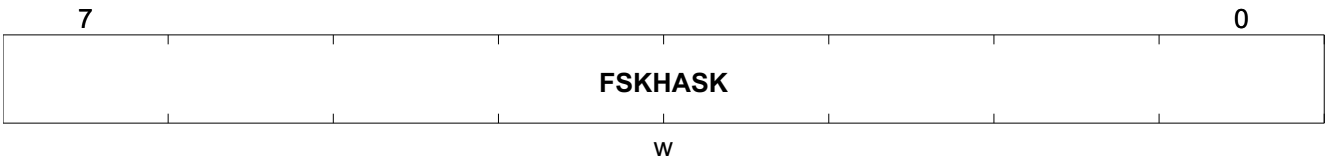
XTAL0	Offset	Wakeup Value	Reset Value
XTAL Frequency Register (FSKLOW)	$C4_H$	UU_H	FF_H



Field	Bits	Type	Description
FSKLOW	7:0	w	**FSK Low Frequency** Pulling/Trimming capacitor select for lower FSK modulation frequency. The capacitor array is binary weighted from 00000001_B: 156fF 00000010_B: 312fF ... 11111111_B: 40pF Reset: FF_H

XTAL Frequency Register (FSKHIGH/ASK)

XTAL1	Offset	Wakeup Value	Reset Value
XTAL Frequency Register (FSKHIGH/ASK)	$C3_H$	UU_H	FF_H



Field	Bits	Type	Description
FSKHASK	7:0	w	**FSK High Frequency / ASK Center Frequency** Pulling/Trimming capacitor select for upper FSK modulation frequency and ASK center frequency. The capacitor array is binary weighted from 00000001_B: 156fF 00000010_B: 312fF ... 11111111_B: 40pF Reset: FF_H

3.9 RF 315/434 MHz FSK/ASK Transmitter

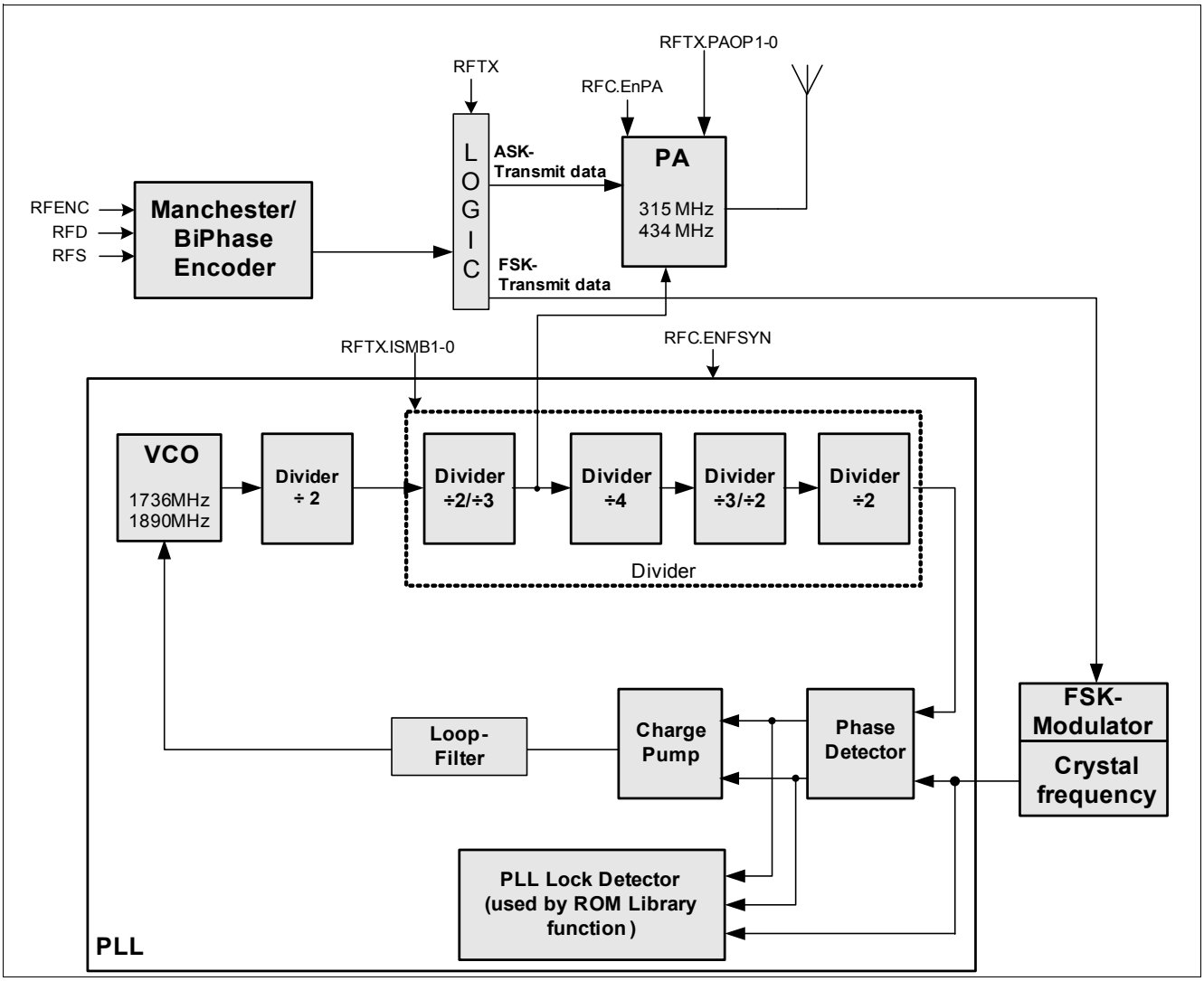


Figure 15 RF Transmitter Block Diagram

The RF-Transmitter can be configured for the 315/434 MHz ISM-Band frequencies by setting SFR bits RFTX.3-2[ISMB1-0] and choosing the proper crystal according to **Table 9** below.

Table 9 Crystal Selection

Center Frequency [MHz]	PLL Divider Factor	Required XTAL Frequency [MHz]
433.92	24	18.0800
315.00	16	19.6875

Voltage Controlled Oscillator (VCO)

The VCO uses on-chip inductors and varactors for tuning. The tuning range VCO is split up into 16 frequency ranges.

A ROM library function (see **[1]**) is available which selects the tuning curve automatically dependent on environmental conditions ($T_{ambient}$, V_{bat}).

Note: Re-calibration of the tuning curve is necessary when V_{bat} changes by more than 800mV or $T_{ambient}$ changes by more than 70°C.

Power Amplifier PA

In a typical application, the highly efficient power amplifier is automatically turned on by the Manchester/BiPhase encoder as soon as data is written to the SFR RFD. After the last bit is transmitted and the shift register is empty the PA is turned off again. If, however, the automatic control of the PA is not desired, then manual control is possible when SFR bit RFC.0[ENPA] is set.
The nominal output power levels are specified in **Table 36 “RF Transmitter” on Page 153**. The output power is determined by SFR bits RFTX.1-0[PAOP1-0] and the matching network (see also **“Test Board” on Page 142** for details on the matching network).

Note: For test purpose the PLL synthesizer and the power amplifier can be enabled separately by using the SFR RFC control register. The power amplifier should be switched on with a delay of at least 100µs after enabling the frequency synthesizer. This delay is needed for the PLL to lock.

PLL Monitoring

In order to avoid unwanted out-of-band emissions in case the PLL goes out-of-lock, the SP37T includes a PLL Monitoring feature . This feature can be enabled via SFR bit RFC.7[ENPLLMON]. If PLL Monitoring is enabled and the PLL becomes unlocked, the RF Power Amplifier is automatically disabled and SFR bit RFS.7[PADIS] bit is set. The application program can verify that a transmission was successful by checking PADIS - if PADIS is clear, the PLL remained locked throughout the transmission.

*Note: The **Manchester/BiPhase Encoder** state machine continues executing transmission even though PA is off.*

RF-Transmitter Control Register

RFC	Offset	Wakeup Value	Reset Value
RF-Transmitter Control Register	$C8_H$	00_H	00_H

7	6	2	1	0
ENPLLMON	UNUSED		ENPLL	ENPA
wr	-		wr	wr

Field	Bits	Type	Description
ENPLLMON	7	wr	**Enables PLL Monitoring** PLL Monitoring will automatically disable the PA during RF transmission if the PLL goes out of lock. 0_B Disable 1_B Enable Reset: 0_H
UNUSED	6:2	-	**UNUSED** Reset: 00_H
ENPLL	1	wr	**Enable RF Frequency Synthesizer (PLL)** The ROM Library Function VCO-Tuning should be used to enable the PLL. After RF transmission is complete this bit may be used to disable the PLL. 0_B Disable 1_B Enable Reset: 0_H
ENPA	0	wr	**Enable RF Power Amplifier (PA)** This bit is normally cleared to allow the Manchester/Bi-Phase Encoder to control the RF PA during transmission. (see SFR CFG1 RFTXPEN for exceptional case) 0_B PA controlled automatically by Manchester/Bi-Phase Encoder 1_B PA controlled manually Reset: 0_H

RF-Transmitter Configuration Register

RFTX	Offset	Wakeup Value	Reset Value
RF-Transmitter Configuration Register	AE_H	$UUU0UUUU_B$	87_H

7	6	5	4	3	2	1	0
FSKSWITCH	ITXD	ASKFSK	UNUSED	ISMB		PAOP	
wr	wr	wr	-	wr		wr	

Field	Bits	Type	Description
FSKSWITCH	7	wr	**FSK modulation switch** 0_B Switch is always open (disabled) - to be used with internal pulling capacitors 1_B Switch is controlled by RF Encoder when ASKFSK = 0_B to be used with external capacitors The FSK Switch is open when the RF Encoder output is 1. The FSK Switch is closed when the RF Encoder output is 0. Switch is closed when ASKFSK = 1_B. Reset: 1_H
ITXD	6	wr	**Invert Transmit Data** 0_B Data not inverted 1_B Data inverted Reset: 0_H
ASKFSK	5	wr	**ASK/FSK Modulation Select** 0_B FSK modulation (Frequency Shift Keying) 1_B ASK modulation (Amplitude Shift Keying) Reset: 0_H
UNUSED	4	-	**UNUSED** Reset: 0_H
ISMB	3:2	wr	**RF Frequency Band Select** 00_B 300MHz - 320MHz 01_B 433MHz - 450MHz 10_B Reserved 11_B Reserved Reset: 1_H
PAOP	1:0	wr	**RF Power Amplifier Output Stage Select** 00_B 1 PA output stage enabled 01_B 2 PA output stages enabled 10_B 2 PA output stages enabled 11_B 3 PA output stages enabled Reset: 3_H

3.10 Manchester/BiPhase Encoder

The SP37T offers a Hardware Manchester/BiPhase encoder which uses Timer 1 (see **"Timer Unit" on Page 105**) to configure the bitrate for the encoder. The application software needs to configure the timer and can subsequently send the raw uncoded data to the Manchester/BiPhase Encoder which takes care about encoding and the RF transmission itself (controlling the Power Amplifier). Using the Hardware encoder allows that the CPU to be operated at a reduced clock rate thereby reducing the peak current consumption during RF transmission. The reduced CPU clock rate also reduces the possibility of clock noise artifacts in the RF signal (see **"Internal Clock Divider" on Page 57**). Furthermore, the encoder creates a resume event after sending each byte so that the application can enter IDLE state while sending each databyte (see **"Resume Event Flag Register" on Page 50**). It is recommended to use both reduced clock rate and IDLE mode for best performance during RF transmission.

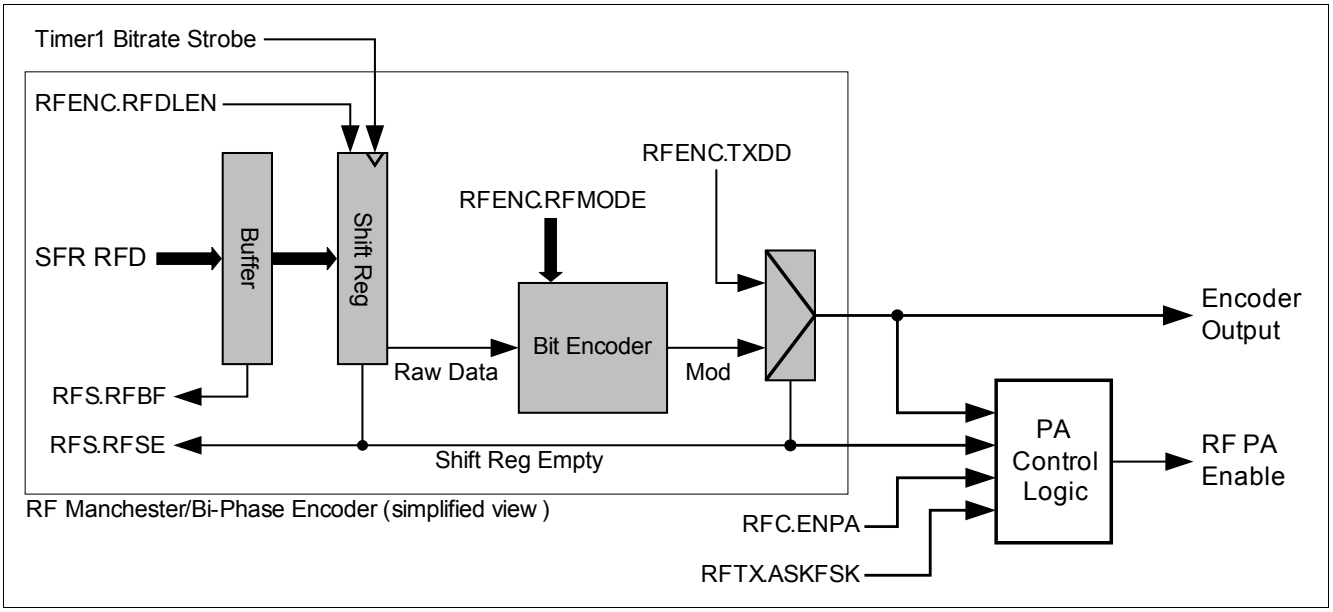


Figure 16 Manchester/BiPhase Encoder

The encoder mode, transmit buffer length, and RF carrier idle state are all controlled by SFR RFENC. The RFENC settings for encoder mode and transmit buffer length take effect upon transfer of the data from SFR RFD to the internal shift register, not at the time of writing to SFR RFENC.

The RF Power Amplifier (RF PA) is controlled by the PA Control Logic. In most cases the control logic enables and disables the RF PA according to the table in **Figure 17**. Cases in which the behavior differs from this table include usage of SFR bit **RFTXPEN** and the **PLL Monitoring** features.

By enabling the RF Encoder Data Output alternate port functionality of PP2 via the SFR bit RFTXPEN in CFG1, the SFR bit ENPA in SFR RFC must be set in order to allow the RF Encoder output to properly modulate the RF PA. It is recommended that the RF Encoder Data Output functionality of PP2 is used only during software development debugging or device testing. Another exception to the behavior in **Figure 17** is when the PLL Monitoring feature is enabled. See **"PLL Monitoring" on Page 65** for more details."

RFC.ENPA	RFS.RFSE	RFTXASKFSK	Encoder Output	RF PA Enable
X	0	0	Mod	ON
X	0	1	Mod	Mod
0	1	X	TXDD	OFF
1	1	0	TXDD	ON
1	1	1	TXDD	TXDD

Figure 17 RF PA Control Logic

By default the transmission takes place byte-aligned (SFR bits RFENC.7-5[RFDLEN2-0]= 111b. If less than 8 Bits should be transmitted, SFR bits RFENC.7-5[RFDLEN2-0] can be set to any value between 110b...000b to transmit only 7...1 MSBs of the transmit buffer SFR RFD. In this case the unused LSBs are disregarded.

In addition to Manchester/BiPhase encoding, it is also possible to send data with a user-defined encoding scheme, e.g. for sending a preamble. This can be achieved by the chipmode (SFR bits RFENC.2-0[RFMOD2-0] = 101b). In chipmode the encoder sends each bit in SFR RFD without any encoding.

The following figure shows the timing diagrams for the different encoding schemes:

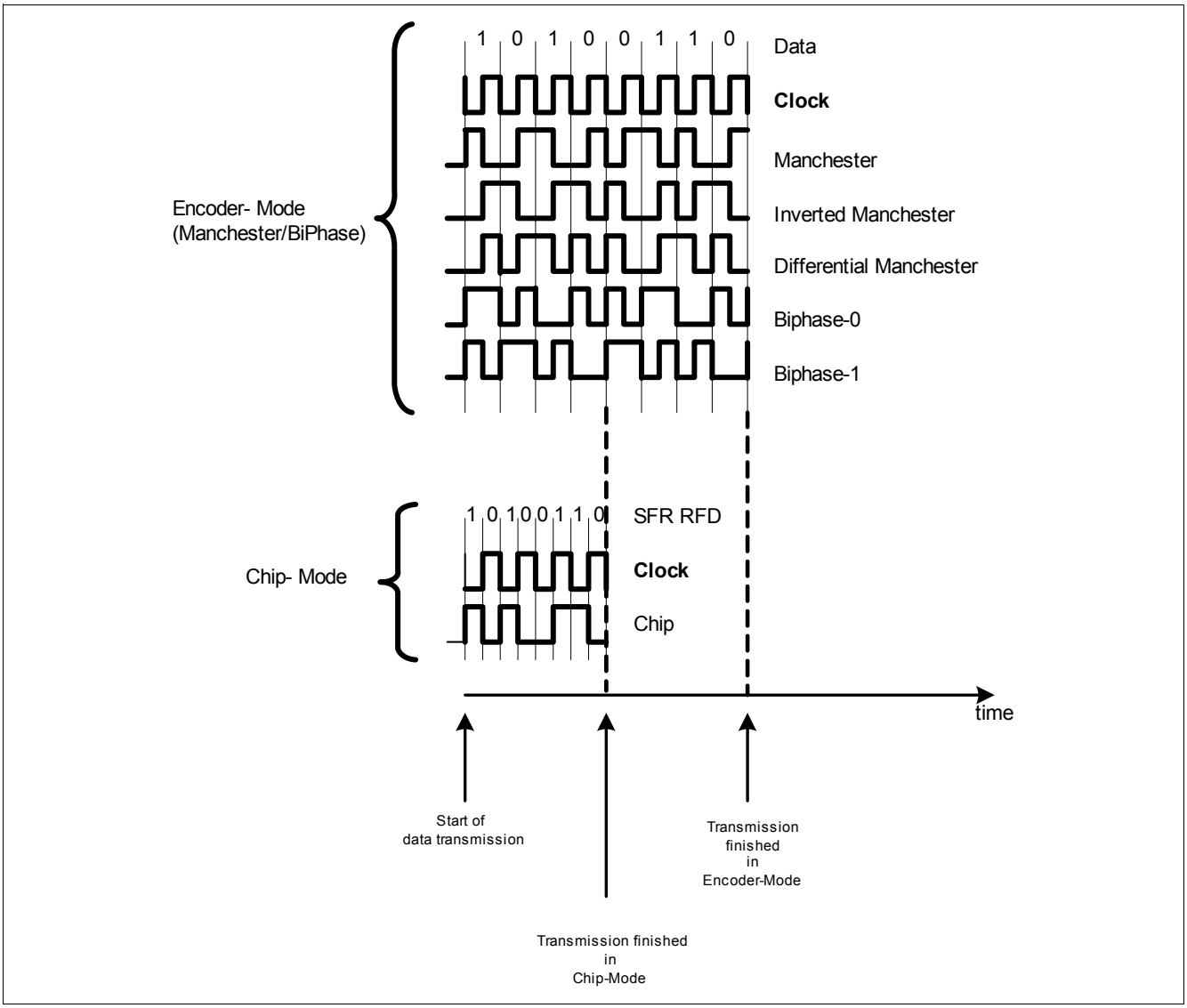


Figure 18 Diagram of the Different RF Encoder Modes

As shown in **Figure 16 “Manchester/BiPhase Encoder” on Page 68** Timer 1 (see **“Timer Unit” on Page 105**) is used as bitrate generator and has to be configured according to the desired bitrate. The required timer clock source is the crystal oscillator. The required timer value can be calculated with the following formula:

$$timervalue = \left(\frac{f_{timerclock\ source}\left[Hz\right]}{8 \cdot Baudrate\left[\frac{1}{s}\right]} \right) - 1 \quad (9)$$

This timer value has to be written to the timer registers (see **“Timer 1 Register High Byte” on Page 115** and **“Timer 1 Register Low Byte” on Page 115**).

RF Encoder Status

SFR RFS represents the status of the RF Encoder.

After writing a databyte to SFR RFD, the SFR bit RFS.0[RFBF] is set by the encoder hardware. It is cleared automatically when the databyte in SFR RFD is transferred to the shift register and the buffer is ready to be filled with the next databyte.

Since the encoder creates a resume event (see **“Resume Event Flag Register” on Page 50**) when the SFR bit RFS.0[RFBF] is cleared, the application can enter IDLE state between sending two consecutive databytes.

Note: It is necessary to provide the RF encoder with a continuous data stream to prevent the RF receiver from losing synchronization.

SFR bit RFS.1[RFSE] is cleared as long as the shift register still contains data that has to be transmitted and is set if there is no more data available in the shift register (this indicates the end of a data transmission) and automatically turns off the RF Power Amplifier.

If PLL Monitoring is enabled and the PLL becomes unlocked, the RF Power Amplifier is automatically disabled and SFR bit RFS.7[PADIS] bit is set. The application program can verify that a transmission was successful by checking PADIS - if PADIS is clear, the PLL remained locked throughout the transmission.

*Note: The **Manchester/BiPhase Encoder** state machine continues executing transmission even though PA is off.*

RF-Encoder Tx Control Register

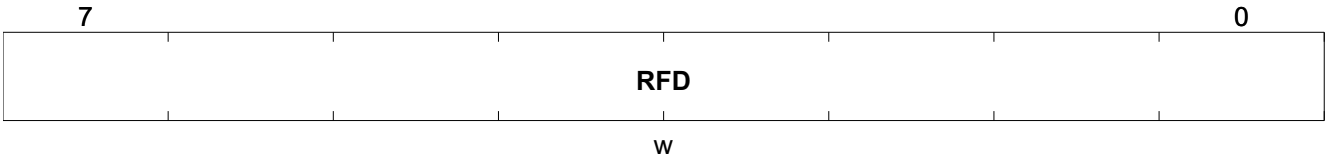
RFENC	Offset	Wakeup Value	Reset Value
RF-Encoder Tx Control Register	CA_H	$E0_H$	$E0_H$

7	5	4	3	2	0
RFDLEN		UNUSED	TXDD	RFMODE	
wr		-	wr	wr	

Field	Bits	Type	Description
RFDLEN	7:5	wr	**RF Data Length** Number of bits to be transmitted from SFR RFD. 000_B Transmit RFD MSB only 001_B Transmit RFD two MSBs 010_B 011_B 100_B 101_B 110_B 111_B Transmit all bits of RFD Reset: 7_H
UNUSED	4	-	**UNUSED** Reset: 0_H
TXDD	3	wr	**RF Encoder Idle state** Determines the state of the RF Transmitter when the RF Shift Register is empty and the SFR bit RFC.0[ENPA] is set. 0_B FSK Carrier low / ASK Carrier off 1_B FSK Carrier high / ASK Carrier on Reset: 0_H
RFMODE	2:0	wr	**RF Encoder Mode** Refer to Diagram of different RF Encoder modes figure. 000_B Manchester 001_B Inverted Manchester 010_B Differential Manchester 011_B Biphase 0 100_B Biphase 1 101_B Chip Mode (NRZ) 110_B Reserved 111_B Reserved Reset: 0_H

RF-Encoder Tx Data Register

RFD	Offset	Wakeup Value	Reset Value
RF-Encoder Tx Data Register	$C9_H$	00_H	00_H



Field	Bits	Type	Description
RFD	7:0	w	**RF Data Transmit Byte** Reset: 00_H

RF-Encoder Tx Status Register

RFS	Offset	Wakeup Value	Reset Value
RF-Encoder Tx Status Register	CB_H	02_H	02_H

7	6	2	1	0
PADIS	UNUSED		RFSE	RFBF
wr	-		r	r

Field	Bits	Type	Description
PADIS	7	wr	**PLL Monitoring PA Status** If the PLL Monitoring is enabled (RFC.ENPLLMON is set) and during RF transmission the PLL goes out of lock, this bit is set and the PA is automatically disabled. The PA remains disabled until this bit is cleared by CPU. This bit can be cleared only when the content of the RF shift register is cleared. Writing a logical '1' to this bit has no effect. 0_B PA is enabled 1_B PLL Monitoring has disabled the PA Reset: 0_H
UNUSED	6:2	-	**UNUSED** Reset: 00_H
RFSE	1	r	**RF Encoder Shift Register Empty Flag** Automatically set by hardware if no further bits are available in RF Shift Register. When RF Shift Register becomes empty, the state of the RF Transmitter is determined by SFR RFENC.3 [TXDD]. 0_B Data transmission in progress 1_B Data transmission complete Reset: 1_H
RFBF	0	r	**RF Encoder Buffer Full** Automatically set by hardware on write to SFR RFD and cleared when data in SFR RFD is transferred to RF Shift Register. 0_B Buffer empty, SFR RFD ready for new data 1_B Buffer full, do not write to SFR RFD Reset: 0_H

3.11 LF Receiver

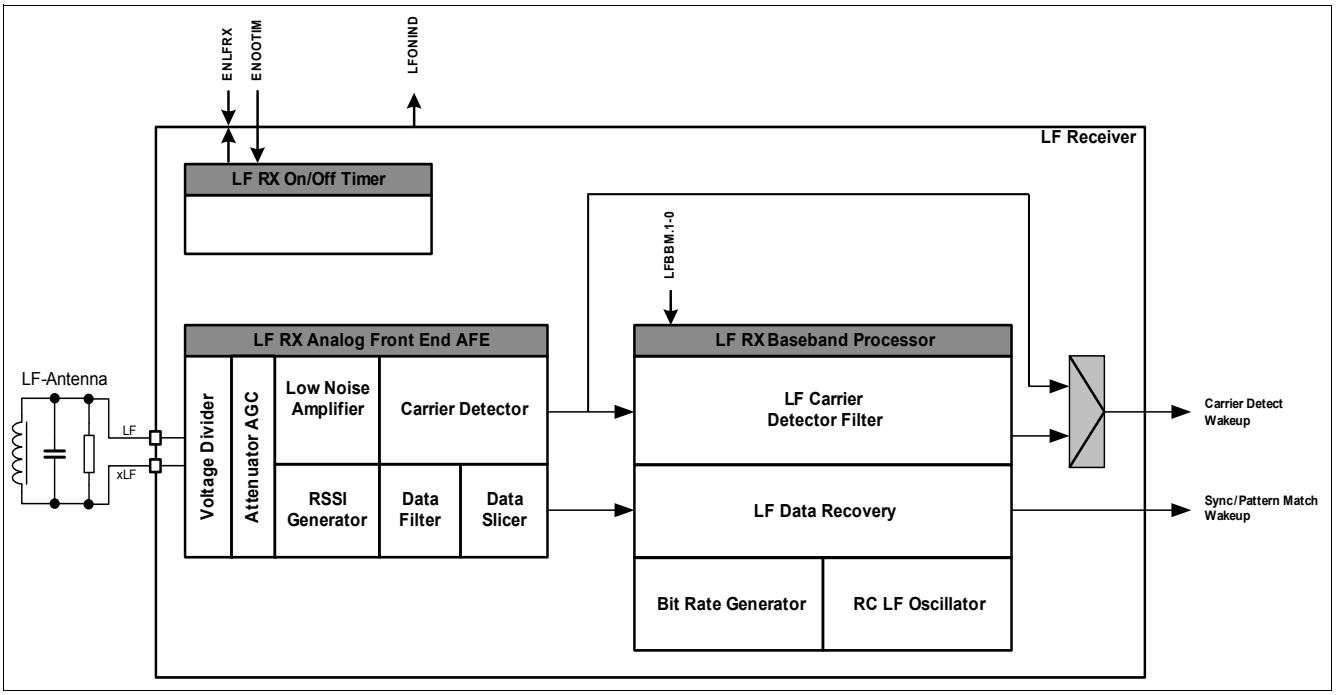


Figure 19 LF Receiver Block Diagram

The LF Receiver is used for wireless data transmission towards the SP37T and for waking up the device from POWER DOWN state.

It can generate a wakeup directly by the carrier detector if the carrier amplitude is above a predefined threshold, or it can decode the received data and wake up the microcontroller only if a sync match pattern or sync match pattern/wakeup pattern is detected in the data stream.

Data recovery using a synchronizer and a decoder is available for Manchester coded data. The synchronizer can also handle Manchester code violations. Other coding scheme can be handled by the microcontroller at the chip level, thus no limitations on data coding schemes apply.

An LF On/Off Timer is implemented to generate periodical On/Off switching (polling) of the LF Receiver in POWER DOWN state to minimize the current consumption.

LF Receiver Control Register

LFRXC	Offset	Wakeup Value	Reset Value
LF Receiver Control Register	98_H	$0UUUUU00_B$	00_H

7	6	5	4	3	2	1	0
CDRECAL	DISAGC	LFBBM		ENOOTIM	ENLFRX	SYNCIND	LFONIND
wc	wr	wr		wr	wr	r	r

Field	Bits	Type	Description
CDRECAL	7	wc	**Restart Carrier Detect Recalibration** Calibration is automatically performed each time the LFRx is powered on. This bit forces manual Recalibration when set. This bit is automatically cleared after Recalibration has started 0_B Cleared automatically after Recalibration has started 1_B Start Carrier Detect Recalibration Reset: 0_H
DISAGC	6	wr	**Disable Automatic Gain Control (AGC)** 0_B Enable 1_B Disable Reset: 0_H
LFBBM	5:4	wr	**LF Baseband Processor Mode** It is recommended to first disable the LF Receiver (ENLFRX = 0) prior to changing the LF Baseband Processor Mode. 00_B Disabled, only Carrier Detect function remains *Note: Carrier Detector Filter may be enabled separately* 01_B Mode 1: LF baseband is enabled while LF Receiver is on 10_B Mode 2: LF baseband is enabled only after carrier detection 11_B Not used Reset: 0_H
ENOOTIM	3	wr	**Enable On/Off Timer** This bit controls the LF On/Off Timer. This bit has to be stable for at least 1 LP RC clock (2 kHz) period in order to take effect. When the LF On/Off Timer is disabled the LF Receiver is controlled by ENLFRX. This bit is automatically cleared if sync or pattern match wakeup occurs. 0_B Disable On/Off Timer 1_B Enable On/Off Timer Reset: 0_H
ENLFRX	2	wr	**Enable LF Receiver** This bit controls power to LF Receiver and has priority over ENOOTIM. 0_B LF Receiver disabled 1_B LF Receiver state is determined by On/Off Timer Reset: 0_H

Field	Bits	Type	Description
SYNCIND	1	r	**Synchronization Indicator** This bit is set upon Sync Match and remains set as long as valid Manchester data is detected. When invalid Manchester bit is detected this bit is cleared and SFR bit LFRXS.DECERR is set.(e.g. **Figure 29**) 0_B No Synchronization 1_B Synchronization achieved Reset: 0_H
LFONIND	0	r	**LF ON/OFF Indicator** Indicates if the LF Analog Frontend is turned on or off. This bit may be used to observe the LF On/Off Timer period and duty cycle. 0_B LF Analog Frontend power is off 1_B LF Analog Frontend power is on Reset: 0_H

3.12 LF Receiver Analog Front End

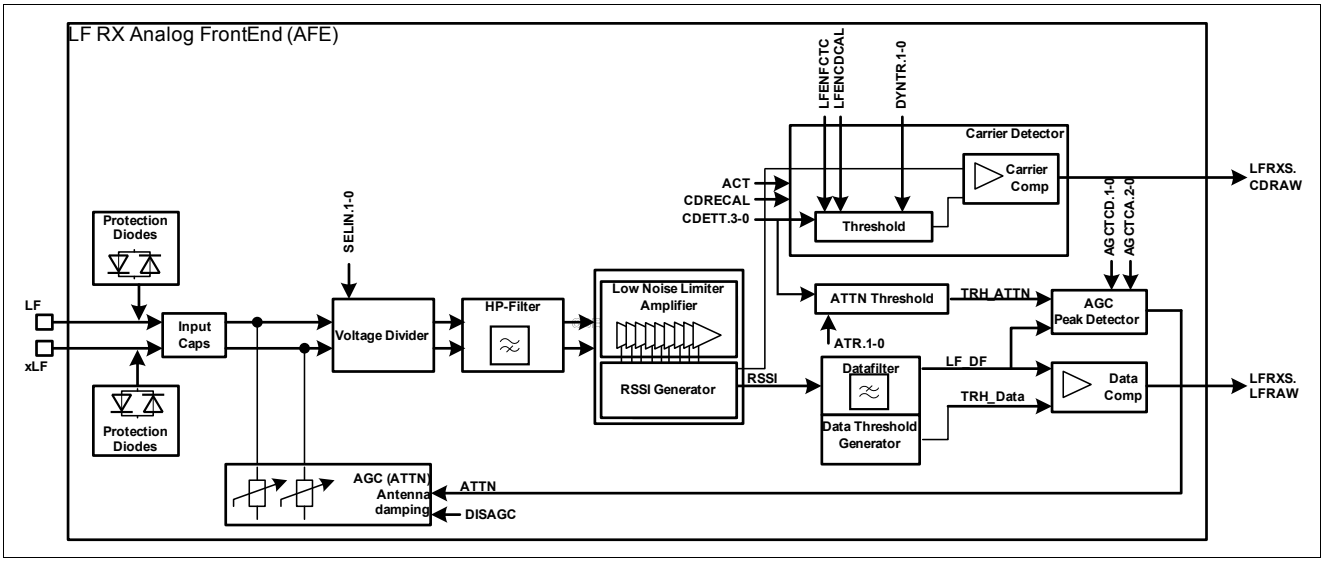


Figure 20 LF Receiver AFE Block Diagram

The LF Receiver Analog Frontend has two input pins LF and xLF. An antenna coil in parallel resonance to a capacitor and resistor are externally connected to them in the application. The LF input pins are protected against overvoltage with antiparallel ESD-Diodes. The **“Differential Input Capacitance” on Page 155** needs to be considered for the calculation of the parallel resonance frequency of the antenna.

A Voltage Divider with three divider factors is available to attenuate the LF input signal. The attenuation is determined by the SFR bits LFRX0.1-0[SELIN1-0].

The LF input signal is amplified with a Low Noise Limiter Amplifier and the signal strength is indicated by the RSSI Generator. The internal RSSI signal is used as input for the Carrier detector and the ASK demodulator.

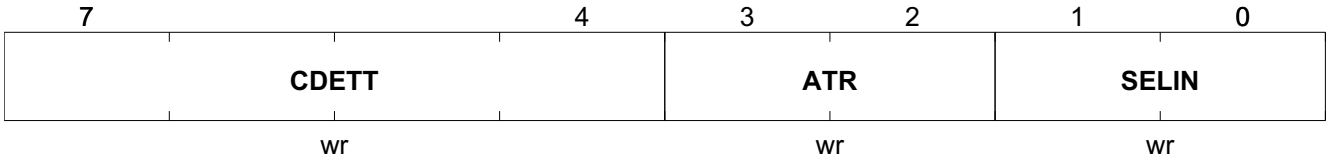
The Carrier Detector has an adjustable threshold which is determined by SFR bits LFRX0.7-4[CDETT3-0]. An LF input signal above the Carrier Detector threshold level may trigger a device wakeup from POWER DOWN state. The Carrier Detector Raw (CDRAW) signal is used as input for the LF Baseband.

The ASK demodulator consists of a datafilter together with a data threshold generator and the dataslicer. The demodulated output signal (LFRAW) is used as input for the LF Baseband.

To cover a high dynamic range of the LF input signal an input attenuator with an Automatic Gain Control (AGC) is implemented. In the event that AGC is not desired, it can be disabled by setting SFR bit LFRXC.6[DISAGC].

LF Receiver Configuration Register 0

LFRX0	Offset	Wakeup Value	Reset Value
LF Receiver Configuration Register 0	$B7_H$	UU_H	38_H



Field	Bits	Type	Description
CDETT	7:4	wr	**Carrier Detector Threshold Level** 0000_B: Lowest threshold ... 1111_B: Highest threshold Reset: 3_H
ATR	3:2	wr	**AGC Threshold** These bits must be set to 11_B. Reset: 2_H
SELIN	1:0	wr	**LF-Receiver Input Select** 00_B Antenna voltage divider factor 1 01_B Antenna voltage divider factor 6,8 10_B Antenna voltage divider factor 22 11_B Do not use Reset: 0_H

3.13 LF Attenuator (AGC)

An input attenuator is provided to limit strong signals and interferers across the differential input. An automatic gain control block (fast attack, slow decay) is implemented to cover a high dynamic range of the LF input signal. The AGC threshold is determined by the SFR bits LFRX0.3-2[ATR1-0] and the carrier detector settings in SFR bits LFRX0.7-4[CDETT3-0]. The attenuator attack time is controlled via the SFR bits LFRX2.2-0[AGCTCA2-0]. The decay slew rate can be adjusted by SFR bits LFRX1.7-6[AGCTCD1-0]. Please refer to the register description for the proper setting of the AGC SFR bits.

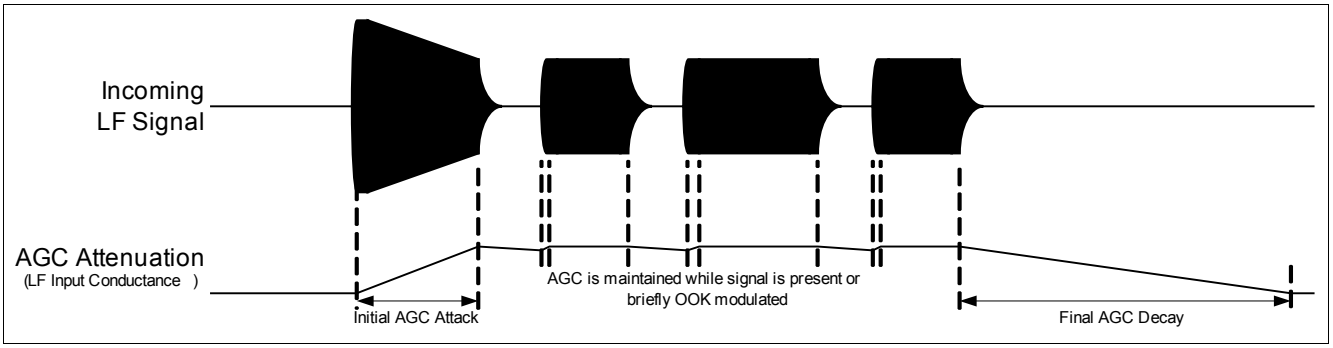


Figure 21 AGC Timing diagram

LF Receiver Configuration Register 1

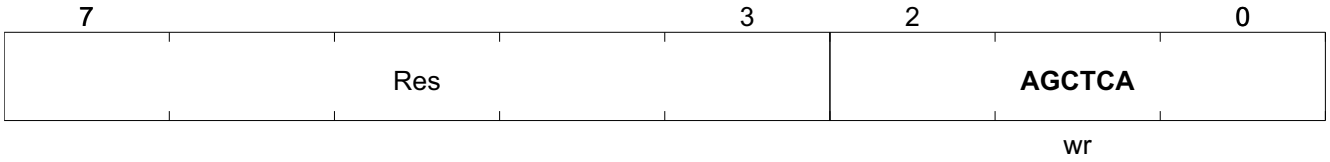
LFRX1	Offset	Wakeup Value	Reset Value
LF Receiver Configuration Register 1	**$B6_H$**	**UU_H**	**00_H**

7	6	5	4	3	0
AGCTCD		**ACT**		Res	
wr		wr			

Field	Bits	Type	Description
AGCTCD	7:6	wr	**AGC Decay Time Constant** Recommended setting 00_B Reset: 0_H
ACT	5:4	wr	**Autocalibration Time** Recommended setting for LF Telegram detection 10_B Recommended setting for carrier detection 01_B Reset: 0_H
Res	3:0		**Reserved** These bits must be set to 0000_B. Reset: 0_H

LF Receiver Configuration Register 2

LFRX2	Offset	Wakeup Value	Reset Value
LF Receiver Configuration Register 2	**AF_H**	**UU_H**	**77_H**



Field	Bits	Type	Description
Res	7:3		**Reserved** These bits must be set to 01110_B. Reset: $0E_H$
AGCTCA	2:0	wr	**AGC Attack Time Constant Selection** Recommended setting 111_B Reset: 7_H

3.14 LF Carrier Detector

A level detection circuit is implemented to determine if the carrier amplitude is above a predetermined level. An LF input signal above the Carrier Detector threshold level may cause a device wakeup from POWER DOWN state.

Three different Carrier Detector thresholds can be chosen by the application. In order to achieve LF sensitivity as specified in **Table 40 “LF Receiver Carrier Detection, Vbat = 2.1 V...3.6 V, fLF = 120 kHz...130 kHz” on Page 157** an appropriate Voltage Divider setting (SFR bits LFRX0.1-0[SELIN1-0]) is used in conjunction with the adjustable threshold level (SFR bits LFRX0.7-4[CDETT3-0]). During the testing and calibration process at the factory, individually calibrated CDETT values are programmed into each device. The CDETT calibration information for each device may vary, and so the application software must retrieve the calibrated CDETT values from the appropriate Flash address and apply it in conjunction with the predefined SELIN setting. The complete proper setting for SFR LFRX0 (CDETT[7:4], ATR[3:2], SELIN[1:0]) for the according Carrier Detector Threshold Level must be read by the application from the following Flash addresses and be written into SFR LFRX0 :

- Carrier Detector Threshold 1: Flash address 5810_H
- Carrier Detector Threshold 2: Flash address $580F_H$
- Carrier Detector Threshold 3: Flash address $580E_H$

Carrier Detector Filtering

To prevent the device from undesired carrier detect wakeups, an LF Carrier Detector Filter is implemented. SFR LFCDFLT is used to determine the Filtering Time. The LF Carrier Detector Filter is enabled/disabled according to LFCDFLT.CDFT[6-0]. The following figure shows the behavior of the LF Carrier Detector Filter.

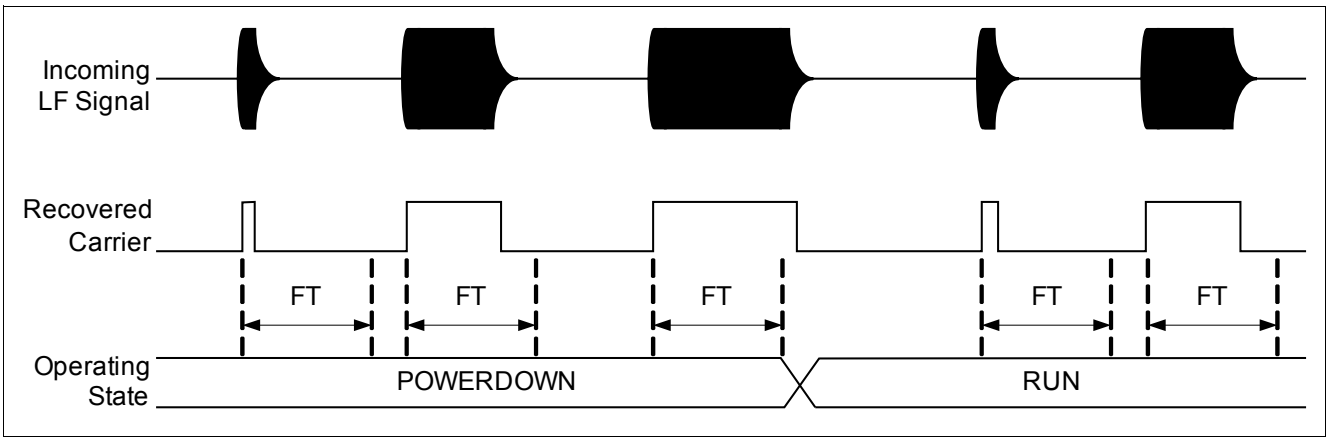


Figure 22 LF Receiver Carrier Detector Filtering

Three different Carrier Detector Filter settings are predefined for the application. In order to achieve LF filter times as specified in **Table 40 “LF Receiver Carrier Detection, Vbat = 2.1 V...3.6 V, fLF = 120 kHz...130 kHz” on Page 157** an appropriate Filter Time setting (SFR LFCDFLT.CDFT[6-0]) needs to be applied. During the testing and calibration process at the factory, individually calibrated CDFT values are programmed into each device. The CDFT calibration information for each device may vary, and so the application software must retrieve the calibrated CDFT values from the appropriate Flash address. The proper settings for SFR LFCDFLT are indicated in following list:

- Carrier Detector Filter Time 1: [CDFT.6-0]: Flash address $580D_H$
- Carrier Detector Filter Time 2: [CDFT.6-0]: Flash address $580C_H$
- Carrier Detector Filter Time 3: [CDFT.6-0]: Flash address $580B_H$

Figure 23 summarizes the LF Carrier Detector response versus input signal duration and amplitude.

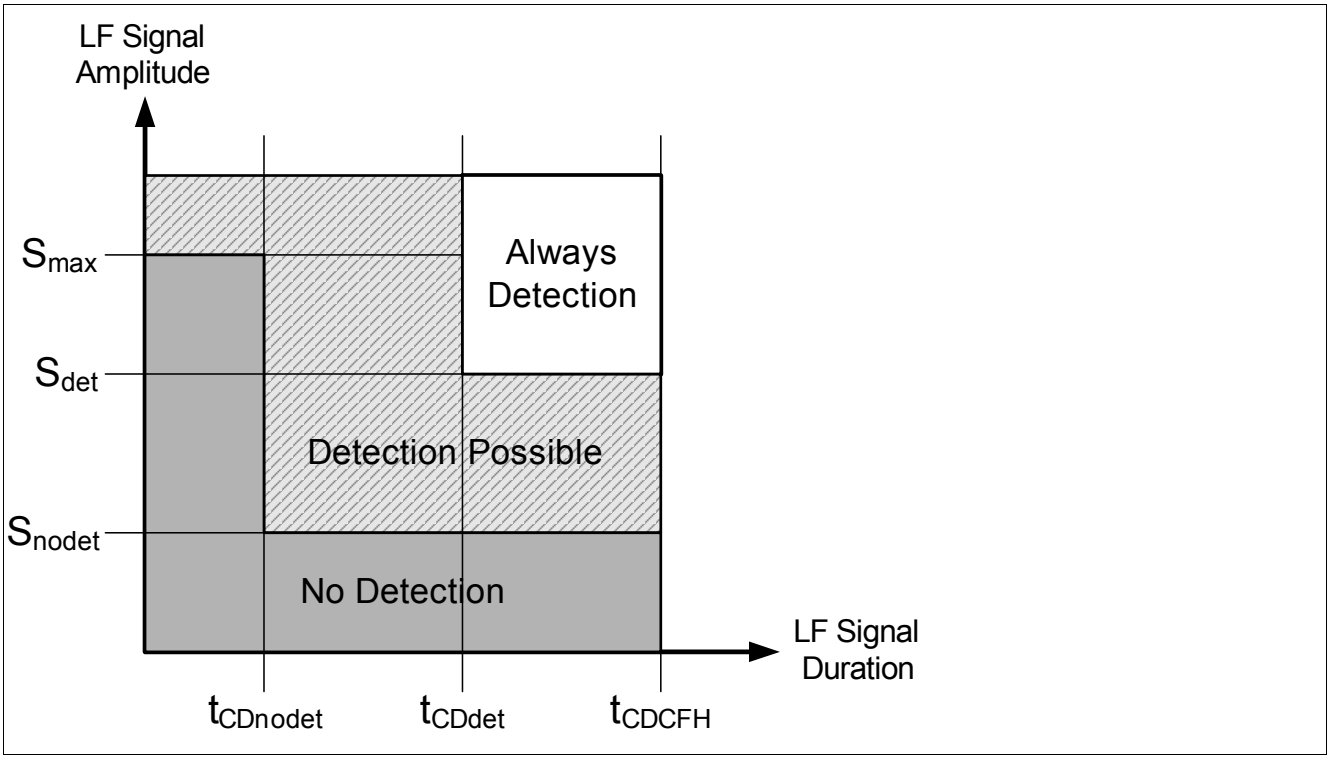


Figure 23 LF Carrier Detector Response

Automatic Carrier Detector Threshold Calibration

To achieve high sensitive thresholds the Carrier Detector has to be calibrated. This auto-calibration is enabled by setting SFR bit LFCDM0.3[LFENCDCAL] and is executed everytime the LF Receiver is turned on (either manually by SFR bit LFRXC.2[ENLFRX] or automatically by the LF On/Off Timer). An auto-calibration sequence can be manually initiated by setting SFR bit LFRXC.7[CDRECAL]. The auto-calibration duration is determined by SFR bits LFRX1.5-4[ATC1-0] and specified in **Table 40 “LF Receiver Carrier Detection, Vbat = 2.1 V...3.6 V, fLF = 120 kHz...130 kHz” on Page 157**. For the proper setting of the auto-calibration please refer to the register description.

If set, SFR Bit LFCDM0.2[LFENFCTC] “freezes” the threshold level after the calibration is finished.
If this bit is not set, the threshold will follow the mean value of the input signal, resulting in a threshold signal that is dependent on the LF signal strength.

*Note: If SFR Bit LFCDM0[LFENFCTC] is set, a periodic recalibration is required especially at higher temperatures since the “frozen” threshold level might drift after the Carrier Detector Freeze Hold Time (TCDCFH). The recalibration is achieved automatically by the next Off/On transition of the LF On/Off Timer or by turning off and on the LF Receiver manually by SFR Bit LFRXC.2[ENLFRX]. The Carrier Detector Freeze Hold Time is specified in **Table 40 “LF Receiver Carrier Detection, Vbat = 2.1 V...3.6 V, fLF = 120 kHz...130 kHz” on Page 157**.*

The following figure shows the timing behavior of the calibration.

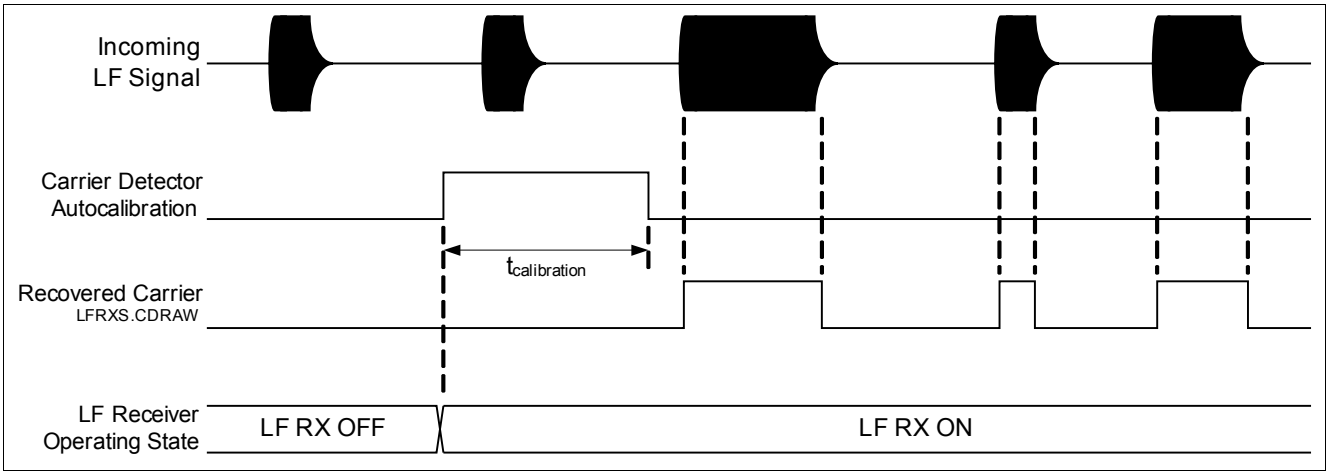
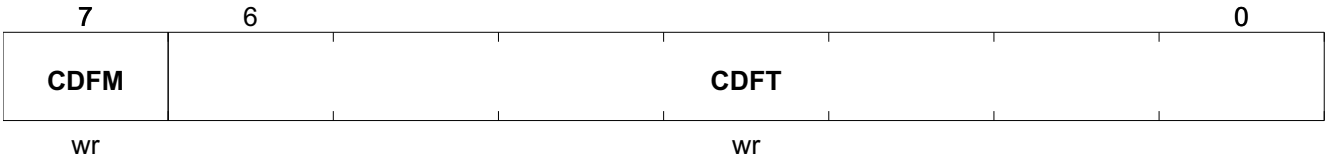


Figure 24 Carrier Detector Threshold Calibration Timing

LF Carrier Detect Filtering

LFCDFLT	Offset	Wakeup Value	Reset Value
LF Carrier Detect Filtering	$B2_H$	UU_H	00_H



Field	Bits	Type	Description
CDFM	7	wr	**Carrier Detector Filtering Mode** For typical applications it is recommended to set this bit to 0_B. 0_B Filter enabled 1_B Filter enabled until Carrier detected Reset: 0_H
CDFT	6:0	wr	**Carrier Detector Filtering Time** 01_H-$7F_H$ Enables and adjusts filtering time in steps of 1 LF RC Oscillator period (typ. 11.1 us). 00_H Disables filtering. Reset: 00_H

LF Carrier Detector Mode Register 0

LFCDM0	Offset	Wakeup Value	Reset Value
LF Carrier Detector Mode Register 0	$B5_H$	$UUUUUUU0_B$	00_H

7	6	5	4	3	2	1	0
Res		DYNTR		LFENCDCAL	LFENFCTC	Res	UNUSED
		wr		wr	wr		-

Field	Bits	Type	Description
Res	7:6		**Reserved** These bits must be set to 00_B. Reset: 0_H
DYNTR	5:4	wr	**Carrier Detector Dynamic Threshold** Recommended setting 01_B Reset: 0_H
LFENCDCAL	3	wr	**Enable LF Carrier Detect Calibration** 0_B Disable Calibration 1_B Calibration occurs each LF Rx power up Reset: 0_H
LFENFCTC	2	wr	**Enable LF Calibration Freeze** 0_B Disable Calibration Freeze 1_B Hold Calibration threshold Reset: 0_H
Res	1		**Reserved** This bit must be set to 0_B. Reset: 0_H
UNUSED	0	-	**UNUSED** Reset: 0_H

3.15 LF Receiver On/Off Timer

An On/Off Timer is implemented to reduce the LF Receiver current consumption in POWER DOWN state. It can be enabled by SFR bit LFRXC.3[ENOOTIM]. The LF Analog Frontend will be periodically turned On and Off corresponding to the timer settings. The current state of the LF Receiver (On or Off) can be evaluated using SFR bit LFRXC.0[LFONIND].The LF Receiver On/Off Timer incorporates a precounter (SFR LFOOTP) as timebase and a postcounter for independently setting the On time and the Off time (SFR LFOOT).

LF Receiver On/Off Timer Calibration

The calibration process is done automatically by a ROM Library function (see **[1]**) which calibrates the timebase to 50ms.

If any other (uncalibrated) timebase is needed SFR LFOOTP can be configured manually according the following equation:

$$timebase\,[s] = \frac{LFOOTP\ +1}{f_{2kHzRCLPOsc\,ilator}[Hz]} \tag{10}$$

The On time and the Off time can be configured individually using SFR LFOOT. They can be calculated using the two following two equations:

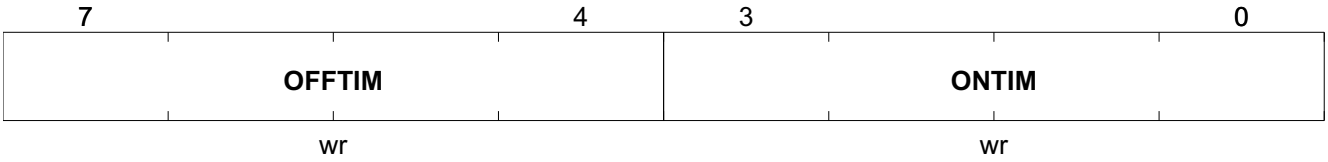
$$ontime[s] = \frac{(ONTIM\ +1)\cdot[Integer((LFOOTP)/4)+1]\cdot(LFOOTP+1)}{(LFOOTP+1)\cdot f_{2kHzRCLPOsalator}[Hz]} \tag{11}$$

$$ontime\,[s] = \frac{(ONTIM\ +1)\cdot[Integer((LFOOTP)/4)+1]\cdot timebase[s]}{(LFOOTP\ +1)} \tag{12}$$

$$offtime[s] = \frac{(OFFTIM+1)\cdot(LFOOTP+1)\cdot 4}{f_{2kHzRCLPOsalator}[Hz]} = (OFFTIM+1)\cdot timebase[s]\cdot 4 \tag{13}$$

LF On/Off Timer Configuration Register

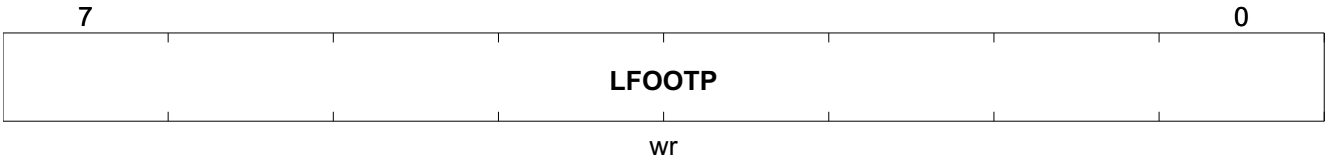
LFOOT	Offset	Wakeup Value	Reset Value
LF On/Off Timer Configuration Register	**$C6_H$**	**UU_H**	**00_H**



Field	Bits	Type	Description
OFFTIM	7:4	wr	**LF Polling OFF-Time** If time base is set to 50 ms (default after calibration) in SFR LFOOTP : 0000_B: 200 ms ... 1111_B: 3.2 s Reset: 0_H
ONTIM	3:0	wr	**LF Polling ON-Time** If time base is set to 50 ms (default after calibration) in SFR LFOOTP : 0000_B: 12.5 ms ... 1111_B: 200 ms Reset: 0_H

LF OnOff Timer Precounter

LFOOTP	Offset	Wakeup Value	Reset Value
LF OnOff Timer Precounter	**$C5_H$**	**UU_H**	**64_H**



Field	Bits	Type	Description
LFOOTP	7:0	wr	**LF ON/OFF Timer Precounter** Establishes timebase for the LF-ON/OFF-Timer. 00_H: 1 RC-LP-Oscillator (2 kHz) periods 01_H: 2 RC-LP-Oscillator (2 kHz) periods ... FF_H: 256 RC-LP-Oscillator (2 kHz) periods Reset: 64_H

3.16 LF Receiver Baseband

The LF Receiver Baseband circuitry allows reception of ASK modulated LF Telegrams. As in the case of the LF Carrier Detector, the LF Receiver Baseband may be enabled and disabled manually via SFR LFRXC.2[ENLFRX] or automatically by the LF Receiver On/Off Timer. The LF Receiver Baseband may be operated in one of two modes: Mode 1, in which the baseband is fully operational whenever the LF receiver is enabled; and Mode 2, in which the baseband is only operational after the LF Carrier Detector has detected an incoming signal. LF Baseband Mode selection is accomplished by SFR bits LFRXC5:4[LFBBM]. The specified telegram sensitivity is only accomplished in Mode 1 and with the proper SFR register settings(see **Table 68 "LF Receiver Special Function Register Settings for Telegram Mode" on Page 156**)

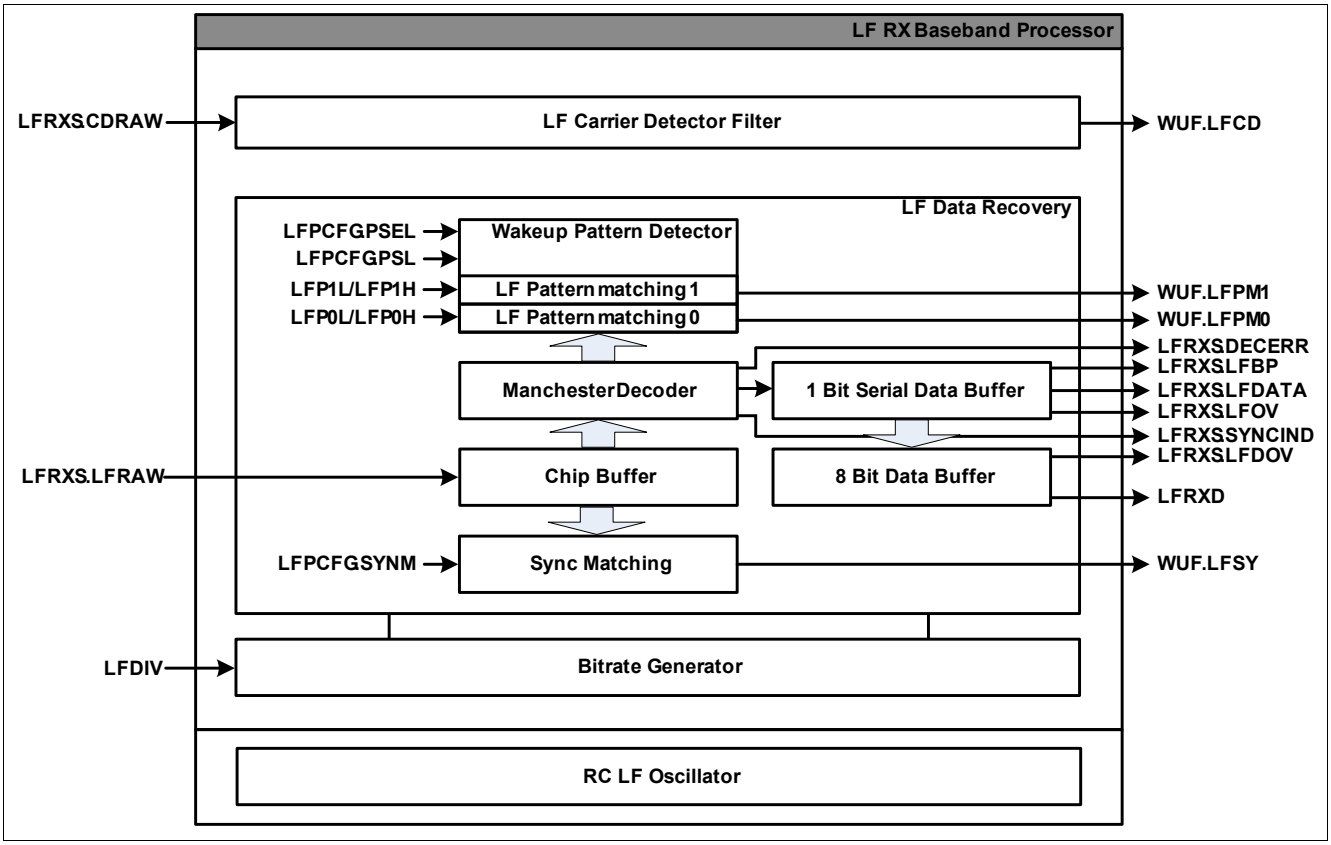


Figure 25 LF Receiver Baseband

LF Telegram Format

The LF Receiver Baseband requires that an LF Telegram contain at least two elements: a Preamble sequence and a Synchronization Pattern. The LF Telegram may also contain a user defined "wakeup ID" field which may be either 8-bits or 16-bits in length. The LF Receiver baseband supports matching against two different wakeup ID patterns, allowing separate "broadcast address" and "unique address" ID patterns to be implemented, for example. Finally, an LF Telegram will typically contain at least one data bit, so the reception of data as individual bits or groups of 8-bit bytes is supported. The CPU must handle the unloading of buffered data bits or bytes to prevent data overflow. The LF Receiver Baseband is configured for a specific LF Telegram format via the SFR LFPCFG. **Figure 26** illustrates typical LF Telegram formats and the relationship of the telegram elements.

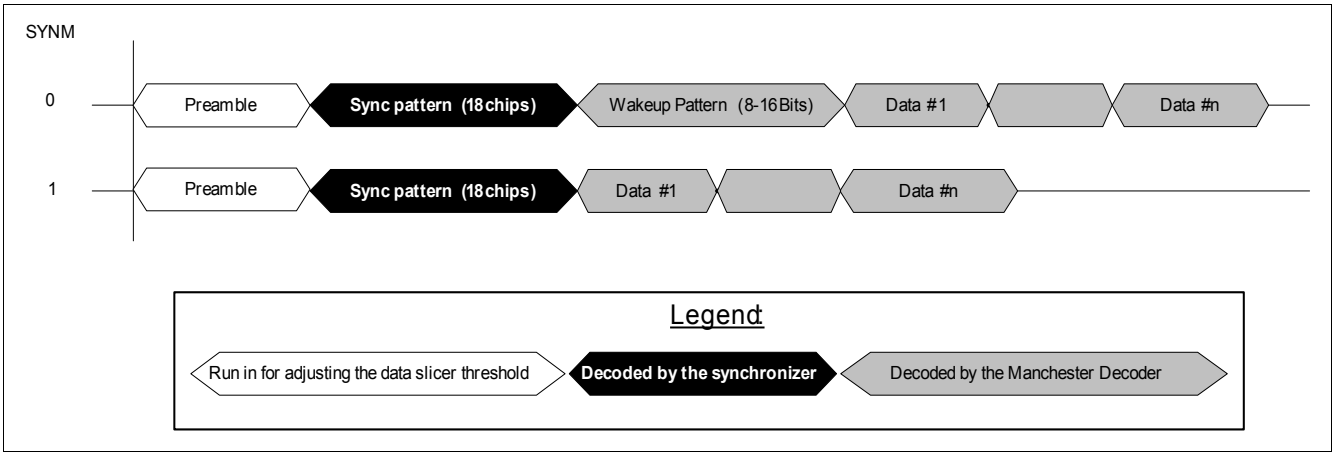


Figure 26 LF Receiver Baseband Configurations

An LF Telegram must begin with a Preamble sequence, which serves to stabilize the LF Data Threshold within the LF Analog Front End. The Preamble typically consists of several Manchester symbols, all of equal value (i.e. all '0' or all '1' bits). A Preamble may consist of mixed value bits, but in this case the duration of the Preamble must be longer than that required for equal value bits. There is no maximum duration for the Preamble. The "raw data" output of the LF Data Comparator may be observed via the SFR bit LFRXS.5[LFRAW].

A Synchronization ("Sync") pattern must follow the Preamble. The Sync pattern is 9.5 bits (18 chips) in duration, and includes non-Manchester symbols so that it is not possible to accidentally encounter the Sync pattern in any other portion of a properly formatted LF Telegram. The Sync Matching circuit within the LF Receiver Baseband is responsible for monitoring the raw data output of the LF Data Comparator and determining when a Sync pattern has been received. Detection of the Sync pattern (a "Sync match") will cause the SFR bit LFRXS.1[SYNCIND] to be set, and may be used as a CPU wakeup event. **Figure 27** provides more detail relating to the Preamble sequence and Sync pattern.

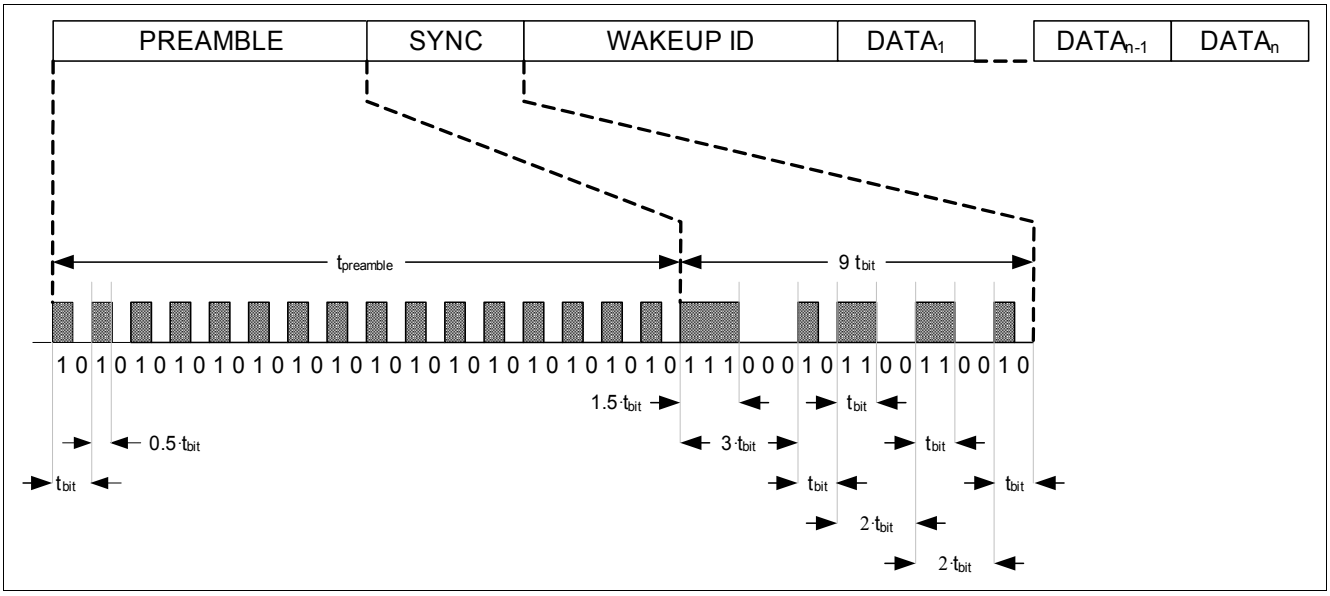


Figure 27 LF Telegram Format

The LF Telegram data payload must follow the synchronization pattern, and may be of any arbitrary length. **Figure 28** illustrates the relationship between modulated Manchester symbols and decoded data bits. In the case that the LF Receiver Baseband is configured to detect a Wakeup ID pattern, the first 8 or 16 bits (depending on length of the wakeup ID) will be considered as ID bits rather than as data bits. Detection of a Wakeup ID pattern (a "Pattern Match") may be used as a CPU wakeup event. Decoding and buffering of incoming LF Telegram bits will continue until the Manchester Decoder within the baseband encounters a decoding error (code violation) or until the LF Receiver Baseband is disabled. A decoding error will cause the SFR bit LFRXS.6[DECERR] to be set and SFR bit LFRXC.1[SYNCIND] to be cleared.

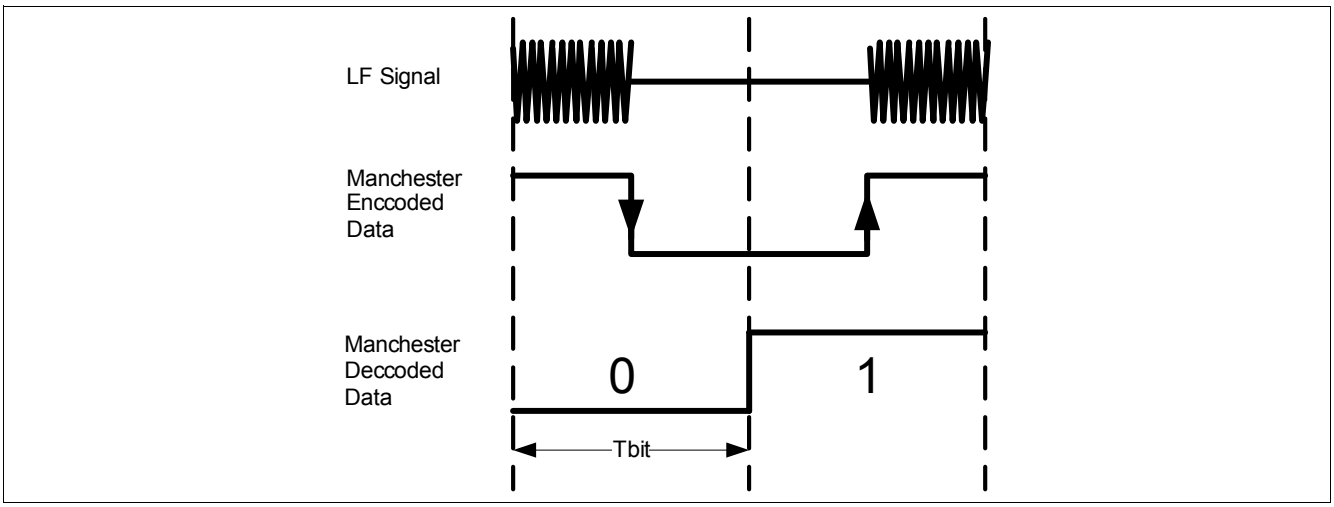


Figure 28 LF Decoder

LF Telegram Mode Settling Time

LF Telegram reception using the LF Receiver Baseband requires some "startup time" to elapse after it is enabled. When the LF Receiver is brought from any other mode (typically "off") into Baseband Mode 1, there is a settling time that must be allowed to elapse before any LF telegram reception may begin.

The sequence of events that take place when Baseband Mode 1 is enabled is shown in **Figure 29**. When the LF Receiver is brought from any other mode into Baseband Mode 2, the LF Carrier Detector auto-calibration time must be allowed to elapse before any LF telegram reception may begin (in Mode 2 the auto-calibration and telegram mode settling times are coincident. The auto-calibration time is always greater than telegram mode settling time, so only the former needs to be considered for timing purposes). The startup sequence for LF Baseband Mode 2 is similar to that for LF Carrier Detection as shown in **Figure 24**. When the LF Receiver Baseband is used in conjunction with the LF Receiver On/Off Timer, the result is a self-polling LF data interface. The appropriate startup time requirement (**"Settling time" on Page 156** for Mode 1, **"Auto-Calibration time" on Page 157** for Mode 2) must be considered and enabled via the SFR bits LFRX1.5:4[ACT]. Furthermore, the startup time must also be included within the LF "On time" duration when configuring the LF Receiver On/Off Timer.

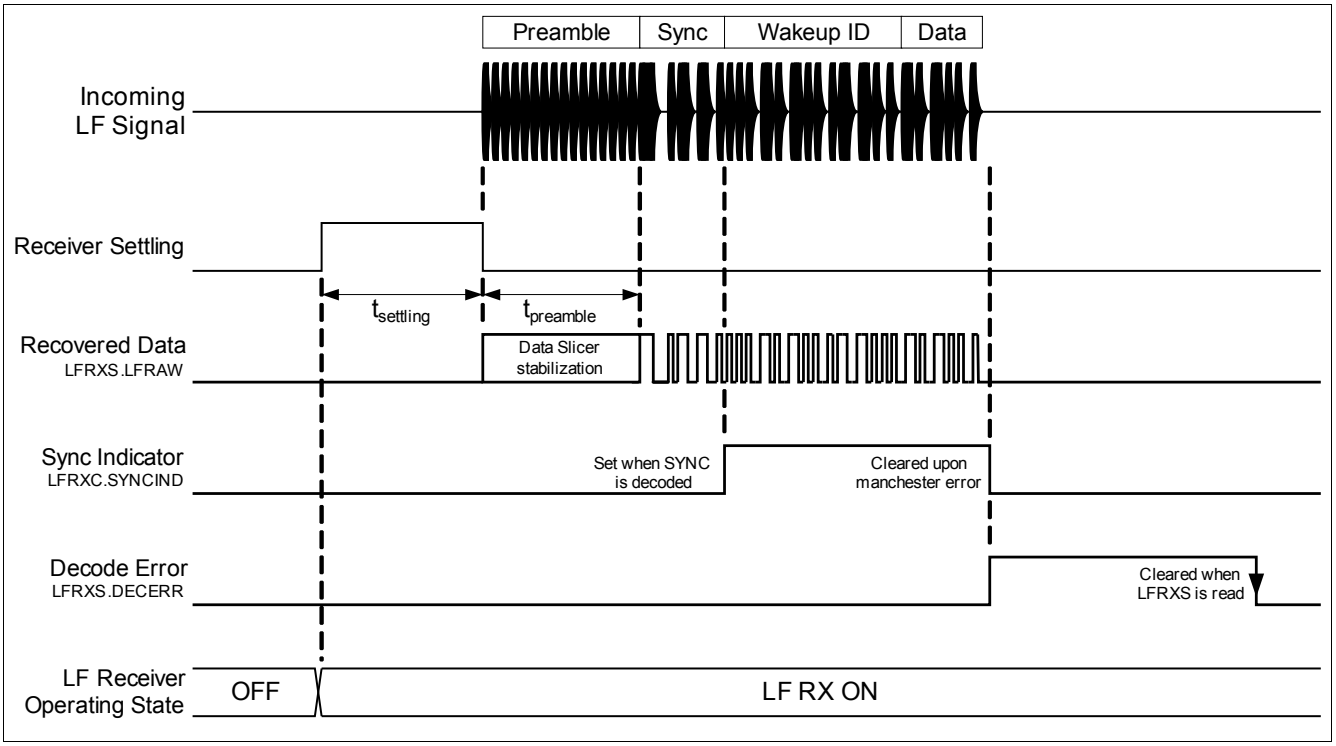


Figure 29 LF Receiver Baseband Telegram Timing

LF Bitrate Generator Calibration

A ROM Library function which automatically configures the bitrate clock divider SFR LFDIV is available. It automatically compensates drift and offset of the RC LF Oscillator.

The ROM Library function compares the current RC LF Oscillator frequency towards the highly accurate crystal oscillator frequency and configures the SFR LFDIV according to frequency of the RC LF Oscillator.

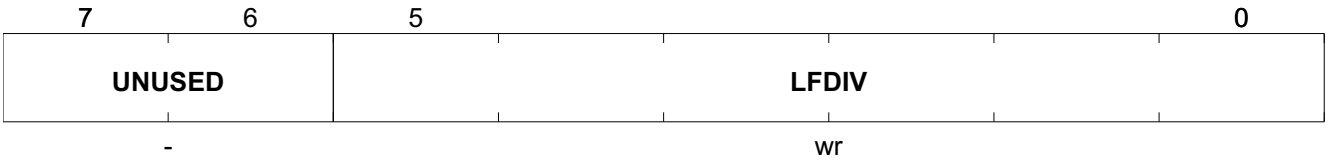
Attention: It is mandatory to call ROM Library function "LF_BaudrateCalibration" at least once before the LF Receiver is used. It is recommended to store the SFR LFDIV value into the FLASH and reprogram SFR LFDIV with such a value anytime the LF Receiver is operated.

The bitrate tolerance is specified in **Table 38 "LF Receiver Telegram, Vbat = 2.1 V...3.6 V, fLF = 120 kHz...130 kHz" on Page 156**; it can only be achieved with the usage of this ROM Library function and under the specified conditions.

If this calibration is performed regularly by the application, the bitrate tolerance for the transmitted data can be increased compared to this specified value. For details on the ROM Library function see **[1]**.

LF Bitrate Divider Factor

LFDIV	Offset	Wakeup Value	Reset Value
LF Bitrate Divider Factor	**$B4_H$**	**$00UUUUUU_B$**	**17_H**



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
LFDIV	5:0	wr	**LF Bitrate Divider** LF Bitrate generator division factor. The reset value corresponds to an LF baudrate of 3.9 kbit/s Reset: 17_H

3.17 Wakeup Pattern Detector

Two independent wakeup patterns - each with a length of 8 or 16 bits (SFR bit LFPCFG.1[PSL]) are available (SFR LFP1L/H and SFR LFP0L/H).

SFR bit LFPCFG.0[PSEL] determines on which pattern (pattern 0 only, or either pattern 0 or pattern 1) a wakeup can occur.

Note: The Wakeup must be enabled in addition in the SFR WUM (see ***Table "Wakeup Mask Register" on Page 49****) to globally enable the wakeup on LF Patterns.*

LF Pattern Detection Configuration Register

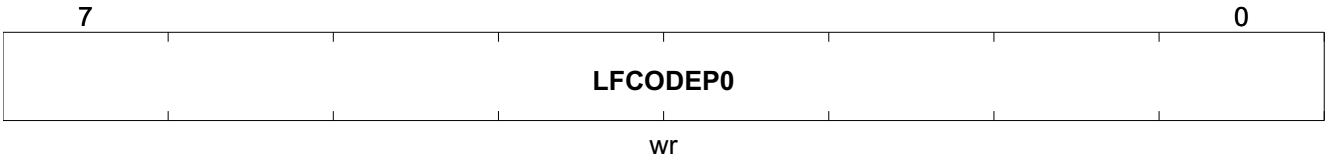
LFPCFG	Offset	Wakeup Value	Reset Value
LF Pattern Detection Configuration Register	**$C7_H$**	**$00UU00UU_B$**	**00_H**

7	6	5	4	3	2	1	0
UNUSED		Res	**SYNM**	**UNUSED**		**PSL**	**PSEL**
-			wr	-		wr	wr

Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
Res	5		**Reserved** This bit must be set to 0_B. Reset: 0_H
SYNM	4	wr	**LF Synchronizer Mode** 0_B Sync and Pattern match 1_B Sync match only Reset: 0_H
UNUSED	3:2	-	**UNUSED** Reset: 0_H
PSL	1	wr	**Pattern Sequence Length** 0_B 8 bit sequence 1_B 16 bit sequence Reset: 0_H
PSEL	0	wr	**Pattern Select** Selects which LF Wakeup Pattern (P0 or P0 and P1) can cause an LF Pattern Match Wakeup. 0_B LFP0 Pattern Detection Enable 1_B LFP0 and LFP1 Pattern Detection Enable Reset: 0_H

LF Pattern 0 Detector Sequence Data MSB

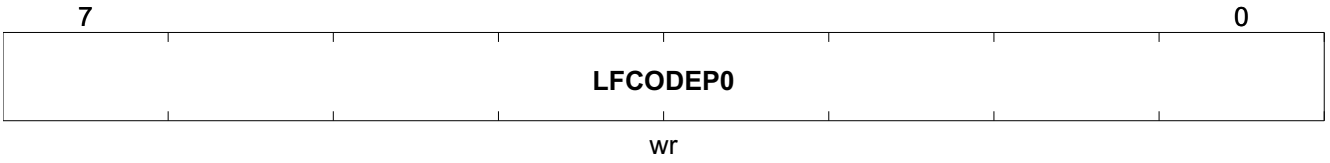
LFP0H	Offset	Wakeup Value	Reset Value
LF Pattern 0 Detector Sequence Data MSB	CD_H	UU_H	FF_H



Field	Bits	Type	Description
LFCODEP0	7:0	wr	**LF Pattern 0 Sequence Data MSB** High Byte of 16 bit pattern, ignored in case of 8 bit pattern. Reset: FF_H

LF Pattern 0 Detector Sequence Data LSB

LFP0L	Offset	Wakeup Value	Reset Value
LF Pattern 0 Detector Sequence Data LSB	CC_H	UU_H	FF_H

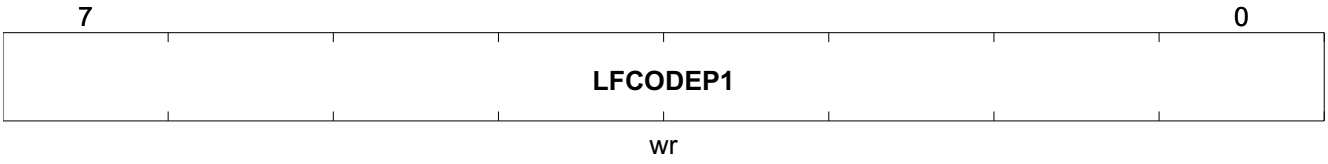


Field	Bits	Type	Description
LFCODEP0	7:0	wr	**LF Pattern 0 Sequence Data LSB** Low Byte of 16 bit pattern, or 8 bit pattern. Reset: FF_H

LF Pattern 1 Detector Sequence Data MSB

Note: LFP1H and LFP1L may be used as two additional GPR registers (value maintained during powerdown, but not in event of RESET) if only wakeup on Pattern Match 0 is required.

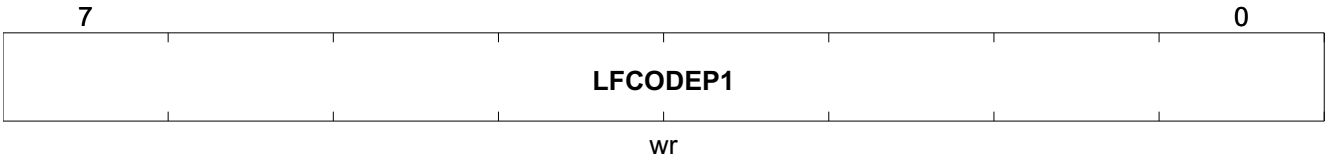
LFP1H	Offset	Wakeup Value	Reset Value
LF Pattern 1 Detector Sequence Data MSB	CF_H	UU_H	FF_H



Field	Bits	Type	Description
LFCODEP1	7:0	wr	**LF Pattern 1 Sequence Data MSB** High Byte of 16 bit pattern, ignored in case of 8 bit pattern. Reset: FF_H

LF Pattern 1 Detector Sequence Data LSB

LFP1L	Offset	Wakeup Value	Reset Value
LF Pattern 1 Detector Sequence Data LSB	CE_H	UU_H	FF_H



Field	Bits	Type	Description
LFCODEP1	7:0	wr	**LF Pattern 1 Sequence Data LSB** Low Byte of 16 bit pattern, or 8 bit pattern. Reset: FF_H

3.18 LF Receiver Data Interface

LF Receiver Data Interface

The received data can be read by the microcontroller using the following different interfaces:

- 8 bit databyte (synchronized, Manchester decoded)
- Serial bitstream data (synchronized, Manchester decoded)
- RAW data (synchronized, chip level)
- RAW Carrier Detect (un-synchronized)

8 Bit databyte

Synchronized and decoded databytes are received using SFR LFRXD.

Decoded bits are shifted into an 8 bit receive buffer, until a byte boundary is reached. The received byte is then shifted into the SFR LFRXD, and a flag SFR bit LFRXS.3[LFDP] is set, while the following byte is shifted into the receive buffer. If the SFR LFRXD is not read before the following byte is received, it will be overwritten, and an overflow flag SFR bit LFRXS.4[LFDOV] is set.

Serial bitstream data

Synchronized and decoded serial data can be received by using SFR bit LFRXS.0[LFDATA].

A flag SFR bit LFRXS.1[LFBP] is set if data is pending, while the following bit is buffered. If the SFR bit LFRXS.0[LFDATA] is not read before the following bit is received, it will be overwritten, and an overflow flag SFR bit LFRXS.2 [LFOV] is set.

RAW data

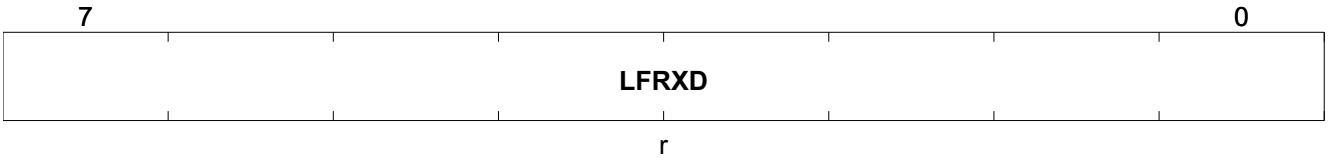
Synchronized and undecoded serial data can be read by the microcontroller using SFR bit LFRXS.5[LFRAW]. This can be used to handle any other coding scheme than Manchester. This bit is the RAW output after the synchronizer, thus the decoding (including identifying the beginning/end of a bit period) has to be done by the application software.

RAW Carrier Detect

Un-synchronized and undecoded serial data can be read by the microcontroller using SFR bit LFRXS.7 [CDRAW]. This indicates if a Carrier Signal is currently present (SFR bit LFRXS.7[CDRAW]==1) or not (SFR bit LFRXS.7[CDRAW]==0). The application software can perform the LF baseband processing; in order to implement non-standard LF information encoding schemes, for example.

LF Receiver Data Register

LFRXD	Offset	Wakeup Value	Reset Value
LF Receiver Data Register	$A5_H$	UU_H	00_H



Field	Bits	Type	Description
LFRXD	7:0	r	**LF Receiver Data** Reset: 00_H

LF Receiver Status Register

LFRXS	Offset	Wakeup Value	Reset Value
LF Receiver Status Register	$A4_H$	$XUXUUUUU_B$	$X0X00000_B$

7	6	5	4	3	2	1	0
CDRAW	DECERR	LFRAW	LFDOV	LFDP	LFOV	LFBP	LFDATA
r	rc	r	rc	r	rc	rc	r

Field	Bits	Type	Description
CDRAW	7	r	**Carrier Detector Raw Data** Instantaneous value of comparison of LF Carrier versus the LF Carrier Detect Threshold. Reset: X_B
DECERR	6	rc	**Manchester Decode Error** 0_B No error detected 1_B Error detected Reset: 0_H
LFRAW	5	r	**LF Receiver Raw Data** Instantaneous output of the LF Data slicer. Reset: X_B
LFDOV	4	rc	**LF Data Byte Overwritten** This bit will be set if a new LF data byte is received prior to the previous byte being read from SFR LFRXD. Reset: 0_H
LFDP	3	r	**LF Data Byte Pending** This bit will be set if a new LF data byte is available in SFR LFRXD. It will be cleared when the LFRXD register is read. Reset: 0_H
LFOV	2	rc	**LF Serial Decoded Data Overwritten** This bit will be set if a new LF data bit is received prior to the previous bit being read from LFDATA. Reset: 0_H
LFBP	1	rc	**LF Serial Decoded Data Pending** This bit will be set if a new LF data bit is available in LFDATA. Reset: 0_H
LFDATA	0	r	**LF Serial Decoded Data** 0_B Manchester 0 decoded 1_B Manchester 1 decoded Reset: 0_H

3.19 16 Bit CRC (Cyclic Redundancy Check) Generator/Checker

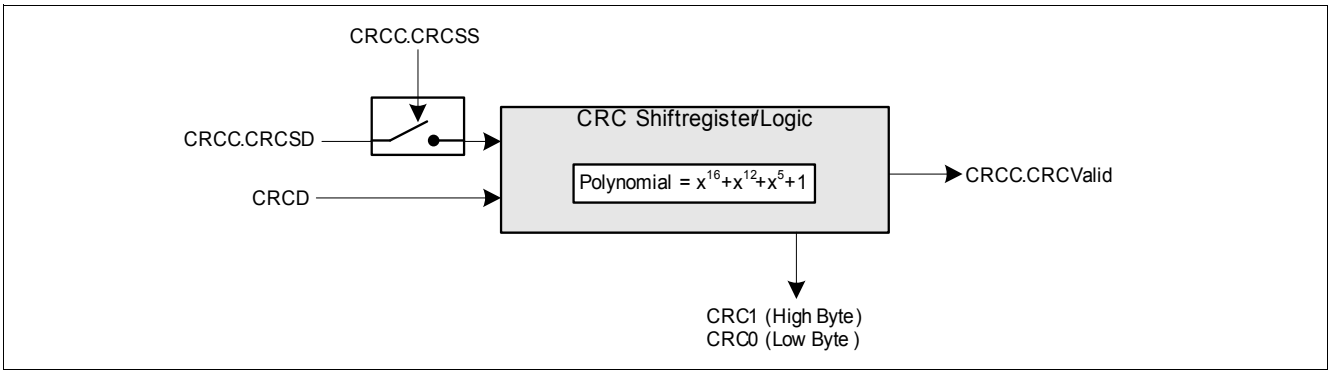


Figure 30 CRC (Cyclic Redundancy Check) Generator/Checker

CRC is a powerful method to detect errors in data packets that have been transmitted over a distorted connection. The CRC Generator/Checker divides each byte of a data packet by a polynomial, leaving the remainder which represents the checksum. The CRC-Generator/Checker is using the 16 Bit CCITT polynomial x16+x12+x5+1. The 16 bit start value is determined by the initial contents of SFR CRC0 and SFR CRC1.

CRC Generation and Checking

Figure 31 shows the basic usage of the CRC16.

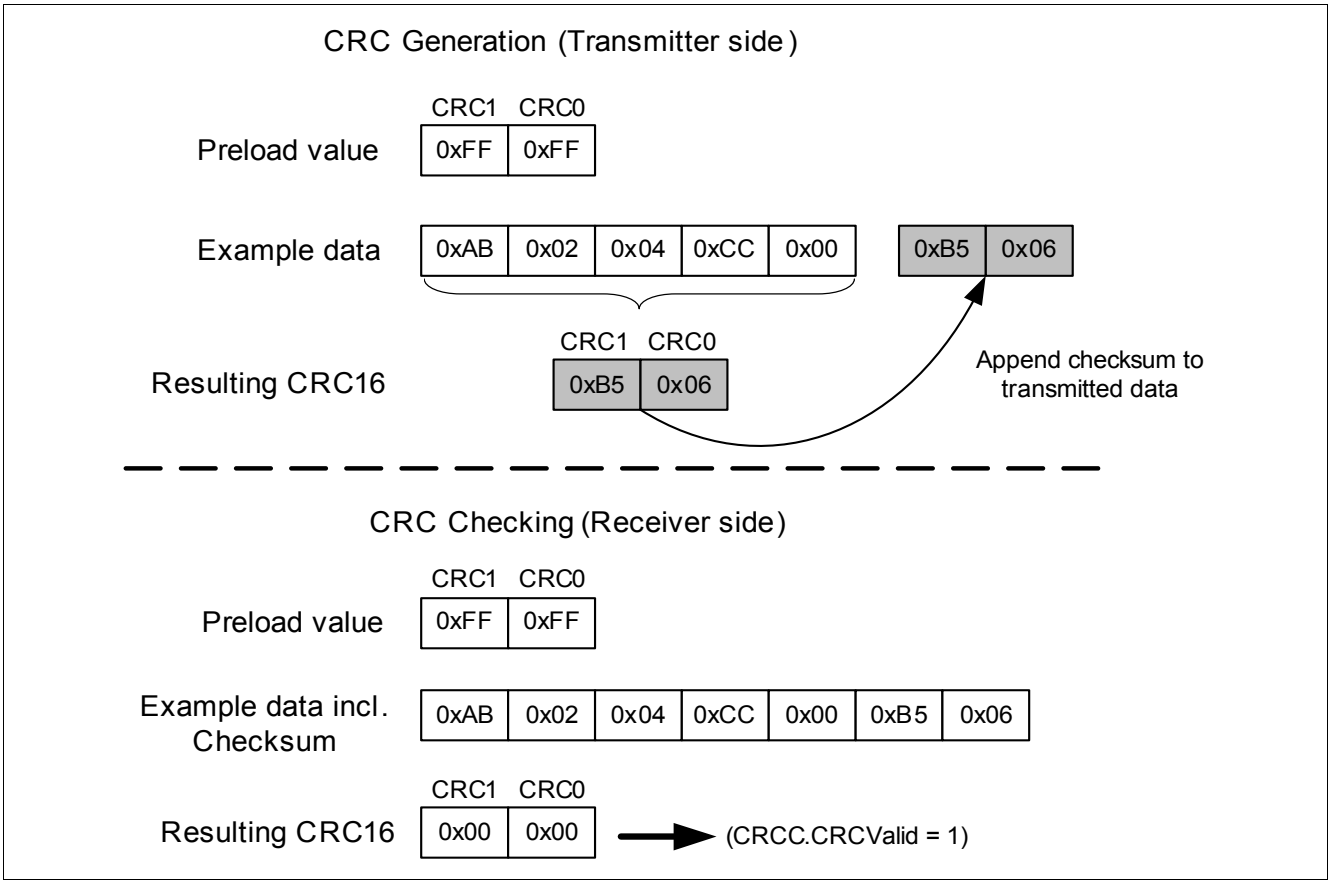


Figure 31 Example for CRC16 usage

Byte aligned CRC Generation

CRC generation is done by executing the following steps:

- The CRC shift register has to be initialized by writing FF_H (or if desired another start value) to both SFR CRC0 and SFR CRC1.
- The databytes which are to be used for the CRC Generation have to be shifted one after the other into the SFR CRCD.The process of CRC Generation is automatically invoked when data bytes are written to the SFR CRCD.

Note: Processing the data in SFR CRCD takes 3 instruction cycles, therefore the application has to assure that there are no consecutive write instructions without one extra instruction cycle between.

- The resulting checksum is available in the CRC Result Register SFR CRC0 and SFR CRC1 after the last data byte has been processed.

Byte aligned CRC Checking

CRC checking is done by executing the following steps:

- The CRC shift register has to be initialized by writing FF_H (or if desired another start value) to both SFR CRC0 and SFR CRC1.
- The databytes which should be checked have to be shifted one after the other into the SFR CRCD. It is important that the order (MSB-LSB) is the same as it was during the CRC Generation. In addition to the data the CRC16 has to be shifted into SFR CRCD as well (first the high byte then the low byte - see also **Figure 31**). The process of CRC Checking is automatically invoked when data bytes are written to the SFR CRCD.

Note: Processing the data in SFR CRCD takes 3 instruction cycles, therefore the application has to assure that there are no consecutive write instructions without one extra instruction cycle between.

Note: One instruction cycle corresponds to 6 system clock cycles.

- After the last byte is processed the SFR bit CRCC.1[CRCValid] indicates the correctness of the CRC calculation after the last data byte has been processed and both - SFR CRC0 and SFR CRC1 are 0.

Serial bitstream CRC Generation/Checking

The CRC Generator/Checker features a serial mechanism to perform CRC generation and checking of non byte-aligned data streams. In this case SFR bit CRCC.5[CRCSS] and SFR bit CRCC.6[CRCSD] are used instead of SFR CRCD.

The data stream is written bit by bit into SFR bit CRCC.6[CRCSD]. Each bit is processed by setting the flag SFR bit CRCC.5[CRCSS].

The following figure shows an example for the usage of SFR bit CRCC.5[CRCSS] and SFR bit CRCC.6[CRCSD].

Note: No time limitations apply when using serial data, so the software can shift and strobe without any wait states between processing consecutive bits.

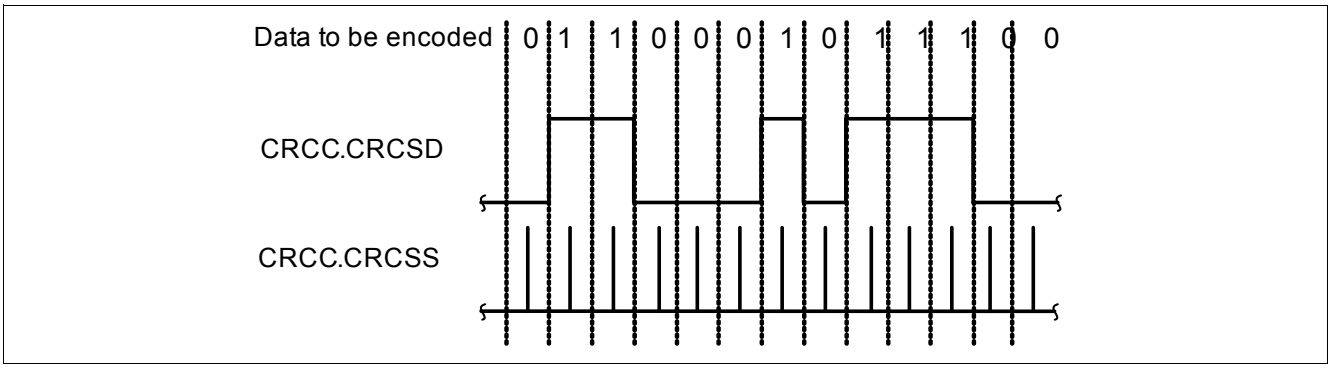


Figure 32 Example for serial CRC generation/checking

Note: The serial and byte-aligned generation/checking mechanism is interchangeable within the same generation/checking process.
Example: If a data packet consists of 18 bits, 16 bits can be processed byte-aligned via SFR CRCD and the two remaining bits can be processed bit-aligned by using SFR bit CRCC.5[CRCSS] and SFR bit CRCC.6[CRCSD].

CRC Control Register

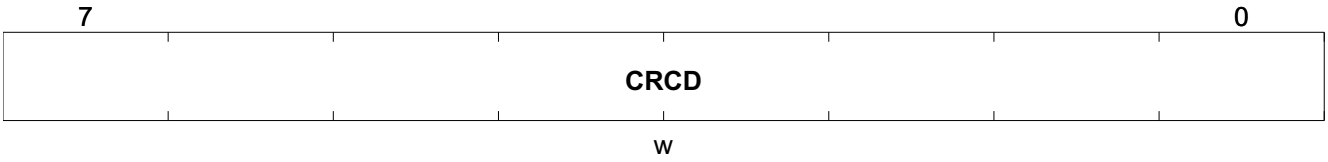
CRCC	Offset	Wakeup Value	Reset Value
CRC Control Register	**$A9_H$**	**02_H**	**02_H**

7	6	5	4	2	1	0
UNUSED	**CRCSD**	**CRCSS**	**UNUSED**		**CRCVALID**	**UNUSED**
-	wr	w	-		r	-

Field	Bits	Type	Description
UNUSED	7	-	**UNUSED** Reset: 0_H
CRCSD	6	wr	**CRC Serial Data** Reset: 0_H
CRCSS	5	w	**CRC Serial Data Strobe** By setting this bit the data bit from CRCSD is strobed into CRC generator/checker Reset: 0_H
UNUSED	4:2	-	**UNUSED** Reset: 0_H
CRCVALID	1	r	**CRC Valid** This bit is set automatically when all CRC result bits are zero. 0_B CRC check failed 1_B CRC check successful Reset: 1_H
UNUSED	0	-	**UNUSED** Reset: 0_H

CRC Data Register

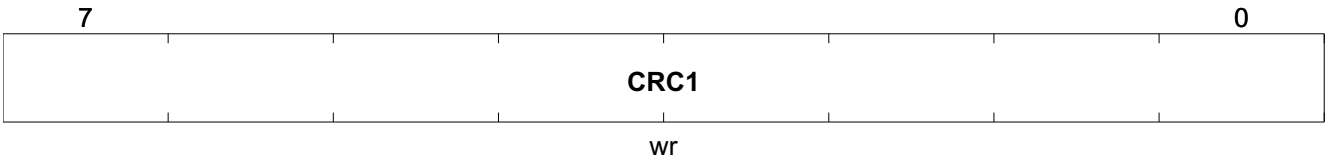
CRCD	Offset	Wakeup Value	Reset Value
CRC Data Register	AA_H	00_H	00_H



Field	Bits	Type	Description
CRCD	7:0	w	**CRC Data Register** Reset: 00_H

CRC Shift Register 1 (high byte)

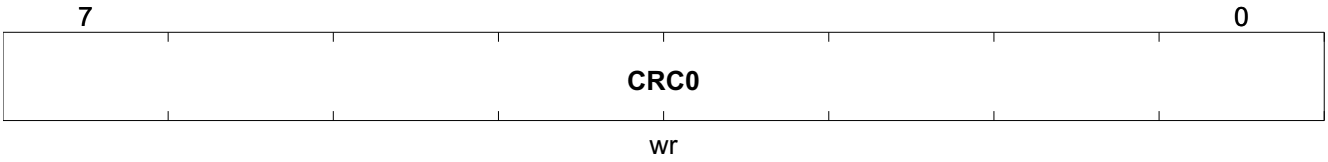
CRC1	Offset	Wakeup Value	Reset Value
CRC Preload/Result Register 1 (high byte)	AD_H	00_H	00_H



Field	Bits	Type	Description
CRC1	7:0	wr	**CRC Preload/Result Register 1 (high byte)** Reset: 00_H

CRC Shift Register 0 (low byte)

CRC0	Offset	Wakeup Value	Reset Value
CRC Preload/Result Register 0 (low byte)	**AC_H**	**00_H**	**00_H**



Field	Bits	Type	Description
CRC0	7:0	wr	**CRC Preload/Result Register 0 (low byte)** Reset: 00_H

3.20 Pseudo Random Number Generator

The SP37T offers a Pseudo Random Number Generator. It consists of a Maximum Length Linear Feedback Shift Register (MLFSR) as built in hardware unit which creates a new pseudo random number everytime SFR bit CFG1.5[RNGEn] is set.

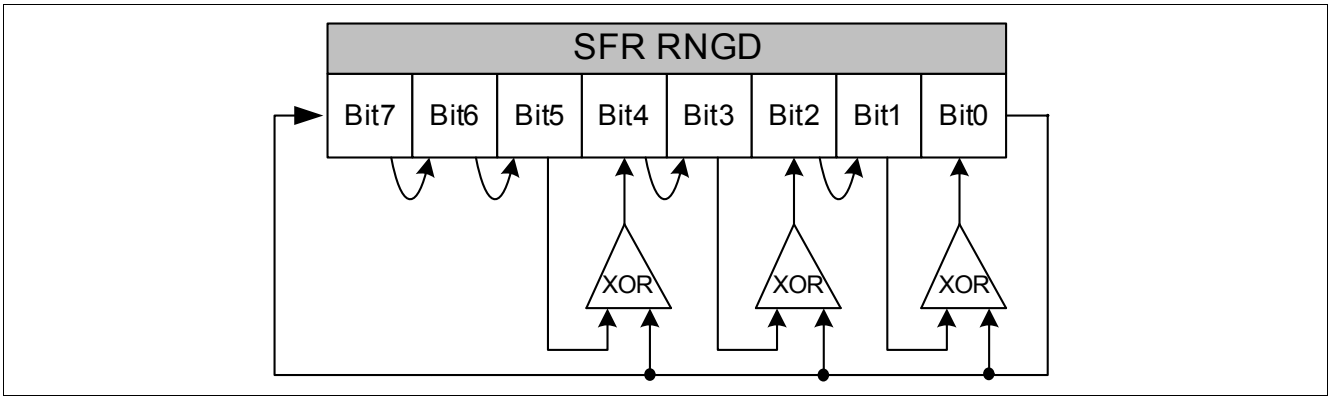


Figure 33 Shift Register Implementation

A user-defined start value (except 00_H) can be written to SFR RNGD. The default value is 55_H.

The generation of a new random number is initiated by setting SFR bit CFG1.5[RNGEn]. The random number generation requires one systemclock cycle, thus the application can read the generated number in the next instruction without any extra wait states.

Random Number Generator Data Register

RNGD	Offset	Wakeup Value	Reset Value
Random Number Generator Data Register	**AB_H**	**UU_H**	**55_H**

7							0
RNGD							
wr							

Field	Bits	Type	Description
RNGD	7:0	wr	**Random Number Generator Data Register** Reset: 55_H

3.21 Timer Unit

The SP37T comprises two independent 16 bit timers which operate as down counters. Different timer modes are available for extended functionality.

Basic Timer Configuration

Timer 0 and Timer 1 comprise two fully programmable 16-bit timers, which can be used for time measurements as well as generating time delays. The clock source is selectable in order to enlarge the timer runtime.SFR TMOD is used to select the clock source and the desired timer mode.

Setting the SFR bit TCON.0[T0Run] (respectively SFR bit TCON.4[T1Run]) starts Timer 0 (resp. Timer 1). The Timer counts down from the start values SFR TH/L0 (resp. SFR TH/L1) using the selected counter clock (see SFR TMOD) until the timer is elapsed. SFR bit TCON.1[T0Full] (resp. SFR bit TCON.5[T1Full]) is set.

Note: The timer full flag is set when the timer would underflow from 0000_H ==> FFFFH. To count e.g. 10 events with timer 0 SFR TL0 has to be configured to 9H instead of 0AH.

After a timer is elapsed there are two possibilities that can occur (dependant on the selected timer mode):

- **Reload:** If the selected timer mode uses timer reload, the timer is automatically reloaded and restarted.
- **Stop:** If the selected timer mode doesn't use timer reload, the timer is stopped and SFR bit TCON.0[T0Run] (resp. SFR bit TCON.4[T1Run]) is cleared.

Timer Modes

Timer mode 0

Comprises:

- 16 bit timer with reload

The timer unit is configured as one 16 bit reloadable timer.

SFR TL0 and SFR TH0 hold the start value.

When SFR bit TCON.0[T0Run] is set, the timer starts counting down.

SFR bit TCON.1[T0Full] is set when the timer is elapsed.

The timer value is reloaded from SFR TL1 and SFR TH1 and the timer is restarted automatically.

SFR bit TCON.1[T0Full] has to be cleared by the application software. It is not cleared automatically on a read-access.

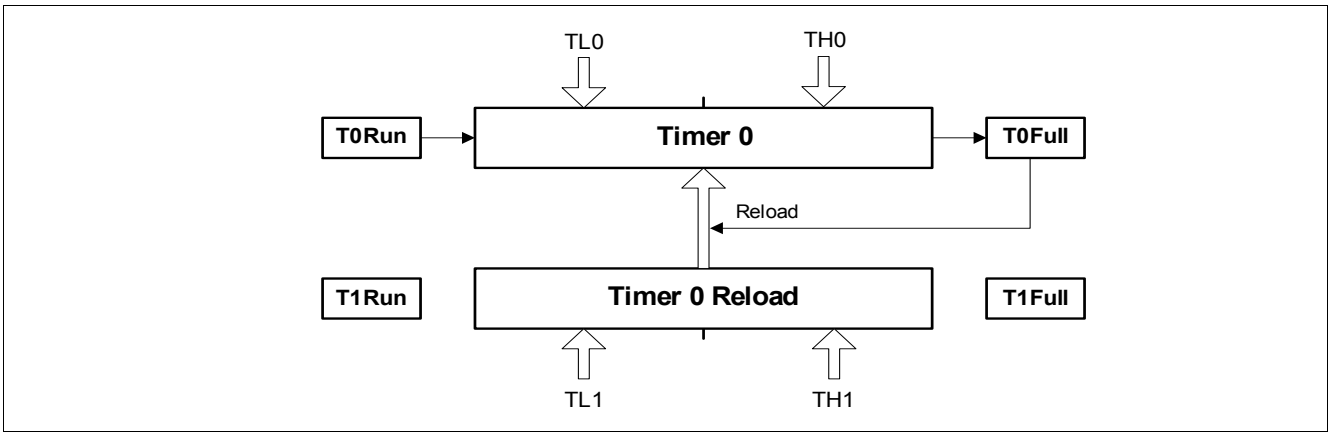


Figure 34 Timer Mode 0

Note: In this mode both SFR bit TCON.4[T1Run] and SFR bit TCON.5[T1Full] are not used.

Timer Mode 1

Comprises:

- 16 bit timer without reload
- 8 bit timer with reload and bitrate strobe signal for RF Transmitter

Timer 0 operates as a 16 bit timer with the start value in SFR TL0 and SFR TH0, timer run bit SFR bit TCON.0[T0Run] and timer elapsed indicator SFR bit TCON.1[T0Full].

If the timer is elapsed, it is stopped, SFR bit TCON.1[T0Full] is set and the timer run bit SFR bit TCON.0[T0Run] is cleared.

Timer 1 sets up a reloadable 8 bit timer holding the startup value in SFR TL1, timer reload value in SFR TH1, timer run bit in SFR bit TCON.4[T1Run] and timer elapsed indicator in SFR bit TCON.5[T1Full].

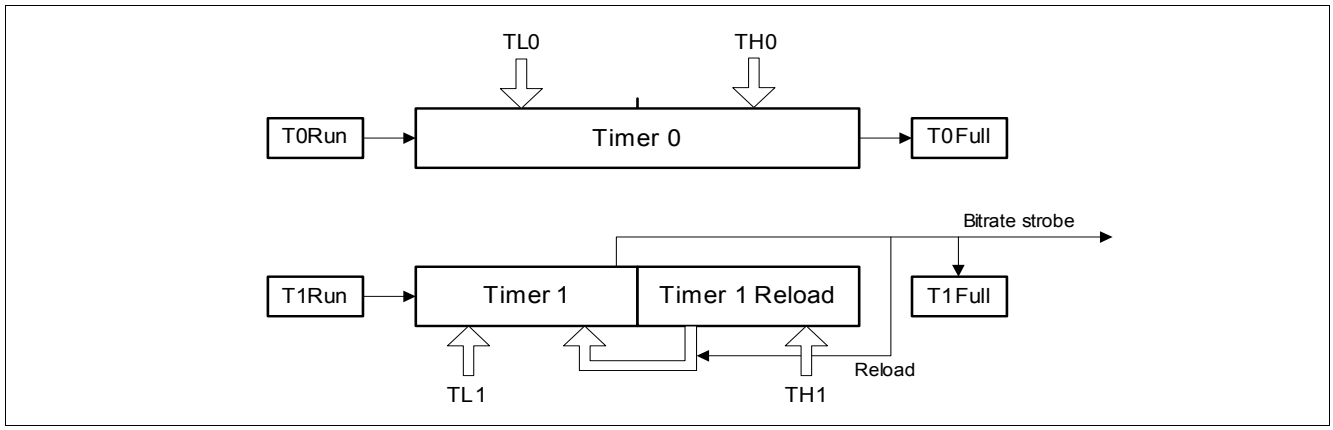


Figure 35 Timer Mode 1

Timer Mode 2

Comprises:

- 8 bit timer with reload
- 8 bit timer with reload and bitrate strobe signal for RF Transmitter

Timer 0 sets up a reloadable 8 bit timer holding the start value SFR TL0, timer reload value SFR TH0, timer run bit SFR bit TCON.0[T0Run] and timer elapsed indicator SFR bit TCON.1[T0Full].

Timer 1 sets up a reloadable 8 bit timer holding the start value SFR TL1, timer reload value SFR TH1, timer run bit SFR bit TCON.4[T1Run] and timer elapsed indicator SFR bit TCON.5[T1Full].

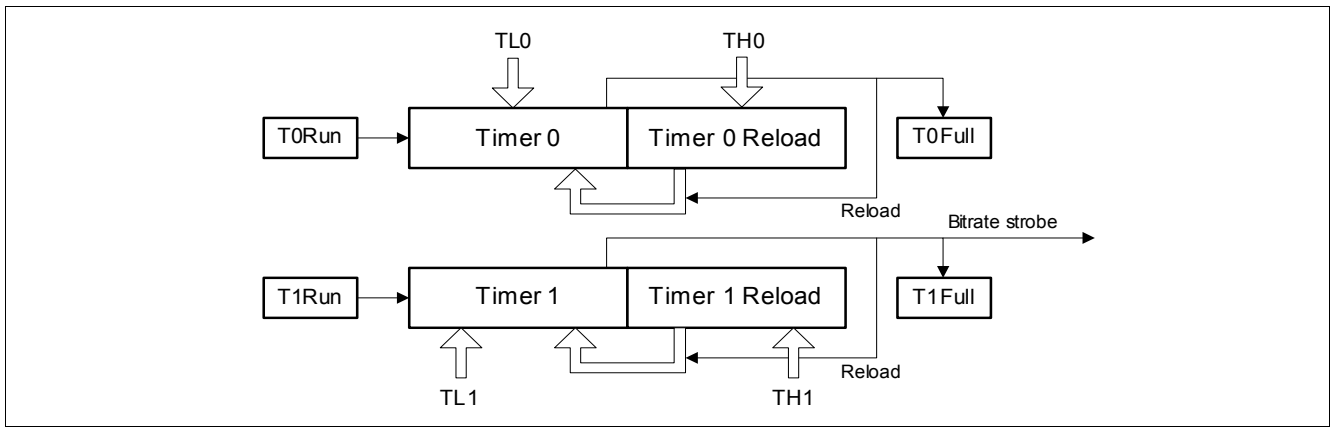


Figure 36 Timer Mode 2

Timer Mode 3

Comprises:

- 8 bit timer without reload (1)
- 8 bit timer without reload (2)
- 8 bit timer with reload and bitrate strobe signal for RF Transmitter

Timer 0 (1) uses SFR TL0 as start value.

Setting SFR bit TCON.0[T0Run] starts the timer.

SFR bit TCON.1[T0Full] is set when the timer is elapsed.

SFR bit TCON.0[T0Run] is cleared automatically when the timer is elapsed.

Timer 0 (2) uses SFR TH0 as start value.

Setting SFR bit TCON.4[T1Run] starts the timer.

SFR bit TCON.5[T1Full] is set when the timer is elapsed.

SFR bit TCON.4[T1Run] is cleared automatically when the timer is elapsed.

Timer 1 operates as a dedicated 8 bit bitrate timer for the RF Encoder. The timer uses no Run bit or Full flag. It is started automatically when the timer mode is activated.

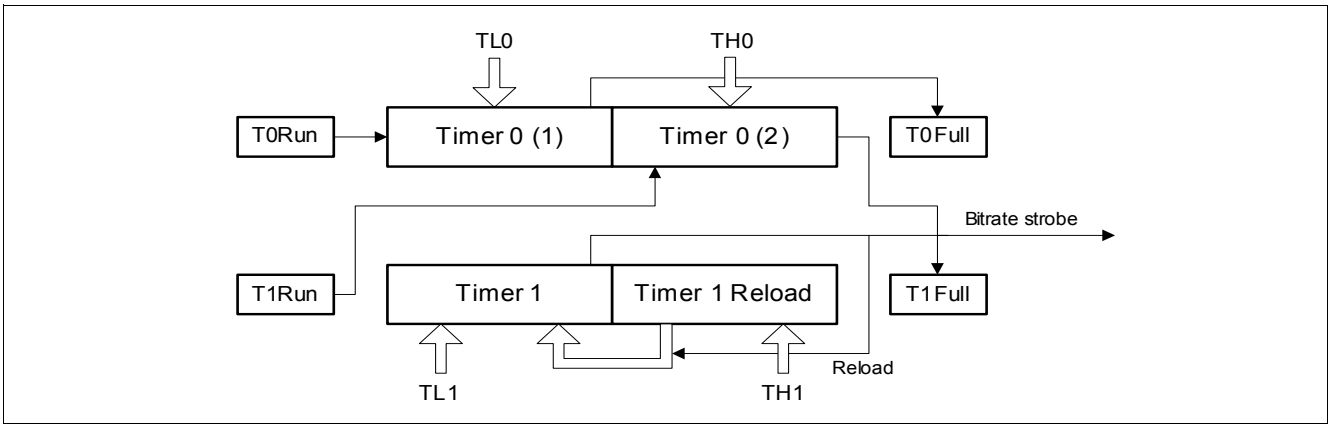


Figure 37 Timer Mode 3

Timer mode 4

Comprises:

- 16 bit timer with reload and bitrate strobe signal for RF Transmitter

The timer unit is configured as one 16 bit reloadable timer.

SFR TL1 and SFR TH1 hold the start value.

If SFR bit TCON.4[T1Run] is set, the timer starts counting.

SFR bit TCON.5[T1Full] is set when the timer is elapsed.

The timer value is reloaded from SFR TL0 and SFR TH0 and the timer is restarted automatically.

SFR bit TCON.5[T1Full] has to be cleared by the application software. It is not cleared on read-access.

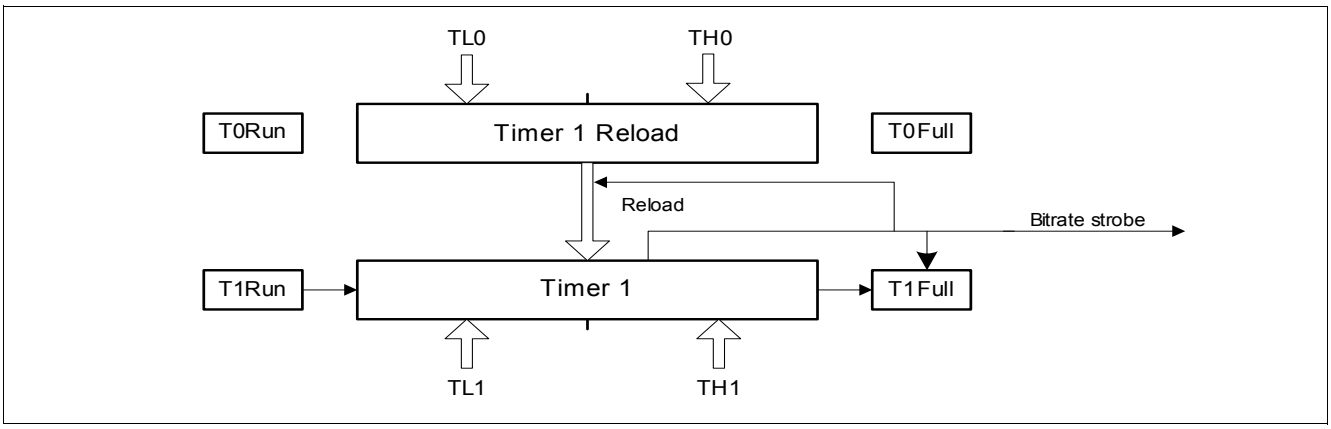


Figure 38 Timer mode 4

Note: In this mode both SFR bit TCON.0[T0Run] and SFR bit TCON.1[T0Full] are not used.

Timer Mode 5

Comprises:

- 8 bit timer with reload
- 16 bit timer without reload and bitrate strobe signal for RF Transmitter

Timer 0 sets up a reloadable 8 bit timer holding the start value in SFR TL0, timer reload value in SFR TH0, timer run bit SFR bit TCON.0[T0Run] and timer elapsed indicator in SFR bit TCON.1[T0Full].

Timer 1 operates as a 16 bit timer with the start value in SFR TL1 and SFR TH1, timer run bit SFR bit TCON.4[T1Run] and timer elapsed indicator SFR bit TCON.5[T1Full]. If the timer is elapsed the timer is stopped, SFR bit TCON.5[T1Full] is set and the timer run bit SFR bit TCON.4[T1Run] is cleared.

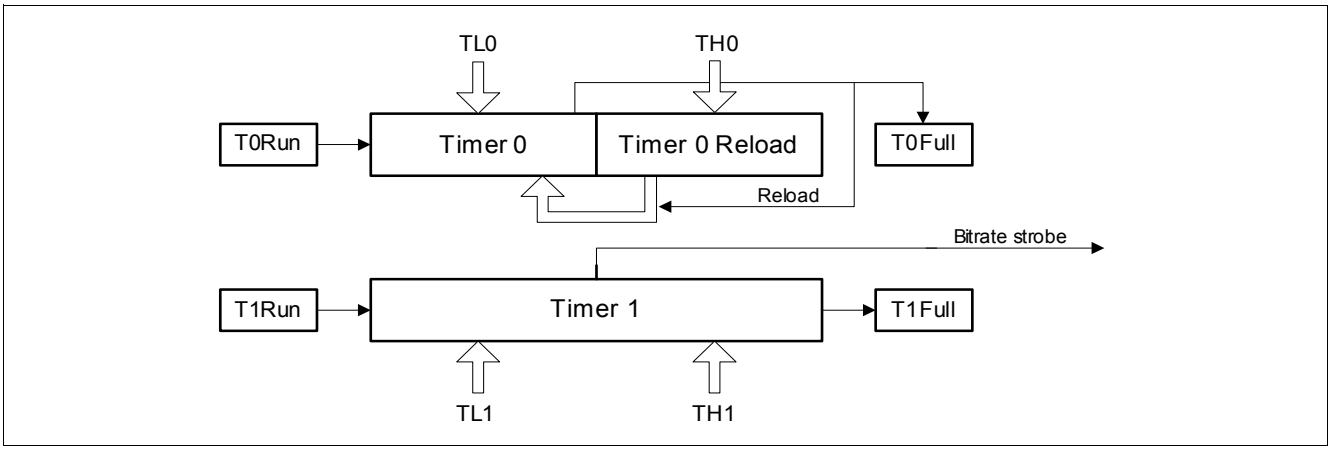


Figure 39 Timer Mode 5

Timer Mode 6

Comprises:

- 16 bit timer without reload
- 16 bit timer without reload and bitrate strobe signal for RF Transmitter

Timer 0 operates as a 16 bit timer with the start value in SFR TL0 and SFR TH0, timer run bit SFR bit TCON.0[T0Run] and timer elapsed indicator SFR bit TCON.1[T0Full].
If the timer is elapsed the timer is stopped, SFR bit TCON.1[T0Full] is set and the timer run bit SFR bit TCON.0[T0Run] is cleared.

Timer 1 operates as a 16 bit timer with the start value in SFR TL1 and SFR TH1, timer run bit SFR bit TCON.4[T1Run] and timer elapsed indicator SFR bit TCON.5[T1Full].
If the timer is elapsed the timer is stopped, SFR bit TCON.5[T1Full] is set and the timer run bit SFR bit TCON.4[T1Run] is cleared.

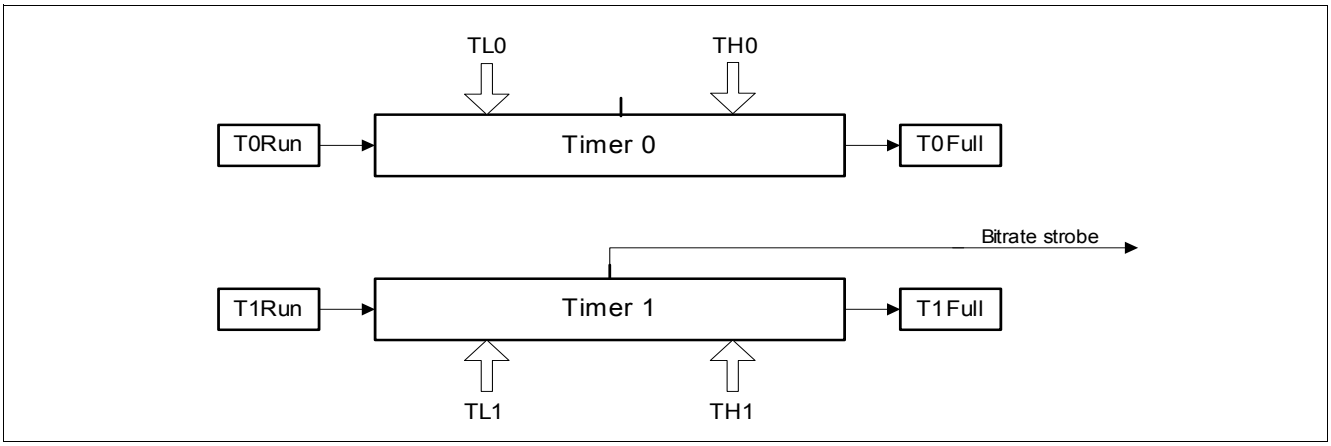


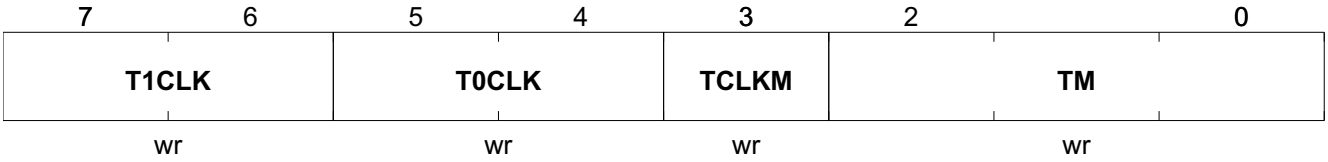
Figure 40 Timer Mode 6

Timer Mode 7

This timer mode is not available for application usage. It is used by the ROM library functions for calibration purpose.

Timer Mode Register

TMOD	Offset	Wakeup Value	Reset Value
Timer Mode Register	89_H	00_H	00_H



Field	Bits	Type	Description
T1CLK	7:6	wr	**Timer 1 Clock Source Select** 00_B System clock 01_B If TCLKM = 0: System clock divided by SFR DIVIC and 8 If TCLKM = 1: Crystal Oscillator divided by 4 10_B 4kHz (2*2kHz LP RC Oscillator) 11_B If TCLKM = 0: PP2 event count (rising edge) Reset: 0_H
T0CLK	5:4	wr	**Timer 0 Clock Source Select** 00_B System clock 01_B If TCLKM = 0: System clock divided by SFR DIVIC and 8 If TCLKM = 1: Crystal Oscillator divided by 4 10_B 4kHz (2*2kHz LP RC Oscillator) 11_B If TCLKM = 0: Timer 1 underflow event count Reset: 0_H
TCLKM	3	wr	**Timer Unit Crystal Clock Source Enable** If TCLKM is set to 1, then Crystal Oscillator is available as T0 and T1 clock source, refer to T0CLK and T1CLK. When TCLKM is set, the Crystal Oscillator is automatically enabled. When TCLKM is cleared, the crystal oscillator will be disabled unless required by other functional blocks (e.g. during RF transmission, or while SFR CFG0.EnXOSC = 1). *Note: It is recommend to call StartXtalOsc() ROM library function prior to setting TCLKM.* 0_B Crystal Oscillator is not available as Timer clock source 1_B Crystal Oscillator is available as Timer clock source Reset: 0_H

Field	Bits	Type	Description
TM	2:0	wr	**Timer Mode** 000_B Mode 0: 16 bit timer w/ reload and no baudrate strobe 001_B Mode 1: 16 bit timer w/o reload and 8 bit timer w/ reload 010_B Mode 2: two 8 bit timers w/ reload 011_B Mode 3: two 8 bit timers w/o reload and 8 bit timer w/ reload 100_B Mode 4: 16 bit timer w/ reload 101_B Mode 5: 8 bit timer w/ reload and 16 bit timer w/o reload 110_B Mode 6: two 16 bit timer w/o reload 111_B Mode 7: Not available for application use Reset: 0_H

Timer Control Register

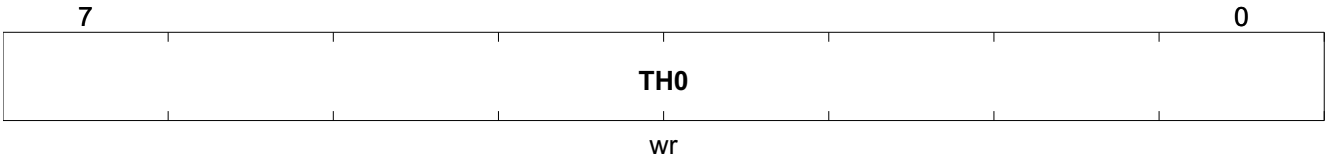
TCON	Offset	Wakeup Value	Reset Value
Timer Control Register	88_H	00_H	00_H

7	6	5	4	3	2	1	0
UNUSED		T1FULL	T1RUN	UNUSED		T0FULL	T0RUN
-		wr	wr	-		wr	wr

Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
T1FULL	5	wr	**Timer 1 Full Flag** Set if a Timer 1 underflow has occurred. Reset: 0_H
T1RUN	4	wr	**Timer 1 Run** 0_B Timer 1 is stopped 1_B Timer 1 counts downward Reset: 0_H
UNUSED	3:2	-	**UNUSED** Reset: 0_H
T0FULL	1	wr	**Timer 0 Full Flag** Set if a Timer 0 underflow has occurred. Reset: 0_H
T0RUN	0	wr	**Timer 0 Run** 0_B Timer 0 is stopped 1_B Timer 0 counts downward Reset: 0_H

Timer 0 Register High Byte

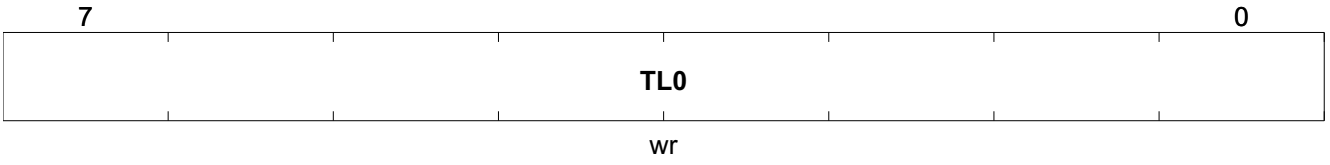
TH0	Offset	Wakeup Value	Reset Value
Timer 0 Register High Byte	$8C_H$	00_H	00_H



Field	Bits	Type	Description
TH0	7:0	wr	**Timer 0 High Byte** Timer 0 [15:8] Reset: 00_H

Timer 0 Register Low Byte

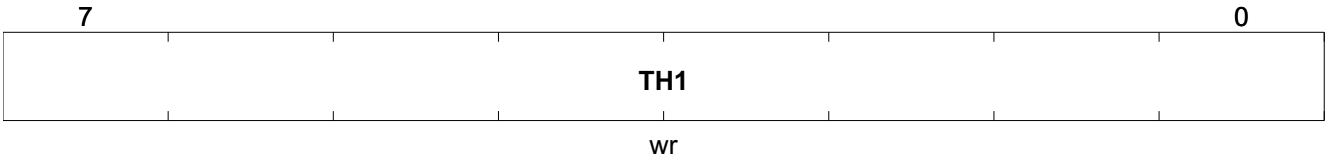
TL0	Offset	Wakeup Value	Reset Value
Timer 0 Register Low Byte	$8A_H$	00_H	00_H



Field	Bits	Type	Description
TL0	7:0	wr	**Timer 0 Low Byte** Timer 0 [7:0] Reset: 00_H

Timer 1 Register High Byte

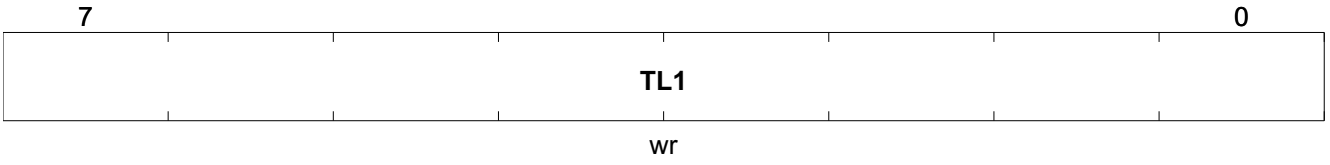
TH1	Offset	Wakeup Value	Reset Value
Timer 1 Register High Byte	$8D_H$	00_H	00_H



Field	Bits	Type	Description
TH1	7:0	wr	**Timer 1 High Byte** Timer 1 [15:8] Reset: 00_H

Timer 1 Register Low Byte

TL1	Offset	Wakeup Value	Reset Value
Timer 1 Register Low Byte	$8B_H$	00_H	00_H



Field	Bits	Type	Description
TL1	7:0	wr	**Timer 1 Low Byte** Timer 1 [7:0] Reset: 00_H

3.22 General Purpose Input/Output (GPIO)

The SP37T has three GPIO pins that are used for:

- General purpose by the application software
- Dedicated digital peripherals (**“Alternative Port Functionality” on Page 118**).
- Operating mode selection (**“Resets and Operating Mode Selection” on Page 20**)
- If configured for general purpose usage, the GPIO pins can be accessed directly by the CPU. All GPIO pins have selectable pull-up and pull-down resistors.

Note: The GPIO pins are configured as input with the pull-up resistor enabled after reset. In POWER DOWN state and THERMAL SHUTDOWN state the GPIOs keep their configuration.

Peripheral Port Configuration

The following table shows the different possible configurations for the GPIO pins.

The ’x’ in the table has to be replaced by either 0,1 or 2 (for PP0, PP1 or PP2).

Table 10 GPIO Port Configuration

P1DIR.x	P1OUT.x	P1SENS.x	I/O	Pull-up/ pull-down	Comment
0	0	-	Output	No	LOW (sink)
0	1	-	Output	No	HIGH (source)
1	0	-	Input	No	high-Z (Tri-State)
1	1	0	Input	Pull-up	Weak-High
1	1	1	Input	Pull-down	Weak-Low

Note: The GPIO pin PP2 can be configured as external wakeup. For the required register settings please refer to ***“External Wakeup on PP2” on Page 118****.*

Spike Suppression on Input Pins

To avoid unstability when reading the GPIO pins, a synchronization stage with a two-stage spike filter is included.

Due to the synchronization stage the following conditions might occur:

- Signal duration (T_{SIGNAL}) < 1 systemclock[1)] period (1 T_{CLK}): Signal is suppressed
- 1 T_{CLK} < T_{SIGNAL} < 2 T_{CLK}: undefined if suppressed or passed
- T_{SIGNAL} > 2 T_{CLK}: Signal appears in SFR P1IN

Figure 41 shows examples of different input signals and how they are processed by the the synchronization stage and the spike filter.

1) For PP0, PP1 and PP2 the synchronization stage uses the undivided systemclock (SFR DIVIC) as clocksource, so SFR DIVIC has no influence.
The synchronization stage is disabled in POWER DOWN state, so it is not used for an external wakeup (see **“External Wakeup on PP2” on Page 118**).

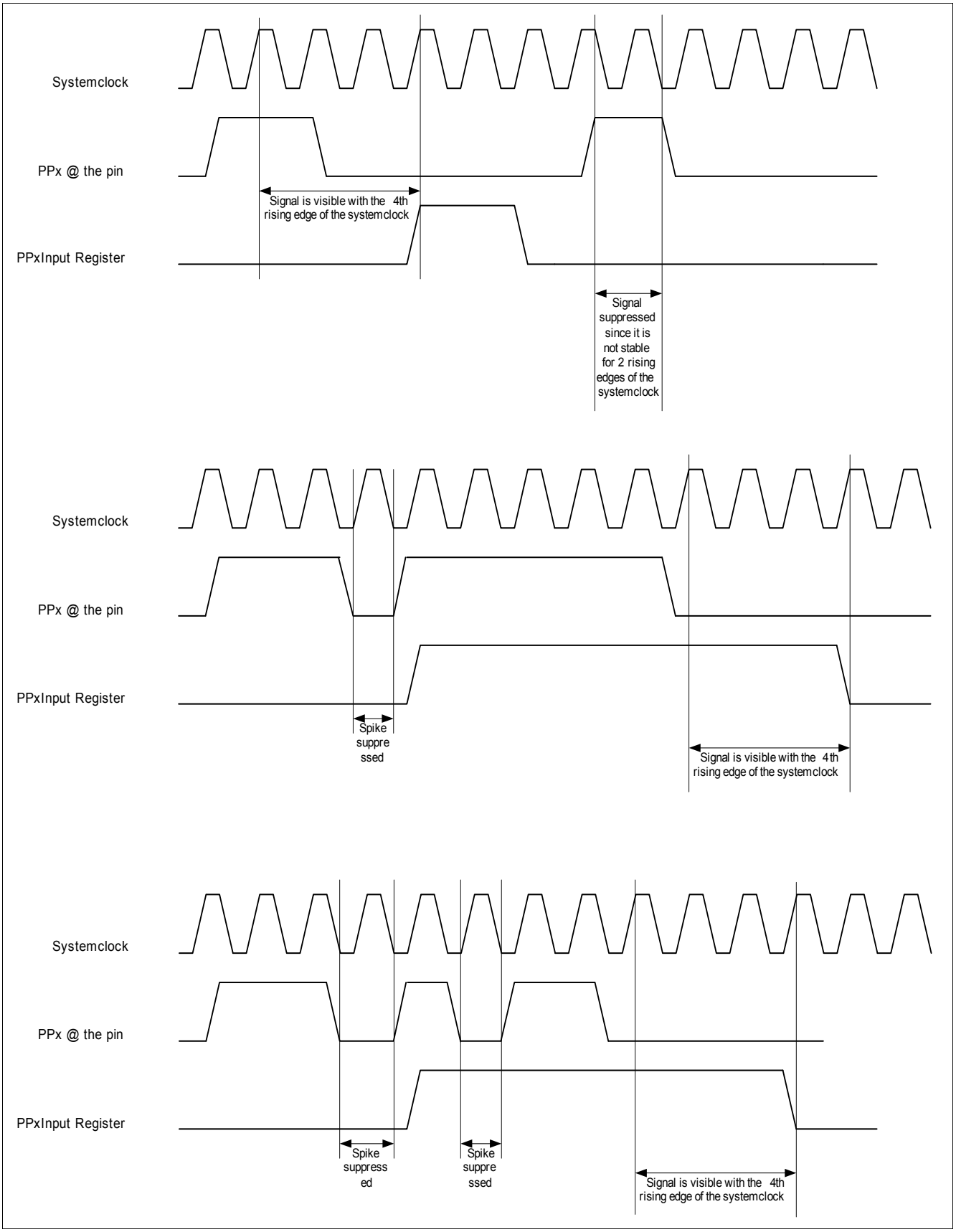


Figure 41 Synchronization Stage & Spike Suppression Examples

External Wakeup on PP2

PP2 can be used as an external wakeup source if enabled by the Wakeup-Mask SFR bit WUM.1[EXT1] and configured as input pin by setting SFR bit P1DIR.2[PPD2].

The internal pull-up/pull-down resistor is enabled if SFR bit P1OUT.2[PPO2] is set. SFR bit P1SENS.2[PPS2] selects the sensitivity (high active/low active):

Table 11 External Wakeup Configuration

SFR Settings	Description
SFR bit P1DIR.2[PPD2] = 1 SFR bit P1OUT.2[PPO2]=1 SFR bitP1SENS.2[PPS2] = 0 SFR bit WUM.1[EXT] = 0	PP2 configured as Input, pull-up enabled, Wakeup occurs if PP2 is forced to LOW externally.
SFR bit P1DIR.2[PPD2] = 1 SFR bit P1OUT.2[PPO2] =1 SFR bitP1SENS.2[PPS2] = 1 SFR bit WUM.1[EXT] = 0	PP2 configured as Input, pull-down enabled, Wakeup occurs if PP2 is forced to HIGH externally.

Alternative Port Functionality

In **Table 12**, the alternative port functionality which has higher priority than standard I/O port functionality is shown.

Table 12 I/O Port 1 - Alternative Functionality

Pin	Function	I/O	Description
PP0	I2C-SCL	I	**I2C Serial Clock Line** Configured to I2C clock pin if SFR bit CFG1.6 [I2CEN] is set. Weak-High has to be provided by an external pull-up resistor or by the I2C master device.
	Port Pin I/O	I/O	Standard I/O port functionality
PP1	I2C-SDA	I/O	I2C Serial Data Configured to I2C data pin if bit CFG1.6 [I2CEN] is set. Weak-High has to be provided either by the internal pull-up resistor, by an external pull-up resistor or by the I2C master device.
	Port Pin I/O	I/O	Standard I/O port functionality
PP2	TX Data Out	O	**RF Encoder Data Output** If bit CFG1.4[RFTXPEN] is set to one, the Manchester/BiPhase encoded data is delivered serially to PP2.
	Port Pin I/O	I/O	Standard I/O port functionality / External Wakeup

IO-Port 1 Direction Register

P1DIR	Offset	Wakeup Value	Reset Value
IO-Port 1 Direction Register	91_H	UU_H	FF_H

7	3	2	1	0
Res		PPD2	PPD1	PPD0
		wr	wr	wr

Field	Bits	Type	Description
Res	7:3		**Reserved** These bits must be set to 11111_B. Reset: $1F_H$
PPD2	2	wr	**PP2 I/O Port Direction** 0_B Output 1_B Input Reset: 1_H
PPD1	1	wr	**PP1 I/O Port Direction** 0_B Output 1_B Input Reset: 1_H
PPD0	0	wr	**PP0 I/O Port Direction** 0_B Output 1_B Input Reset: 1_H

IO-Port 1 Data In Register

P1IN	Offset	Wakeup Value	Reset Value
IO-Port 1 Data In Register	92_H	$00000XXX_B$	$00000XXX_B$

7	3	2	1	0
UNUSED		PPI2	PPI1	PPI0
-		r	r	r

Field	Bits	Type	Description
UNUSED	7:3	-	**UNUSED** Reset: 00_H
PPI2	2	r	**PP2 I/O-Port Input Data** 0_B LOW Level 1_B HIGH Level Reset: X_B
PPI1	1	r	**PP1 I/O-Port Input Data** 0_B LOW Level 1_B HIGH Level Reset: X_B
PPI0	0	r	**PP0 I/O-Port Input Data** 0_B LOW Level 1_B HIGH Level Reset: X_B

IO-Port 1 Data Out Register

P1OUT	Offset	Wakeup Value	Reset Value
IO-Port 1 Data Out Register	90_H	UU_H	FF_H

7	6	5	4	3	2	1	0
Res					PPO2	PPO1	PPO0
					wr	wr	wr

Field	Bits	Type	Description
Res	7:3		**Reserved** These bits must be set to 11111_B. Reset: $1F_H$
PPO2	2	wr	**PP2 I/O-Port Output Data / Pulling Resistor** When SFR P1DIR.PPD2 is clear (output), then PPO2 defines the output port state. When SFR P1DIR.PPD2 is set (input), then PPO2 controls the input pulling resistor. 0_B Output low / Tristate 1_B Output high / Pulling Resistor enabled Reset: 1_H
PPO1	1	wr	**PP1 I/O-Port Output Data / Pulling Resistor** When SFR P1DIR.PPD1 is clear (output), then PPO1 defines the output port state. When SFR P1DIR.PPD1 is set (input), then PPO1 controls the input pulling resistor. 0_B Output low / Tristate 1_B Output high / Pulling Resistor enabled Reset: 1_H
PPO0	0	wr	**PP0 I/O-Port Output Data / Pulling Resistor** When SFR P1DIR.PPD0 is clear (output), then PPO0 defines the output port state. When SFR P1DIR.PPD0 is set (input), then PPO0 controls the input pulling resistor. 0_B Output low / Tristate 1_B Output high / Pulling Resistor enabled Reset: 1_H

IO-Port 1 Sensitivity Register

P1SENS	Offset	Wakeup Value	Reset Value
IO-Port 1 Sensitivity Register	93_H	$00000UUU_B$	00_H

7	6	5	4	3	2	1	0
UNUSED					PPS2	PPS1	PPS0
-					wr	wr	wr

Field	Bits	Type	Description
UNUSED	7:3	-	**UNUSED** Reset: 00_H
PPS2	2	wr	**PP2 I/O-Port Sensitivity** Only applies when SFR P1DIR.PPD2 is set (input) and SFR P1OUT.PPO2 is set (enable pulling). 0_B Pull-up Resistor 1_B Pull down Resistor Reset: 0_H
PPS1	1	wr	**PP1 I/O-Port Sensitivity** Only applies when SFR P1DIR.PPD1 is set (input) and SFR P1OUT.PPO1 is set (enable pulling). 0_B Pull-up Resistor 1_B Pull down Resistor Reset: 0_H
PPS0	0	wr	**PP0 I/O-Port Sensitivity** Only applies when SFR P1DIR.PPD0 is set (input) and SFR P1OUT.PPO0 is set (enable pulling). 0_B Pull-up Resistor 1_B Pull down Resistor Reset: 0_H

3.23 I²C Interface

For communication between a host and the SP37T a I2C slave interface is implemented.

- PP1 is used as serial data line (SDA)
- PP0 is used as serial clock line (SCL)
- SP37T responds to I²C Address $6C_H$ or a general call (if enabled) by addressing slave address 00_H. General call can be enabled by setting SFR bit CFG2.6[I2CGCEN].
- The data transfer rate is specified in **"I2C Interface" on Page 166**.

Note: In PROGRAMMING mode and DEBUG mode the I²C Interface is handled by the mode handlers located in the ROM automatically. Manual access to those registers is only required if the I²C Interface is utilized in NORMAL mode

Using the slave I²C interface in NORMAL mode

To enable the I2C interface the SFR bit CFG1.6[I2CEN] has to be set. Once the I2C interface has been enabled, the SP37T waits for a start condition to occur.

After the SP37T has received a start condition, the following received 8 bits are compared to the device address. If the address matches, the hardware automatically generates an acknowledge, sets SFR bit I2CS.7[AM] and configures SFR bit I2CS.3[RNW] according to the received address which determines if the I²C access is read or write.

Dependant on SFR bit I2CS.3[RNW] the following two actions has to be performed by the application software:

(SFR bit I2CS.3[RnW] == 0) - Receive I²C-data

- If SFR bit I2CS.0[RBF] is set, one byte has been received and can be read by the application software via SFR I2CD.
  Each byte is acknowledged automatically as long as no receive buffer overflow (SFR bit I2CS.5[OV]) occurs.
- If SFR bit I2CS.4[S] is set, a stop condition has occurred; the transmission was closed by the I²C master device.
- If SFR bit I2CS.7[AM] is set, a restart condition has been initiated. In case of a write access (SFR bit I2CS.3[RNW] == 1) a branch to the transmit subroutine has to be performed.

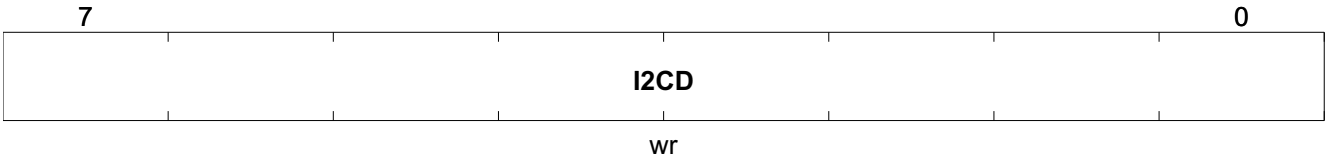
(SFR bit I2CS.3[RnW] == 1) - Transmit I²C-data

- Data to be transmitted has to be written to SFR I2CD.
  SFR bit I2CS.1[TBF] cleared when the data written to SFR I2CD is taken over by the shift-register. If the I²C master device requests more data bytes it creates an acknowledge (SFR bit I2CS.2[RACK]) and subsequently new data may be written to SFR I2CD. If no data is provided, the I²C-interface automatically sets line SCL to low until data is written to SFR I2CD (slave device gains access over the I²C clock line).
- If SFR bit I2CS.4[S] is set, the transmission process has been terminated by the I²C master device and the transmission subroutine can be left.

To control I²C slave interface the following registers are implemented:

I2C Data Register

I2CD	Offset	Wakeup Value	Reset Value
I2C Data Register	$9A_H$	00_H	00_H



Field	Bits	Type	Description
I2CD	7:0	wr	**I2C Data Register** Reset: 00_H

I2C Status Register

I2CS	Offset	Wakeup Value	Reset Value
I2C Status Register	$9B_H$	00_H	00_H

7	6	5	4	3	2	1	0
AM	**UNUSED**	**OV**	**S**	**RNW**	**RACK**	**TBF**	**RBF**
rc	-	rc	rc	r	r	r	r

Field	Bits	Type	Description
AM	7	rc	**I2C Address Match** This bit will be set when the device address or general call matches with received address byte. It is automatically cleared by hardware after I2CS is read. Reset: 0_H
UNUSED	6	-	**UNUSED** Reset: 0_H
OV	5	rc	**I2C Overflow** This bit will be set when a received byte is not read out before a new byte is received. In this case the old byte value is kept, the new byte is rejected. Overflow also occurs if a new byte is written to register I2CD prior to transmitting the previous byte. In this case the old byte value is overwritten with the new byte. This bit is automatically cleared by hardware after I2CS is read. Reset: 0_H

Field	Bits	Type	Description
S	4	rc	**I2C Stop Condition** This bit will be set when a stop condition is detected. It is automatically cleared by hardware after I2CS is read. Reset: 0_H
RNW	3	r	**I2C Read/Write Information** RnW reflects the state of the Read/Write bit received within the I2C address byte. 0_B I2C Write Command 1_B I2C Read Command Reset: 0_H
RACK	2	r	**I2C Acknowledge** 0_B Not acknowledged 1_B Acknowledged Reset: 0_H
TBF	1	r	**I2C Transmit Buffer Full** Bit is automatically cleared after the data byte is transferred to the shift register. 0_B Ready to accept new byte 1_B Byte transmission is pending Reset: 0_H
RBF	0	r	**I2C Receive Buffer Full** Bit is automatically cleared by hardware after I2CD is read. 0_B No new received data 1_B Received data byte is available Reset: 0_H

3.23.1 Programming mode Operation

In PROGRAMMING mode the SP37T is only accessible via the I²C Interface.

The device is operating using the internal 12 MHz RC HF Oscillator.

If started up in PROGRAMMING mode (see **"Resets and Operating Mode Selection" on Page 20**), the SP37T waits until an I²C commands is received.

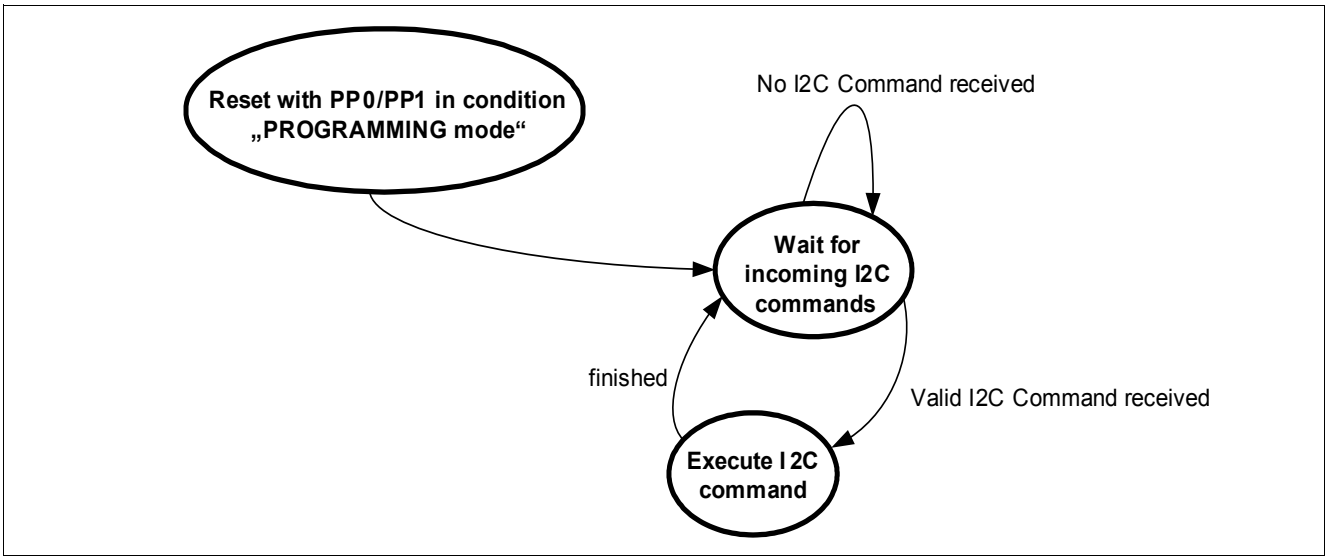


Figure 42 PROGRAMMING Mode State Diagram

*Note: To avoid programming failures all PROGRAMMING mode commands are protected by a 16 bit CRC at the end of each command (**"16 Bit CRC (Cyclic Redundancy Check) Generator/Checker" on Page 99** shows details about the used CRC polynomial).*
The checksum has to be calculated over all bytes in the command excluding the SP37T I²C device address.

PROGRAMMING Mode Commands

- **"FLASH Write Line" on Page 127**
- **"FLASH Erase" on Page 127**
- **"FLASH Check Erase Status" on Page 128**
- **"FLASH Read Line" on Page 129**
- **"Read Status" on Page 130**
- **"FLASH Check CRC" on Page 131**
- **"FLASH Set User Configuration Sector Lock" on Page 131**
- **"Measure Pressure" on Page 132**
- **"Measure Acceleration" on Page 134**
- **"Measure Temperature" on Page 136**
- **"Measure Supply Voltage" on Page 137**

Figure 43 shows the nomenclature for the I2C commands.

■	from master to slave	S	start condition	nA	not acknowledge
□	from slave to master	P	stop condition	A	acknowledge

SR repeated start condition, may be replaced by Stop Start condition

Figure 43 I²C Legend - PROGRAMMING Mode

3.23.1.1 FLASH Write Line

The FLASH Write Line command writes 32 bytes to the FLASH. The start address has to be a multiple of 20_H.

This command should only be used if the FLASH line is fully erased. If an already programmed FLASH line gets overwritten (without being erased before) the resulting data is undefined.

*Note: After the Stop condition (P) is received the data is programmed into the FLASH. During the programming time incoming I²C commands are not acknowledged. This programming time is specified in **Table 49**.*

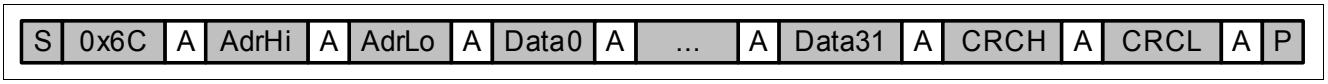


Figure 44 FLASH Write Line I2C Command

Table 13 FLASH Write Line Parameters

Parameter	Description
AdrHi	High Byte of FLASH start address
AdrLo	Low Byte of FLASH start address Must be a multiple of 20_H
Data0 - Data 31	32 Databytes that shall be written to the FLASH line indicated with AdrHi&AdrLo
CRCH	High Byte of CRC16
CRCL	Low Byte of CRC16

3.23.1.2 FLASH Erase

The FLASH Erase command erases the individual sectors of the FLASH.

*Note: After the Stop condition (P) is received the selected FLASH sectors are being erased. During the erase time incoming I²C commands are not acknowledged. This erase time is specified in **Table 49**.*

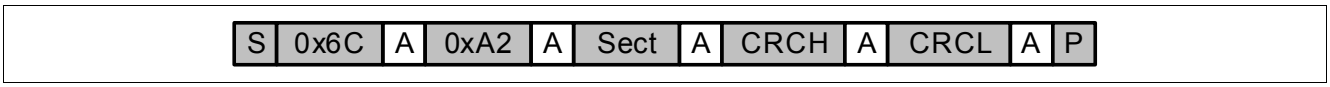


Figure 45 FLASH Erase Command

Table 14 FLASH Erase Parameters

Parameter	Description
Sect	**Selects which sectors to erase** *Note: Set individual bits to '1' to erase or to '0' to NOT erase* Bit7:2 protected FLASH area -don't care Bit1 FLASH User Configuration Sector Bit0 FLASH Code Sector
CRCH	High Byte of CRC16
CRCL	Low Byte of CRC16

3.23.1.3 FLASH Check Erase Status

This function returns the status of the selected FLASH sector(s).

Note: After the first Stop condition (P) is received the selected FLASH sectors are checked. During this time incoming I²C commands are not acknowledged.

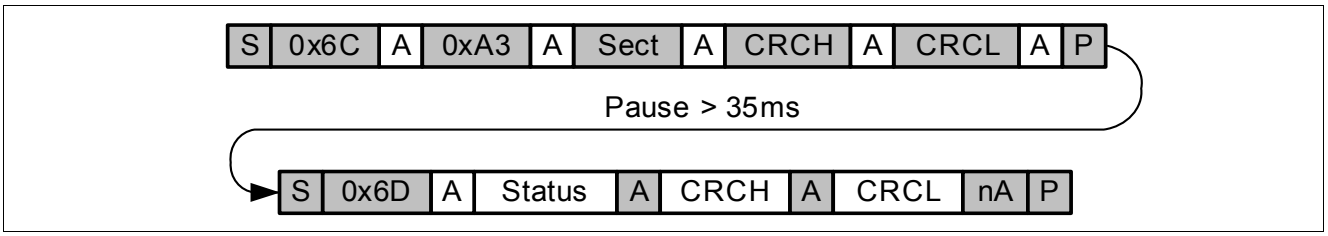


Figure 46 FLASH Check Erase Status Command

Table 15 FLASH Check Erase Parameters

Parameter	Description
Sect	**Selects which sectors to erase** *Note: Set individual bits to '1' to check or to '0' to NOT check.* Bit7:2 protected FLASH area -don't care Bit1 FLASH User Configuration Sector Bit0 FLASH Code Sector
CRCH	High Byte of CRC16
CRCL	Low Byte of CRC16

Table 16 FLASH Check Erase Return values

Parameter	Description
Status	**Returns the Status of the Check** *Note: '0' means Sector is erased or unchecked '1' means that at least one bit is not erased in the checked Sector.* Bit7:2 protected FLASH area -don't care Bit1 FLASH User Configuration Sector Bit0 FLASH Code Sector
CRCH	High Byte of CRC16
CRCL	Low Byte of CRC16

3.23.1.4 FLASH Read Line

The contents of the FLASH memory can be read out using the following command.

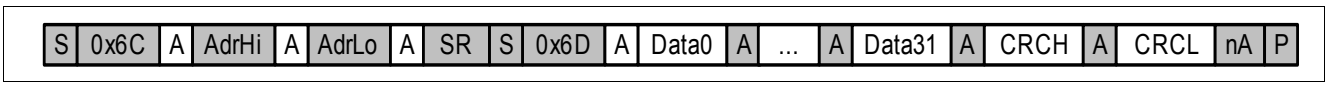


Figure 47 FLASH Read Line Command

Table 17 FLASH Read Line Parameters

Parameter	Description
AdrHi	High Byte of FLASH start address
AdrLo	Low Byte of FLASH start address Must be a multiple of 20_H

Table 18 FLASH Read Line Return values

Parameter	Description
Data0 - Data 31	32 Databytes Read from FLASH starting at address AdrHi&AdrLo
CRCH	High Byte of CRC16
CRCL	Low Byte of CRC16

3.23.1.5 Read Status

This function is intended to read out the status of previous I²C commands. It can be called whenever desired to verify if errors occurred since the last Read Status call.

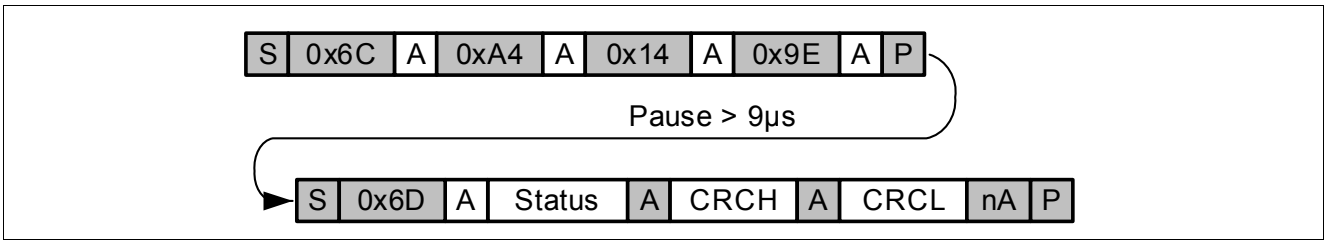


Figure 48 FLASH Read Status Command

Table 19 FLASH Read Status Return values

Parameter	Description
Status	**Status byte** Bit7:4 CmdCnt Counter indicating the number of executed commands since first detected error *Note: 0000b = no error occurred since the last call* *0001b = 1 command* *...* *1111b = 15 commands or more* Bit3:2 ErrCntInvCmdL Counter of erroneous events since last call *Note: 00b = no error* *01b = one error* *10b = two errors* *11b = three or more errors* Bit1 InvCmdL Flag indicating if there was a invalid command or execution failure since the last call. *Note: 0b = no failure found* *1b = failure found* Bit0 CRCFail CRC Failure detected since the last call *Note: 0b = no CRC Error detected since the last call* *1b = one or more CRC Error detected since last call*
CRCH	High Byte of CRC16
CRCL	Low Byte of CRC16

3.23.1.6 FLASH Check CRC

This function performs a CRC check on the locked FLASH Code sector. The CRC-Generator/Checker is using the 16 bit CCITT polynomial x16+x12+x5+1 with a preload value of $FFFF_H$. The resulting CRC checksum (CRCHi, CRCLo) is compared with value stored at the FLASH addresses $577D_H$ and $577E_H$ in the FLASH Code sector. For this function to operate correctly the CRC of the entire code sector, including memory locations otherwise unused by the application software, must be considered.

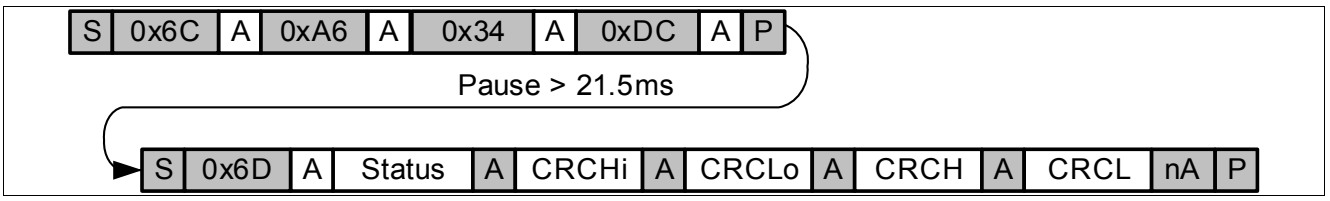


Figure 49 FLASH Check CRC

Table 20 FLASH Check CRC Return values

Parameter	Description
Status	**Status Byte** Returns the pass/fail information of the FLASH Check CRC *Note: 00_H = CRC Check passed, no ECC error detected* *FF_H = CRC Check failed* *FE_H = CRC Check passed, but ECC error detected (correctable error)*
CRCHi	High Byte of calculated CRC16 (not the CRCH Byte stored in the FLASH address $577D_H$)
CRCLo	Low Byte of calculated CRC16 (not the CRCL Byte stored in the FLASH address $577E_H$)
CRCH	High Byte of CRC16
CRCL	Low Byte of CRC16

3.23.1.7 FLASH Set User Configuration Sector Lock

This command may be issued in order to lock the User Configuration Sector from any further writing or reading. This command causes Lockbyte 3 to become set. The structure for this command is as follows:

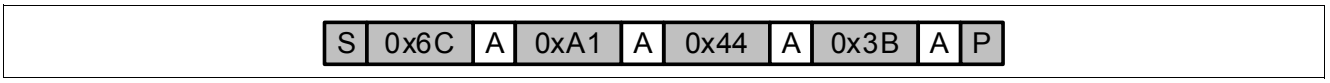


Figure 50 FLASH Set User Configuration Sector Lock

3.23.1.8 Measure Pressure

This function performs a pressure sensor measurement.

The result can either:

- Compensated for sensitivity, offset and temperature
- Output as raw value without performing the compensation

The function can measure up to 64 samples with a specified sample rate and can average them in order to compensate for noise.

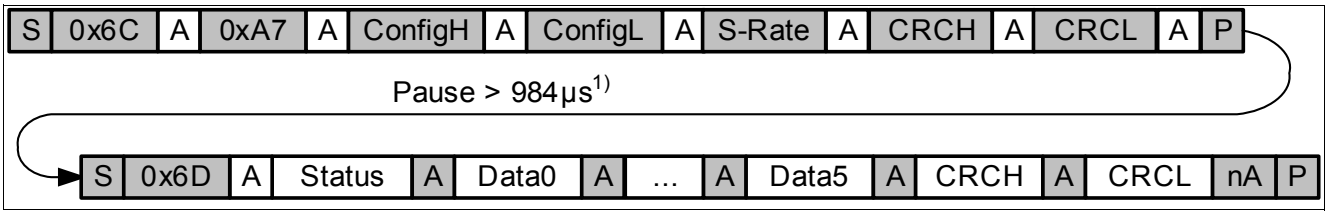


Figure 51 Measure Pressure

Note: 1) When the sample rate is > 0, this time increases

Table 21 Measure Pressure Parameters

Parameter	Description
ConfigH	**Config Parameters** Bit7:1 Reserved Bit0 Selects source of raw temperature data for compensation *Note: 0b = Perform new raw temperature measurement* *1b = Use raw temperature data from previous measurement*
ConfigL	**Config Parameters** Bit7 Select Pressure Measurement, set to 1b Bit6 Defines if the RAW ADC result is compensated *Note: 0b = temperature compensation is performed. Returns Compensated & RAW value* *1b = no compensation is performed. Returns only RAW value* Bit5:4 Select Pressure Range *Note: 00b = Reserved* *01b = Reserved* *10b = Reserved* *11b = 1300 kPa* Bit3 Reserved, set to 0b Bit2:0 Number of ADC measurements that are taken and averaged *Note: 000b = 1 Samples (default)* *001b = 2 Samples* *010b = 4 Samples* *011b = 8 Samples* *100b = 16 Samples* *101b = 32 Samples* *110b = 64 Samples* *111b = 64 Samples*

Table 21 Measure Pressure Parameters (cont'd)

Parameter	Description
S-Rate	Bit7:0 Number of systemclock cycles divided by 8 between two consecutive samples (only applicable if more than one sample is taken and averaged) *Note: 00_H = No delay (fastest possible samplerate)* *01_H..$4F_H$ = Not allowed* *50_H..FF_H = 1/samplerate (samplerate in systemclocks divided by 8)*
CRCH	High Byte of CRC16
CRCL	Low Byte of CRC16

Table 22 Measure Pressure Return Values

Parameter	Description
Status	**Status Byte** Bit7 Reserved Bit6 Reserved Bit5 Reserved Bit4 VMIN warming *Note: 0_B= Battery Supply Voltage above VMIN threshold* *1_B= Battery Supply Voltage below VMIN threshold* Bit3 Reserved Bit2 Sensor Fault Wire Bond Check *Note: 0_B = Wire Bond Check successful* *1_B = Wire Bond Check Failed* Bit1 Overflow of ADC Result *Note: 0_B= No overflow of the ADC Result* *1_B= Overflow of the ADC Result* Bit0 Underflow of the ADC Result *Note: 0_B= No underflow of the ADC Result* *1_B= underflow of the ADC Result*
Data0	Compensated Pressure High Byte
Data1	Compensated Pressure Low Byte
Data2	RAW Pressure High Byte
Data3	RAW Pressure Low Byte
Data4	RAW Temperature High Byte
Data5	RAW Temperature Low Byte
CRCH	High Byte of CRC16
CRCL	Low Byte of CRC16

3.23.1.9 Measure Acceleration

This function performs an acceleration sensor measurement.

The result can either:

- Compensated for sensitivity, offset and temperature
- Output as raw value without performing the compensation

The function can measure up to 64 samples with a specified sample rate and can average them in order to compensate for noise.

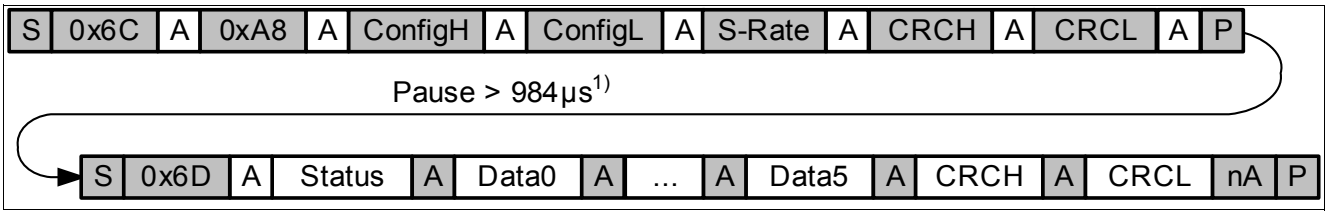


Figure 52 Measure Acceleration

Note: 1) When the sample rate is > 0, this time increases

Table 23 Measure Acceleration Parameters

Parameter	Description
ConfigH	**Config Parameters** Bit7:1 Reserved Bit0 Selects source of raw temperature data for compensation *Note: 0b = Perform new raw temperature measurement* *1b = Use raw temperature data from previous measurement*
ConfigL	**Config Parameters** Bit7 Select Acceleration Measurement, set to 0b Bit6 Defines if the RAW ADC result is compensated *Note: 0b = temperature compensation is performed. Returns Compensated & RAW value* *1b = no compensation is performed. Returns only RAW value* Bit5:4 Specifies the sensor gain, set to 00b Bit3 Measure Mode: *Note: 0b = Average value* *1b = Maximum value* Bit2:0 Number of ADC measurements that are taken and averaged *Note: 000b = 1 Samples (default)* *001b = 2 Samples* *010b = 4 Samples* *011b = 8 Samples* *100b = 16 Samples* *101b = 32 Samples* *110b = 64 Samples* *111b = 64 Samples*

Table 23 Measure Acceleration Parameters (cont'd)

Parameter	Description
S-Rate	Bit7:0 Number of systemclock cycles divided by 8 between two consecutive samples (only applicable if more than one sample is taken and averaged) *Note: 00_H = No delay (fastest possible samplerate)* *01_H..$5E_H$ = Not allowed* *$5F_H$..FF_H = 1/samplerate (samplerate in systemclocks divided by 8)*
CRCH	High Byte of CRC16
CRCL	Low Byte of CRC16

Table 24 Measure Acceleration Return values

Parameter	Description
Status	**Status Byte** Bit7 Reserved Bit6 Reserved Bit5 Reserved Bit4 VMIN warning *Note: 0b = Battery Supply Voltage above VMIN threshold* *1b = Battery Supply Voltage below VMIN threshold* Bit3 Sensor Fault Diagnosis Resistor *Note: 0b = Diagnosis Resistor Check successful* *1b = Diagnosis Resistor Check failed* Bit2 Sensor Fault Wire Bond Check *Note: 0b = Wire Bond Check successful* *1b = Wire Bond Check failed* Bit1 Overflow of ADC Result *Note: 0b = No overflow of the ADC Result* *1b = Overflow of the ADC Result* Bit0 Underflow of ADC Result *Note: 0b = No underflow of the ADC Result* *1b = Underflow of the ADC Result*
Data0	Compensated Acceleration High Byte
Data1	Compensated Acceleration Low Byte
Data2	RAW Acceleration High Byte
Data3	RAW Acceleration Low Byte
Data4	RAW Temperature High Byte
Data5	RAW Temperature Low Byte
CRCH	High Byte of CRC16
CRCL	Low Byte of CRC16

3.23.1.10 Measure Temperature

This function performs a temperature measurement. The result is compensated for sensitivity and offset.

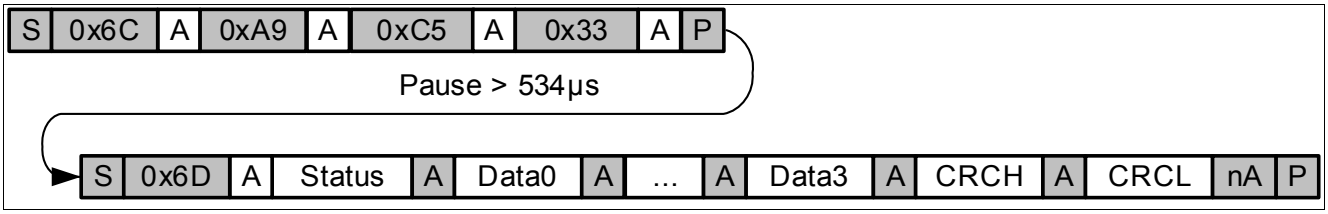


Figure 53 Measure Temperature

Table 25 Measure Temperature Return values

Parameter	Description
Status	**Status Byte** Bit7 Reserved Bit6 Reserved Bit5 Reserved Bit4 VMIN warning *Note: 0b = Battery Supply Voltage above VMIN threshold* *1b = Battery Supply Voltage below VMIN threshold* Bit3 Reserved Bit2 Reserved Bit1 Overflow of ADC Result *Note: 0b = No overflow of the ADC Result* *1b = Overflow of the ADC Result* Bit0 Underflow of ADC Result *Note: 0b = No underflow of the ADC Result* *1b = Underflow of the ADC Result*
Data0	Compensated Temperature High Byte
Data1	Compensated Temperature Low Byte
Data2	RAW Temperature High Byte
Data3	RAW Temperature Low Byte
CRCH	High Byte of CRC16
CRCL	Low Byte of CRC16

3.23.1.11 Measure Supply Voltage

This function performs a battery voltage measurement. The result is compensated for offset.

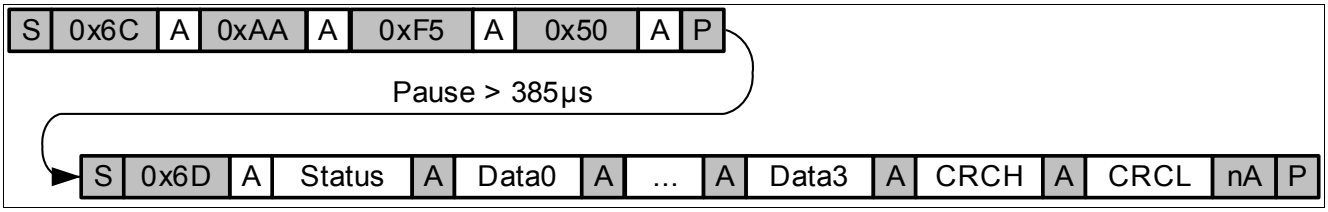


Figure 54 Measure Supply Voltage

Table 26 Measure Supply Voltage Return values

Parameter	Description
Status	**Status Byte** Bit7 Reserved Bit6 Reserved Bit5 Reserved Bit4 Reserved Bit3 Reserved Bit2 Reserved Bit1 Overflow of ADC Result *Note: 0b = No overflow of the ADC Result* *1b = Overflow of the ADC Result* Bit0 Underflow of ADC Result *Note: 0b = No underflow of the ADC Result* *1b = Underflow of the ADC Result*
Data0	Compensated Battery Voltage High Byte
Data1	Compensated Battery Voltage Low Byte
Data2	RAW Battery Voltage High Byte
Data3	RAW Battery Voltage Low Byte
CRCH	High Byte of CRC16
CRCL	Low Byte of CRC16

3.23.2 DEBUG Mode Operation

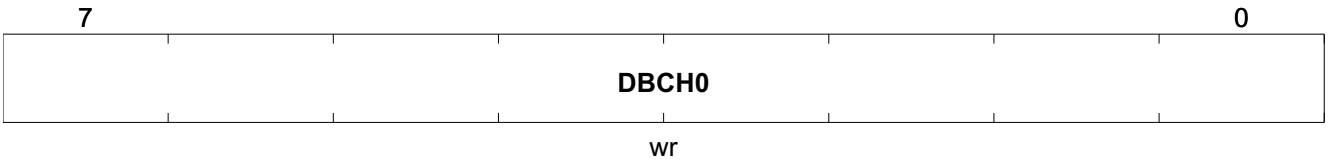
*Note: DEBUG mode operation is automatically handled by the development environment provided by Infineon. Manual changes of the SFRs (see **Table 27**) and/or usage of the Debugger Commands (see **"Debugger Commands" on Page 139**) by other tools may result in undefined operation.*

3.23.2.1 Debug Special Function Register

The SP37T incorporates 8 debug registers that are cleared after Wakeup and Reset.

CPU Debug Compare Register 0 (high)

DBCH0	Offset	Wakeup Value	Reset Value
CPU Debug Compare Register 0 (high)	**95_H**	**00_H**	**00_H**



Field	Bits	Type	Description
DBCH0	7:0	wr	**CPU Debug Compare Register 0 (high)** Reset: 00_H

Table 27 DEBUG mode SFRs

Register Short Name	Register Long Name	Offset Address	Wakeup Value	Reset Value
DBCH0	Debug Compare Register 0 (highbyte)	95_H	00_H	00_H
DBCL0	Debug Compare Register 0 (lowbyte)	94_H	00_H	00_H
DBCH1	Debug Compare Register 1 (highbyte)	$9D_H$	00_H	00_H
DBCL1	Debug Compare Register 1(lowbyte)	$9C_H$	00_H	00_H
DBTH0	Debug Target Register 0 (highbyte)	97_H	00_H	00_H
DBTL0	Debug Target Register 0 (lowbyte)	96_H	00_H	00_H
DBTH1	Debug Target Register 1 (highbyte)	$9F_H$	00_H	00_H
DBTL1	Debug Target Register 1 (lowbyte)	$9E_H$	00_H	00_H

3.23.2.2 Debugging Functionality

During program execution the Program Counter (PC) of the microcontroller is continuously compared with the contents of the DBCHx + DBCLx registers.

In case of a match the PC is automatically set to the address given in DBTHx + DBTLx to handle exceptions (e.g. breakpoints).

The debugger consists of a debug handler and a single stepper. The debug handler processes the I2C communication and debug command interpretation. The debug commands **SetSFR, ReadSFR, SetMemory, ReadMemory** and **SetPC, ReadPC** are executed directly by the debug handler. The debug commands **Single Step, Run Interruptible** and **Run to next Breakpoint** are executed by the single stepper.

3.23.2.3 Debugger Commands

The following figure shows the I^2C nomenclature for the commands.

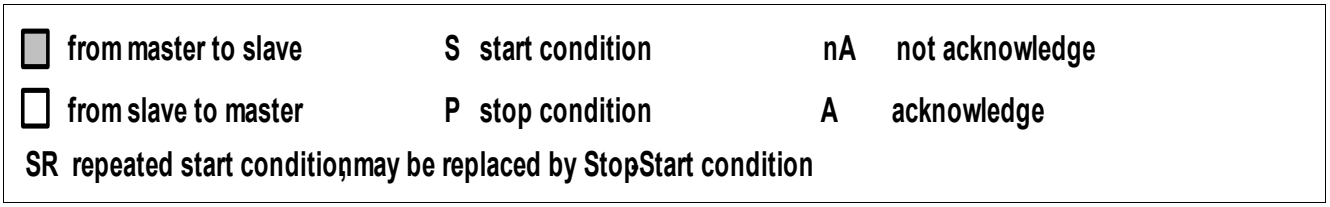


Figure 55 I^2C Legend - DEBUG Mode

3.23.2.3.1 SetSFR - Set an SFR to a User-defined Value

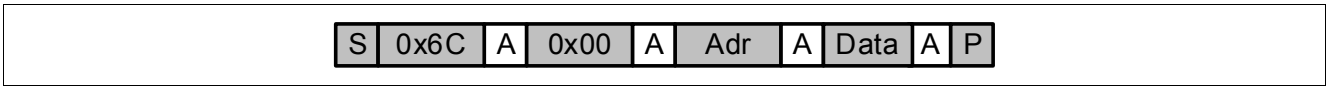


Figure 56 DEBUG SetSFR Command

Addr: represents the address of the SFR to be set.

Data: this value has to be put into the SFR address specified by Addr.

3.23.2.3.2 ReadSFR - Read the Value of One SFR

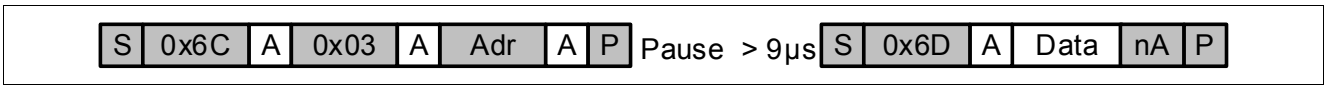


Figure 57 DEBUG ReadSFR Command

Addr: represents the address of the SFR to be read.

Data: this value was read on the SFR address specified by Addr.

3.23.2.3.3 SetMemory - Set one Byte in RAM to a User-defined Value

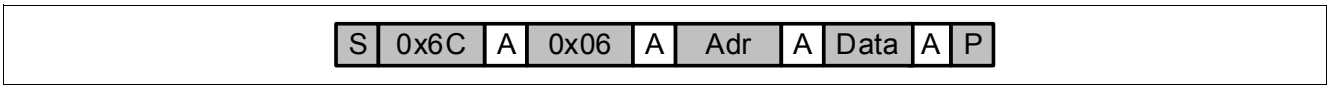


Figure 58 DEBUG SetMemory Command

Addr: represents the address of the internal data memory to be set.

Data: this value that has to be written into the internal data memory byte specified by Addr.

3.23.2.3.4 ReadMemory - Read One Byte of the RAM

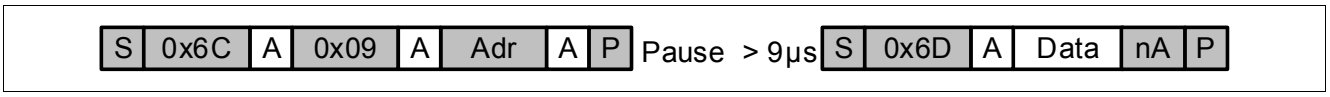


Figure 59 DEBUG ReadMemory Command

Addr: represents the address of the Internal data memory location to be read.

Data: this value was read from the internal data memory address specified by Addr.

3.23.2.3.5 SetPC - Set the Program Counter to a user-defined value

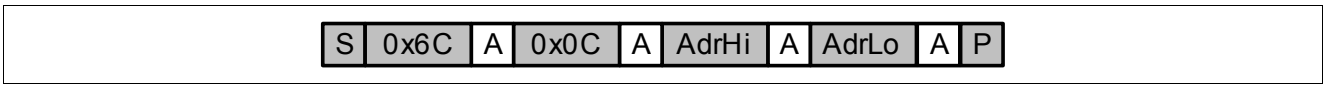


Figure 60 DEBUG SetPC Command

AdrHi: MSB of the new Program Counter.

AdrLo: LSB of the new Program Counter.

3.23.2.3.6 ReadPC - Read the Program Counter

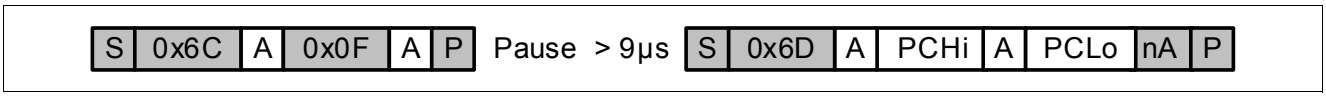


Figure 61 DEBUG ReadPC Command

PCHi: MSB of the Program Counter.

PCLo: LSB of the Program Counter.

3.23.2.3.7 SingleStep

Execute one Opcode Instruction and return to the debug handler.

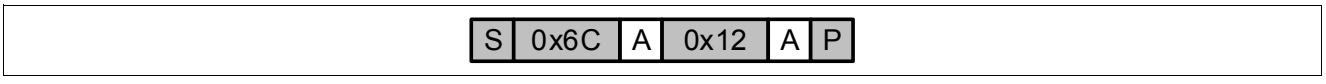


Figure 62 DEBUG SingleStep Command

3.23.2.3.8 Run Interruptible

The function executes consecutive single steps until any I²C command is received on the bus. Compared to running the program in real-time this function has a slower execution speed by a factor of roughly 1/50, thus it cannot be used for debugging time critical application code.

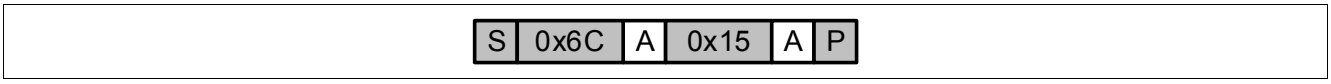


Figure 63 DEBUG Run Interruptible Command

3.23.2.3.9 Run to Next Breakpoint

The debugged program is executed without single steps in real-time. This enables debugging of runtime critical functions like RF transmission or LF data receiving. The execution is stopped when the PC matches one of the two hardware breakpoints. The second Breakpoint (Register 1) can be set if required using the SetSFR command.

Note: If none of these breakpoints is hit the communication to the debugger is lost.

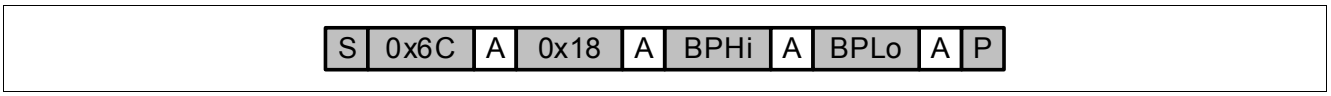


Figure 64 DEBUG Run to Next Breakpoint Command

BPHi: MSByte of the Breakpoint Register 0.

BPLo: LSByte of the Breakpoint Register 0.

4 Specification

4.1 Test Board

The parameters described in Table 35 “Supply Currents” on Page 151 and Table 36 “RF Transmitter” on Page 153 were obtained using the SP37T Testboard described in this chapter. The environment of the customer application have not been taken into account.

4.1.1 SP37T Test Board Schematics

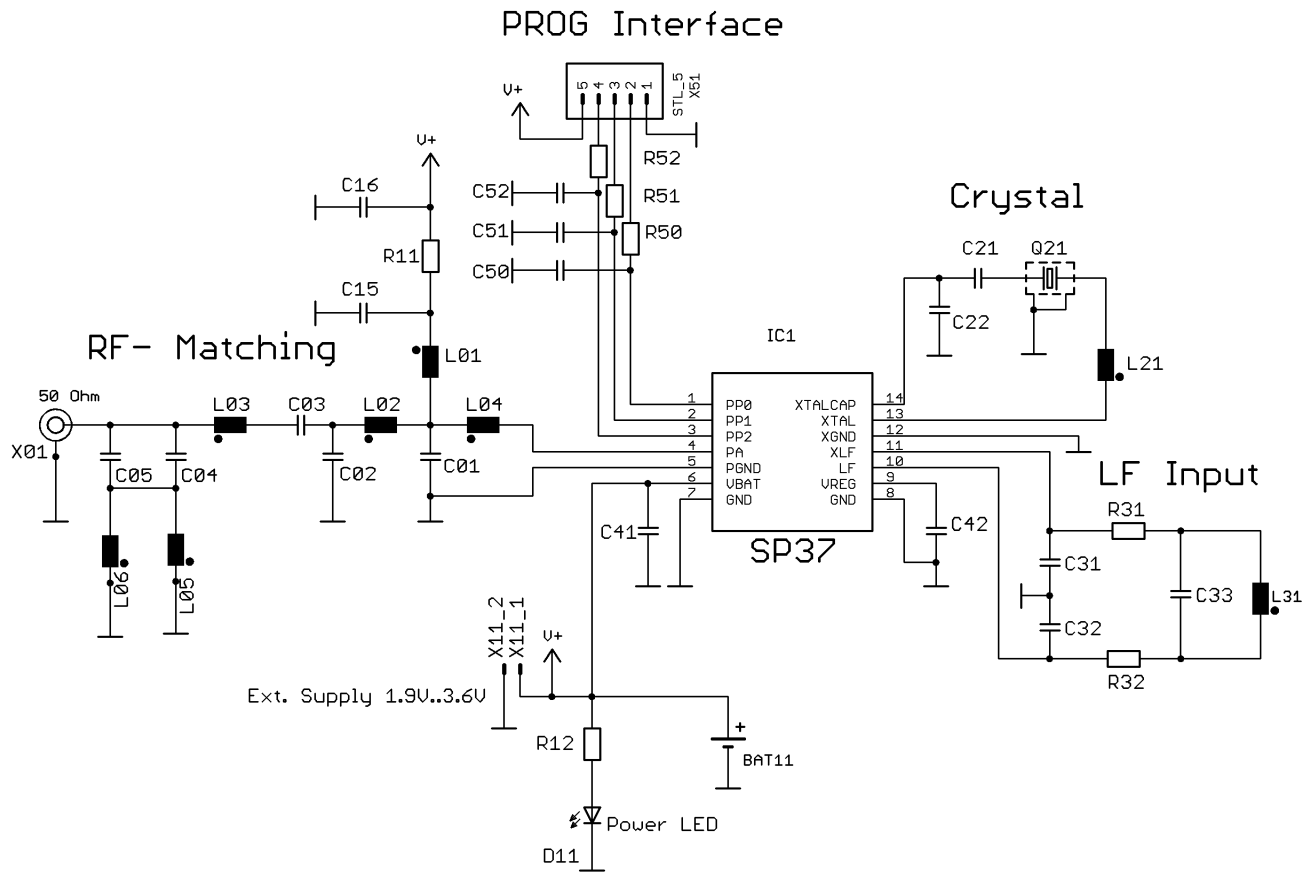


Figure 65 SP37T Test Circuit / Schematic

4.1.2 SP37T Test Board Layout

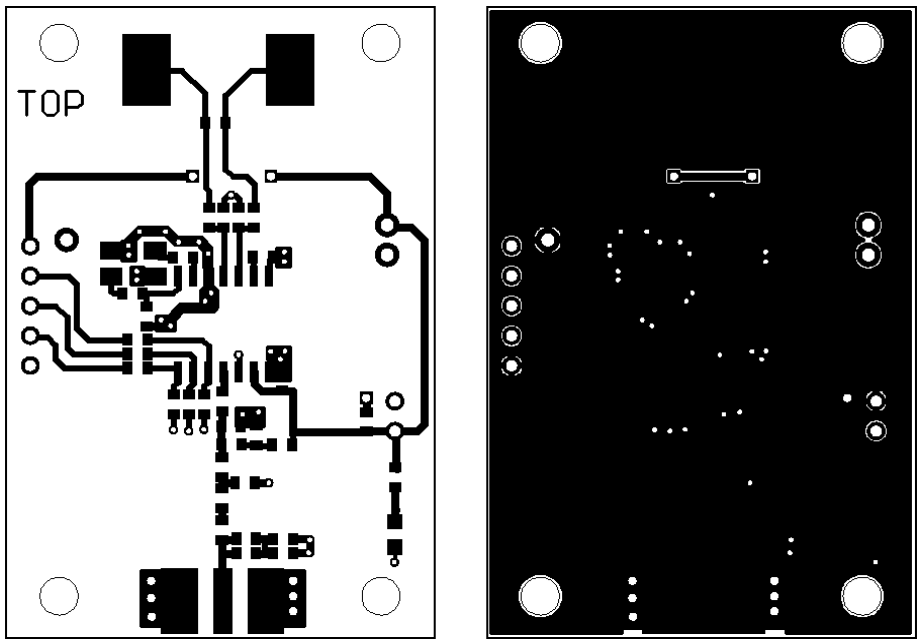


Figure 66 SP37T Test Board Layout

4.1.3 SP37T Test Board Placement

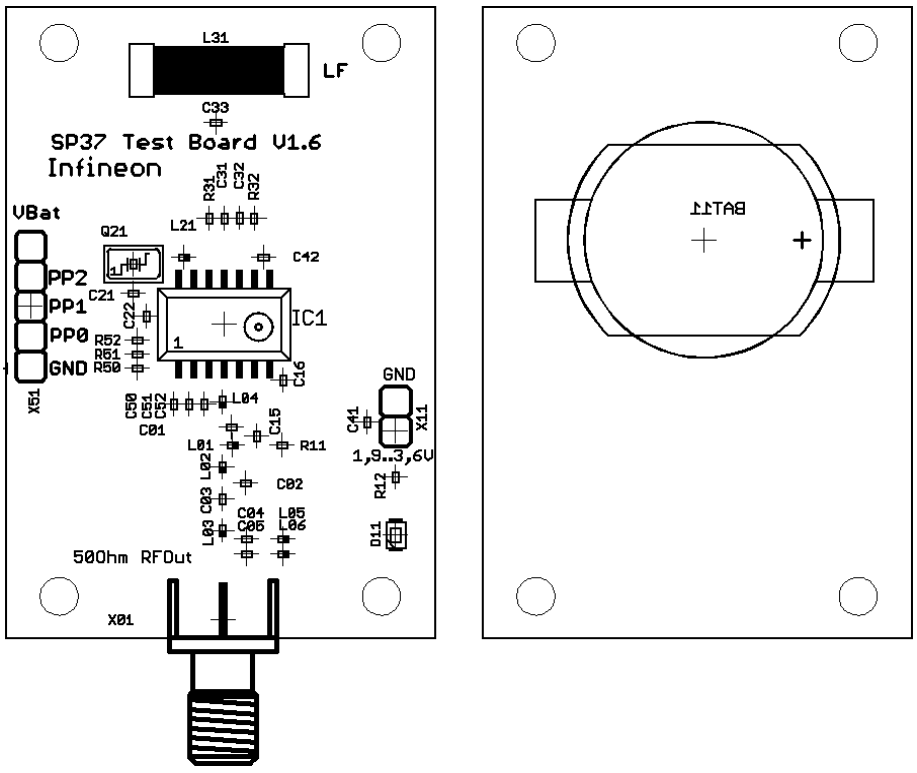


Figure 67 SP37T Test Board Placement

4.1.4 SP37T Test Board Bill of Material

Table 28 SP37T Test Board Bill of Material

Part	Value			
C41	100 nF			
C42	100 nF, ESR max. 15 Ohm			
IC1	SP37T			
R11, R50, R51, R52,	0R Jumper			
X11	2pin Header (male)			
X51	5pin Header (male)			
X01	SMA Connector (female)			
	315 MHz		434 MHz	
	PLow	PMed/High	PLow	PMed/High
C01	5.6 pF	4.7 pF	2.7 pF	2.7 pF
C02	n.p.	n.p.	n.p.	n.p.
C03	51 nH[1)]	39 pF	0 Ohm	0 Ohm
C04	12 pF	8.2 pF	2.2 nH[1)]	2.2 nH[1)]
C05	2.7 pF	1.5 pF	n.p.	n.p.
C15	100 pF	100 pF	100 pF	47 pF
L01	43 nH[1)]	47 nH[1)]	22 nH[1)]	30 nH[1)]
L02	27 pF	47 nH[1)]	30 nH[1)]	18 nH[1)]
L03	0 Ohm	0 Ohm	33 pF	27 pF
L04	18 nH[1)]	18 nH[1)]	12 nH[1)]	18 nH[1)]
L05	0 Ohm	0 Ohm	5.6 pF	5.6 pF
L06	n.p.	n.p.	n.p.	n.p.
Q21	NDK NX5032SD 19.6875 MHz EXS00A-02825		NDK NX5032SD 18.0800 MHz EXS00A-03552	
C21	15 pF		15 pF	
C22	4.7 pF		7.5 pF	
L21	82 nH		82 nH	
BAT11	Battery Clip 2032			
C31, C32, C33, C50, C51, C52, L31, R12, R31, R32	Not placed			

1) Coilcraft 0603CS

4.2 Absolute Maximum Ratings

Table 29 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Max. Supply Voltage	V_{batmax}	-0.3	–	+4.0	V		■	1.1
Operating Temperature	T_j	-40	–	+150	°C	Max 24 hrs accumulated over lifetime between 125°C and 150°C. Device powered V_{bat}=3.6 V	■	1.2
		-55		-40	°C	Temperature measurement, operation of interval timer	■	1.3
Operating temperature (transient)	T_{trans}	+150	–	+175	°C	Max 3 min., 10 times over lifetime device powered V_{bat}=3.6 V	■	1.4
Storage temperature	$T_{storage}$	-40°C	–	+150	°C	Max 1000 hours accumulated over lifetime between 125°C and 150°C. Device not powered	■	1.5
ESD robustness HBM	$V_{ESD,HBM}$		–	5000	V	All pins According to EIA/JESD22-A114-B	■	1.6
ESD robustness CDM	$V_{ESD,CDM}$		–	500	V	All pins (According to ESDA STM 5.3.1)	■	1.7
			–	750	V	Corner pins (According to ESDA STM 5.3.1)	■	1.8
Latch up	I_{LU}	-100	–	+100	mA	AEC-Q100 (transient current)	■	1.9
Input voltage	$V_{In,Digital}$	-0,3	–	V_{bat} + 0,3	V	Pin PP0, PP1, PP2	■	1.10
	$V_{In,LF}$	-0,3	–	+0,3	V	Pin LF, XLF	■	1.11
XTAL Input Voltage	$V_{In,XTAL}$	-0,3	–	V_{reg} + 0,3	V	Pin XTAL	■	1.12
Input and Output current (digital I/O pins)	$I_{IO,Digital}$	–	–	4	mA	Pin PP0, PP1, PP2	■	1.13
Input current (LF pins)	$I_{In,LF}$	–	–	4	mA	Pin LF, XLF	■	1.14
Input Pressure range	p_{In}	0	–	2000	kPa	–	■	1.15
		2000	–	2500	kPa	Max. 2 sec. 5 times over lifetime	■	1.16

Table 29 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Static acceleration	a_{static}		–	3000	g	–	■	1.17
Mechanical shock	a_{shock}		–	4000	g	Level: 4000 g peak Pulse duration: 0.3ms Waveform: Half sine Power: 3.0 V 5 shocks each dir. +/- x,y,z-axis (MIL-STD 883E)	■	1.18

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

4.3 Operating Range

The following operating conditions must not be exceeded in order to ensure correct operation of the SP37T.
All parameters specified in the following sections refer to these operating conditions unless otherwise mentioned.

Table 30 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Supply Voltage	V_{bat1}	2.1	–	3.6	V	Measurement of pressure, acceleration or temperature. Operation of LF receiver	■	2.1
	V_{bat2}	1.9	–	3.6	V	Battery measurements, microcontroller, RF transmitter, FLASH reading	■	2.2
	V_{bat3}	2.5	–	3.6	V	FLASH programming/erasing	■	2.5
Ambient Temperature	$T_{Operating}$	-40	–	125	°C	Normal Operation	■	2.11
	T_{Flash}	0	–	60	°C	FLASH programming/erasing	■	2.12
z-axis acceleration	$a_{Operating}$		–	1600	g	Exceeding this value will result in a higher pressure error than specified in Table 31	■	2.13

Attention: Test ■ means that the parameter is not subject to production test.
It was verified by design/characterization.

4.4 Characteristics

Product characteristics involve the spread of values within the specified voltage and ambient temperature range.

Supply voltage: Vbat = 1.9 V ... 3.6 V, unless otherwise specified

Ambient temperature: Tamb = -40°C ... +125°C, unless otherwise specified

4.4.1 Pressure Sensor (1300kPa variant)

Table 31 Pressure Sensor (1300 kPa variant)[1] , V_{bat} = 2.1 V...3.3 V

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Minimum Input Pressure	$p_{in,\ min}$	–	–	100	kPa	T= -40...125°C		4.1
Maximum Input Pressure[2]	$p_{in,\ max}$	1300	–	–	kPa	T= -40...125°C		4.2
Input Pressure Range	$p_{in,100\text{-}500}$	100	–	500	kPa	T= -40...125°C		4.3
Measurement Error	$p_{Error,100\text{-}500}$	-35	–	+35	kPa	T= -40...0°C		4.4
		-23	–	+23	kPa	T= 0...80°C		4.5
		-50	–	+50	kPa	T= 80...125°C		4.6
Input Pressure Range	$p_{in,500\text{-}1050}$	500	–	1050	kPa	T= -40...125°C		4.8
Measurement Error	$p_{Error,500\text{-}1050}$	-30	–	+30	kPa	T= -40...0°C		4.9
		-23	–	+23	kPa	T= 0...40°C		4.10
		-30	–	+30	kPa	T= 40...80°C		4.11
		-40	–	+40	kPa	T= 80...125°C		4.12
Input Pressure Range	$p_{in,1050\text{-}1300}$	1050	–	1300	kPa	T= -40...125°C		4.14
Measurement Error	$p_{Error,1050\text{-}1300}$	-35	–	+35	kPa	T= -40...0°C		4.15
		-25	–	+25	kPa	T= 0...40°C		4.16
		-30	–	+30	kPa	T= 40...80°C		4.17
		-50	–	+50	kPa	T= 80...125°C		4.18
RAW LSB resolution	$p_{LSB,RAW}$	0.9	–	2.0	kPa	T= -40°C	■	4.19
		1.12	–	2.3	kPa	T= 25°C	■	4.20
		1.3	–	2.75	kPa	T= 125°C	■	4.21
Pressure Measurement Stability Range	p_{sta}	-4.7		4.7	kPa	Minimum 95% of the measurements	■	4.22

1) This table is based on the average of 2 ADC samples

2) The maximum input pressure is equal or greater than 1300 kPa for +40°C< T < 125°C. For -40°C < T < + 40°C, the maximum input pressure is allowed to decrease below 1300 kPa but shall respect the following law:
Pin max >= 1300kPa + 4.15 * (T - 40°C)

Attention: Test ■ means that the parameter is not subject to production test.
It was verified by design/characterization.

4.4.2 z-axis Acceleration Sensor

Table 32 z-axis Acceleration Sensor[1], V_{bat} = 2.1 V...3.3 V

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Input Acceleration Range	a_{in}	-115	–	115	g	T= -40...125°C	■	5.1
Sensitivity Error	$a_{Sensitivity}$	-18.75	–	+18.75	%	T= -40...90°C		5.2
		-24	–	+24	%	T= 90...125°C		5.3
Offset Error	a_{Offset}	-6	–	+6	g	T= -20...70°C		5.4
		-8.5	–	+8.5	g	T= -40...-20°C T= 70...90°C		5.5
		-12	–	+12	g	T= 90...125°C		5.6
RAW LSB resolution	$a_{LSB,RAW}$	0.46	–	0.82	g	T= -40°C	■	5.9
		0.53	–	0.93	g	T= 25°C	■	5.10
		0.62	–	1.14	g	T= 125°C	■	5.11
Acceleration Measurement Stability Range	a_{random}	-1.6	–	+1.6	g	Minimum 95% of the measurements	■	5.12
Accelerometer Quality Factor	Q_{acc}	–	–	600	–		■	5.13

1) This table is based on the average of 2 ADC samples

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

4.4.3 Temperature Sensor

Table 33 Temperature Sensor[1], V_{bat} = 2.1 V...3.6 V

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Measurement Error	T_{Error}	-3	–	+3	°C	T= -20...70°C		6.1
		-5	–	+5	°C	T= -40..-20°C T= 70..125°C		6.2
Temperature Measurement Stability Range	T_{sta}	-1		+1	°C	Minimum 95% of the measurements	■	6.3

1) This table is based on the average of 2 ADC samples

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

4.4.4 Battery Sensor

Table 34 Battery Sensor[1], V_{bat} = 2.1 V...3.6 V

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Measurement Error	V_{Error}	-100	–	+100	mV	–		7.1

1) This table is based on the average of 2 ADC samples

4.4.5 Supply Currents

Table 35 Supply Currents

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Supply Current RF Transmission[1)] Modulation: FSK SFR DIVIC[1:0]: 11_B	$I_{P\ Low,1.9V,-40}$	–	–	8	mA	V_{bat}= 1.9 V, T= -40°C SFR RFTX.PAOP = 00_b P_{out} ~ 1 dBm $Z_{load,434MHz}$ ~ 500 Ohm $Z_{load,315MHz}$ ~ 650 Ohm	■	8.1
	$I_{P\ Low,3.0V,-40}$	–	–	9	mA	V_{bat}= 3.0 V, T= -40°C SFR RFTX.PAOP = 00_b P_{out} ~ 5 dBm $Z_{load,434MHz}$ ~ 500 Ohm $Z_{load,315MHz}$ ~ 650 Ohm	■	8.3
	$I_{P\ Low,3.0V,25}$	–	–	10	mA	V_{bat}= 3.0 V, T= 25°C SFR RFTX.PAOP = 00_b P_{out} ~ 5 dBm $Z_{load,434MHz}$ ~ 500 Ohm $Z_{load,315MHz}$ ~ 650 Ohm		8.4
	$I_{P\ Low,3.0V,125}$	–	–	12	mA	V_{bat}= 3.0 V, T= 125°C SFR RFTX.PAOP = 00_b P_{out} ~ 5 dBm $Z_{load,434MHz}$ ~ 500 Ohm $Z_{load,315MHz}$ ~ 650 Ohm	■	8.5
	$I_{P\ Med,1.9V,-40}$	–	–	10	mA	V_{bat}= 1.9 V, T= -40°C SFR RFTX.PAOP = 01_b P_{out} ~ 4 dBm $Z_{load,434MHz}$ ~ 300 Ohm $Z_{load,315MHz}$ ~ 450 Ohm	■	8.6
	$I_{P\ Med,3.0V,-40}$	–	–	12	mA	V_{bat}= 3.0 V, T= -40°C SFR RFTX.PAOP = 01_b P_{out} ~ 8 dBm $Z_{load,434MHz}$ ~ 300 Ohm $Z_{load,315MHz}$ ~ 450 Ohm	■	8.8
	$I_{P\ Med,3.0V,25}$	–	–	14	mA	V_{bat}= 3.0 V, T= 25°C SFR RFTX.PAOP = 01_b P_{out} ~ 8 dBm $Z_{load,434MHz}$ ~ 300 Ohm $Z_{load,315MHz}$ ~ 450 Ohm		8.9
	$I_{P\ Med,3.0V,125}$	–	–	15	mA	V_{bat}= 3.0 V, T= 125°C SFR RFTX.PAOP = 01_b P_{out} ~ 8 dBm $Z_{load,434MHz}$ ~ 300 Ohm $Z_{load,315MHz}$ ~ 450 Ohm	■	8.10

Table 35 Supply Currents (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
POWER DOWN current RAM lower memory block powered down SFR CFG2.PDLMB:1_b	$I_{PD,3.0V,25°C}$	–	–	700	nA	V_{bat}= 3.0 V, T= 25°C		8.13
	$I_{PD,3.0V,90°C}$	–	–	3.5	µA	V_{bat}= 3.0 V, T= 90°C	■	8.14
	$I_{PD,3.0V,125°C}$	–	–	19.5	µA	V_{bat}= 3.0 V, T= 125°C		8.15
POWER DOWN current RAM lower memory block kept powered SFR CFG2.PDLMB:0_b	$I_{PD\_RAMen,3.0V,25°C}$	–	–	750	nA	V_{bat}= 3.0 V, T= 25°C	■	8.16
	$I_{PD\_RAMen,3.0V,90°C}$	–	–	3.9	µA	V_{bat}= 3.0 V, T= 90°C	■	8.17
	$I_{PD\_RAMen,3.0V,125°C}$	–	–	21	µA	V_{bat}= 3.0 V, T= 125°C	■	8.18
THERMAL SHUTDOWN current RAM lower memory block powered down SFR CFG2.PDLMB:1_b	$I_{TS,3.0V,125°C}$	–	–	170	µA	V_{bat}= 3.0 V, T= 125°C		8.19
THERMAL SHUTDOWN current RAM lower memory block powered down SFR CFG2.PDLMB:1_B	$I_{TS\_RAMen,3.0V, 125°C}$	–	–	175	µA	V_{bat}= 3.0 V, T= 125°C	■	8.20
IDLE current SFR DIVIC: 00_B Timer0 active	$I_{Idle,3.0V,25°C}$	–	–	1	mA	V_{bat}= 3.0 V, T= 25°C		8.21
	$I_{Idle,3.0V,125°C}$	–	–	1.1	mA	V_{bat}= 3.0 V, T= 125°C	■	8.22
RUN current (Peripheral units in active state) SFR DIVIC: 00_B	$I_{Run,3.0V,25°C}$	–	–	2.1	mA	V_{bat}= 3.0 V, T= 25°C		8.23
	$I_{Run,3.0V,125°C}$	–	–	2.4	mA	V_{bat}= 3.0 V, T= 125°C	■	8.24
RUN current (PLL enabled) SFR DIVIC: 11_B	$I_{PLL,3.0V,25°C}$	–	–	8	mA	V_{bat}= 3.0 V, T= 25°C	■	8.25
	$I_{PLL,3.0V,125°C}$	–	–	9	mA	V_{bat}= 3.0 V, T= 125°C	■	8.26
LF Receiver current SFR bits LFBBM: 00_B	$I_{LF\_Add,AFE}$			4	µA		■	8.27
LF Receiver current[2] SFR bits LFBBM: 01_B	$I_{LF\_Add,I}$			6.1	µA	V_{bat}= 3.0 V, T= -40...90°C	■	8.28
	$I_{LF\_Add,f,}$			7.8	µA	V_{bat}= 3.0 V, T=-40...125°C	■	8.29

1) These parameters were obtained using the SP37T Test Board. Tolerances of the passive elements (matching network) not taken into account. The environment of the customer application have not been taken into account

2) This additional LF current is valid for all LF baseband conditions. The difference in current consumption between decoding and not decoding is negligible.

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

4.4.6 RF Transmitter

Table 36 RF Transmitter[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Transmit Frequency	$f_{Tx,315MHz}$	300		320	MHz	–	■	9.1
	$f_{Tx,433.92MHz}$	433		450	MHz	–	■	9.2
Output Power transformed into 50 Ohm	$P_{low,}$ 433.92 MHz	4	5	6	dBm	V_{bat}= 3.0 V, T= 25°C SFR RFTX.PAOP = 00_b Zload~ 500 Ohm		9.5
	$P_{med,}$ 433.92 MHz	7	8	9	dBm	V_{bat}= 3.0 V, T= 25°C SFR RFTX.PAOP = 01_b Zload~ 300 Ohm		9.6
	$P_{low, 315 MHz}$	4	5	6	dBm	V_{bat}= 3.0 V, T= 25°C SFR RFTX.PAOP = 00_b Zload~ 650 Ohm		9.9
	$P_{med, 315 MHz}$	7	8	9	dBm	V_{bat}= 3.0 V, T= 25°C SFR RFTX.PAOP = 01_b Zload~ 450 Ohm		9.10
Output Power change over temperature	$dP_{-40°C}$	0	–	+1	dB	V_{bat}= 3.0 V, T= -40°C	■	9.13
Output Power change over temperature	$dP_{125°C}$	0	–	-1.5	dB	V_{bat}= 3.0 V, T= 125°C	■	9.14
Output Power change over supply voltage	$dP_{1.9V}$	0	–	-8	dB	V_{bat}= 1.9 V, T= 25°C	■	9.15
Output Power change over supply voltage	$dP_{2.5V}$	0	–	-2.8	dB	V_{bat}= 2.5 V, T= 25°C	■	9.17
Output Power change over supply voltage	$dP_{3.6V}$	0	–	+2.8	dB	V_{bat}= 3.6 V, T= 25°C	■	9.18
Datarate	DR_{RF}	–	–	10	kBit/s	Equivalent to 20 kchips/s	■	9.19
Datarate accuracy	dDR_{RF}	–	–	+/-1	%	$f_{crystal}$ = 18.080/19.6875MHz DR_{RF} = 9600Bit/s SFR TMOD.T1CLK = 01_b SFR TMOD.TCLKM = 1_b	■	9.20
Spurious emissions (incl. harmonics) @ f_{Tx} = 315 MHz	$P_{spurii,FCC}$	–	–	-28	dBc	FCC 15.231a/e 2nd - 10th harmonic other spurious <1GHz	■	9.21

Table 36 RF Transmitter[1)] (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Spurious emissions (incl. harmonics) @ f_{Tx} = 433.92 MHz	$P_{spurii,ETSI,RB}$	–	–	-54	dBm	ETSI EN300220 BW = 10 kHz, 47-74 MHz, 87.5 MHz-118 MHz, 174-230 MHz, 470-862 MHz	■	9.22
Spurious emissions (incl. harmonics) @ f_{Tx} = 433.92 MHz	$P_{spurii,ETSI,<1G}$	–	–	-36	dBm	ETSI EN300220 BW = 10 kHz other <1 GHz	■	9.23
Spurious emissions (incl. harmonics) @ f_{Tx} = 433.92 MHz	$P_{spurii,ETSI,>1G}$	–	–	-30	dBm	ETSI EN300220 BW = 10 kHz >1 GHz	■	9.24
Phase Noise	$P_{PN,\ 10kHz}$	–	–	-80	dBc/Hz	fCarrier +/- 10 kHz	■	9.25
	$P_{PN,\ 100kHz}$	–	–	-80	dBc/Hz	fCarrier +/- 100 kHz	■	9.26
	$P_{PN,\ 1\ MHz}$	–	–	-90	dBc/Hz	fCarrier +/- 1 MHz	■	9.27
	$P_{PN,\ 10\ MHz}$	–	–	-120	dBc/Hz	fCarrier +/- 10 MHz	■	9.28

1) The parameter in this table were obtained using the SP37T Test Board. Tolerances of the passive elements (matching network) not taken into account. The environment of the customer application have not been taken into account.

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

4.4.7 LF Receiver

Table 37 LF Receiver, V_{bat} = 2.1 V...3.6 V

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Differential Input Capacitance	$C_{Input,LF}$	8	–	12	pF	@ 125 kHz	■	10.1
Differential Input Resistance DC	$R_{Input,LF}$	1M			Ohm	AGC disabled		10.2

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

LF Receiver Telegram

```
// Basic LF Telegram Configuration
LFRX0  = 0x8C;   // AGC Threshold, LF Antenna Voltage Divider Factor
LFRX1  = 0x20;   // AGC Decay Time Constant, Autocalibration Time
LFRX2  = 0x77;   // AGC Attack Time Constant
LFCDM0 = 0x1C;   // Enable Autocalibration
LFRXC  = 0x14;   // Enable AGC, LF Baseband on while LFRx enabled, Enable LFRx
```

Figure 68 LF Receiver Special Function Register Settings for Telegram Mode

Table 38 LF Receiver Telegram, V_{bat} = 2.1 V...3.6 V, f_{LF} = 120 kHz...130 kHz

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Datarate	DR_{LF}	–	3.9	–	kBit/s	–		10.6
Datarate error	$DR_{error,c}$	-2.5		2.5	%	Using “LFBaudrateCalibration ” ROM Library function once for initial calibration in production @ Vbat= 2.5 V, T= 25°C	■	10.8
Preamble length	$t_{preamble}$	2	4	–	ms	DR_{LF} = 3.9 kbit/s,t_{bit} = 1/DR_{LF}	■	10.9
Settling time	$t_{settling}$	2.4	3.5	5.8	ms	LFRX enabled by LFOOT[1)] Min/Max tolerances from 2 kHz RC Oscillator applied SFR LFRX1.ACT = 10_b SFR bit ENOOTIM = 1_b	■	10.10
LF Telegram Sensitivity	$LF_{tele,det,f}$			2.5	mVpp	Refer to test case T-1.2	■	10.13

1) If LF Receiver (LFRX) is enabled by CPU via SFR LFRXC.ENLFRX or autocalibration cycle is started by SFR LFRXC.CDRECAL then up to one additional 2 kHz RC oscillator period must be added to the given times

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

Table 39 LF Receiver Telegram, V_{bat} = 2.1 V...3.6 V, T = -20 °C...90 °C, f_{LF} = 120 kHz...130 kHz

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
LF Telegram Sensitivity	$LF_{tele,det,l}$			1.3	mVpp	Refer to test case T-1.2		10.19

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

LF Receiver Carrier Detector

```
// Defines
#define CDETT_Levels_Base_Address 0x580E
#define CDETT_Level 1  // Configure Carrier Detector Threshold Level (values 1, 2 or 3)

#define CDFLT_Times_Base_Address 0x580B
#define CDFLT_Time 1   // Configure Carrier Detector Filter Time (values 1, 2 or 3)

// Basic LF Carrier Detection Configuration, Sensitivity Settings, Filter Settings
LFCDM0 = 0x1C;   // Carrier Detector Dynamic Treshold, Enable Autocalibration & Freeze Hold

// Load Carrier Detector Filter Time from Flash
LFCDFLT = CBYTE[CDFLT_Times_Base_Address-(CDFLT_Time-3)];

// Load Carrier Detector Threshold from Flash
LFRX0 = CBYTE[CDETT_Levels_Base_Address-(CDETT_Level-3)];

LFRX1 = 0x10;    // AGC Decay Time Constant, Autocalibration Time
LFRX2 = 0x77;    // AGC Attack Time Constant
LFRXC = 0x04;    // Enable AGC, LF Baseband off, Enable LFRx
```

Figure 69 LF Receiver Special Function Register Settings for Carrier Detection

Table 40 LF Receiver Carrier Detection, V_{bat} = 2.1 V...3.6 V, f_{LF} = 120 kHz...130 kHz

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Auto-Calibration time	$t_{calibration,1}$	3.8	5.5	9.1	ms	LFRX enabled by LFOOT[1)] Min/Max tolerances from 2 kHz RC Oscillator applied SFR LFRX1.ACT = 01_b SFR bit ENOOTIM = 1_b	■	10.20
Maximum Amplitude for Carrier Detector Filter	$S_{max,f}$	30			mVpp	Refer to test case **T-1.1**	■	10.22
LF Carrier Detect Threshold 1[2)]	$S_{nodet,1,f}$	0.33			mVpp	Refer to test case **T-1.2**	■	10.23
	$S_{det,1,f}$			3.35	mVpp		■	10.24
LF Carrier Detect Threshold 2[2)]	$S_{nodet,2,f}$	2			mVpp	Carrier Detector Filter Time 1 Refer to test case **T-1.2**	■	10.25
	$S_{det,2,f}$			11	mVpp		■	10.26
LF Carrier Detect Threshold 3[2)]	$S_{nodet,3,f}$	10			mVpp	Refer to test case **T-1.2**	■	10.27
	$S_{det,3,f}$			50	mVpp		■	10.28
Carrier Detector Filter Time 1	$t_{CDnodet,1}$	62			µs	Refer to test case **T-1.1**		10.29
	$t_{CDdet,1}$			240	µs			10.30
Carrier Detector Filter Time 2	$t_{CDnodet,2}$	500			µs	Refer to test case **T-1.1**	■	10.31
	$t_{CDdet,2}$			800	µs		■	10.32
Carrier Detector Filter Time 3	$t_{CDnodet,3}$	800			µs	Refer to test case **T-1.1**	■	10.33
	$t_{CDdet,3}$			1150	µs		■	10.34

Table 40 LF Receiver Carrier Detection, V_{bat} = 2.1 V...3.6 V, f_{LF} = 120 kHz...130 kHz (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Carrier Detection Freeze Hold Time	$t_{CDCFH,125}$	2			s	T=125°C	■	10.35
	$t_{CDCFH,25}$	300			s	T=25°C	■	10.36

1) If LF Receiver (LFRX) is enabled by CPU via SFR LFRXC.ENLFRX or autocalibration cycle is started by SFR LFRXC.CDRECAL then up to one additional 2 kHz RC oscillator period must be added to the given times
2) For reliable carrier detection a minimum pulse length of 240µs is required

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

Table 41 LF Receiver Carrier Detection, V_{bat} = 2.3 V...3.3 V, T = -20 °C...90 °C, f_{LF} = 120 kHz...130 kHz

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Maximum Amplitude for Carrier Detector Filter	$S_{max,I}$	100			mVpp	Refer to test case T-1.1	■	10.37
LF Carrier Detect Threshold 2[1)2)]	$S_{nodet,2,I}$	3			mVpp	Carrier Detector Filter Time 1 Refer to test case T-1.2		10.38
	$S_{det,2,I}$			10	mVpp			10.39

1) For reliable carrier detection a minimum pulse length of 240µs is required
2) Tested with LF Carrier Detector Filter Time 1 - verified by characterization/design for LF Carrier Detector Filter Times 2, 3

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

4.4.8 LF Test Cases

T-1.1, Test Case for large LF signal measurements

Setup

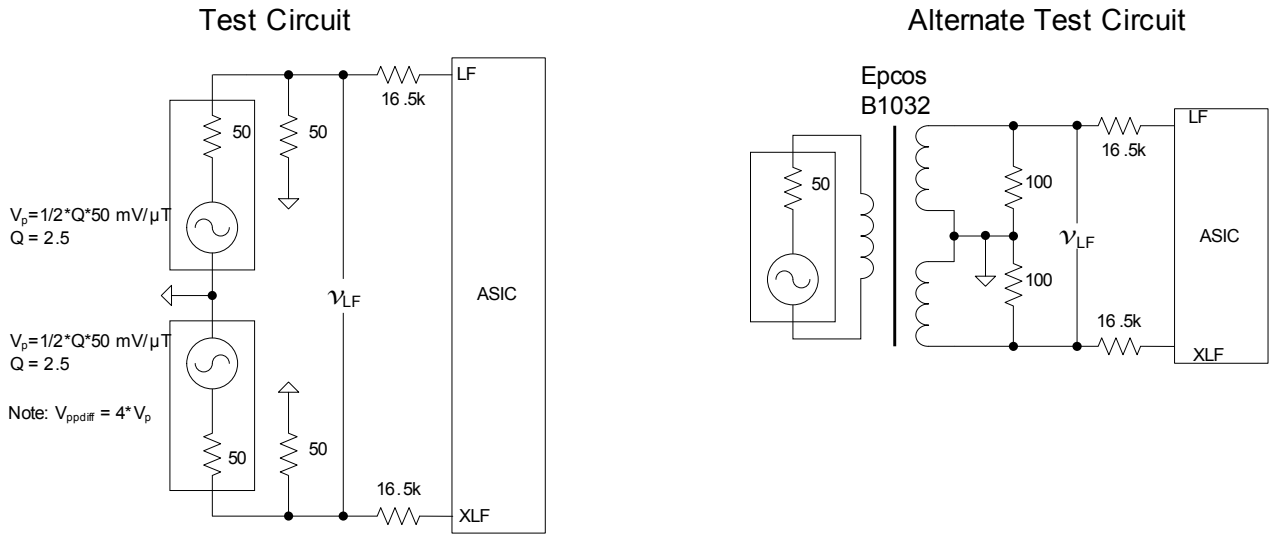


Figure 70 Test Circuit for large LF signal measurements

T-1.2, Test Case for small LF signal measurements

Setup

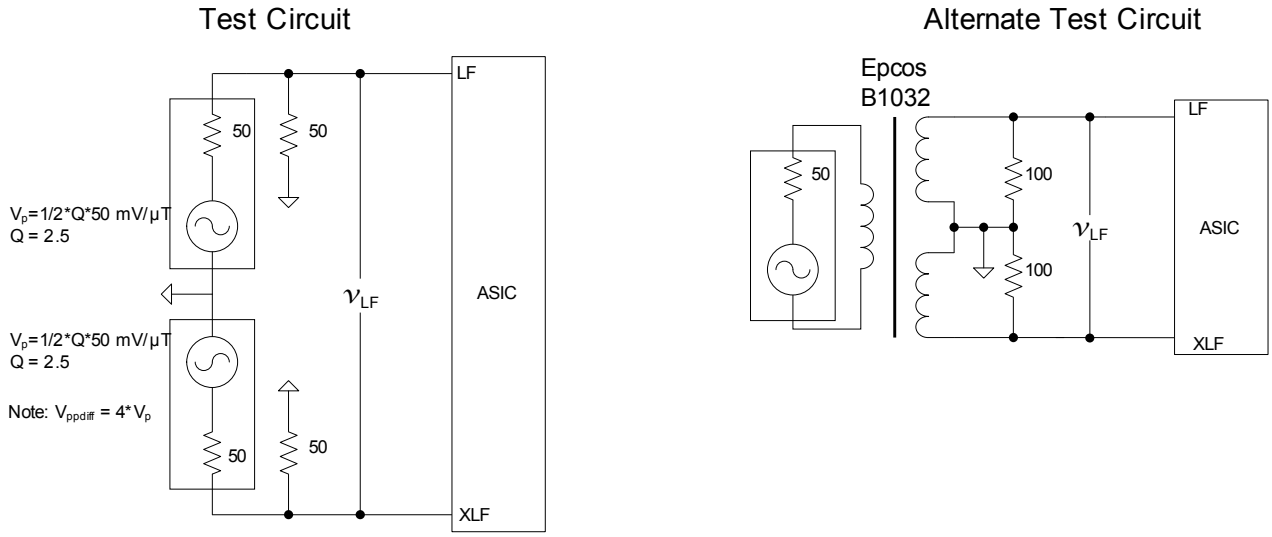


Figure 71 Test Circuit for small LF signal measurements

4.4.9 Crystal Oscillator

Table 42 Crystal Oscillator, $f_{Crystal}$ = 18 MHz...20 MHz

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Crystal startup time	$t_{XTAL,Startup}$	–	700	1250	µs	Measured on SP37T Test Board (see **"Test Board" on Page 142**) with Crystal NX5032SD EXS00A-03552 C_L=12 pF, $f_{Crystal}$ = 18,08 MHz	■	12.1
Parasitic capacitance from XTAL pin to GND (PCB tracks, XTAL shield, etc.)	$C_{parasitic}$	–	–	4	pF	–	■	12.2
Serial resistance of the crystal	R_{Rmax}	–	–	60	Ohm	–		12.3
Input inductance	$L_{OSC,3.0V,25°C}$	2.0	2.9	3.8	µH	V_{bat}= 3.0 V, T= 25°C		12.4
	L_{OSC}	1.8	2.9	4.3	µH	–	■	12.5
Internal cap bank maximum capacitance	C_{bank}	36	40	44	pF	Between pin XTALCAP and pin XGND SFR XTAL1 = FF_H SFR RFENC.TXDD = 1	■	12.6
FSK Switch ON resistance	$R_{Switch,ON}$			60	Ohm	Between pin XTALCAP and pin XGND SFR bit FSKSWITCH = 1_B SFR RFENC.TXDD = 1		12.7
FSK Switch OFF resistance	$R_{Switch,OFF}$	100			kOhm	Between pin XTALCAP and pin XGND SFR bit FSKSWITCH = 0_B SFR RFENC.TXDD = 1		12.8
FSK Switch OFF capacitance	$C_{Switch,OFF}$	3.2	3.5	3.8	pF	Between pin XTALCAP and pin XGND SFR XTAL1 = $0x00_B$ SFR bit FSKSWITCH = 0_B SFR RFENC.TXDD = 1	■	12.9

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

4.4.10 12 MHz RC HF Oscillator

Table 43 12 MHz RC HF Oscillator

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Operating frequency	$f_{RC,HF}$	11.04	12.00	12.96	MHz			13.1

4.4.11 2 kHz RC LP Oscillator

Table 44 2 kHz RC LP Oscillator

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Operating frequency	$f_{RC,LP}$	1.3	2	2.7	kHz	V_{bat}= 3.0 V, T= 25°C		14.1
Frequency drift	$df_{RC,LP}$	-7	–	+7	%	–		14.2

4.4.12 Interval Timer & LF On/Off Timer

Table 45 Interval Timer / LF On/Off Timer

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Interval Timer Precounter calibration error	df_{ITP}	-0.083	–	0	%/Hz	Error is dependent upon Interval Timer timebase specified to “Interval Timer Calibration” ROM Library function. This error does not include reference clock (XTAL or 12 MHz RC oscillator) and 2 kHz RC LP oscillator drift errors.	■	15.1
LF On/Off Timer calibration error “On” Time	df_{LFON}	-1.64	–	4.92	%	Error is assumes usage of “Interval Timer Calibration” ROM Library function. This error does not include reference clock (XTAL or 12 MHz RC oscillator) and 2 kHz RC LP oscillator drift errors.	■	15.2
LF On/Off Timer calibration error “Off” Time	df_{LFOFF}	-1.64	–	0	%	Error is assumes usage of “Interval Timer Calibration” ROM Library function. This error does not include reference clock (XTAL or 12 MHz RC oscillator) and 2 kHz RC LP oscillator drift errors.	■	15.3

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

4.4.13 Voltage Regulator

Table 46 Voltage Regulator[1)2)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Regulated output voltage in RUN state	V_{REG}	1.9	2.1	2.4	V	V_{bat}= 2.1 V - 3.6 V,		17.1
Regulated output voltage at low battery in RUN state	$V_{REG,Low}$	1.8	–	2.1	V	V_{bat}= 1.9 V - 2.1 V		17.2
Regulated output voltage in Programming mode	V_{REG}	2.3	2.5	2.75	V	V_{bat}= 2.5 V - 3.6 V		17.4
Regulated output voltage in POWERDOWN and THERMAL SHUTDOWN	$V_{REG,PD}$	1.7	–	2.5	V	–		17.5
External Capacitance at Vreg Pin	C_{VREG}	60	100	–	nF	Maximum ESR 15 Ohm	■	17.6

1) The voltage regulator is designed to supply only the internal blocks of the SP37T and not designed to drive any external circuitry, thus only the decoupling cap is allowed to be connected to pin V_{reg}. A 100nF decoupling cap with an maximum ESR of 15 Ohm is recommended for proper operation.

2) The voltage regulator is designed to supply only the internal blocks of the SP37T. It is not designed to drive any external circuitry, including the embedded PA. A 100nF decoupling cap with an maximum ESR of 15 Ohm is recommended for proper operation. It is not prohibited to connect the PA to pin Vreg as long as the customer verifies that the behavior of the different SP37T devices is always correct and within the specification.

Attention: Test ■ means that the parameter is not subject to production test.
It was verified by design/characterization.

4.4.14 Power On Reset / Brown Out Reset

Table 47 Power On Reset / Brown Out Reset

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Power On Reset level	V_{POR}	0.2	0.4	1.7	V	Min. supply voltage level measured at Pin V_{REG} for a valid logic LOW at Power On Reset circuit	■	16.1
Power On Reset release level	V_{THR}	1.7	–	1.8	V	Measured at Pin V_{REG}		16.3
Power On reset time	t_{POR}	0.25	–	10	ms	–		16.4
Brown Out detect level in RUN state	$V_{RUN,BRD}$	1.7	–	1.8	V	Measured at Pin V_{REG}		16.5
Brown Out detect level in POWERDOWN and THERMAL SHUTDOWN	$V_{PD,BRD}$	0.7	–	1.7	V	Measured at Pin V_{REG}		16.8
Mode selection time	t_{mode}	–	–	2.5	ms	–	■	16.10
Minimum detectable Brown Out glitch in RUN state	$t_{Brownout,RUM}$	–	–	1	µs	–	■	16.11
Minimum detectable Brown Out glitch in POWERDOWN and THERMAL SHUTDOWN state	$t_{Brownout,PD}$	–	–	100	µs	–	■	16.12

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

4.4.15 VMIN Detector

Table 48 VMIN Detector

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Low battery threshold warning level	TH_{LBAT}	2.0	2.1	2.2	V	Used by ROM Library functions only		18.1

4.4.16 FLASH Memory

Table 49 FLASH Memory

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Erase/Program temperature	T_{FL}	0	–	+60	°C	–	■	19.1
Erase/Program supply voltage	V_{bat3}	2.5	–	3.6	V	–	■	19.2
Endurance	En_{Flash}	100	–	–	cycles	Programming/erase cycles per wordline	■	19.3
Erase time	t_{Erase}	–	102	–	ms	Min/max can be derived by adding the tolerance and drift of the 12 MHz RC HF Osc. (see Table 43)	■	19.4
Write time per FLASH line	$t_{Program}$	–	2.2	–	ms	FLASH line = 32 Byte min/max can be derived by adding the tolerance and drift of the 12 MHz RC HF Osc. (see Table 43)	■	19.5

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

4.4.17 TMAX Detector

Table 50 TMAX Detector

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
THERMAL SHUTDOWN release temperature	$T_{TMAX,Release}$	115.5	–	–	°C	Used by “ThermalShutdown” ROM Library function only. The TMAX enable temperature is verified to be above the release temperature.	■	20.1
THERMAL SHUTDOWN enable temperature	$T_{TMAX, Enable}$	117	–	125	°C			20.2

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

4.4.18 Watchdog Timer

Table 51 Watchdog Timer

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Watchdog timeout	$t_{Watchdog}$	0.6	1	1.7	s	Min/max is derived by considering the tolerance and drift of the 2 kHz RC LP Osc. (see Table 44)	■	21.1

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

4.4.19 Digital I/O pins

Table 52 Digital I/O pins

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Input LOW voltage	V_{IL}	-0.2	–	0.4	V	–		22.1
Input HIGH voltage	V_{IH}	VBat - 0.4	–	VBat + 0.2	V	–		22.2
Output LOW voltage	V_{OL}	–	–	0.5	V	IOL= 1.6 mA		22.3
Output HIGH voltage	V_{OH}	VBat - 0.5	–	–	V	IOH= -1.6 mA		22.4
Output transition time	$t_{HL, LH}$	–	–	30	ns	20 pF load, 10% ... 90%	■	22.5
Parasitic capacitance	C_{pad}	–	–	5	pF	–	■	22.6
Internal pullup / pulldown resistor	$R_{up/down}$	35	50	70	kOhm	Pin PP0, PP1		22.7
	$R_{up/down}$	175	250	335	kOhm	Pin PP2		22.8

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

4.4.20 I²C Interface

Table 53 I²C Interface

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
I²C bitrate	DR_{I2C}	–	–	400	kbit/s	SFR DIVIC[1:0]: 00_B	■	23.1

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

5 Package Information

5.1 Package Outline

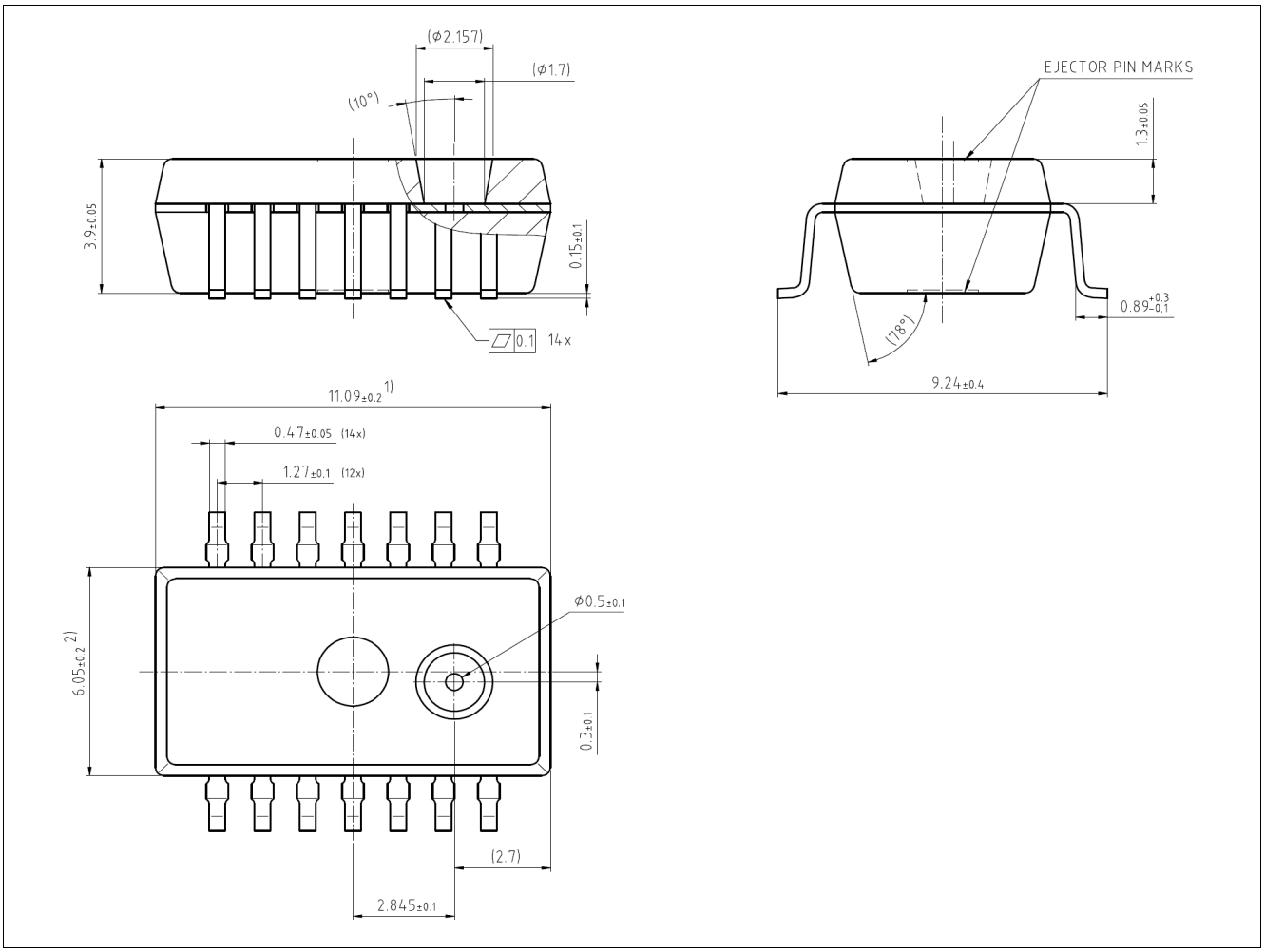


Figure 72 PG-DSOSP-14-6 Package Dimensions

Dimensions in [mm][1)2)]

1) Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs do not exceed 0.15mm (0.006 inch) per side.

2) Dimension does not include inter-lead flash or protrusions. Inter-lead flash and protrusions do not exceed 0.25mm (0.010 inch) per side.

5.2 Identification Code

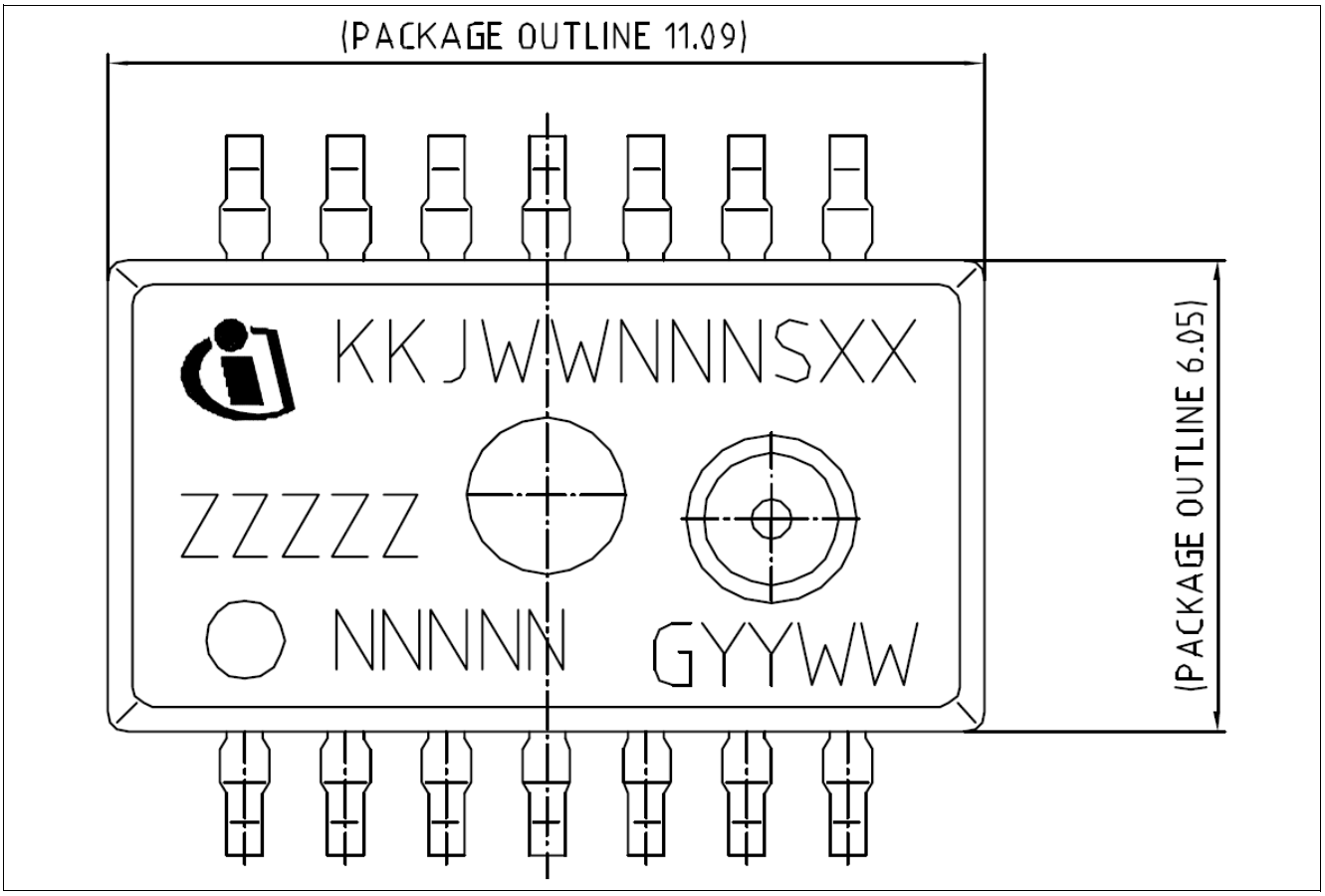


Figure 73 PG-DSOSP-14-6 marking

The marking for the SP37T is on the topside of the package.

5.2.1 Identification Code Definition

KKJWWNNNSXX: Infineon Lot Number

ZZZZZ: Product Identification (SP370)

O: Pin 1 Marking

NNNNN: Manufacturer Version (NN = 23 Villach Sensor) and Sensor Information Code (NN = 15)

G: Green Package Indicator[1)]

YYWW: Date Code (YY = Year, WW = week)

1) The Green Package fulfils the solder condition for Pb-Free Assembly according to IPC/JEDEC J-STD-020C.

References

This section contains documents used for cross-reference throughout this document.

[1] SP37T ROM Library function guide

www.infineon.com

Published by Infineon Technologies AG