CoolMOS^{TM} Power Transistor

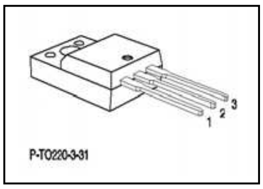
Product Summary

V_{DS} @T_{jmax}	550	V
$R_{DS(on),max}$	0.250	Ω
$Q_{g,typ}$	27	nC

Features

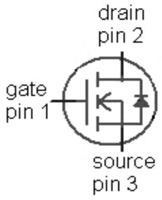
- Lowest figure of merit R_{ON} x Q_g
- Ultra low gate charge
- Extreme dv/dt rated
- High peak current capability
- Pb-free lead plating; RoHS compliant; Halogen free for mold compound
- Qualified for industrial grade applications according to JEDEC[0)]

TO220 FP



CoolMOS CP is designed for:

- Hard- & Softswitching SMPS topologies
- CCM PFC for ATX, Notebookadapter, PDP and LCD TV
- PWM for ATX, Notebookadapter, PDP and LCD TV



Type	Package	Marking
IPA50R250CP	PG-TO220FP	5R250P

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current[1)]	I_D	T_C=25 °C	13	A
		T_C=100 °C	9	
Pulsed drain current[2)]	$I_{D,pulse}$	T_C=25 °C	31	
Avalanche energy, single pulse	E_{AS}	I_D=5.2 A, V_{DD}=50 V	345	mJ
Avalanche energy, repetitive t_{AR}[2),3)]	E_{AR}	I_D=5.2 A, V_{DD}=50 V	0.52	
Avalanche current, repetitive t_{AR}[2),3)]	I_{AR}		5.2	A
MOSFET dv/dt ruggedness	dv/dt	V_{DS}=0...400 V	50	V/ns
Gate source voltage	V_{GS}	static	±20	V
		AC (f>1 Hz)	±30	
Power dissipation	P_{tot}	T_C=25 °C	33	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
Mounting torque		M2.5 screws	60	Ncm

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous diode forward current[1]	I_S	T_C=25 °C	7.8	A
Diode pulse current[2]	$I_{S,pulse}$		31	
Reverse diode dv/dt[4]	dv/dt		15	V/ns

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	3.75	K/W
Thermal resistance, junction - ambient	R_{thJA}	leaded	-	-	62	
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	1.6 mm (0.063 in.) from case for 10 s	-	-	260	°C
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=250 µA	500	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=0.52 mA	2.5	3	3.5	
Zero gate voltage drain current	I_{DSS}	V_{DS}=500 V, V_{GS}=0 V, T_j=25 °C	-	-	1	µA
		V_{DS}=500 V, V_{GS}=0 V, T_j=150 °C	-	10	-	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=7.8 A, T_j=25 °C	-	0.22	0.25	Ω
		V_{GS}=10 V, I_D=7.8 A, T_j=150 °C	-	0.54	-	
Gate resistance	R_G	f=1 MHz, open drain	-	2.2	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz	-	1420	-	pF
Output capacitance	C_{oss}		-	63	-	
Effective output capacitance, energy related[5)]	$C_{o(er)}$	V_{GS}=0 V, V_{DS}=0 V to 400 V	-	60	-	
Effective output capacitance, time related[6)]	$C_{o(tr)}$		-	130	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=400 V, V_{GS}=10 V, I_D=7.8 A, R_G=23.1 Ω	-	35	-	ns
Rise time	t_r		-	14	-	
Turn-off delay time	$t_{d(off)}$		-	80	-	
Fall time	t_f		-	11.0	-	
Gate Charge Characteristics						
Gate to source charge	Q_{gs}	V_{DD}=400 V, I_D=7.8 A, V_{GS}=0 to 10 V	-	6	-	nC
Gate to drain charge	Q_{gd}		-	9	-	
Gate charge total	Q_g		-	27	36	
Gate plateau voltage	$V_{plateau}$		-	5.2	-	V
Reverse Diode						
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=7.8 A, T_j=25 °C	-	0.9	1.2	V
Reverse recovery time	t_{rr}	V_R=400 V, I_F=I_S, di_F/dt=100 A/µs	-	300	-	ns
Reverse recovery charge	Q_{rr}		-	3.1	-	µC
Peak reverse recovery current	I_{rrm}		-	23	-	A

[0)] J-STD20 and JESD22

[1)] Limited only by $T_{j,max}$

[2)] Pulse width t_p limited by $T_{j,max}$

[3)] Repetitive avalanche causes additional power losses that can be calculated as $P_{AV}=E_{AR}*f$.

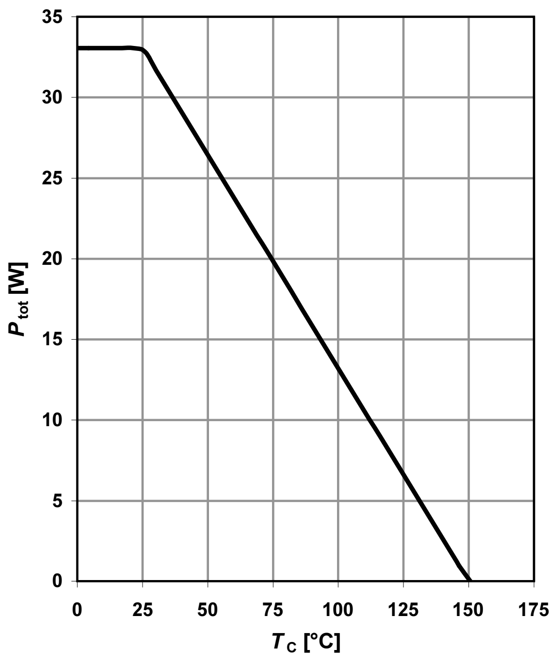
[4)] $I_{SD} \leq I_D$, $di/dt \leq 200$A/µs, V_{DClink}=400V, $V_{peak}<V_{(BR)DSS}$, $T_j<T_{jmax}$, identical low and high side switch

[5)] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

[6)] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

1 Power dissipation

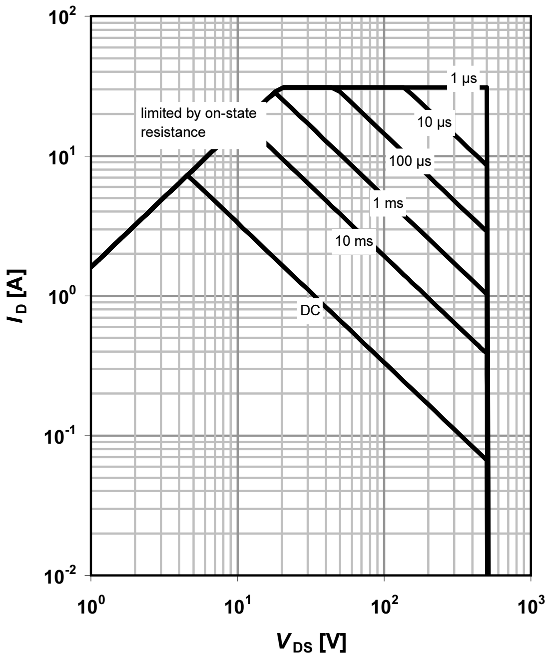
P_{tot}=f(T_C)



2 Safe operating area

I_D=f(V_{DS}); T_C=25 °C; D=0

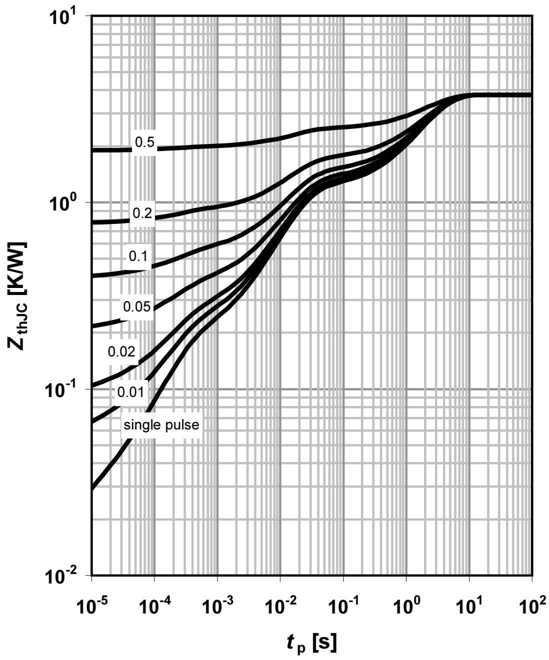
parameter: t_p



3 Max. transient thermal impedance

$Z_{(thJC)}$=f(t_p);

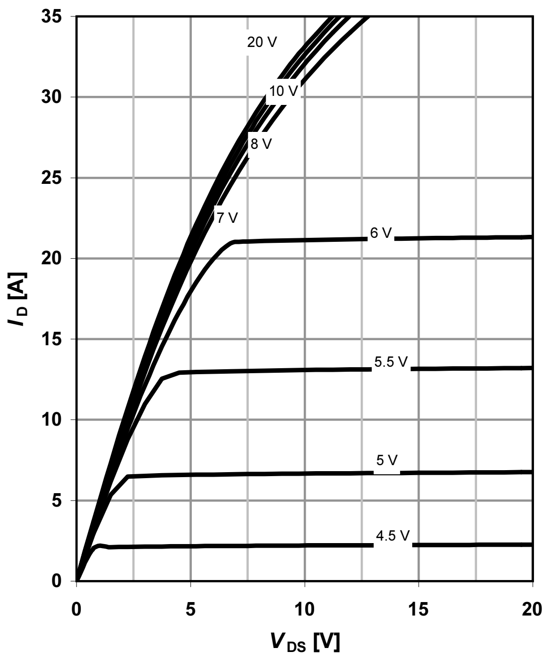
parameter: $D=t_p/T$



4 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

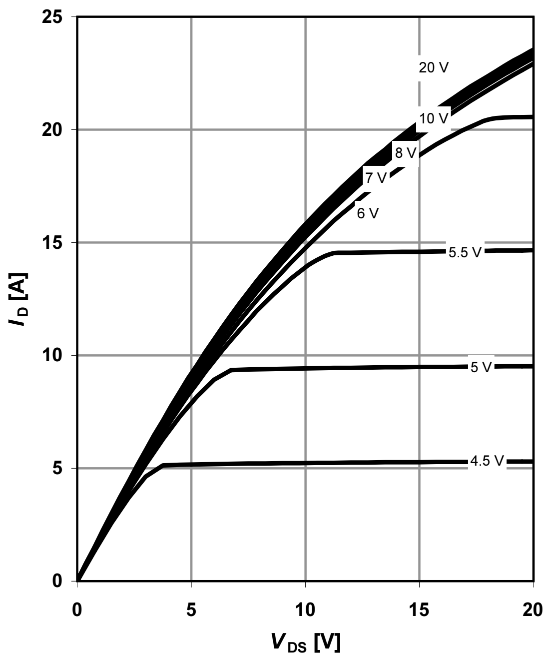
parameter: V_{GS}



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=150 °C

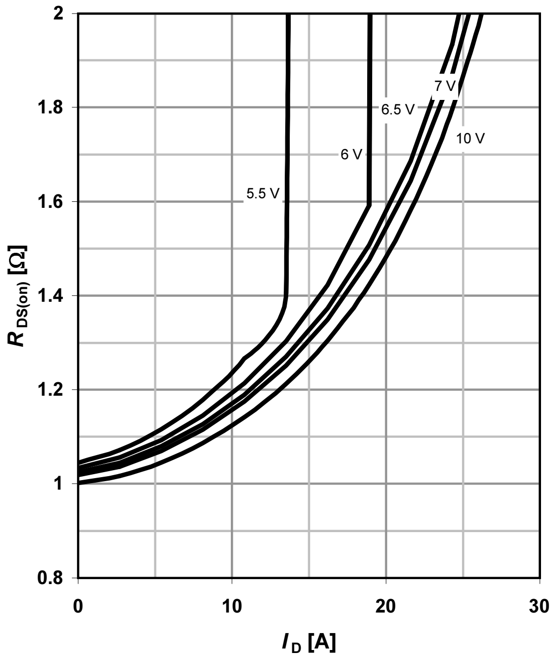
parameter: V_{GS}



6 Typ. drain-source on-state resistance

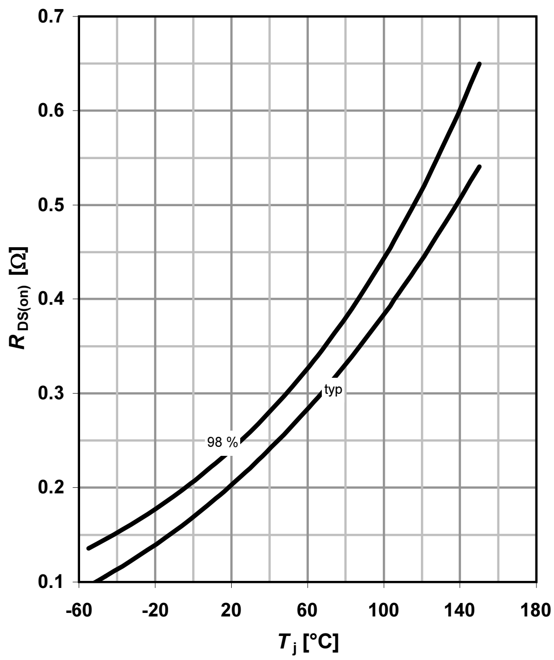
$R_{DS(on)}$=f(I_D); T_j=150 °C

parameter: V_{GS}



7 Drain-source on-state resistance

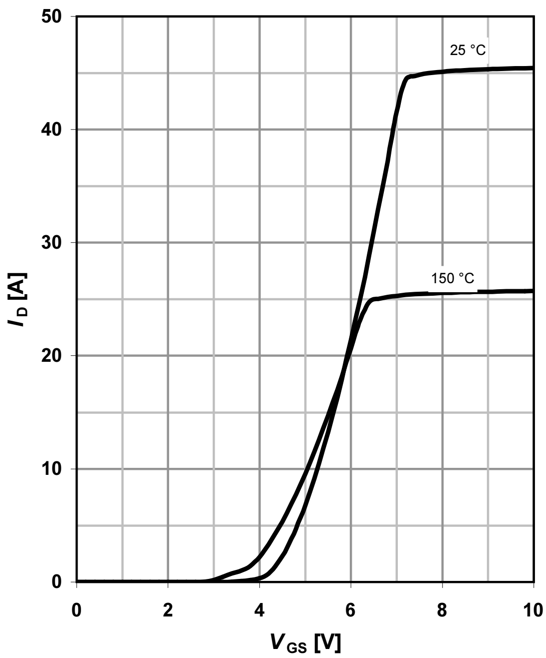
$R_{DS(on)}$=f(T_j); I_D=7.8 A; V_{GS}=10 V



8 Typ. transfer characteristics

I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$

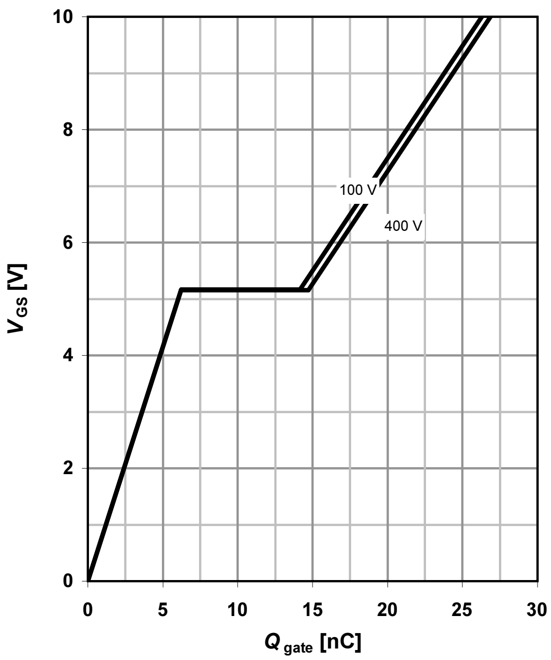
parameter: T_j



9 Typ. gate charge

V_{GS}=f(Q_{gate}); I_D=7.8 A pulsed

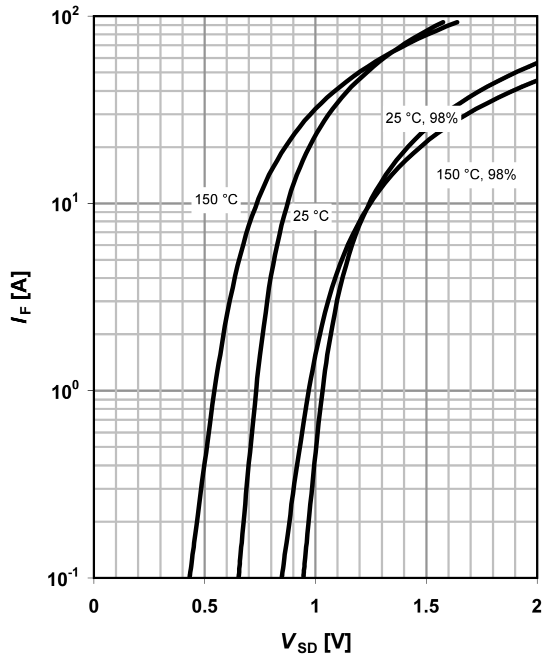
parameter: V_{DD}



10 Forward characteristics of reverse diode

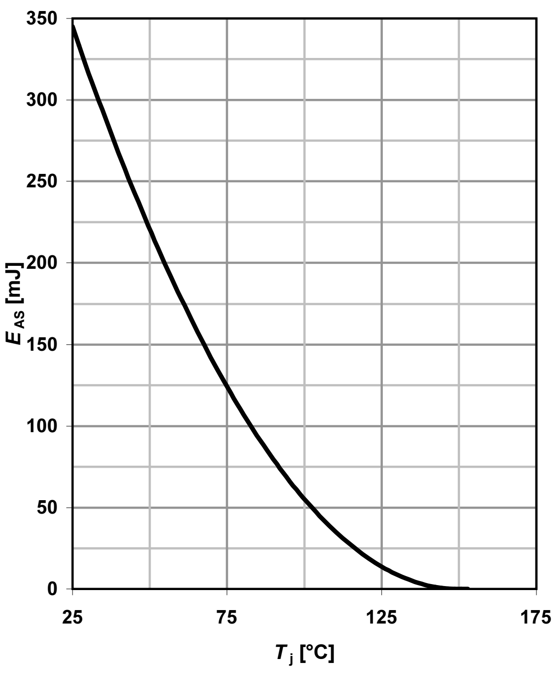
I_F=f(V_{SD})

parameter: T_j



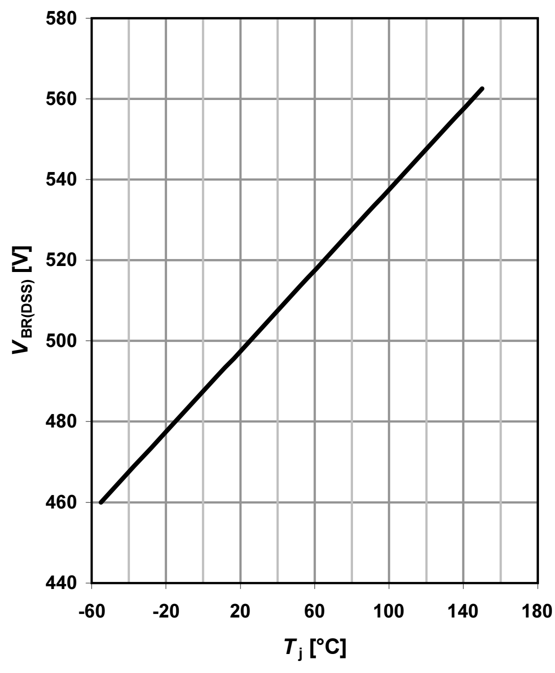
11 Avalanche energy

E_{AS}=f(T_j); I_D=5.2 A; V_{DD}=50 V



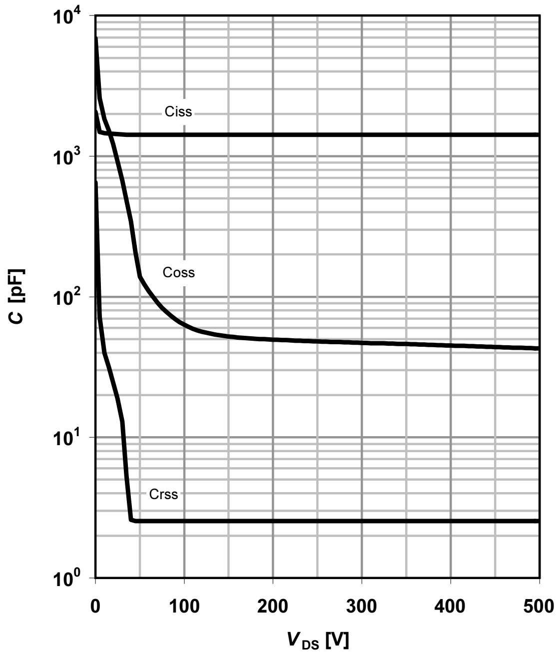
12 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=0.25 mA



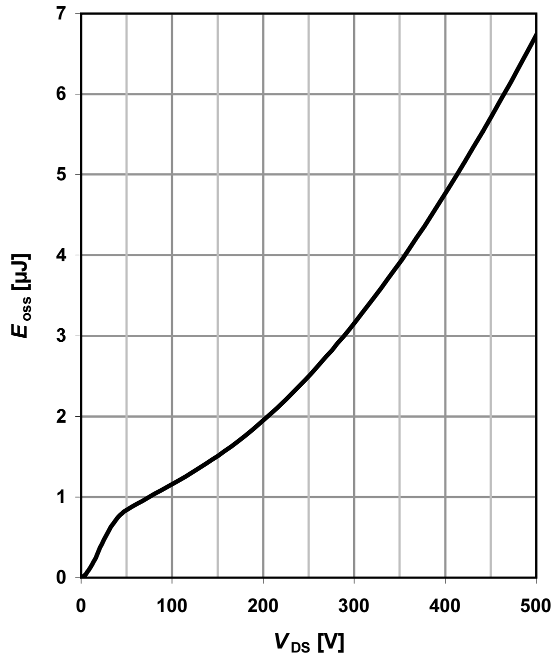
13 Typ. capacitances

C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

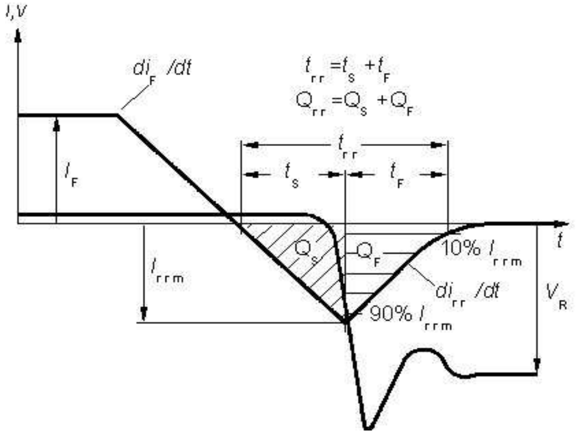


14 Typ. Coss stored energy

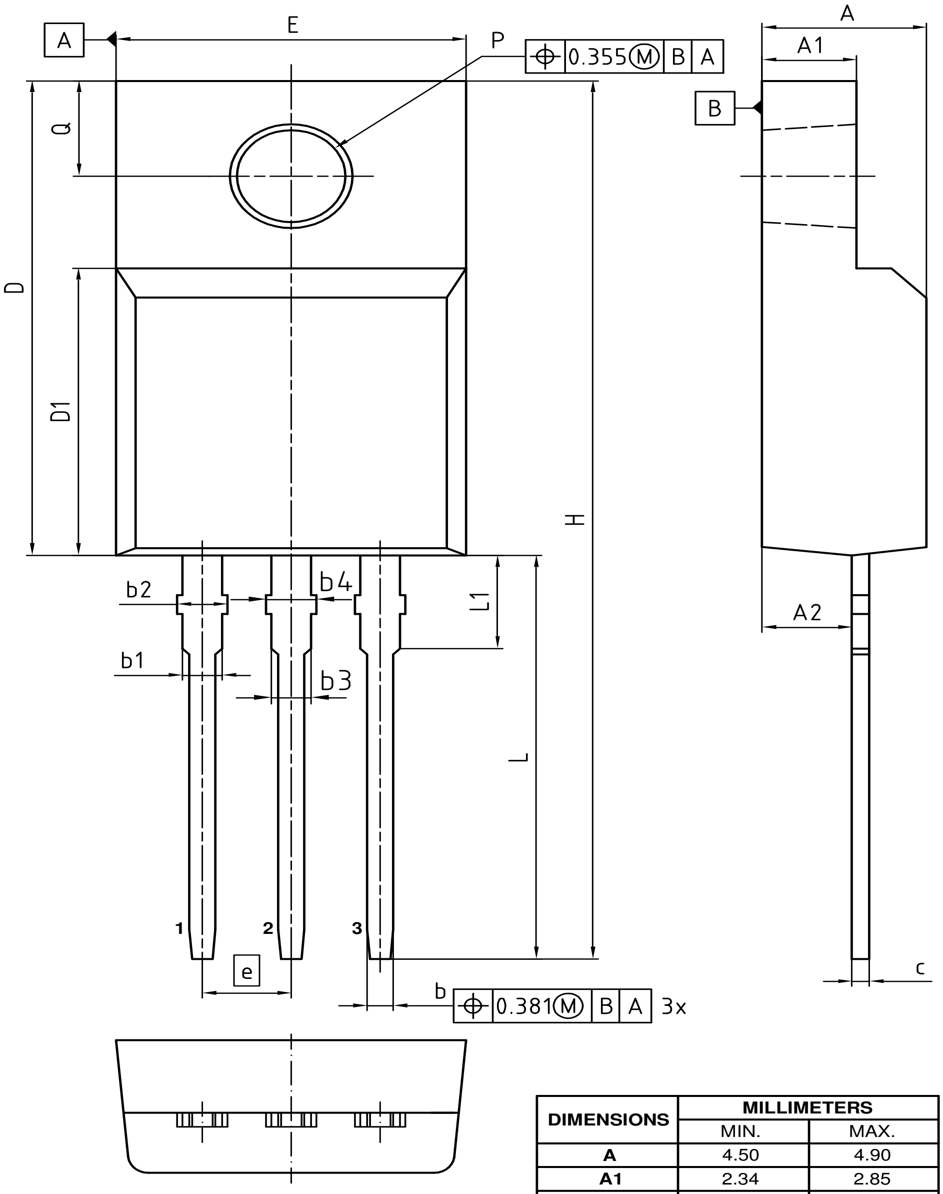
E_{oss}=f(V_{DS})



Definition of diode switching characteristics



Outline PG-TO220 FullPAK



DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.50	4.90
A1	2.34	2.85
A2	2.42	2.86
b	0.65	0.90
b1	0.95	1.38
b2	0.95	1.51
b3	0.65	1.38
b4	0.65	1.51
c	0.40	0.63
D	15.67	16.15
D1	8.97	9.83
E	10.00	10.65
e	2.54	
H	28.70	29.75
L	12.78	13.75
L1	2.83	3.45
øP	3.00	3.30
Q	3.15	3.50

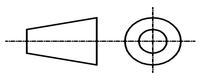
NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD TO-281
AND DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS
OR GATE BURRS
GATE BURRS ARE LESS THAN 0.5 mm

DOCUMENT NO.
Z8B00003319

REVISION
07

SCALE 5:1
0 1 2 3 4 5mm

EUROPEAN PROJECTION



ISSUE DATE
27.01.2017

Revision History

IPA50R250CP

Revision: 2018-02-26, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.1	2018-02-26	Outline PG-TO220 FullPAK update

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