

IRF7493PbF

HEXFET[®] Power MOSFET

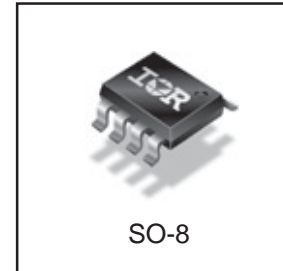
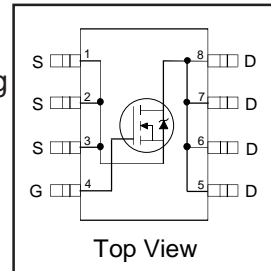
Applications

- High frequency DC-DC converters
- Lead-Free

V_{DSS}	R_{DS(on)} max	Qg (typ.)
80V	15mΩ@V_{GS}=10V	35nC

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
V _{DS}	Drain-to-Source Voltage	80	V
V _{GS}	Gate-to-Source Voltage	± 20	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	9.3	A
I _D @ T _C = 70°C	Continuous Drain Current, V _{GS} @ 10V	7.4	
I _{DM}	Pulsed Drain Current ①	74	
P _D @ T _C = 25°C	Maximum Power Dissipation ④	2.5	W
P _D @ T _C = 70°C	Maximum Power Dissipation ④	1.6	
	Linear Derating Factor	0.02	W/°C
T _J	Operating Junction and	-55 to + 150	°C
T _{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Lead	—	20	
R _{θJA}	Junction-to-Ambient ④	—	50	

Notes ① through ⑤ are on page 9

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International
IR Rectifier

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	80	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.074	—	mV/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	11.5	15	m Ω	$V_{GS} = 10V, I_D = 5.6A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 80V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 64V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

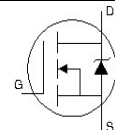
gfs	Forward Transconductance	13	—	—	S	$V_{DS} = 15V, I_D = 5.6A$
Q_g	Total Gate Charge	—	35	53	ns	$I_D = 5.6A$ $V_{DS} = 40V$ $V_{GS} = 10V$
Q_{gs}	Gate-to-Source Charge	—	5.7	—		
Q_{gd}	Gate-to-Drain Charge	—	12	—		
$t_{d(on)}$	Turn-On Delay Time	—	8.3	—		
t_r	Rise Time	—	7.5	—	ns	$V_{DD} = 40V, \text{ ③}$ $I_D = 5.6A$ $R_G = 6.2\Omega$ $V_{GS} = 10V$
$t_{d(off)}$	Turn-Off Delay Time	—	30	—		
t_f	Fall Time	—	12	—		
C_{iss}	Input Capacitance	—	1510	—		
C_{oss}	Output Capacitance	—	320	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$
C_{riss}	Reverse Transfer Capacitance	—	130	—		
C_{oss}	Output Capacitance	—	1130	—		
C_{oss}	Output Capacitance	—	210	—		
$C_{riss\text{ eff.}}$	Effective Output Capacitance	—	320	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	180	mJ
I_{AR}	Avalanche Current ①	—	5.6	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	9.3	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	74		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 5.6A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	37	56	ns	$T_J = 25^\circ\text{C}, I_F = 5.6A, V_{DD} = 15V$
Q_{rr}	Reverse Recovery Charge	—	52	78	nC	$di/dt = 100A/\mu s$ ③



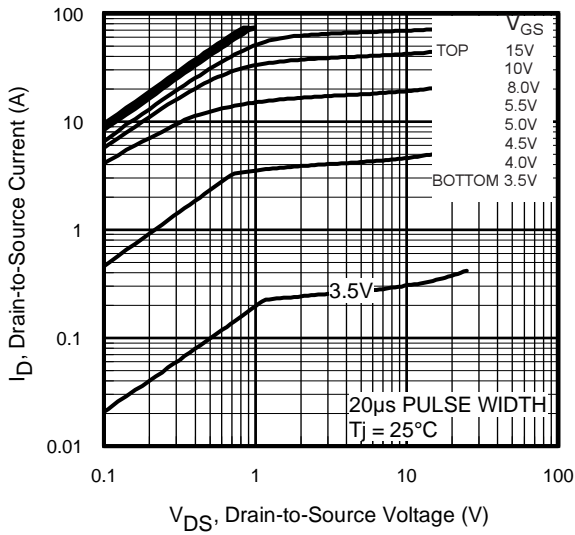


Fig 1. Typical Output Characteristics

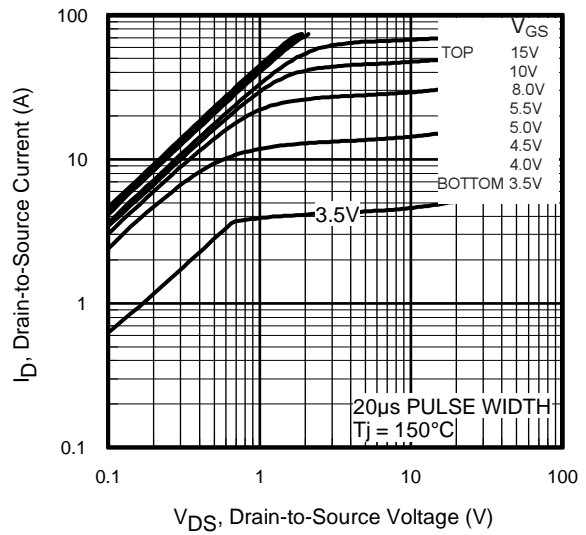


Fig 2. Typical Output Characteristics

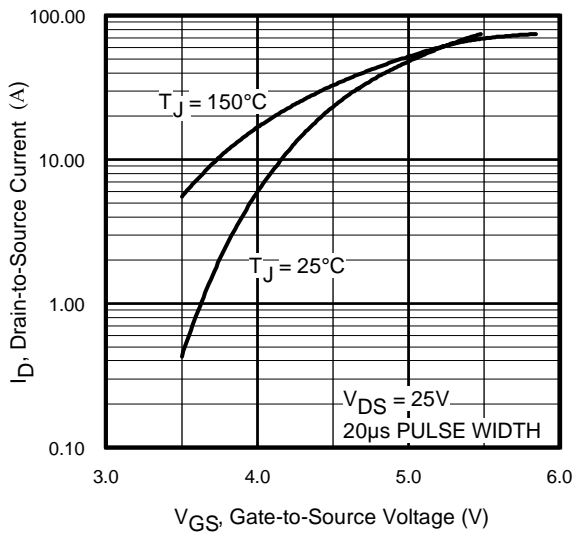


Fig 3. Typical Transfer Characteristics

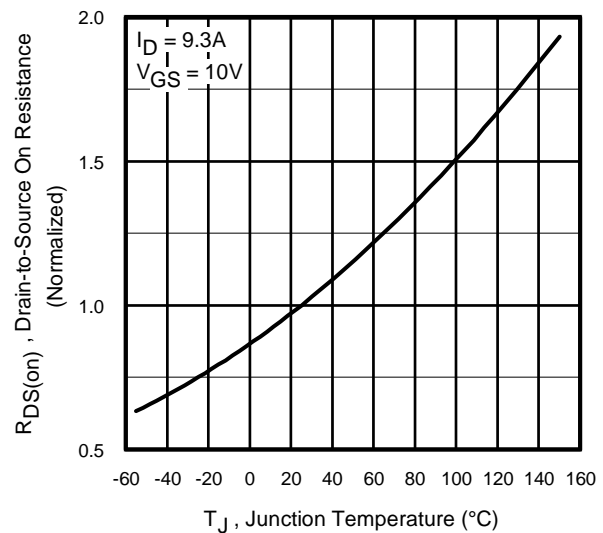


Fig 4. Normalized On-Resistance Vs. Temperature

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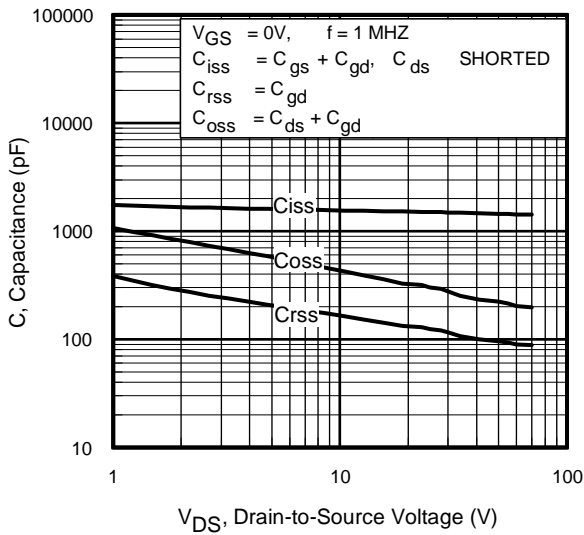


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

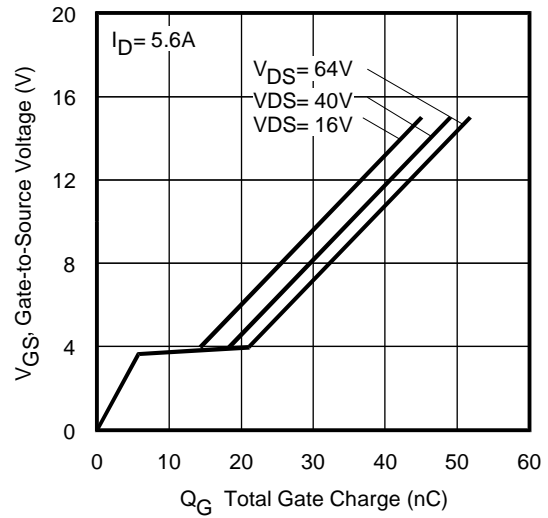


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

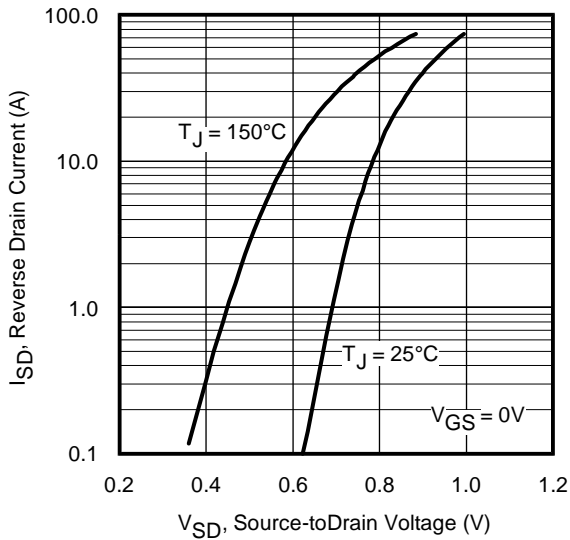


Fig 7. Typical Source-Drain Diode Forward Voltage

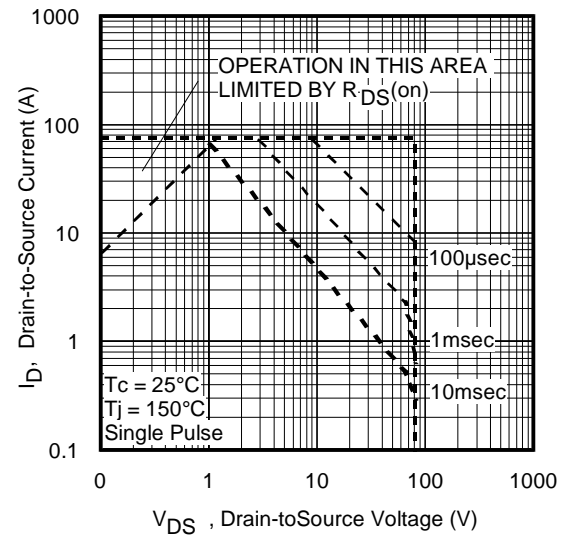


Fig 8. Maximum Safe Operating Area

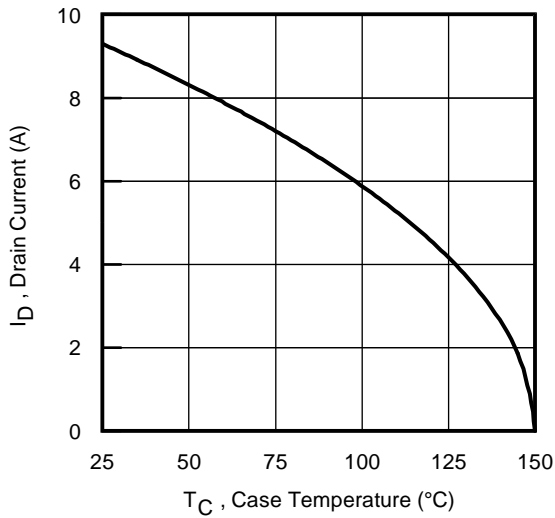


Fig 9. Maximum Drain Current Vs. Ambient Temperature



Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

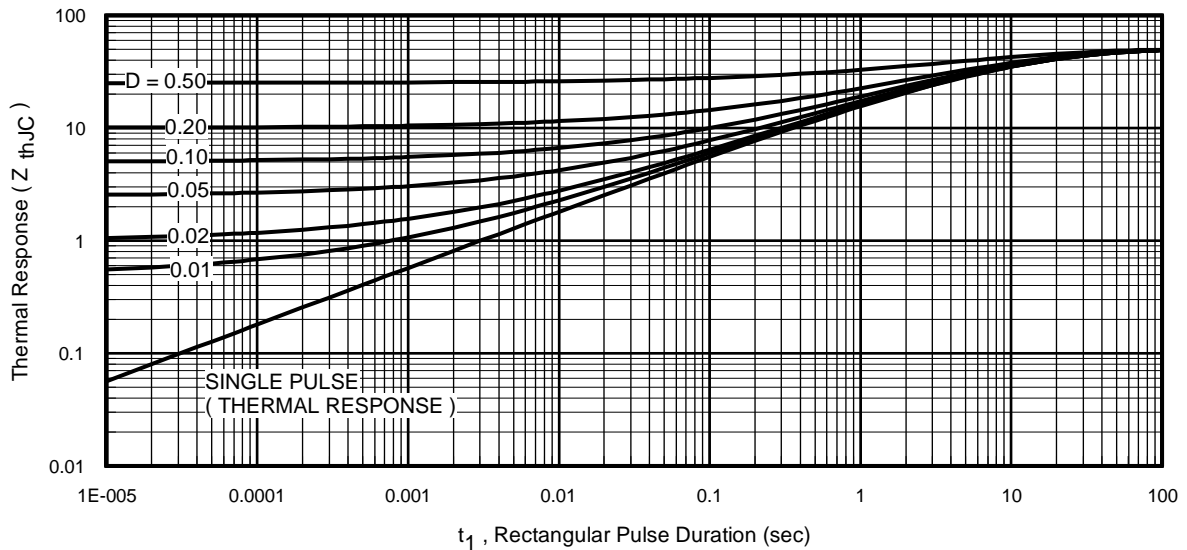


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

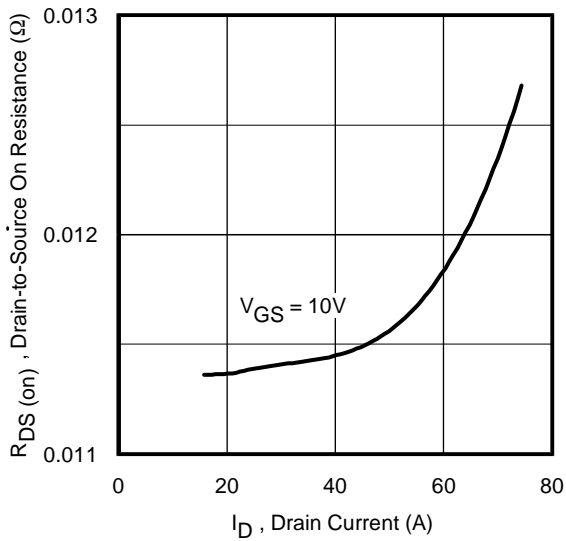


Fig 12. On-Resistance Vs. Drain Current

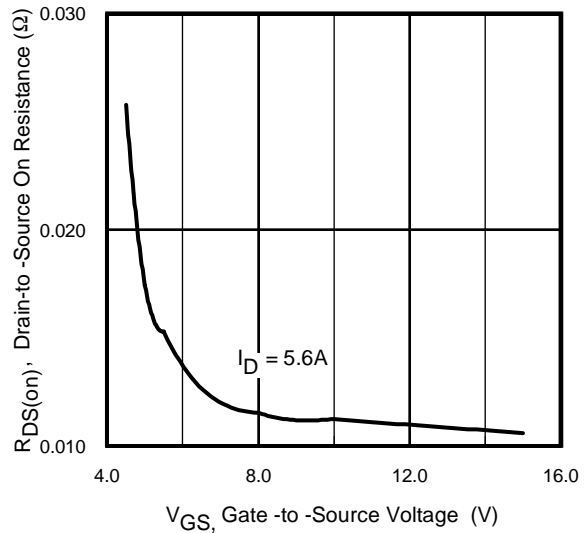


Fig 13. On-Resistance Vs. Gate Voltage



Fig 14a&b. Basic Gate Charge Test Circuit and Waveform



Fig 15a&b. Unclamped Inductive Test circuit and Waveforms

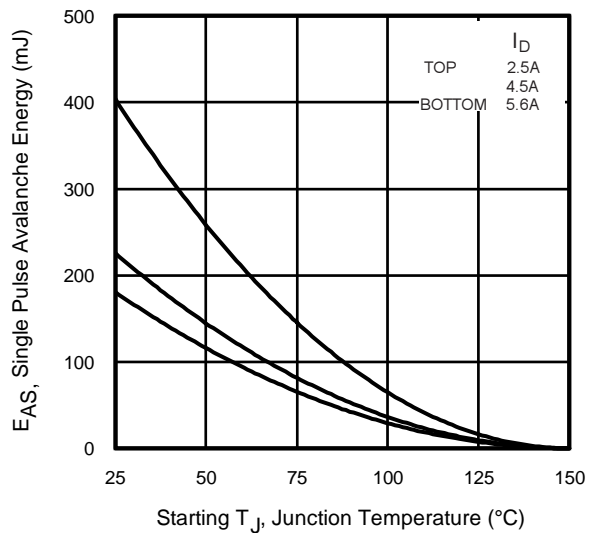


Fig 15c. Maximum Avalanche Energy Vs. Drain Current

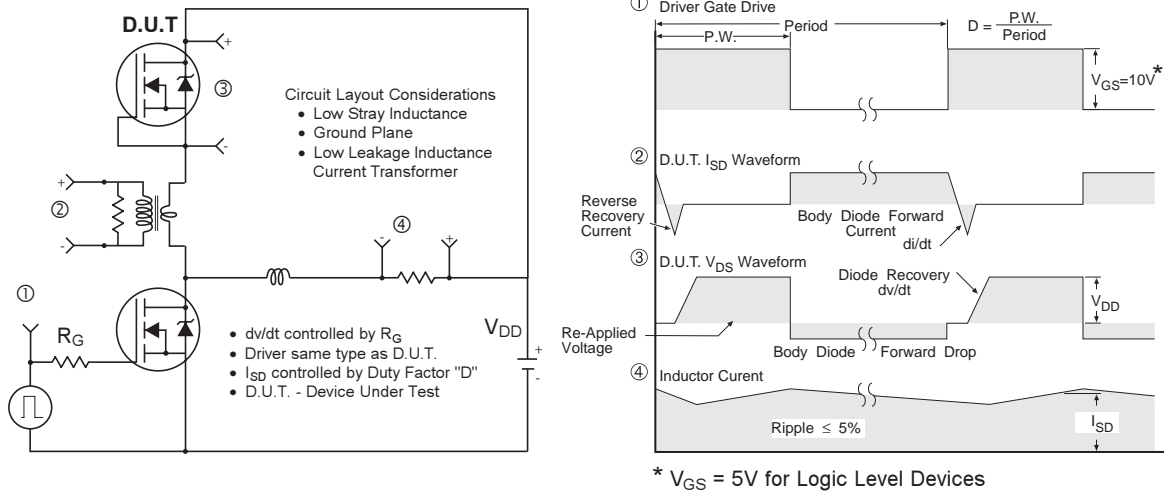


Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

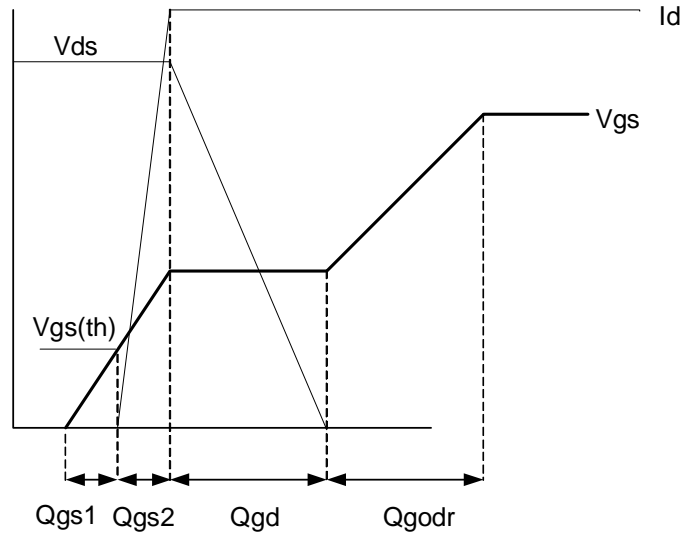
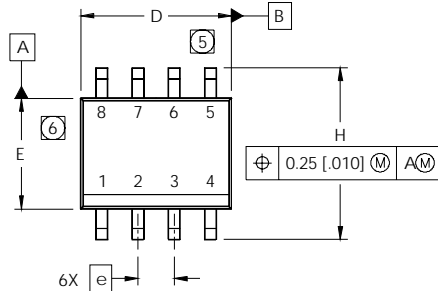


Fig 17. Gate Charge Waveform

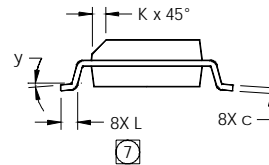
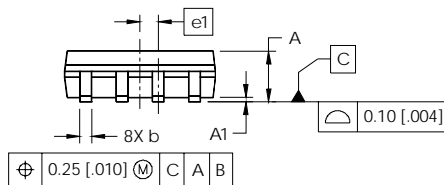
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SO-8 Package Outline

Dimensions are shown in millimeters (inches)



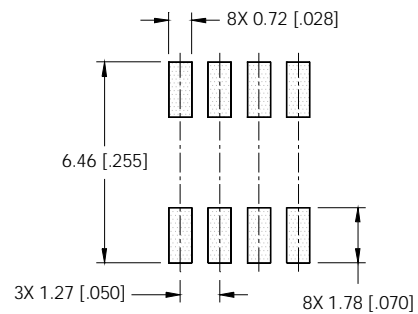
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



NOTES:

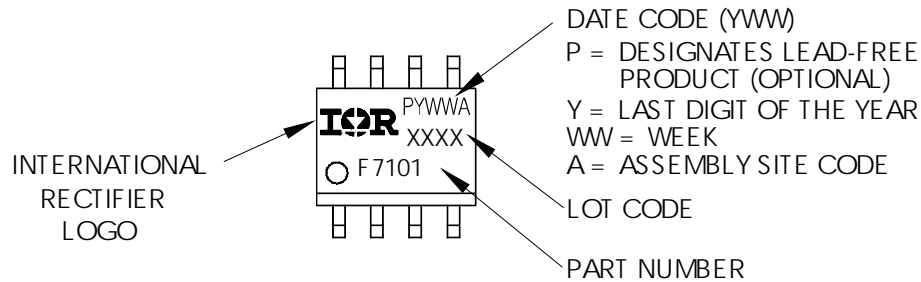
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
- 5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [0.006].
- 6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [0.010].
- 7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT



SO-8 Part Marking

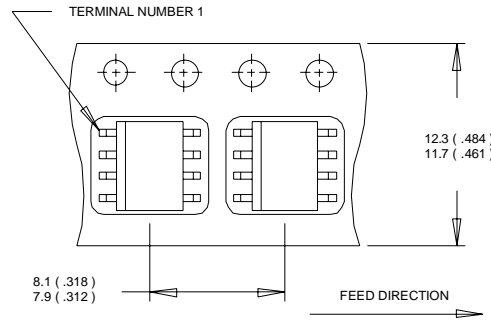
EXAMPLE: THIS IS AN IRF7101 (MOSFET)



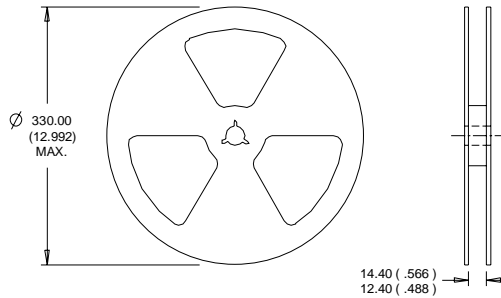
SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)

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- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 12\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 5.6\text{A}$.
- ③ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ When mounted on 1 inch square copper board
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Consumer market.
 Qualifications Standards can be found on IR's Web site.