HIGH PERFORMANCE BYTE ORGANIZED ROMS

Features

- Eight JEDEC Standard Versions:

IMP23064	28 Pin	64K	(8,192 word × 8 Bit)
IMP23128	28 Pin	128K	(16,384 word × 8 Bit)
IMP23256	28 Pin	256K	(32,768 word × 8 Bit)
IMP23512	28 Pin	512K	(65,536 word × 8 Bit)
IMP23100	28 Pin	1Meg	(131,072 word × 8 Bit)
IMP23101	32 Pin	1Meg	(131,072 word × 8 Bit)
IMP23201	32 Pin	2Meg	(262,144 word × 8 Bit)
IMP23401	32 Pin	4Meg	(524,288 word × 8 Bit)

- Very Fast Access Times:

From Chip Enable	100 ns
From Any Address	90 ns
From Output Enable	50 ns

- Single +5 Volt Power Supply
- Low Power Supply Current (worst case):

	t_{AA} < 190ns	t_{AA} = 190ns
Operating Current	50 mA	45 mA
Standby Current	7 mA	5 mA

- Class 2 (2,000 volt) ESD Protection
- Programmable Active Level on Select Output Enable Pins for Maximum System Flexibility. See Figure 1.
- Available in both Standard Dual In-Line and Surface Mount Packages
- Automatic Low-Power Standby Mode initiated by Chip Enable going to Non-select Mode
- Complete Latch-up Immunity on all Pins
- DC Noise Immunity:

Guaranteed	400 mV
Typical	> 1 Volt

- Expandable Design Hierarchy and Common Process provide Simplified IMP23000 Series Family Qualification

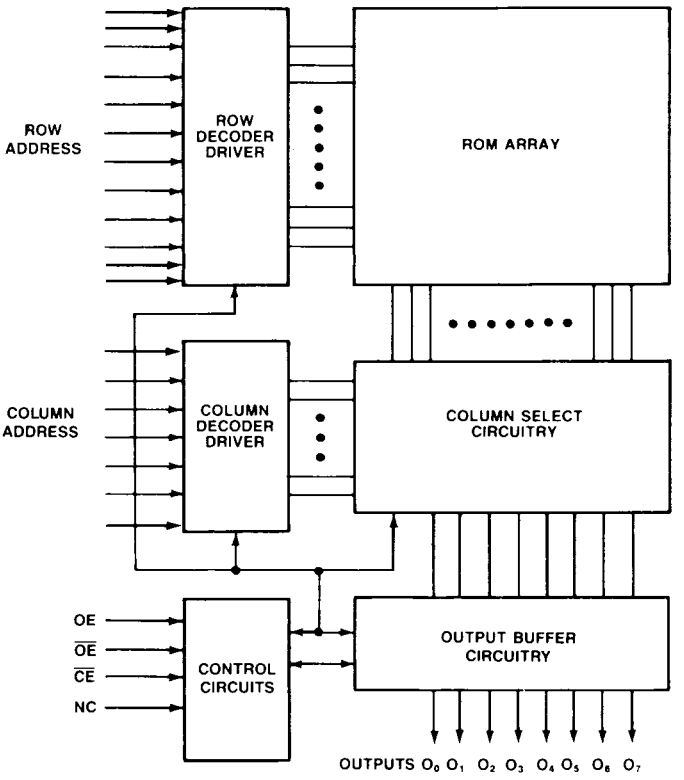

Fig. 1 Block Diagram

Note: Select control circuit pins input pins are not programmable on some devices.

Packaging Options

IMP P/N	28 PDIP	32 PDIP	32 PLCC
IMP23064	•		•
IMP23128	•		•
IMP23256	•		•
IMP23512	•		•
IMP23100	•		
IMP23101		•	•
IMP23201		•	•
IMP23401		•	•

Alternate Packages Available

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HIGH PERFORMANCE BYTE ORGANIZED ROMS

Absolute Maximum Ratings

Ambient Operating Temperature ..... -10 to +80°C
Storage Temperature ..... -65 to +150°C
Supply Voltage to Ground Potential ..... -0.5 to +7.0 V
Applied Output Voltage ..... -0.5 to +7.0 V
Applied Input Voltage ..... -0.5 to +7.0 V
Power Dissipation ..... 1.0 W

Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliablity.

Capacitance: T_A = 25°C, f = 1.0 MHz, Note 5

Symbol	Parameter	Min	Max	Unit	Conditions
C_I	Input Capacitance	—	5	pF	V_{IN} = 0 V
C_O	Output Capacitance	—	5	pF	V_{OUT} = 0 V

DC Characteristics: T_A = 0 to +70°C, V_{CC} = +5 V ± 10%

Symbol	Parameter		Min	Max	Unit	Conditions
V_{OH}	Output HIGH Voltage		2.4	V_{CC}	V	I_{OH} = -1.0 mA
V_{OL}	Output LOW Voltage		—	0.4	V	I_{OL} = 3.2 mA
V_{IH}	Input HIGH Voltage		2.0	V_{CC}	V	
V_{IL}	Input LOW Voltage		-0.5	0.8	V	
I_{LI}	Input Leakage Current		—	1	μA	V_{IN} = 0 V to V_{CC}
I_{LO}	Output Leakage Current		—	1	μA	V_{OUT} = 0 V to V_{CC}
I_{CC}	Operating Supply Current	-19 only	—	45	mA	Note 1
I_{CC}	Operating Supply Current	-14, -11, -9	—	50	mA	Note 1
I_{SB}	Standby Supply Current	-19 only	—	5	mA	$\overline{CE}$ = V_{IH}
I_{SB}	Standby Supply Current	-14, -11, -9	—	7	mA	$\overline{CE}$ = V_{IH}
I_{OS}	Output Short Circuit Current		—	70	mA	Note 2

AC Characteristics: T_A = 0 to +70°C, V_{CC} = +5 V ± 10%

		-9		-11		-14		-19			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Units	Conditions
t_{AA}	Address Access Time	—	90	—	110	—	140	—	190	ns	
t_{OH}	Output Hold After Address Change	10	—	10	—	10	—	10	—	ns	
t_{ACE}	Chip Enable Access Time	—	100	—	120	—	150	—	200	ns	
t_{AOE}	Output Enable Access Time	—	45	—	50	—	60	—	75	ns	
t_{LZ}	Output LOW Z Delay	10	—	10	—	10	—	10	—	ns	Note 3
t_{HZ}	Output HIGH Z Delay	—	40	—	40	—	50	—	65	ns	Note 4
t_{PU}	Power-Up Time	0	—	0	—	0	—	0	—	ns	
t_{PD}	Power-Down Time	—	40	—	40	—	50	—	65	ns	

Notes

1. Measured with device selected and outputs unloaded.
2. For a duration not to exceed 30 seconds.
3. Output LOW impedance delay (TLZ) is measured from $\overline{CE}$ or $\overline{OE}$ going active.
4. Output HIGH impedance delay (THZ) is measured from $\overline{CE}$ or $\overline{OE}$ going inactive.
5. This parameter is periodically sampled and is not 100% tested.

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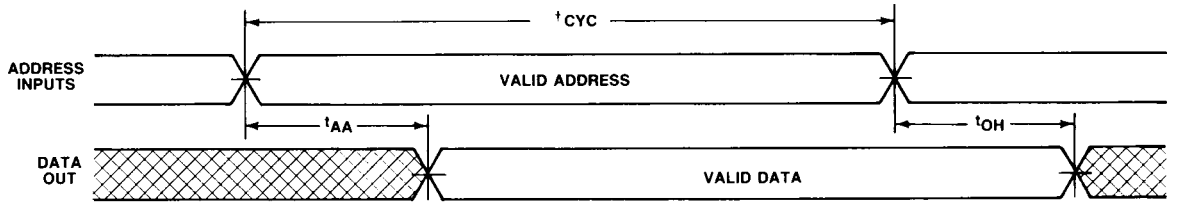
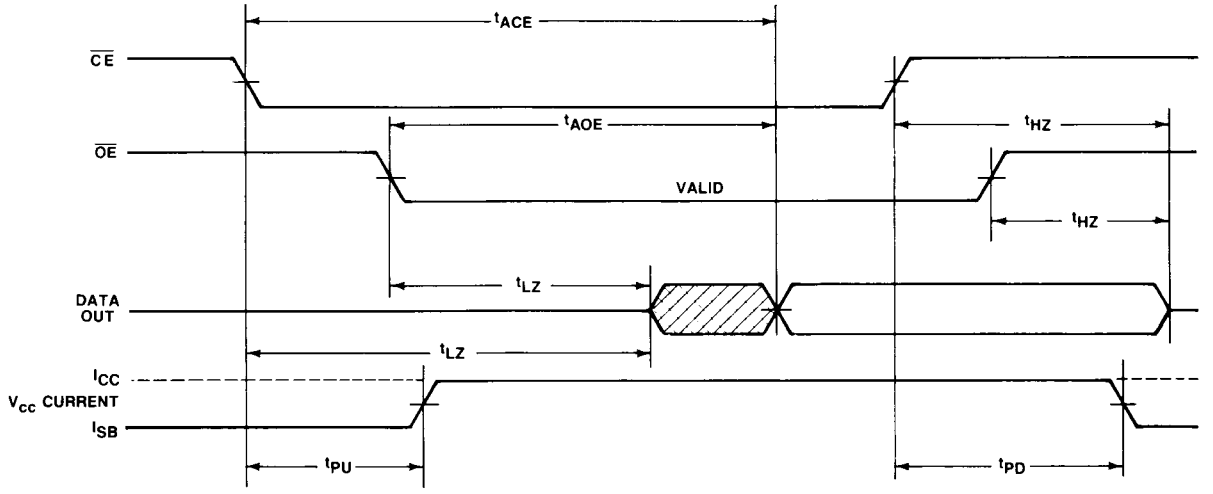
HIGH PERFORMANCE BYTE ORGANIZED ROMS

Timing Diagrams

Propagation Delay From Address ($\overline{CE}$/$\overline{OE}$ = Active)



Propagation Delay From Chip Enable or Output Enable (Address Valid)



AC Test Conditions

Input Pulse Levels	0.4 to 2.4 V
Input Rise and Fall Times	10 ns
Input Timing Level	1.5 V
Output Timing Level	1.5 V
Output Load	See Figure 2

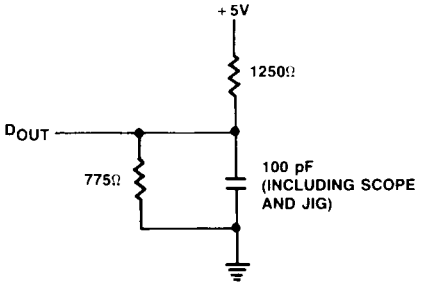


Fig. 2 AC Test Output Load Condition

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IMP23064 (64K) BYTE ORGANIZED HIGH PERFORMANCE ROMS

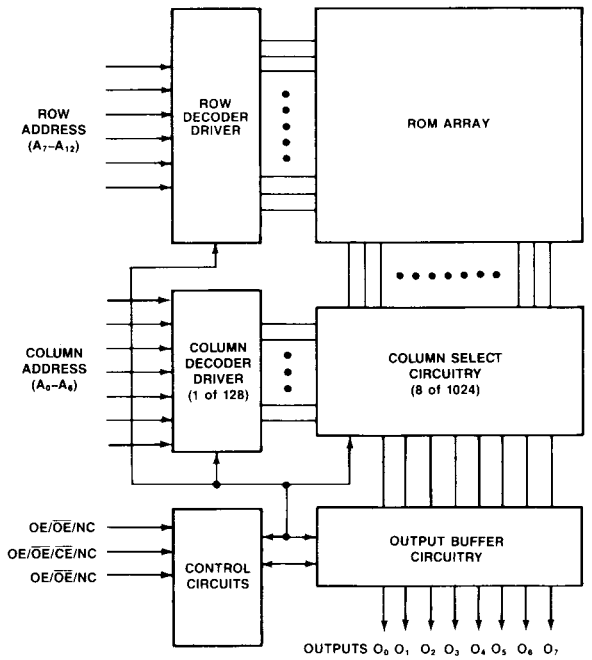
Features

- JEDEC Standard Version
- Very High Speed Access Times:
  - From Chip Enable 100 ns
  - From Any Address 90 ns
  - From Output Enable 50 ns
- Low Power Supply Current (worst case):

	t_{AA} < 190ns	t_{AA} = 190ns
Operating Current	50 mA	45 mA
Standby Current	7 mA	5 mA

- Single +5 Volt Power Supply
- Class 2 (2,000 volt) ESD Protection
- Programmable Chip and Output Enable Pins for Maximum System Flexibility
- Available in Both Standard Dual In-Line and Surface Mount Packages
- Complete Latch-Up Immunity On All Pins
- DC Noise Immunity:
  - Guaranteed 400 mV
  - Typical > 1 Volt
- Expandable Design Hierarchy and Common Process Provides Simplified IMP23000 Family Qualification

Block Diagram



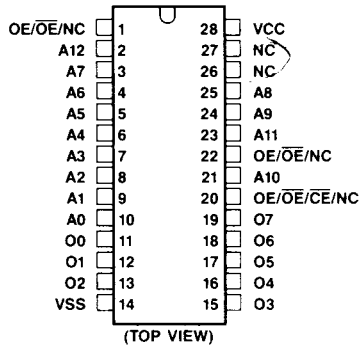
Description

The IMP23064 is an 8192 word × 8 bits mask programmable read only memory device. The IMP23064 is a byte-wide compatible JEDEC standard pin configuration encapsulated in a plastic 28 pin dual-in-line or 32 pin leaded chip carrier (PLCC) package. IMP23064 devices offer selectable address access times including 190, 140, 110, and 90 ns while realizing low power consumption.

The IMP23064 is fabricated utilizing IMP's advanced RMOS™ design and process methodology to achieve superior speed and power performance. IMP's high performance memories are compatible with battery and non-battery operated systems. The IMP23064 memory capacity is ideally suited for storing printer control programs, personal and micro computer bias programs, and video game software.

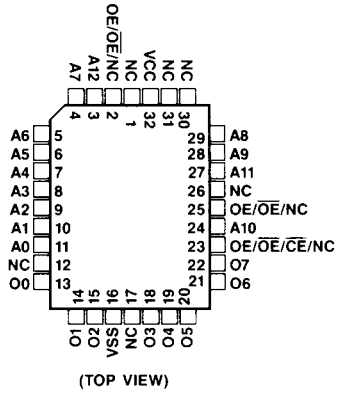
Package Configurations:

Plastic 28 PDIP



(TOP VIEW)

Plastic 32 PLCC



(TOP VIEW)

Pin Nomenclature

A_0–A_6	Column Address Inputs	$\overline{OE}$	Output Enable Input (Low)
A_7–A_{12}	Row Address Inputs	$\overline{CE}$	Chip Enable Input (Low)
OE	Output Enable Input (High)	NC	No Connect

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IMP23128 (128K) BYTE ORGANIZED HIGH PERFORMANCE ROMS

Features

- JEDEC Standard Version
- Very High Speed Access Times:

From Chip Enable	100 ns
From Any Address	90 ns
From Output Enable	50 ns

- Low Power Supply Current (worst case):

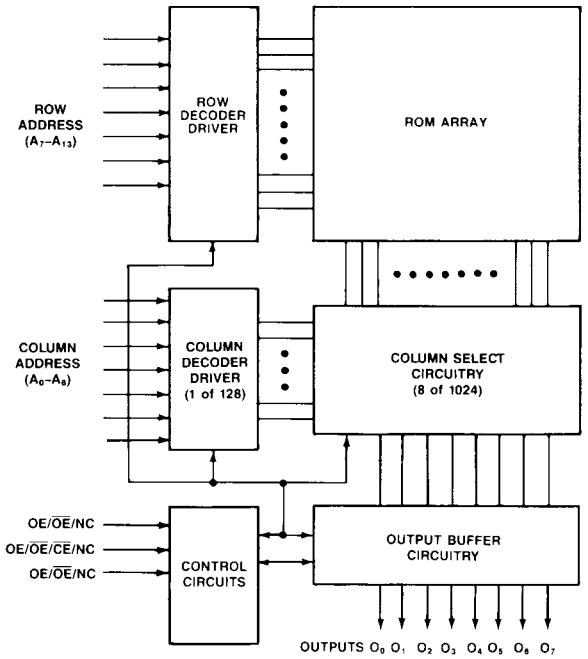
	t_{AA} < 190ns	t_{AA} = 190ns
Operating Current	50 mA	45 mA
Standby Current	7 mA	5 mA

- Single +5 Volt Power Supply
- Class 2 (2,000 volt) ESD Protection
- Programmable Chip and Output Enable Pins for Maximum System Flexibility
- Available in Both Standard Dual In-Line and Surface Mount Packages
- Complete Latch-Up Immunity On All Pins
- DC Noise Immunity:

Guaranteed	400 mV
Typical	> 1 Volt

- Expandable Design Hierarchy and Common Process Provides Simplified IMP23000 Family Qualification

Block Diagram



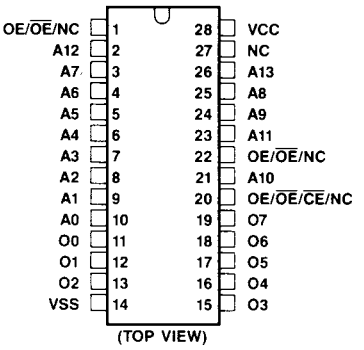
Description

The IMP23128 is a 16,384 word × 8 bits mask programmable read only memory device. The IMP23128 is a byte-wide compatible JEDEC standard pin configuration encapsulated in a plastic 28 pin dual-in-line or 32 pin leaded chip carrier (PLCC) package. IMP23128 devices offer selectable address access times including 190, 140, 110, and 90 ns while realizing low power consumption.

The IMP23128 is fabricated utilizing IMP's advanced RMOS™ design and process methodology to achieve superior speed and power performance. IMP's high performance memories are compatible with battery and non-battery operated systems. The IMP23128 memory capacity is ideally suited for storing printer control programs, personal and micro computer bias programs, disk drive control data, and video game software.

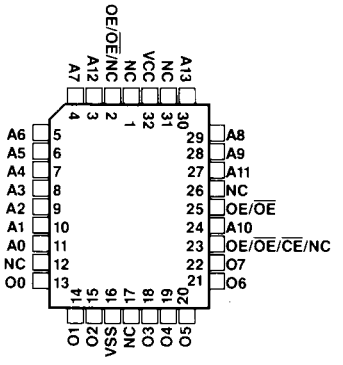
Package Configurations:

Plastic 28 PDIP



(TOP VIEW)

Plastic 32 PLCC



(TOP VIEW)

Pin Nomenclature

A_0–A_6	Column Address Inputs	$\overline{OE}$	Output Enable Input (Low)
A_7–A_{13}	Row Address Inputs	$\overline{CE}$	Chip Enable Input (Low)
OE	Output Enable Input (High)	NC	No Connect

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IMP23256 (256K) BYTE ORGANIZED HIGH PERFORMANCE ROMS

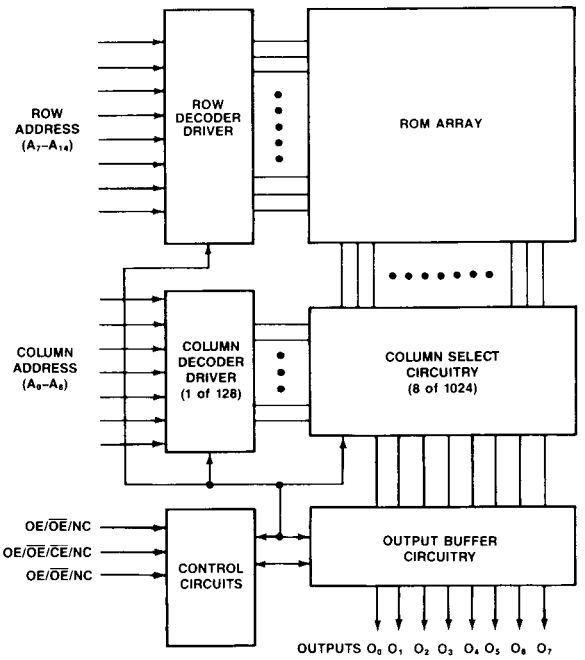
Features

- JEDEC Standard Version
- Very High Speed Access Times:
  - From Chip Enable 100 ns
  - From Any Address 90 ns
  - From Output Enable 50 ns
- Low Power Supply Current (worst case):

	t_{AA} < 190ns	t_{AA} = 190ns
Operating Current	50 mA	45 mA
Standby Current	7 mA	5 mA

- Single +5 Volt Power Supply
- Class 2 (2,000 volt) ESD Protection
- Programmable Chip and Output Enable Pins for Maximum System Flexibility
- Available in Both Standard Dual In-Line and Surface Mount Packages
- Complete Latch-Up Immunity On All Pins
- DC Noise Immunity:
  - Guaranteed 400 mV
  - Typical > 1 Volt
- Expandable Design Hierarchy and Common Process Provides Simplified IMP23000 Family Qualification

Block Diagram



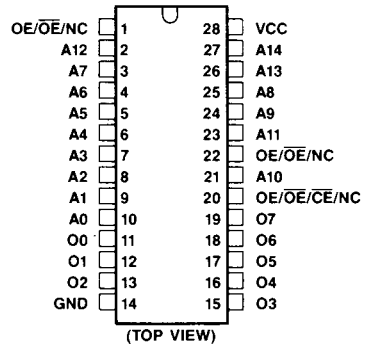
Description

The IMP23256 is a 32,768 word × 8 bits mask programmable read only memory device. The IMP23256 is a byte-wide compatible JEDEC standard pin configuration encapsulated in a plastic 28 pin dual-in-line or 32 pin leaded chip carrier (PLCC) package. IMP23256 devices offer selectable address access times including 190, 140, 110, and 90 ns while realizing low power consumption.

The IMP23256 is fabricated utilizing IMP's advanced RMOS™ design and process methodology to achieve superior speed and power performance. IMP's high performance memories are compatible with battery and non-battery operated systems. The IMP23256 memory capacity is ideally suited for storing printer control programs, personal and micro computer bias programs, disk drive control data, and video game software.

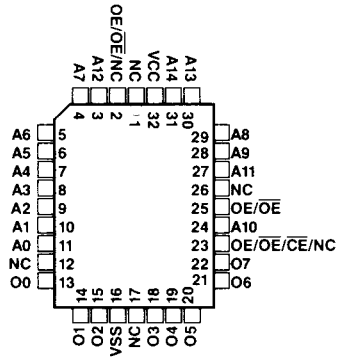
Package Configurations:

Plastic 28 PDIP



(TOP VIEW)

Plastic 32 PLCC



(TOP VIEW)

Pin Nomenclature

A_0–A_6	Column Address Inputs	$\overline{OE}$	Output Enable Input (Low)
A_7–A_{14}	Row Address Inputs	$\overline{CE}$	Chip Enable Input (Low)
OE	Output Enable Input (High)	NC	No Connect

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IMP23512 (512K) BYTE ORGANIZED HIGH PERFORMANCE ROMS

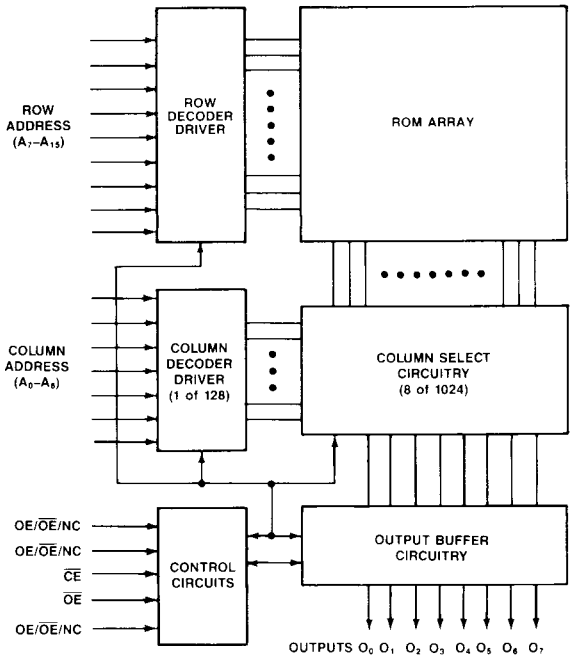
Features

- JEDEC Standard Version
- Very High Speed Access Times:
  - From Chip Enable 100 ns
  - From Any Address 90 ns
  - From Output Enable 50 ns
- Low Power Supply Current (worst case):

	t_{AA} < 190ns	t_{AA} = 190ns
Operating Current	50 mA	45 mA
Standby Current	7 mA	5 mA

- Single +5 Volt Power Supply
- Class 2 (2,000 volt) ESD Protection
- Programmable Chip and Output Enable Pins for Maximum System Flexibility
- Available in Both Standard Dual In-Line and Surface Mount Packages
- Complete Latch-Up Immunity On All Pins
- DC Noise Immunity:
  - Guaranteed 400 mV
  - Typical > 1 Volt
- Expandable Design Hierarchy and Common Process Provides Simplified IMP23000 Family Qualification

Block Diagram



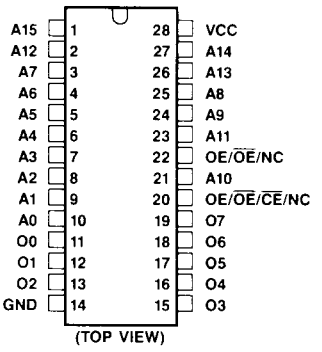
Description

The IMP23512 is a 65,536 word × 8 bits mask programmable read only memory device. The IMP23512 is a byte-wide compatible JEDEC standard pin configuration encapsulated in a plastic 28 pin dual-in-line or 32 pin leaded chip carrier (PLCC) package. IMP23512 devices offer selectable address access times including 190, 140, 110, and 90 ns while realizing low power consumption.

The IMP23512 is fabricated utilizing IMP's advanced RMOS™ design and process methodology to achieve superior speed and power performance. IMP's high performance memories are compatible with battery and non-battery operated systems. The IMP23512 memory capacity is ideally suited for storing printer control programs, personal and micro computer bias programs, disk drive control data, and video game software.

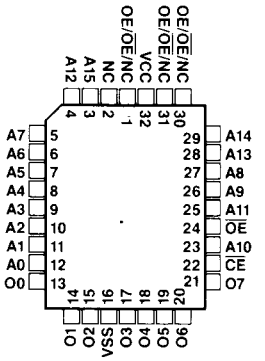
Package Configurations:

Plastic 28 PDIP



(TOP VIEW)

Plastic 32 PLCC



(TOP VIEW)

Pin Nomenclature

A_0–A_6	Column Address Inputs	$\overline{OE}$	Output Enable Input (Low)
A_7–A_{15}	Row Address Inputs	$\overline{CE}$	Chip Enable Input (Low)
OE	Output Enable Input (High)	NC	No Connect

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IMP23100 (1024K) BYTE ORGANIZED HIGH PERFORMANCE ROMS

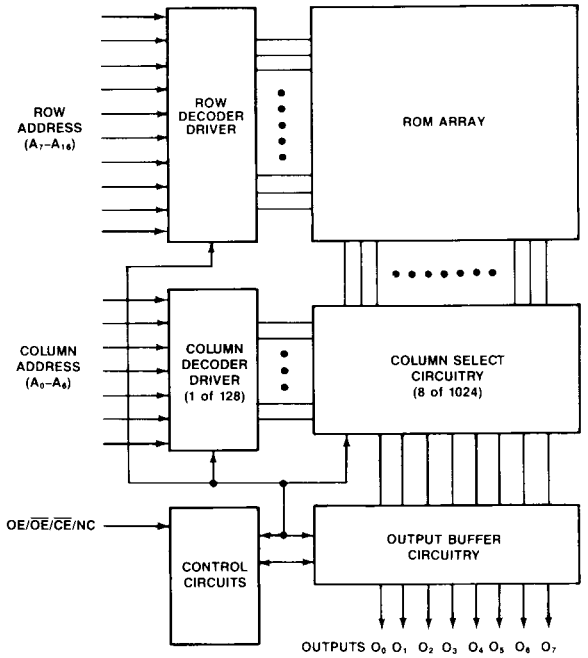
Features

- JEDEC Standard Version
- Very High Speed Access Times:
  - From Chip Enable 100 ns
  - From Any Address 90 ns
  - From Output Enable 50 ns
- Low Power Supply Current (worst case):

	t_{AA} < 190ns	t_{AA} = 190ns
Operating Current	50 mA	45 mA
Standby Current	7 mA	5 mA

- Single +5 Volt Power Supply
- Class 2 (2,000 volt) ESD Protection
- Programmable Chip and Output Enable Pins for Maximum System Flexibility
- Available in Both Standard Dual In-Line and Surface Mount Packages
- Complete Latch-Up Immunity On All Pins
- DC Noise Immunity:
  - Guaranteed 400 mV
  - Typical > 1 Volt
- Expandable Design Hierarchy and Common Process Provides Simplified IMP23000 Family Qualification

Block Diagram



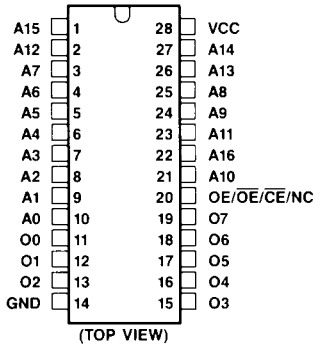
Description

The IMP23100 is a 131,072 word × 8 bits mask programmable read only memory device. The IMP23100 is a byte-wide compatible JEDEC standard pin configuration encapsulated in a plastic 28 pin dual-in-line package. IMP23100 devices offer selectable address access times including 190, 140, 100, and 90 ns while realizing low power consumption.

The IMP23100 is fabricated utilizing IMP's advanced RMOS™ design and process methodology to achieve superior speed and power performance. IMP's high performance memories are compatible with battery and non-battery operated systems. The IMP23100 memory capacity is ideally suited for storing application program software, printer control and font programs, graphic look-up tables and video game software.

Package Configurations:

Plastic 28 PDIP



(TOP VIEW)

Pin Nomenclature

A_0–A_6	Column Address Inputs	$\overline{OE}$	Output Enable Input (Low)
A_7–A_{16}	Row Address Inputs	$\overline{CE}$	Chip Enable Input (Low)
OE	Output Enable Input (High)	NC	No Connect

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IMP23101 (1024K) BYTE ORGANIZED HIGH PERFORMANCE ROMS

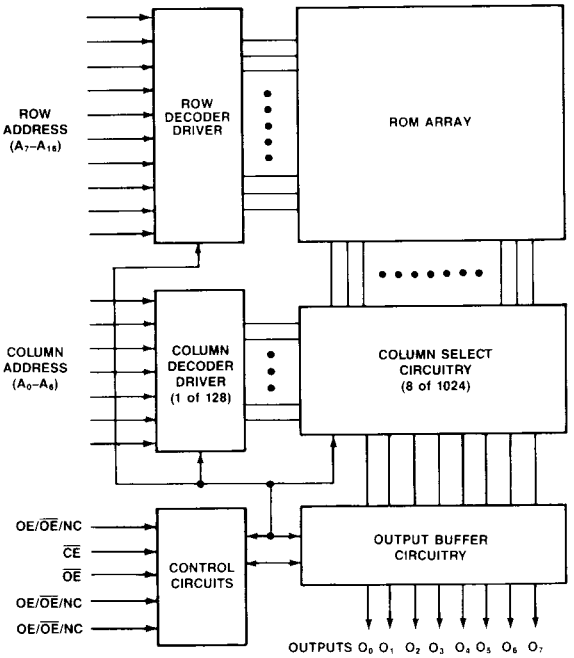
Features

- JEDEC Standard Version
- Very High Speed Access Times:
  - From Chip Enable 100 ns
  - From Any Address 90 ns
  - From Output Enable 50 ns
- Low Power Supply Current (worst case):

	t_{AA} < 190ns	t_{AA} = 190ns
Operating Current	50 mA	45 mA
Standby Current	7 mA	5 mA

- Single +5 Volt Power Supply
- Class 2 (2,000 volt) ESD Protection
- Programmable Chip and Output Enable Pins for Maximum System Flexibility
- Available in Both Standard Dual In-Line and Surface Mount Packages
- Complete Latch-Up Immunity On All Pins
- DC Noise Immunity:
  - Guaranteed 400 mV
  - Typical > 1 Volt
- Expandable Design Hierarchy and Common Process Provides Simplified IMP23000 Family Qualification

Block Diagram



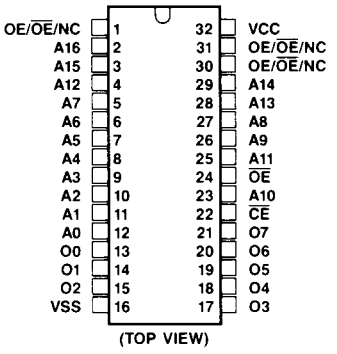
Description

The IMP23101 is a 131,072 word × 8 bits mask programmable read only memory device. The IMP23101 is a byte-wide compatible JEDEC standard pin configuration encapsulated in a plastic 32 pin dual-in-line or leaded chip carrier (PLCC) package. IMP23101 devices offer selectable access times including 190, 140, 110, and 90 ns while realizing low power consumption.

The IMP23101 is fabricated utilizing IMP's advanced RMOS™ design and process methodology to achieve superior speed and power performance. IMP's high performance memories are compatible with battery and non-battery operated systems. The IMP23101 memory capacity is ideally suited for storing application program software, printer control and font programs, graphic look-up tables and video game software.

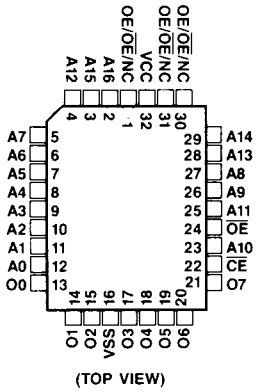
Package Configurations:

Plastic 32 PDIP



(TOP VIEW)

Plastic 32 PLCC



(TOP VIEW)

Pin Nomenclature

A_0–A_6	Column Address Inputs	$\overline{OE}$	Output Enable Input (Low)
A_7–A_{16}	Row Address Inputs	NC	No Connect
OE	Output Enable Input (High)		

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IMP23201 (2048K) BYTE ORGANIZED HIGH PERFORMANCE ROMS

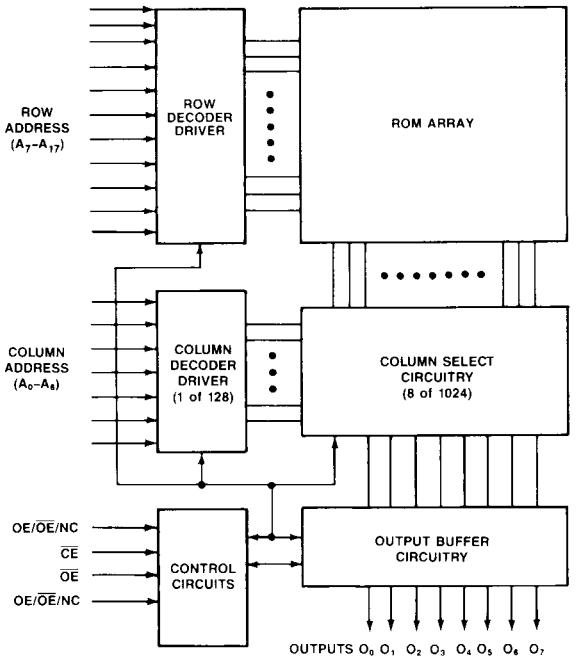
Features

- JEDEC Standard Version
- Very High Speed Access Times:
  - From Chip Enable 100 ns
  - From Any Address 90 ns
  - From Output Enable 50 ns
- Low Power Supply Current (worst case):

	t_{AA} < 190ns	t_{AA} = 190ns
Operating Current	50 mA	45 mA
Standby Current	7 mA	5 mA

- Single +5 Volt Power Supply
- Class 2 (2,000 volt) ESD Protection
- Programmable Chip and Output Enable Pins for Maximum System Flexibility
- Available in Both Standard Dual In-Line and Surface Mount Packages
- Complete Latch-Up Immunity On All Pins
- DC Noise Immunity:
  - Guaranteed 400 mV
  - Typical > 1 Volt
- Expandable Design Hierarchy and Common Process Provides Simplified IMP23000 Family Qualification

Block Diagram



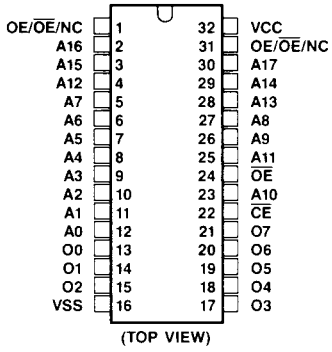
Description

The IMP23201 is a 262,144 word x 8 bits mask programmable read only memory device. The IMP23201 is a byte-wide compatible JEDEC standard pin configuration encapsulated in a plastic 32 pin dual-in-line or leaded chip carrier (PLCC) package. IMP23201 devices offer selectable access times including 190, 140, 110, and 90 ns while realizing low power consumption.

The IMP23201 is fabricated using IMP's advanced RMOS™ design and process methodology to achieve superior speed and power performance. IMP's high performance memories are compatible with battery and non-battery operated systems. The IMP23201 memory capacity is ideally suited for storing application program software, printer control and font programs, graphic look-up tables, dictionary/thesaurus software, digital music waveforms, and video game software.

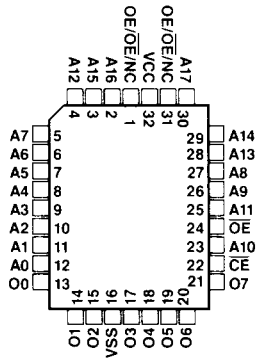
Package Configurations:

Plastic 32 PDIP



(TOP VIEW)

Plastic 32 PLCC



(TOP VIEW)

Pin Nomenclature

A_0-A_6	Column Address Inputs	OE	Output Enable Input (Low)
A_7-A_{17}	Row Address Inputs	NC	No Connect
OE	Output Enable Input (High)		

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IMP23401 (4096K) BYTE ORGANIZED HIGH PERFORMANCE ROMS

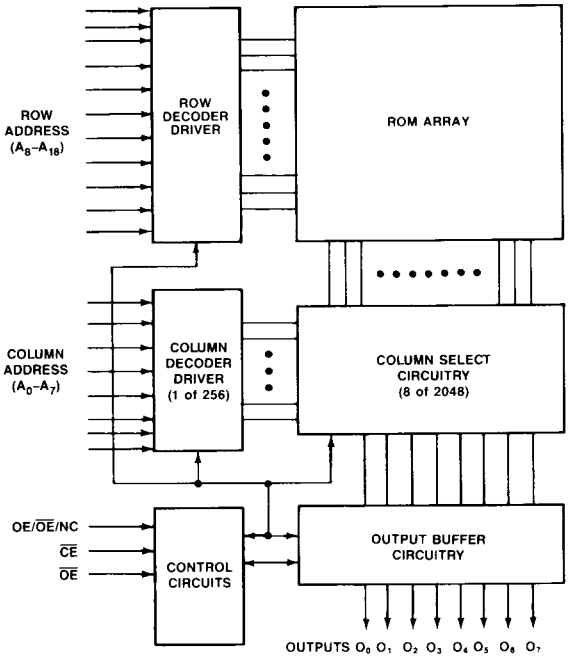
Features

- JEDEC Standard Version
- Very High Speed Access Times:
  - From Chip Enable 100 ns
  - From Any Address 90 ns
  - From Output Enable 50 ns
- Low Power Supply Current (worst case):

	t_{AA} < 190ns	t_{AA} = 190ns
Operating Current	50 mA	45 mA
Standby Current	7 mA	5 mA

- Single +5 Volt Power Supply
- Class 2 (2,000 volt) ESD Protection
- Programmable Chip and Output Enable Pins for Maximum System Flexibility
- Available in Both Standard Dual In-Line and Surface Mount Packages
- Complete Latch-Up Immunity On All Pins
- DC Noise Immunity:
  - Guaranteed 400 mV
  - Typical > 1 Volt
- Expandable Design Hierarchy and Common Process Provides Simplified IMP23000 Family Qualification

Block Diagram



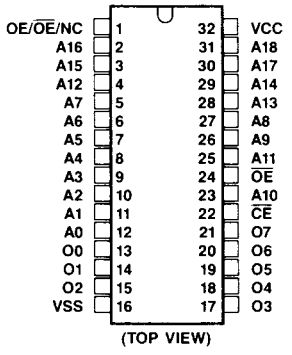
Description

The IMP23401 is a 524,288 word × 8 bits mask programmable read only memory device. The IMP23401 is a byte-wide compatible JEDEC standard pin configuration encapsulated in a plastic 32 pin dual-in-line or leaded chip carrier (PLCC) package. IMP23401 devices offer selectable access times including 190, 140, 110, and 90 ns while realizing low power consumption.

The IMP23401 is fabricated using IMP's advanced RMOS™ design and process methodology to achieve superior speed and power performance. IMP's high performance memories are compatible with battery and non-battery operated systems. The IMP23401 memory capacity is ideally suited for storing application program software, printer control and font programs, graphic look-up tables, dictionary/thesaurus software, digital music waveforms, computer operating system programs, and video game software.

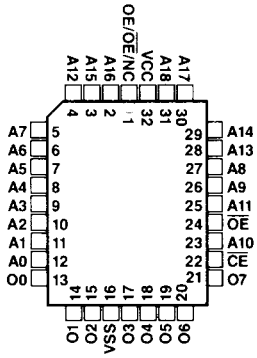
Package Configurations:

Plastic 32 PDIP



(TOP VIEW)

Plastic 32 PLCC



(TOP VIEW)

Pin Nomenclature

A_0–A_7	Column Address Inputs	$\overline{OE}$	Output Enable Input (Low)
A_8–A_{18}	Row Address Inputs	$\overline{CE}$	Chip Enable Input (Low)
OE	Output Enable Input (High)	NC	No Connect

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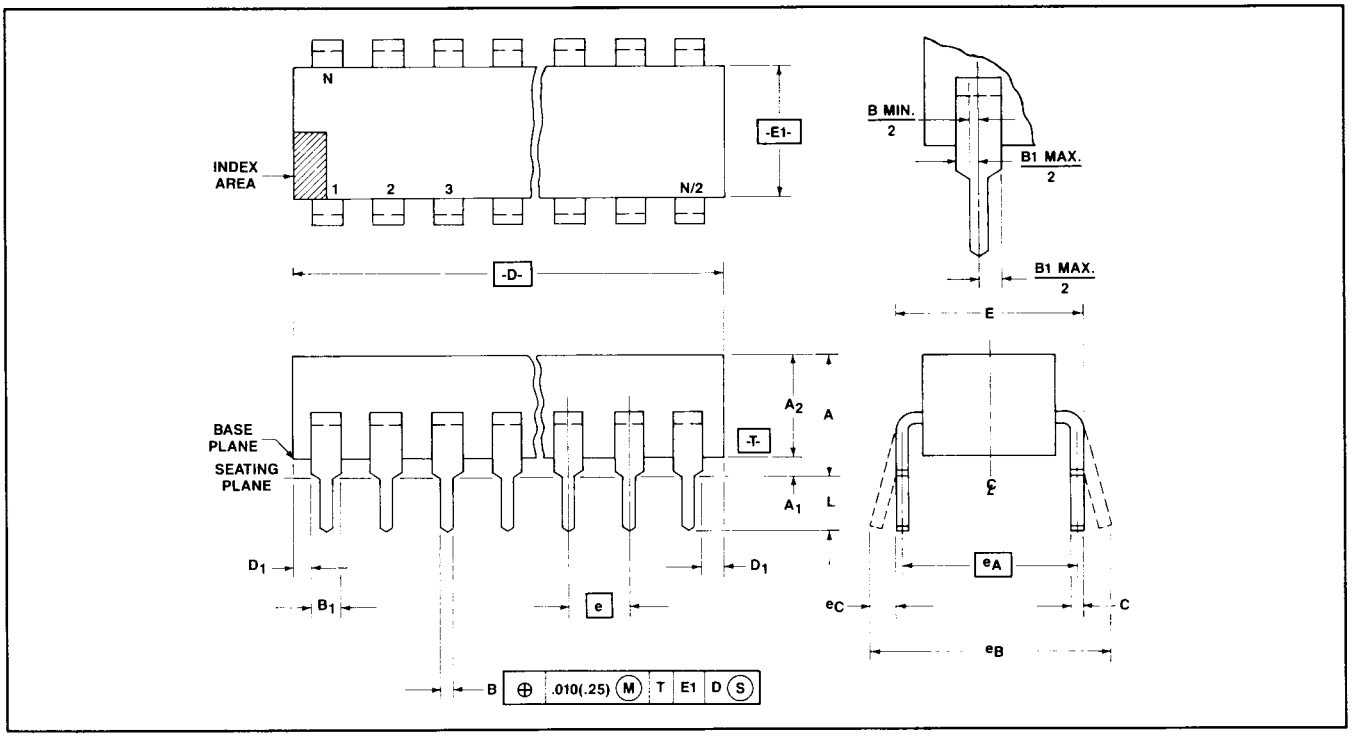
23000 SERIES PACKAGE OUTLINE DRAWINGS

Plastic Dual In-Line (PDIP) .300 Width



NOTE: 1, 2, 3, 8, 12

SYMBOL	NOTE	DIMENSIONS IN INCHES MIN	MAX	DIMENSIONS IN MILLIMETERS MIN	MAX	SYMBOL	NOTE	DIMENSIONS IN INCHES MIN	MAX	DIMENSIONS IN MILLIMETERS MIN	MAX
A	4,11	—	.210	—	5.33	E	6	.300	.325	7.62	8.25
A1	4	.015	—	.39	—	E1	5	.240	.280	6.10	7.11
A2		.115	.195	2.93	4.95	e		.100 BSC		2.54 BSC	
B	10	.014	.022	.356	.558	eA		.300 BSC		7.62 BSC	
B1	9	.045	.070	1.15	1.77	eB	7	—	.430	—	10.92
C		.008	.015	.204	.381	L	4	.115	.160	2.93	4.06
D1		.005	—	.13	—						
NUMBER OF LEADS											
D	28	1.380	1.565	35.1	38.7	D	32	1.560	1.745	39.6	44.3

NOTES

1. Controlling Dimensions. INCH
   In case of conflict between the English and metric dimensions, the inch dimensions control.
2. Dimensioning and tolerating per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of JEDEC Publication No. 95.
4. Dimensions A, A1, and L are measured with the package seated in JEDEC Seating Plane Gauge GS-3.
5. D and E1 dimensions for plastic packages, do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (0.25 mm).
6. E and eA measured with the leads contrained to be perpendicular to plane T.
7. eB and eC are measured at the lead tips with the loads unconstrained. eC must be zero or greater.
8. N is the number of terminal positions.
9. Corner leads (1, N, N/2, and N/2+1) may be configured as half leads.
10. Pointed versus rounded lead tips are preferred to ease insertion.
11. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
12. The package outline applies to devices in plastic packages.

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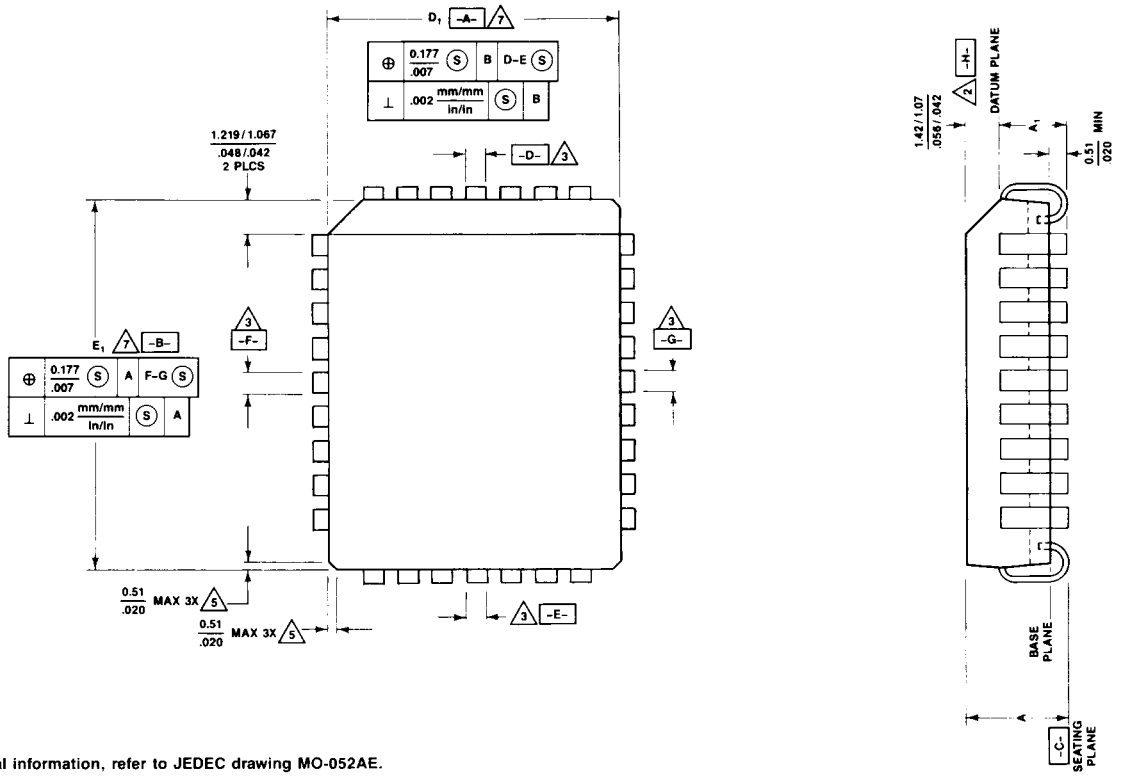
23000 SERIES PACKAGE OUTLINE DRAWINGS

Plastic Leaded Chip Carrier (PLCC)



For additional information, refer to JEDEC drawing MO-052AE.

Variations (Dimensions in Inches)

SYMBOL	AE MIN	AE MAX	NOTE
A	.100	.140	
A_1	.060	.095	
D	.485	.495	
D_1	.447	.453	7
D_2	.390	.430	
D_3	.300 REF.		
E	.585	.595	
E_1	.547	.553	7
E_2	.490	.530	
E_3	.400 REF.		
N	32		
ND	7		8
NE	9		8
DP	.130	.205	

Variations (Dimensions in Millimeters)

SYMBOL	AE MIN	AE MAX	NOTE
A	2.450	3.556	
A_1	1.524	2.413	
D	12.319	12.573	
D_1	11.354	11.506	7
D_2	9.906	10.922	
D_3	7.620 REF.		
E	14.859	15.113	
E_1	13.894	14.046	7
E_2	12.446	13.462	
E_3	10.160 REF.		
N	32		
ND	7		8
NE	9		8
DP	3.302	5.207	

NOTES:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Datum Plane -H- located at top of Mold Parting Line and coincident with top of lead, where lead exits plastic body.
3. Datums D-E and F-G to be determined where center leads exit plastic body at Datum Plane -H-.
4. **Controlling dimension: INCH.**
5. Exact shape of this feature is optional.
6. Location to Datums -A- and -B- to be determined at Plane -H-.
7. Dimensions D_1 and E_1 do not include mold protrusion. Allowable mold protrusion is .254 mm/.010 in.
8. N_D denotes the number of leads on the two short sides of the package, one of which contains Pin #1. N_E denotes the number of leads on the two long sides of the package.

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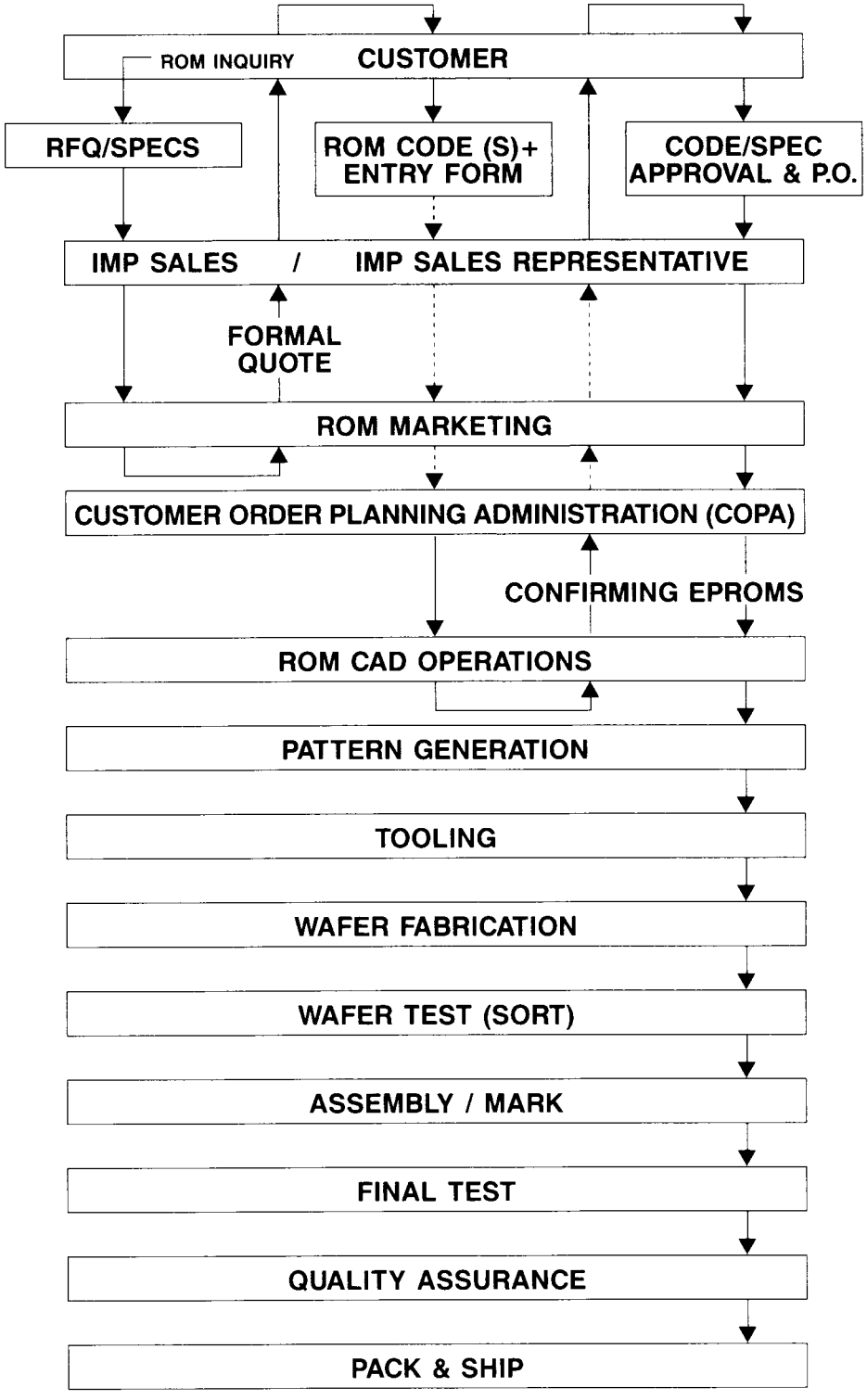
DEVELOPMENT & PRODUCTION FLOWCHART



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