General Description

The IDT8V40817 is a PLL-based clock generator specifically designed for Freescale Semiconductor Microprocessor and Microcontroller applications including the PowerPC and PowerQUICC. This device generates the microprocessor input clock and other microprocessor system and bus clocks at any one of four output frequencies. These frequencies include the popular 33- and 66-MHz PCI bus frequencies. The device offers five low-skew clock outputs plus three reference outputs. The clock input reference is 25 MHz and may be derived from an external source or by the addition of a 25MHz crystal to the on-chip crystal oscillator. The extended temperature range of the IDT8V40817 supports telecommunication and networking requirements.

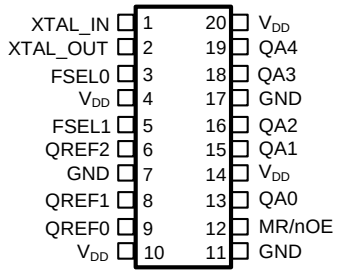
Functional Description

The IDT8V40817 uses a PLL with a 25MHz input reference frequency to generate a single bank of five configurable LVCMOS output clocks. The output frequency of this bank is configurable to either 25MHz, 33MHz, 50MHz, or 66MHz by two FSEL pins. The 25MHz reference may be either an external frequency source or a 25MHz crystal. The 25MHz crystal is directly connected to the XTAL_IN and XTAL_OUT pins with no additional components required. An external reference may be applied to the XTAL_IN pin with the XTAL_OUT pin left floating. The input reference, whether provided by a crystal or an external input, is also directly buffered to a second bank of three LVCMOS outputs. These outputs may be used as the clock source for processor I/O applications such as an Ethernet PHY. When FSEL0 and FSEL1 are both configured low, the QA outputs are directly fed from the input reference providing a total of eight low-skew 25MHz outputs. For all other combinations of FSEL0 and FSEL1 the single-ended LVCMOS outputs provide five low-skew outputs for use in driving a microprocessor or microcontroller clock input as well as other system components.

Features

- Five LVCMOS single-ended outputs for processor and other system circuitry
- Three buffered 25MHz reference clock outputs
- Crystal oscillator or external reference input
- Input reference frequency: 25MHz
- Selectable output frequencies: 25MHz, 33MHz, 50MHz or 66MHz
- Low Cycle-to-Cycle and Period jitter
- Supports Computing, Networking, and Telecommunications Applications
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in Lead-free (RoHS 6) packaging

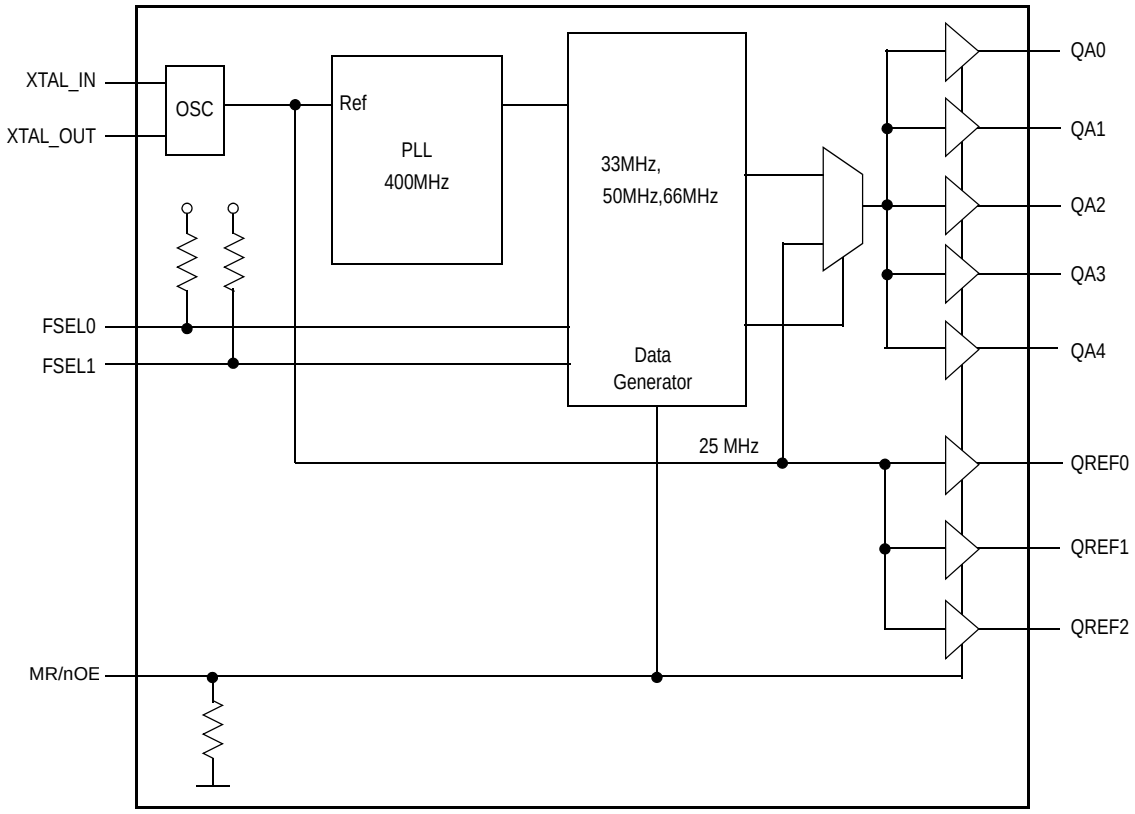
Pin Assignment



IDT8V40817

20 LEAD QSOP
0.194” x 0.236” x 0.058” package body
QG Package
Top View

Block Diagram



Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1	XTAL_IN	Input		Crystal oscillator input.
2	XTAL_OUT	Output		Crystal oscillator output.
3, 5	FSEL0, FSEL1	Input	Pullup	Select pins. Configures Bank A output frequency.
4, 10, 14, 20	V_{DD}	Power		Power supply pins.
6, 8, 9	QREF2, QREF1, QREF0	Output		Single-ended reference clock output pins (25MHz). LVCMOS/LVTTL interface levels.
7, 11, 17	GND	Power		Power supply ground.
12	MR/nOE	Input	Pulldown	Master Reset/Output Enable pin. Enables all outputs.
13, 15, 16, 18, 19	QA0, QA1, QA2, QA3, QA4	Output		Single-ended clock output pins. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	MR/nOE, FSEL0, FSEL1			4		pF
C_{PD}	Power Dissipation Capacitance (per output)		V_{DD} = 3.465V		8.5		pF
R_{PULLUP}	Input Pullup Resistor				75		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				75		kΩ

Function Table

Table 3. FSELx Function Table)

Control	Default	00	01	10	11
FSEL[0:1]	11	25MHz fed directly from reference input, PLL disabled	33MHz	50MHz	66MHz

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	-0.3V to 3.8V
DC Input Current, I_{IN}	±20mA
DC Output Current, I_{OUT}	±75mA
Storage Temperature, T_{STG}	-65°C to +125°C
Package Thermal Impedance, θ_{JA}	107.3°C/W

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Quiescent Supply Current			12	23	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IH}	Input High Voltage	XTAL_IN	Input Threshold = V_{DD}/2	2.4		V_{DD} + 0.3	V
I_{IN}(1)	Input Leakage Current		V_{IN} = V_{DDL} or GND			150	µA
V_{OL}	Output Low Voltage		I_{OL} = 12mA			0.4	V
V_{OH}	Output High Voltage		I_{OH} = -12mA	2.4			V
Z_{OUT}	Output Impedance				14		Ω

NOTE 1: Inputs have pulldown resistors affecting the input current.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Resonance		Parallel Resonance			
Frequency			25		MHz
Load Capacitance (C_L)			12		pF
Equivalent Series Resistance (ESR)			20		Ω
Shunt Capacitance		5		7	pF

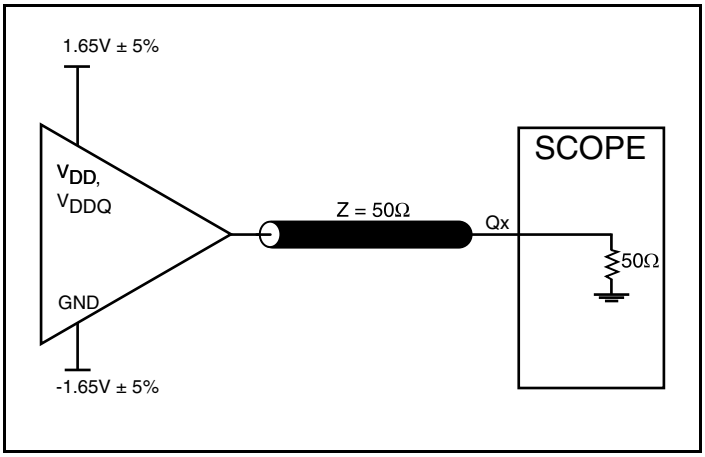
AC Electrical Characteristics

Table 6. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

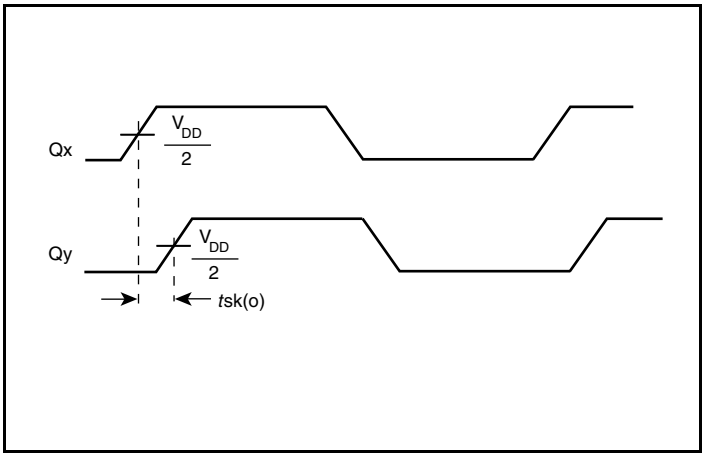
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
Input / Output Timing Specification							
f_{REF}	Input Reference Frequency		25MHz Input Crystal		25		MHz
f_{VCO}	VCO Frequency Range				400		MHz
f_{OUT}	Output Frequency	QAx	FSEL[0:1] = 00		25		MHz
		QAx	FSEL[0:1] = 01, PLL Locked		33		MHz
		QAx	FSEL[0:1] = 10, PLL Locked		50		MHz
		QAx	FSEL[0:1] = 11, PLL Locked		66		MHz
		QREFx			25		MHz
f_{REFPW}	Reference Input Pulse Width		25MHz Reference	10			ns
odc	Output Duty Cycle			47	50	53	%
PLL Specifications							
BW	PLL Closed Loop Bandwidth; NOTE 2				500		kHz
t_{LOCK}	Maximum PLL Lock Time					10	ms
Skew and Jitter Specifications							
*t*sk(b)	Bank Skew; NOTE 3, 4					100	ps
*t*sk(o)	Output Skew; NOTE 3, 5		FSEL[0:1] = 00			200	ps
tjit(cc)	Cycle-to-Cycle Jitter	QAx	25MHz Input Reference			150	ps
tjit(per)	Period Jitter	QAx	25MHz Input Reference			100	ps
t_R / t_F	Rise and Fall Time		20% to 80%			1	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: AC Characteristics apply for parallel output termination of 50Ω to V_{TT}.
NOTE 1: Based upon recommended crystal specifications as outlined in IDT8V40817 Operation.
NOTE 2: -3dB point of PLL transfer characteristics.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew within a bank of outputs at the same voltage and with equal load conditions. Measured at $V_{DD}/2$.
NOTE 5: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DD}/2$.

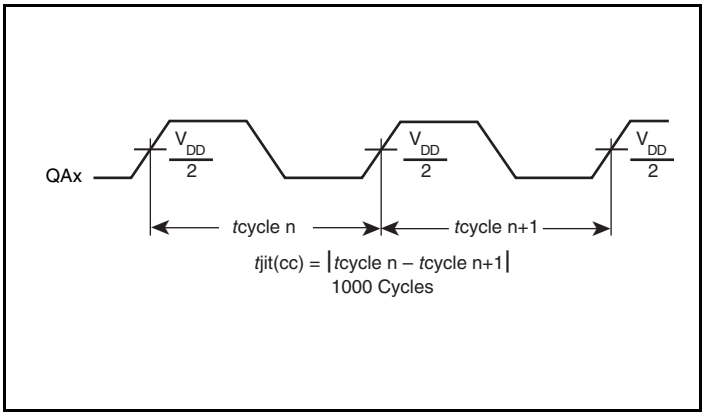
Parameter Measurement Information



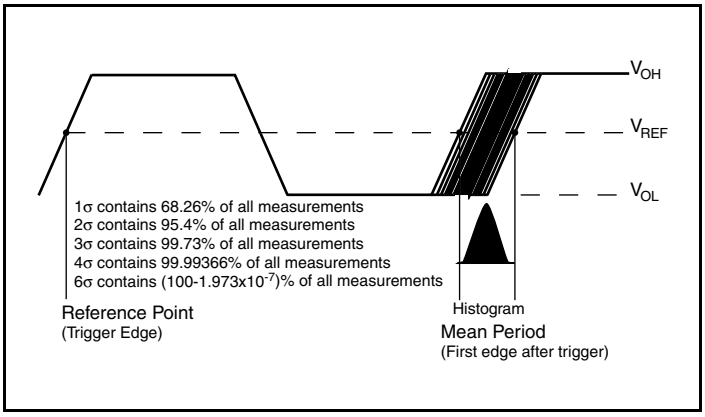
LVCMOS Output Load Test Circuit



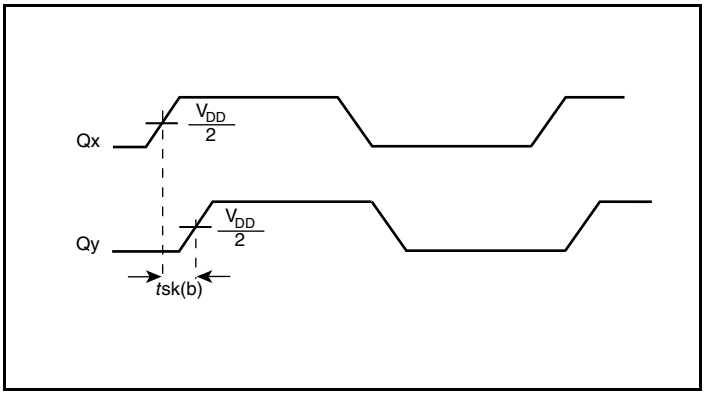
Output Skew



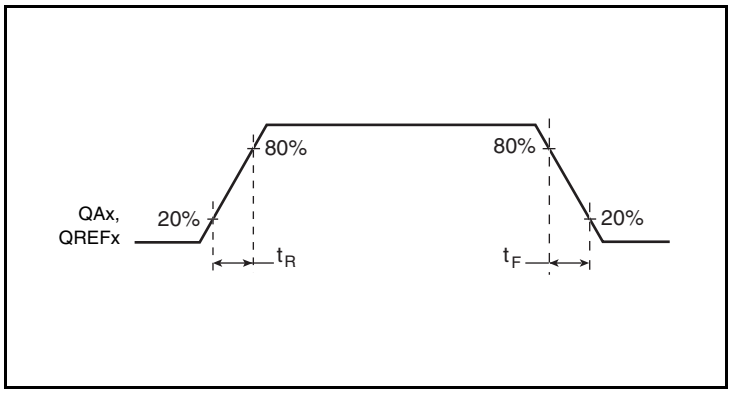
Cycle-to-Cycle Jitter



Period Jitter

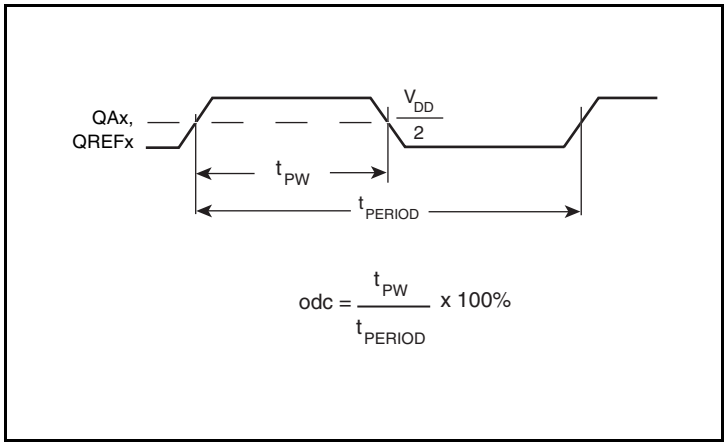


Bank Skew

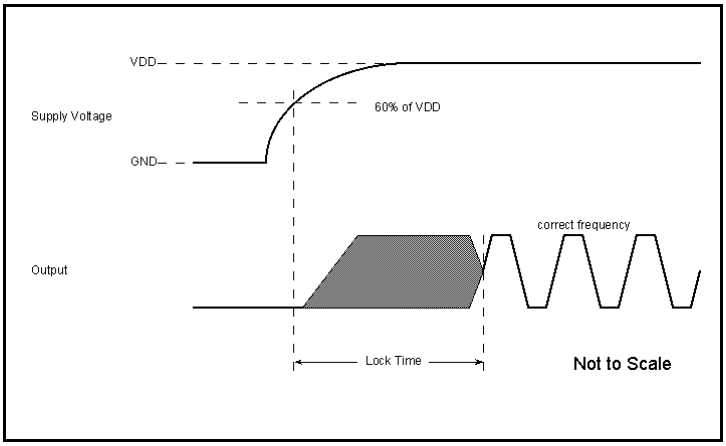


Rise/Fall Time

Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period



Lock Time

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS outputs can be left floating. There should be no trace attached.

Schematic Example

Figure 1 (next page) shows an example IDT8V40817 application schematic in which the device is operated at V_{DD} = 3.3V.

This example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set for the application.

The 12pF parallel resonant Fox FX325BS 25MHz crystal is used with tuning capacitors C1 = C2 = 5pF recommended for frequency accuracy. Depending on the parasitic of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting C1 and C2. For this device, the crystal tuning capacitors are required for proper operation.

Crystal layout is very important to minimize capacitive coupling between the crystal pads and leads and other metal in the circuit board. Capacitive coupling to other conductors has two adverse effects; it reduces the oscillator frequency leaving less tuning margin and noise coupling from power planes and logic transitions on signal traces can pull the phase of the crystal resonance, inducing jitter. Routing I^2C under the crystal is a very common layout error, based on the assumption that it is a low frequency signal and will not affect the crystal oscillation. In fact, I^2C transition times are short enough to capacitively couple into the crystal if they are routed close enough to the crystal traces.

In layout, all capacitive coupling to the crystal from any signal trace is to be minimized, that is to the XTAL_IN and XTAL_OUT pins, traces to the crystal pads, the crystal pads and the tuning capacitors. Using a crystal on the top layer as an example, void all signal and power layers under the crystal connections between the top layer and the ground plane used by the IDT8V40817. Then calculate the parasitic capacity to the ground and determine if it is large enough to preclude tuning the oscillator. If the coupling is excessive, particularly if the first layer under the crystal is a ground plane, a layout option is to void the ground plane and all deeper layers until the next ground plane is reached. The ground connection of the tuning capacitors should first be made between the capacitors on the top layer, then a single ground via is dropped to connect the tuning cap ground to the ground plane as close to the IDT8V40817 as possible as shown in the schematic.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The IDT8V40817 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

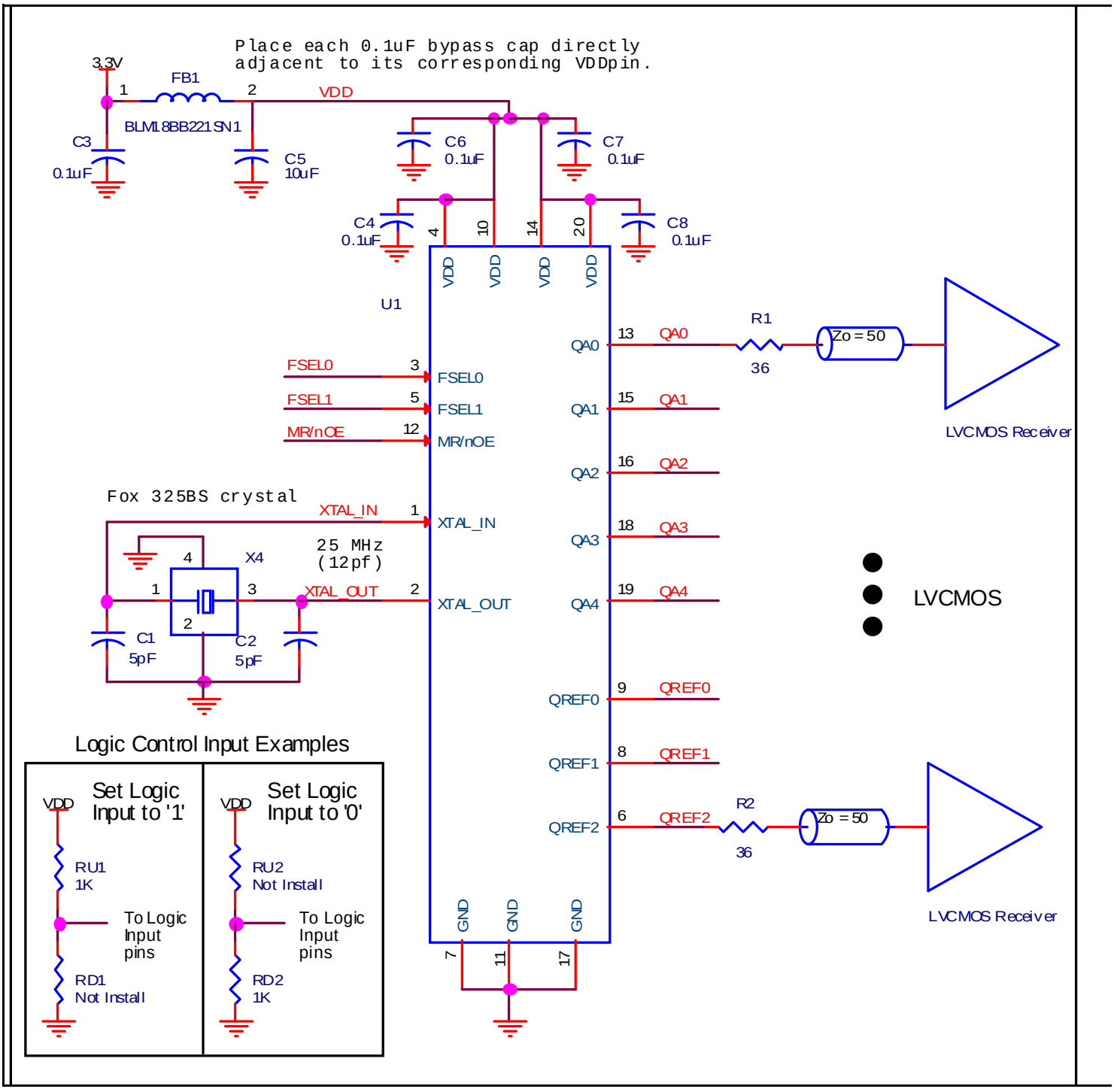


Figure 1. IDT8V40817 Application Schematic.

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8V40817.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8V40817 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD}$ = 3.465V * 23mA) = **79.7mW**

Total Static Power:

Power $(core)_{MAX}$ = **79.7mW**

Dynamic Power Dissipation at F_{OUT} (max.)

Total Power ($\mathbf{F_{OUT\_MAX}}$) = $[(C_{PD} * N) * Frequency * (V_{DDO})^2$ = 8.5pF * 66MHz * $(3.465V)^2$ = **6.7mW per output**
N = number of outputs

= **53.844mW**

Total Power Dissipation

- **Total Power**
  = Total Static Power + Dynamic Power Dissipation
  = 79.7mW + 53.844mW
  = 133.58mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 107.3°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.134W *107.3°C/W = 99.3°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 20 Lead QSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	107.3°C/W	96.5°C/W	87.6°C/W

Reliability Information

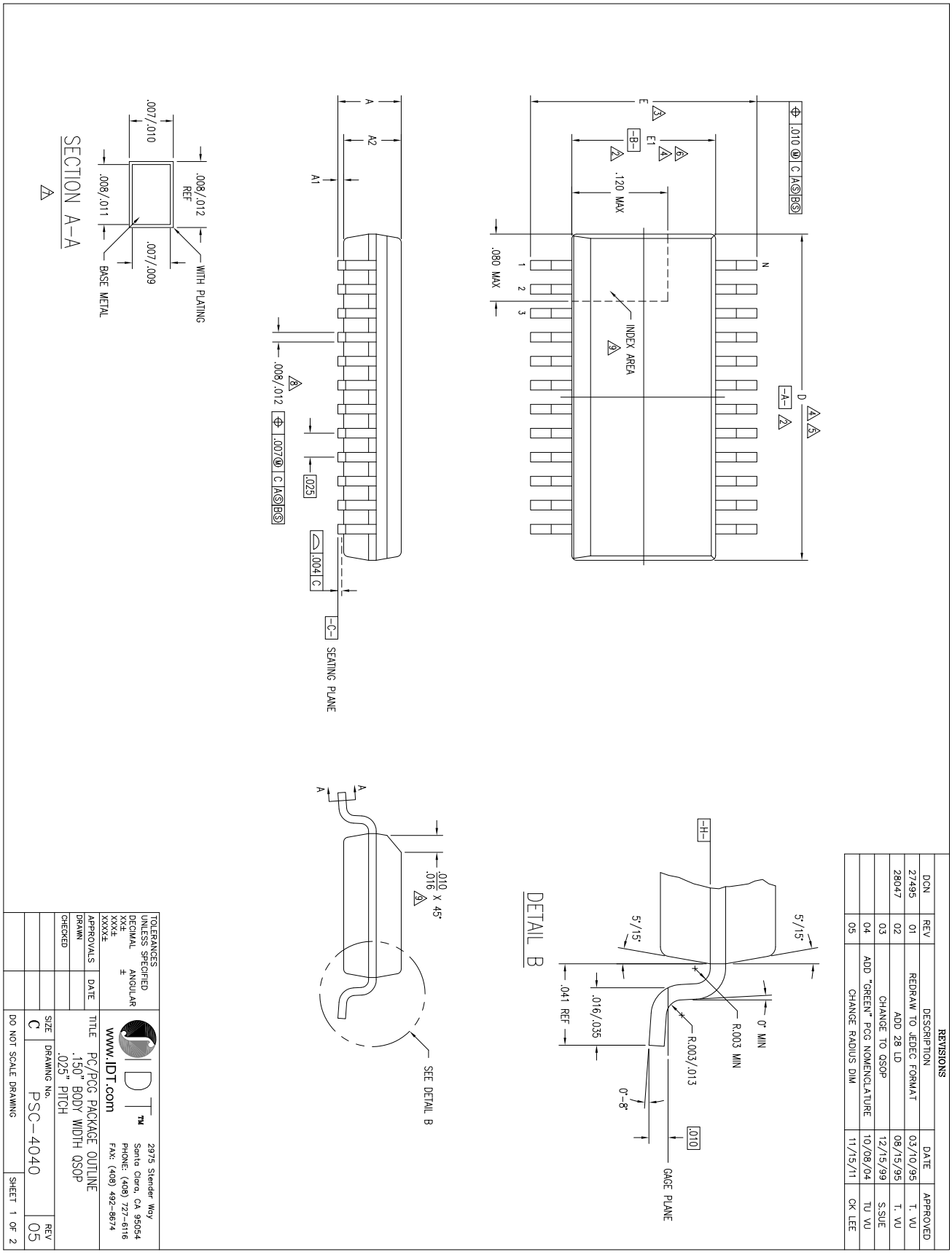
Table 8. θ_{JB} vs. Air Flow Table for a 20 Lead QSOP

θ_{JB} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	107.3°C/W	96.5°C/W	87.6°C/W

Transistor Count

The transistor count for the IDT8V40817 is: 933

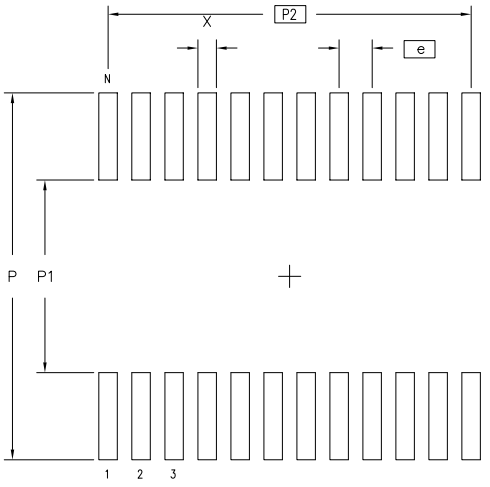
Package Outline and Package Dimensions



REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
28047	02	ADD 28 LD	08/15/95	T. VU
	03	CHANGE TO QSOP	12/15/99	S.SUE
	04	ADD "GREEN" PCG NOMENCLATURE	10/08/04	TU VU
	05	CHANGE RADIUS DIM	11/15/11	CK LEE

SYMBOL	JEDEC VARIATION AB			NOTE	JEDEC VARIATION AD			NOTE	JEDEC VARIATION AE			NOTE	JEDEC VARIATION AF			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	.061	.064	.068		.061	.064	.068		.061	.064	.068		.061	.064	.068	
A1	.004	.006	.010		.004	.006	.010		.004	.006	.010		.004	.006	.010	
A2	.055	.058	.061	11	.055	.058	.061	11	.055	.058	.061	11	.055	.058	.061	11
D	.189	.194	.196	4,5	.337	.342	.344	4,5	.337	.342	.344	4,5	.386	.390	.394	4,5
E	.230	.236	.244	3	.230	.236	.244	3	.230	.236	.244	3	.230	.236	.244	3
E1	.150	.155	.157	4,6	.150	.155	.157	4,6	.150	.155	.157	4,6	.150	.155	.157	4,6
N	16				20				24				28			

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	.274	.282	.274	.282	.274	.282	.274	.282
P1	.142	.150	.142	.150	.142	.150	.142	.150
P2	.175 BSC		.225 BSC		.275 BSC		.325 BSC	
X	.010	.018	.010	.018	.010	.018	.010	.018
e	.025 BSC		.025 BSC		.025 BSC		.025 BSC	
N	16		20		24		28	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982

2 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3 DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-

4 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE

6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE

7 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP

8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

9 THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED

10 ALL DIMENSIONS ARE IN INCHES

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–137, VARIATION AB, AD, AE & AF. EXCEPTIONS: JEDEC DIMENSION A2 MAX IS .059

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

APPROVALS DATE
DRAWN
CHECKED

IDT™ www.IDT.com
2975 Stender Way
Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674

TITLE PC/PCG PACKAGE OUTLINE
.150" BODY WIDTH QSOP
.025" PITCH

SIZE C | DRAWING No. PSC–4040 | REV 05

DO NOT SCALE DRAWING | SHEET 2 OF 2

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8V40817QG	IDT8V40817QG	“Lead-Free” 20 Lead QSOP	Tube	-40°C to 85°C
8V40817QG8	IDT8V40817QG	“Lead-Free” 20 Lead QSOP	Tape & Reel	-40°C to 85°C

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