Integrated Device Technology, Inc.

PARALLEL ASYNCHRONOUS SINGLE-BANK BIDIRECTIONAL FIFO 512 x 9, 1024 x 9, 2048 x 9

PRELIMINARY
IDT7271
IDT7272
IDT7273

INTEGRATED DEVICE

FEATURES:

- Bidirectional data transfer
- 512 x 9 organization (IDT7271)
- 1024 x 9 organization (IDT7272)
- 2048 x 9 organization (IDT7273)
- Fast 15ns access time
- Single bank FIFO memory with data flow in one direction at a time
- Direction pin controls data flow from Port A-to-B, or Port B-to-A
- Full and Empty flags
- Fixed Almost-Full and Almost-Empty partial flags
- Bypass and Diagnostic modes
- 32-pin PLCC

DESCRIPTION:

The IDT7271/7272/7273 are very high speed, low power FIFO memories that enhance processor-to-processor and processor-to-peripheral communications. The 727x family use a single bank of memory; therefore, allowing one port to be accessed at any time. A direction pin (DIR) is provided to determine data flow direction. When the DIR pin is Low, data flows from port A-to-B. Data flows in the opposite direction when the DIR pin is High.

A device reset can be initiated at any time by bringing the Reset ($\overline{RS}$) pin LOW while holding the Read ($\overline{RD}$), Bypass ($\overline{BYP}$), Diagnostic ($\overline{DIAG}$) and Write ($\overline{WR}$) pins High.

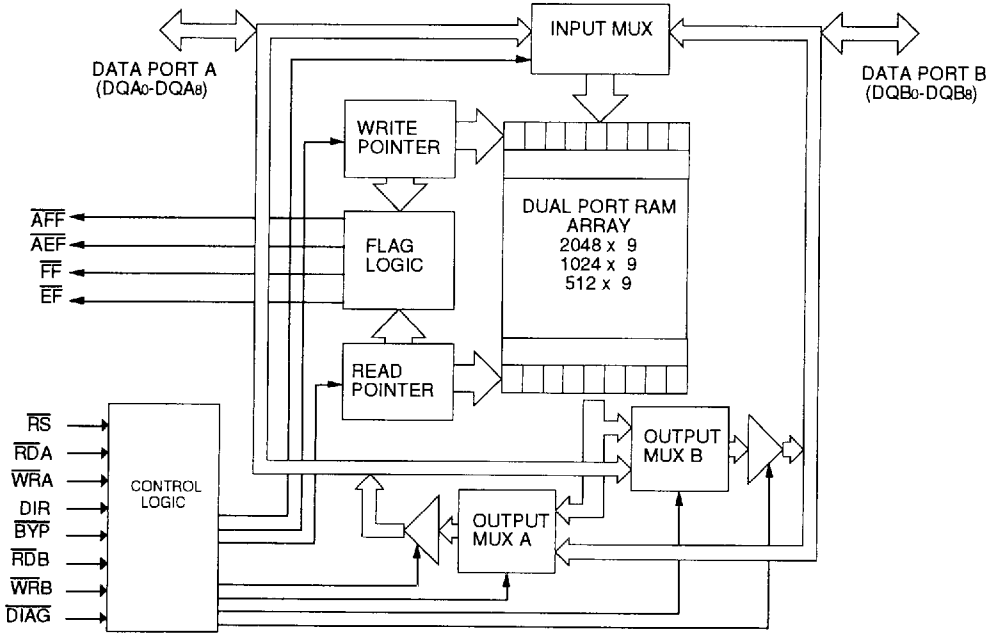
There are four separate flags on these BiFIFOs. The two end-point flags are Empty ($\overline{EF}$) and Full ($\overline{FF}$); and the two partial flags with fixed offset size of 07H (eight bytes from the boundaries) are Almost-Empty ($\overline{AE}$) and Almost-Full ($\overline{AF}$). All flags are active low.

Bypass control allows data to be directly transferred from port A to port B, or vice versa, without going through the memory array. The bypass mode can be set by asserting the $\overline{BYP}$ pin (active Low).

The diagnostic mode allows written data to be read through the same port. This provides systems memory self-test upon power up or after a system failure.

The IDT7271/2/3 are fabricated using IDT's high speed submicron CMOS technology.

FUNCTIONAL BLOCK DIAGRAMS



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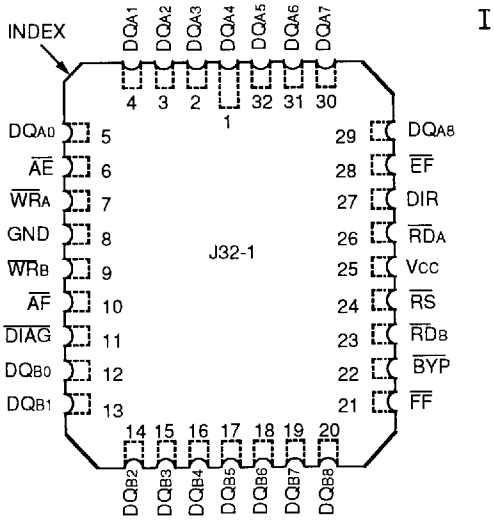
PIN CONFIGURATIONS



PLCC
TOP VIEW

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PIN DESCRIPTION

Symbol	Name	I/O	Description
DQA0-DQA8	Data A	I/O	9-bit data pins for port A The DIR pin controls direction of these pins (input or output)
DQB0-DQB8	Data B	I/O	9-bit data pins for port B The DIR pin controls state of these pins (inputs or outputs)
$\overline{RD}_A$	Read A	I	This input pin controls port A read operation In bypass mode this pin controls the A port output enables Active Low input.
$\overline{RD}_B$	Read B	I	This input pin controls port B read operation. Active Low input
$\overline{WR}_A$	Write A	I	This input pin controls port A write operation In bypass mode this pin controls the port B output enables Active Low input
$\overline{WR}_B$	Write B	I	This input pin controls port B write operation Active Low input.
DIR	Direction	I	This input pin determines data flow direction When it is Low, data flows from port A to port B When it is High, data flows in the opposite direction
$\overline{DIAG}$	Diagnostic	I	Once the data is loaded, the $\overline{DIAG}$ pin can be asserted followed by the DIR pin's state change, the written data can then be read through the same port
$\overline{BYP}$	Bypass	I	This input pin sets the FIFO in the bypass mode, in which the FIFO acts as a transceiver Active Low input.
$\overline{RS}$	Reset	I	This pin resets all functions Active Low input
$\overline{AE}$	Partial Flag	O	This output pin is asserted when the FIFO is almost empty Active Low output
$\overline{AF}$	Partial Flag	O	This output pin is asserted when the FIFO is almost full Active Low output
$\overline{FF}$	Full Flag	O	This output is asserted when the FIFO is completely full Active Low output
$\overline{EF}$	Empty Flag	O	This output is asserted when the FIFO is completely empty Active Low output
VCC	Power		One +5V power pins
GND	Ground		One ground pin at 0V

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7 0	–0 5 to +7 0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +155	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2529 tbl 02

1 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect reliabilty

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	5 0	5 5	V	
GND	Supply Voltage	0	0	0	V
VIH	Input High Votage	2 0	—	—	V
VIL(1)	Input Low Voltage	—	—	0 8	V

NOTE: 2529 tbl 04

1 1 5V undershoots are allowed for 10ns once per cycle

DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	IDT7271L IDT7272L IDT7273L Commercial tA = 15, 20, 25, 35 Min.	Typ.	Max.	Unit
ILI(1)	Input Leakage Current (Any Input)	-1	—	1	µA
ILO(2)	Output Leakage Current	-10	—	10	µA
VOH	Output Logic "1" Voltage, IOUT = -2 mA	2 4	—	—	V
VOL	Output Logic "0" Voltage, IOUT = 8 mA	—	—	0 4	V
ICC1(3)	Average VCC Power Supply Current	—	75	120	mA
ICC2(3)	Average Standby Current ($\overline{R}_A$ = $\overline{W}_A$ = $\overline{R}_B$ = $\overline{W}_B$ = $\overline{RS}$ = VIH	—	8	15	mA
ICC3(3)	Power Down Current (All Inputs = VCC - 0 2V)	—	—	8	mA

NOTES: 2529 tbl 04

1 Measurements with 0 4 ≤ VIN ≤ VCC
2. $\overline{OE}$ ≥ VIH, 0 4 ≤ VOUT ≤ VCC
3 Tested at f = 20 MHz.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3 0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1 5V
Output Reference Levels	1 5V
Output Load	See Figure 1

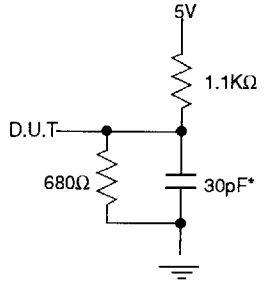
2529 tbl 05

CAPACITANCE(1) (TA = +25°C, f = 1.0 MHz)

Symbol	Parameter	Condition	Max.	Unit
CIN(3)	Input Capacitance	VIN = 0V	10	pF
COUT(2 3)	Output Capacitance	VOUT = 0V	10	pF

NOTES: 2529 tbl 06

1 This parameter is sampled and not 100% tested
2. With output deselected
3 Characterized values, not currently tested



or equivalent circuit 2529 drw 04

Figure 1. Output Load

*Includes jig and scope capacitances

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5.0V ± 10%, TA = 0°C to +70°C)

		Commercial								
		IDT7271L15 IDT7272L15 IDT7273L15		IDT7271L20 IDT7272L20 IDT7273L20		IDT7271L25 IDT7272L25 IDT7273L25		IDT7271L35 IDT7272L35 IDT7273L35		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Reset Timing										
tRSC	Reset Cycle Time	25	—	30	—	35	—	45	—	ns
tRS	Reset Pulse Width	15	—	20	—	25	—	35	—	ns
tRSS	Reset Set-up Time	15	—	20	—	25	—	35	—	ns
tRSR	Reset Recovery Time	10	—	10	—	10	—	15	—	ns
tRFV	Reset to Flag Valid	—	15	—	20	—	25	—	35	ns
Read/Write Timing										
tA	Read Access Time	—	15[1]	—	20	—	25	—	35	ns
tRC	Read Cycle Time	25	—	30	—	35	—	45	—	ns
tRPW	Read Pulse Width	15[1]	—	20	—	25	—	35	—	ns
tRR	Read Recovery Time	10	—	10	—	10	—	10	—	ns
tDV	Data valid from read pulse HIGH	3	—	3	—	3	—	3	—	ns
tRHZ	Read HIGH to data bus at High Z[2]	—	15	—	16	—	18	—	20	ns
tRLZ	Read LOW to data bus at Low Z[2]	3	—	3	—	3	—	3	—	ns
tWC	Write Cycle Time	25	—	30	—	35	—	45	—	ns
tWPW	Write Pulse Width	15	—	20	—	25	—	35	—	ns
tWR	Write Recovery Time	10	—	10	—	10	—	10	—	ns
tDS	Data Set-up Time	12	—	13	—	15	—	18	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	1	—	ns
Direction Change, Diagnostic and Bypass Timing										
tDFWL	DIR Change to Write Low	15	—	20	—	25	—	35	—	ns
tDFV	DIR Change to Valid Flags	—	18	—	20	—	20	—	30	ns
tDRL	DIR Change to Read Low	12	—	15	—	20	—	30	—	ns
tDHDGL	DIR Change to DIAG High	0	—	0	—	0	—	1	—	ns
tDRSU	DIR Setup	7	—	10	—	10	—	20	—	ns
tDGLDC	DIAG Low to DIR Change	7	—	10	—	10	—	20	—	ns
tDGHWL	DIAG High to Write Low	15	—	20	—	25	—	35	—	ns
tDGWR	DIAG Low to Write Low (either port)	7	—	10	—	10	—	20	—	ns
tBYSU	BYP Set-up Time	7	—	10	—	10	—	20	—	ns
tBYA	Bypass Access Time	—	15	—	20	—	25	—	35	ns
tBYD	Bypass Delay Time	—	15	—	20	—	25	—	35	ns
Flag Timing										
tFEFV	Full or Empty Flag Valid	—	15	—	15	—	20	—	30	ns
tAFAEV	Almost-Full or Empty Flag Valid	—	28	—	30	—	35	—	45	ns

2529 tbl 07

NOTES:
1. In diagnostic mode, tA(max) = 20ns, TRPW (min) = 20ns
2. Values guaranteed by design, not currently tested

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FUNCTIONAL DESCRIPTION

IDT's Single-Bank BiFIFO family is versatile for both multiprocessor and peripheral applications. The 727x family is a low-cost solution for bidirectional systems where data flow in only one direction at a time is needed. The Single-Bank BiFIFO implies that there is only one bank of memory shared by two ports, with a direction pin provided for altering data flow direction.

Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the writing side; $\overline{EF}$ is monitored on the reading side). In general a write cycle cannot be allowed to begin if $\overline{FF}$ is asserted and a read cycle cannot be allowed to begin if $\overline{EF}$ is asserted. For additional information, refer to Tech Note 8: *Operating FIFOs on Full and Empty Boundary Conditions* and Tech Note 6: *Designing with FIFOs.*

Reset

A reset is initiated by bringing the Reset ($\overline{RS}$) pin Low, while holding the Read ($\overline{RD}$), Bypass ($\overline{BYP}$), Diagnostic ($\overline{DIAG}$) and Write ($\overline{WR}$) pins High. After a device reset, all internal pointers are cleared and flags are adjusted accordingly. For proper device operation, all control inputs pins must be stable before the reset signal is deasserted. A recovery time is required before loading the device or altering operation mode (Bypass, Diagnostic, etc).

Flags

There are four separate flags on the 7271/2/3 BiFIFO, two partial flags, a full flag and an empty flag. All are active low. The two partial flags are the Almost Full ($\overline{AF}$) and the Almost Empty ($\overline{AE}$) flags, each with a fixed offset size of 07H (eight bytes from the empty or full conditions). These can be used as an early warning signal. The two other flags are fixed at Empty $\overline{EF}$ and Full $\overline{FF}$. These are asserted during the last read or write operation respectively. These are used to prevent device overflow or underflow.

Data Flow Direction

Data can only flow from one port to another at any given time. The direction of data flow is determined by the state of the DIR pin. When the DIR pin is Low, data can be written only into port A. Data can be read only out of port B. Data flows in the opposite direction when the DIR pin is High. Data flow function can be changed at any time. By altering the DIR state, the two read and write pointers are reset and data flows in the opposite direction. The falling edge of the first write cycle is used to determine the end of the reset cycle. Flags outputs reflect the pointer states and thus change on the change of the DIR signal.

Bypass Mode

Asserting the $\overline{BYP}$ pin (active Low) places the device in the bypass mode. The FIFO functions as a simple transciever in this mode. Data can be directly written into or read out of a device which is connected to the B port by a device connected to the A port.

While in this mode, both $\overline{RDB}$ and $\overline{WRB}$ must be held High. By asserting the $\overline{WRA}$, data on the A port will be driven out the B port. By asserting the $\overline{RDA}$, data on the B port will be driven out the A port. The $\overline{WRA}$ signal is used to enable the B port's bus drivers. The $\overline{RDA}$ signal is used enable the A ports. $\overline{WRA}$ and $\overline{RDA}$ must not be low at the same time.

Entering and exiting the bypass mode does not affect the internal pointers. The state of the DIR pin is ignored in the bypass mode. If DIR changes state in Bypass mode, the pointers will not reset until leaving the Bypass mode. If DIR changes state momentarily in Bypass mode there is no effect. Bypass mode does not alter flag states.

Diagnostic Mode

Many systems require memory testing upon power up or after a system failure. The 727x family has a built-in diagnostic mode for self test. When in the diagnostic mode, written data can be read through the same port by altering the state of the DIR pin. In this case, the pointers are not reset (with direction change) allowing the retrieval of written data. The read and write pointers are reset upon exiting the diagnostic mode. The leading edge of the first write cycle experienced after leaving diagnostic mode is used to terminate the reset cycle. Flag operations are normal in diagnostic mode, reflecting only the relative states of the read and write pointers. Thus they change on the rising edge of the $\overline{DIAG}$ signal when the pointers are reset upon leaving diagnostic mode.

The state of the DIR pin is latched when $\overline{DIAG}$ is brought low, determining which port of the FIFO is used for diagnostics. If DIR is Low at the High-to-Low transition of $\overline{DIAG}$, A port is used for diagnostics. If High, B port is used. Figure 12 shows diagnostics for B port, but the timing also applies to A port diagnostics if DIR is inverted.

Data can be loaded into the memory array before or after setting the part into diagnostic mode. The $\overline{DIAG}$ pin must be asserted before by the DIR pin's first state change. Once in the diagnostic mode, data that has been written can be retrieved through the same port by reading from that port. Reading and writing can continue indefinately until the diagnostic mode has been exited.

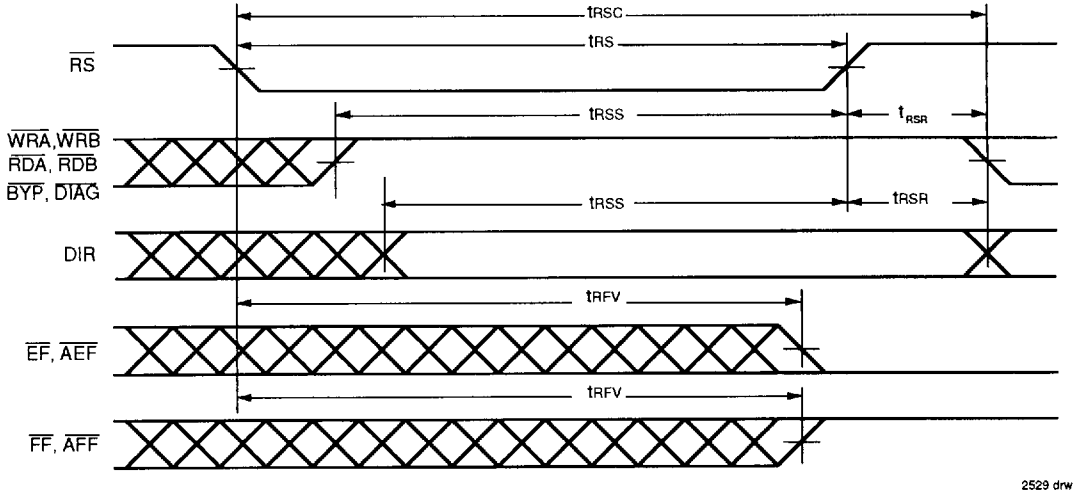

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Figure 2. Reset Cycle Timing

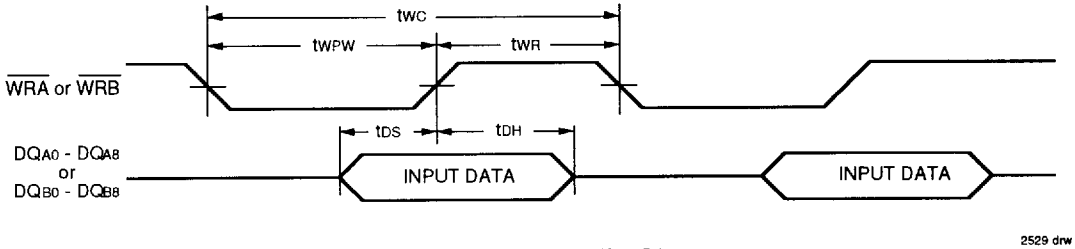

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Figure 3. Write Timing (A or B)

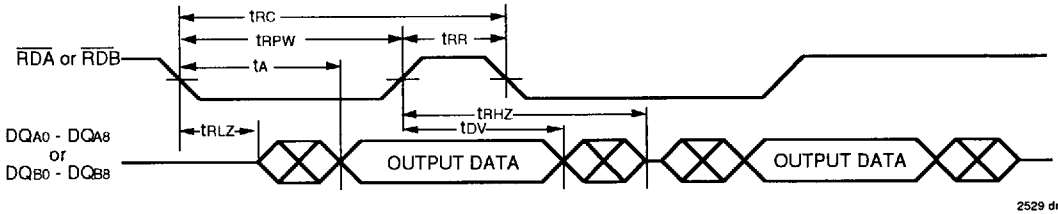

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Figure 4. Read Timing (A or B)

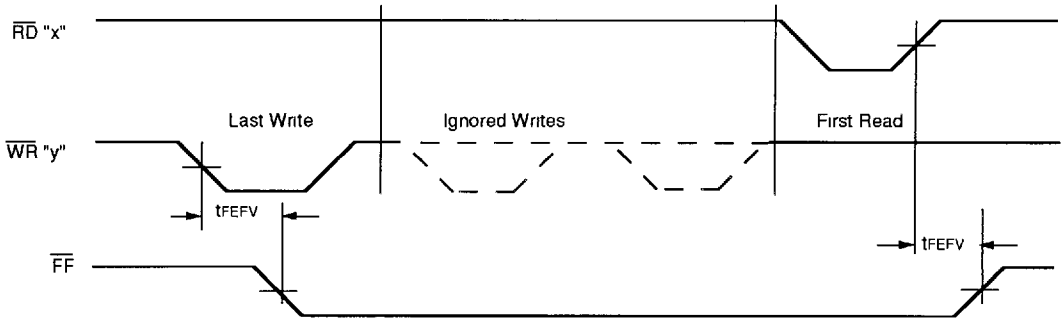

Figure 5. Full Flag Assertion/Deassertion Timing, in either direction or in Diagnostic mode

2529 drw 08

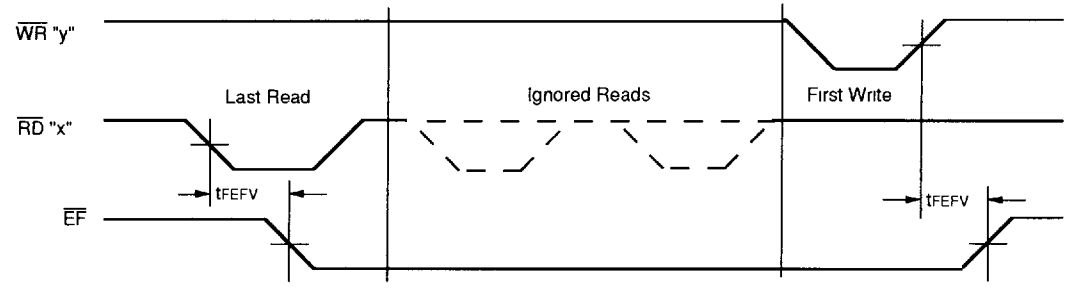

Figure 6. Empty Flag Assertion/Deassertion Timing, in either direction or in Diagnostic mode

2529 drw 09

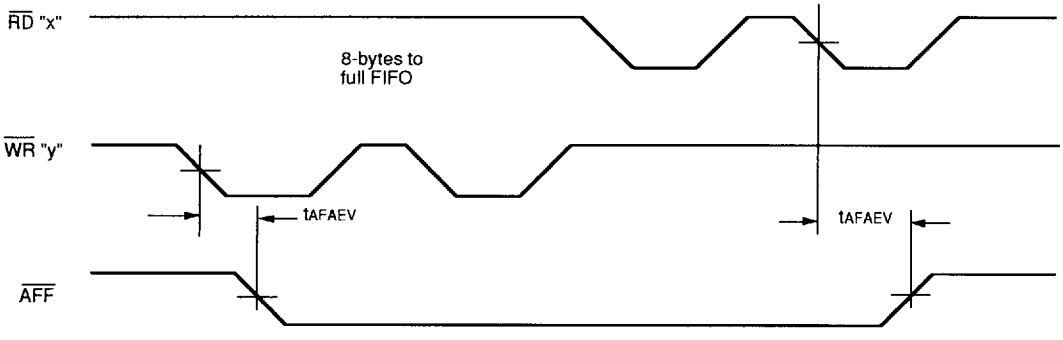

Figure 7. Almost Full Flag Assertion/Deassertion Timing, in either direction or in Diagnostic mode

2529 drw 10

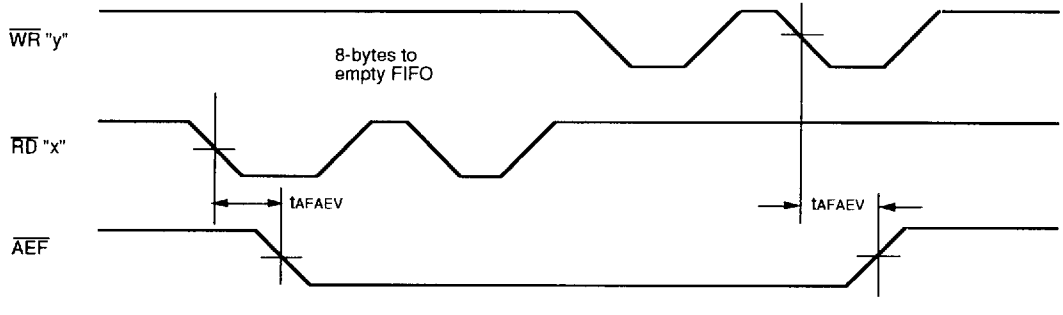

Figure 8. Almost Empty Flag Assertion/Deassertion Timing, in either direction or in Diagnostic mode

2529 drw 11

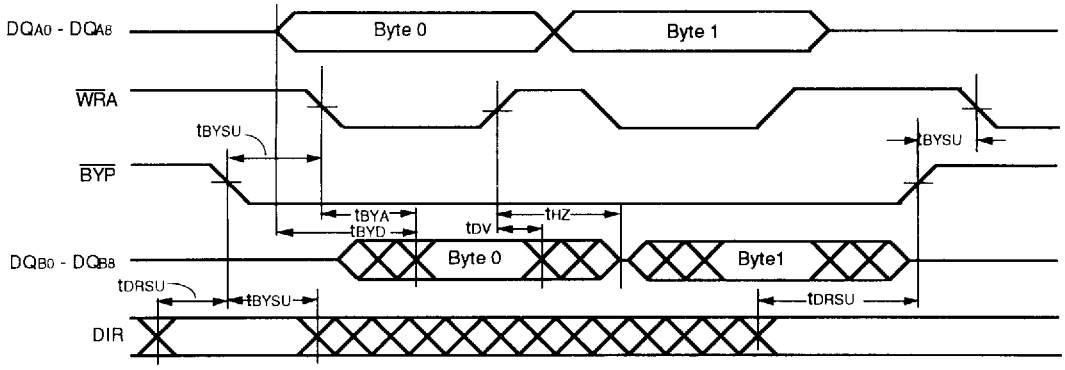

Figure 9. Bypass mode: Data flow from A to B

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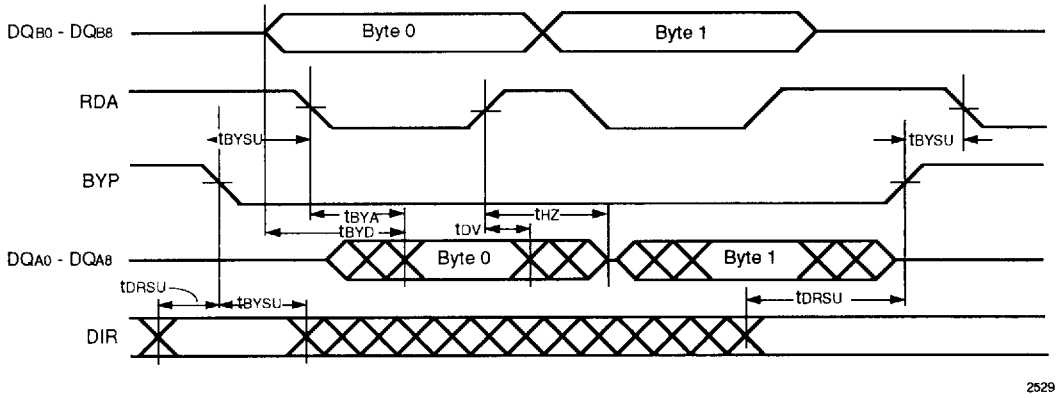

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Figure 10. Bypass mode: Data Flow from B to A

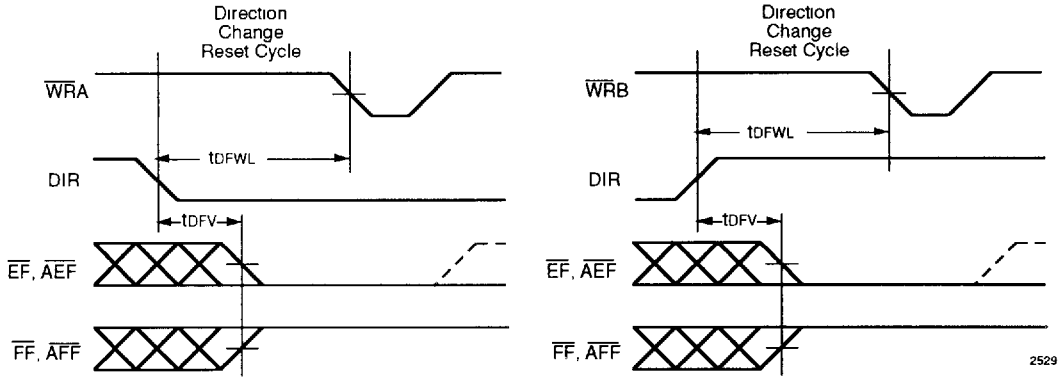

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Figure 11. Data Flow Direction Change and Reset cycle Timing

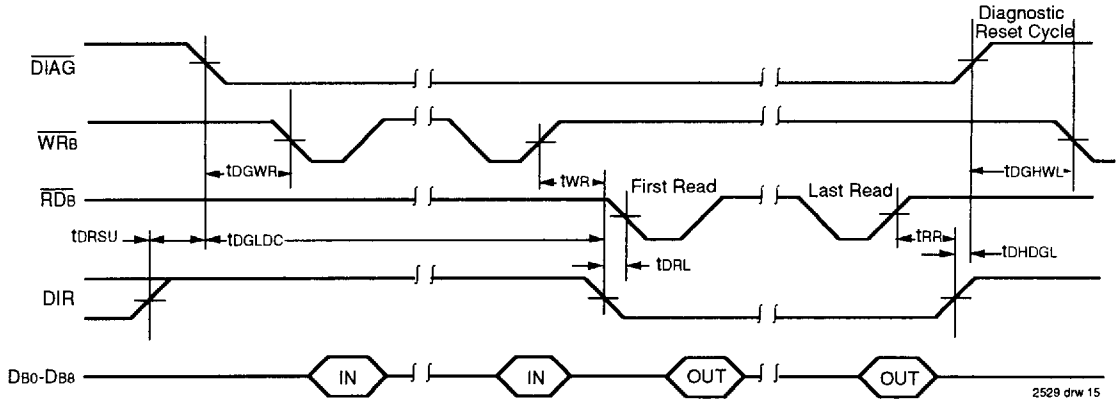


Figure 12. Diagnostic Mode Read/Write Timing and Diagnostic Reset Cycle.

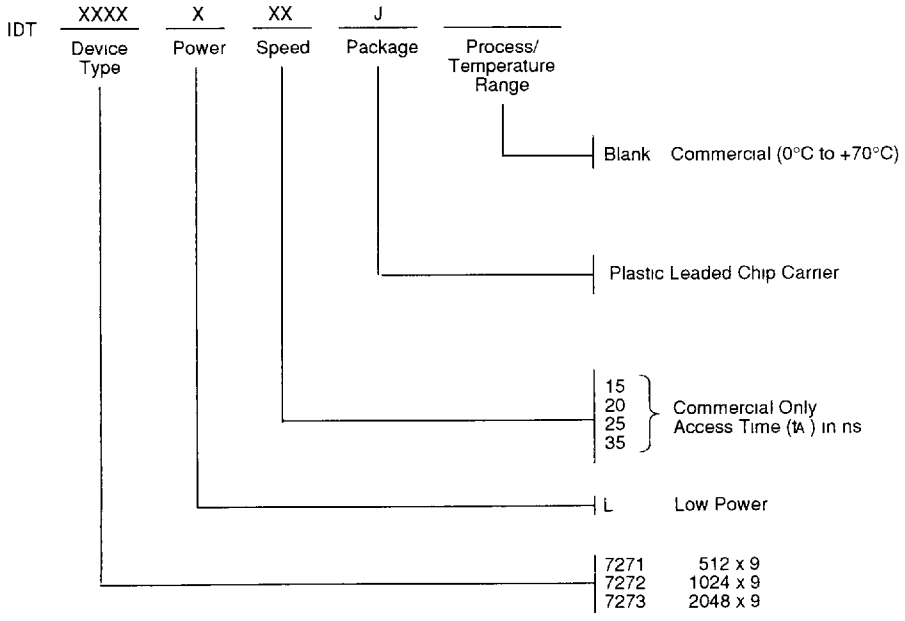
TABLE I — OPERATING MODES

$\overline{RS}$	$\overline{BYP}$	$\overline{DIAG}$	DIR	$\overline{RDA}$	$\overline{WRA}$	$\overline{RDB}$	$\overline{WRB}$	Operating Mode
⊓	1	1	x	1	1	1	1	Device reset
1	1	0	0	1	⊓	1	1	Diagnostic mode: data is being loaded through A port
1	1	0	1	⊓	1	1	1	Diagnostic mode: data is being retrieved through A port
1	1	0	1	1	1	1	⊓	Diagnostic mode: data is being loaded through B port
1	1	0	0	1	1	⊓	1	Diagnostic mode: data is being retrieved through B port
1	0	1	X	1	0	1	1	Bypass mode: Data flows from A port to B port
1	0	1	X	0	1	1	1	Bypass mode: Data flows from B port to A port
1	1	1	0	1	⊓	⊓	1	FIFO Mode: Asynchronous read/write. Data flows from port A to port B.
1	1	1	1	⊓	1	1	⊓	FIFO Mode: Asynchronous read/write. Data flows from port B to port A

2529 tbl 07

Unspecified states are not allowed

ORDERING INFORMATION



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