General Description

The 8T49N4811 is a highly flexible FemtoClock® NG pin-programmable clock generator suitable for networking and communications applications. It is able to generate five different output frequencies with multiple copies of each. A fundamental mode crystal, single-ended, or differential input reference may be used as the source for the output frequency.

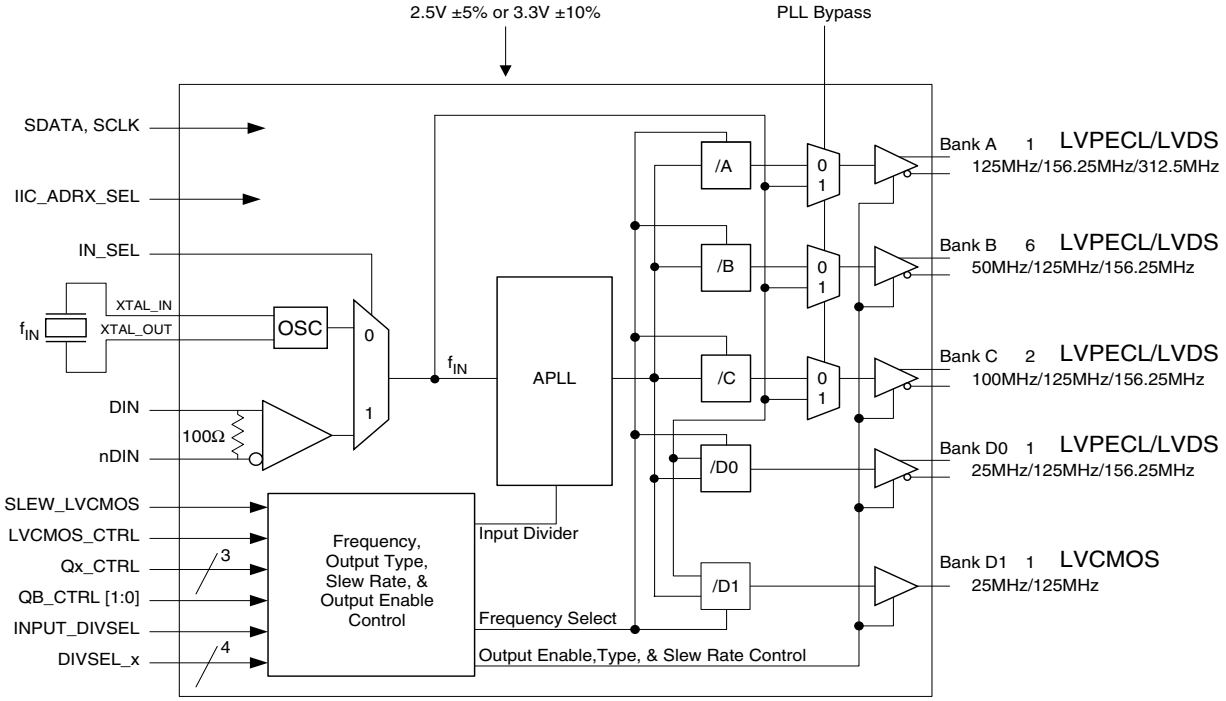
The use of pin-programming to select the input source / frequency, desired output frequencies and output styles allow a single device to be used in a wide variety of applications without the need for register programming.

Selection pins use 3-level options to maximize flexibility while minimizing package size. Selection is performed by tying a selection pin high or low or by leaving it floating, eliminating the need for passive components to drive a desired logic level.

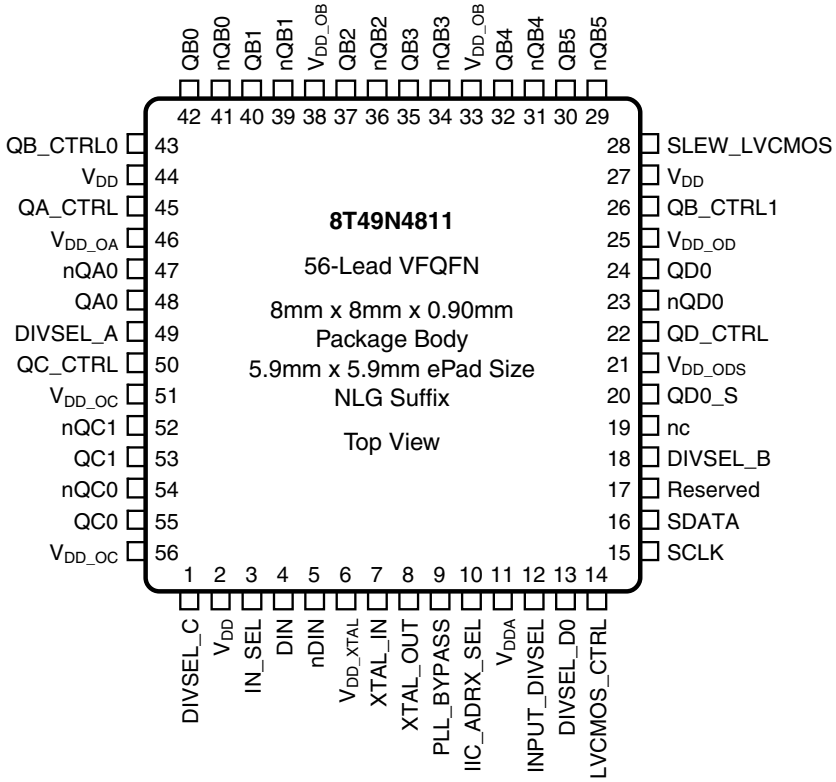
Features

- Fourth generation FemtoClock® NG technology
- Generates multiple copies of 25MHz, 50MHz, 100MHz, 125MHz, 156.25MHz or 312.5MHz
- Typical input frequency is 25MHz, with optional 125MHz and 156.25MHz input support
- Differential outputs are pin programmable for LVDS or LVPECL
- RMS phase jitter at 156.25MHz: <300fs typical
- Power Supply Rejection Ratio better than -50dBc from 10k-1.5MHz at 3.3V power supply
- Full 3.3V and 2.5V Supply Voltages
- -40°C to +85°C ambient operating temperature
- 56-pin VFQFPN, lead-free (RoHS 6) packaging

Block Diagram



Pin Assignment



Pin Description and Pin Characteristic Tables

Table 1. Pin Description

Number	Name	Type		Description
1	DIVSEL_C	Input	Pullup/Pulldown	Output divider selection for Bank C. LVCMOS interface levels.
2	V_{DD}	Power		Core supply.
3	IN_SEL	Input	Pullup/Pulldown	Input select between XTAL or differential input. LVCMOS interface levels.
4	DIN	Input		Differential Reference Input. Accepts DC-coupled LVDS and is internally biased to accept AC-coupled LVPECL, CML, HCSL or LVPECL signals. The differential inputs have an internal 100Ω resistor biased to V_{DD}–1.3V approximately.
5	nDIN	Input		
6	V_{DD_XTAL}	Power		Crystal oscillator power supply.
7	XTAL_IN	Input		Crystal input.
8	XTAL_OUT	Output		Crystal output.
9	PLL_BYPASS	Input	Pulldown	PLL Bypass. Provides copy of f_{IN} to output banks A, B, C. LVCMOS interface levels.
10	IIC_ADRX_SEL	Input	Pulldown	Selects between I^2C addresses. LVCMOS interface levels.
11	V_{DDA}	Power		Analog supply.
12	INPUT_DIVSEL	Input	Pullup/Pulldown	Selects proper divide ratios for differential reference input. LVCMOS interface levels.
13	DIVSEL_D0	Input	Pullup/Pulldown	Output divider selection for Bank D0 differential output. LVCMOS interface levels.
14	LVCMOS_CTRL	Input	Pullup/Pulldown	Divider and output enable control for Bank D1 LVCMOS output. LVCMOS interface levels.
15	SCLK	Input	Pullup	I^2C Clock Input. LVCMOS/LVTTL interface levels.
16	SDATA	I/O	Pullup	I^2C Data Input/Output. Input: LVCMOS/LVTTL interface levels. Output: Open Drain.
17	Reserved		Pulldown	Reserved. Internally connected to 50kΩ pulldown.
18	DIVSEL_B	Input	Pullup/Pulldown	Output divider selection for Bank B. LVCMOS interface levels.
19	nc			This pin is not internally connected. Connect to ground to maintain second source compatibility.
20	QD0_S	Output		Bank D1 LVCMOS Output.
21	V_{DD_ODS}	Power		Power supply for Bank D1 LVCMOS output.
22	QD_CTRL	Input	Pullup/Pulldown	Control input for bank D0 output type and OE status. LVCMOS interface levels.
23	nQD0	Output		Bank D0 Differential Output. LVDS or LVPECL output levels.
24	QD0	Output		Bank D0 Differential Output. LVDS or LVPECL output levels.
25	V_{DD_OD}	Power		Power supply for Bank D0 differential output.
26	QB_CTRL1	Input	Pullup/Pulldown	Control input for bank B outputs QB3 to QB5 output type and OE status. LVCMOS interface levels.
27	V_{DD}	Power		Power supply.
28	SLEW_LVCMOS	Input	Pulldown	Slew rate control pin for LVCMOS output. LVCMOS interface levels.
29	nQB5	Output		Bank B Differential Output. LVDS or LVPECL output levels.
30	QB5	Output		Bank B Differential Output. LVDS or LVPECL output levels.
31	nQB4	Output		Bank B Differential Output. LVDS or LVPECL output levels.
32	QB4	Output		Bank B Differential Output. LVDS or LVPECL output levels.
33	V_{DD_OB}	Power		Power supply for Bank B.
34	nQB3	Output		Bank B Differential Output. LVDS or LVPECL output levels.

Table 1. Pin Description (Continued)

35	QB3	Output		Bank B Differential Output. LVDS or LVPECL output levels.
36	nQB2	Output		Bank B Differential Output. LVDS or LVPECL output levels.
37	QB2	Output		Bank B Differential Output. LVDS or LVPECL output levels.
38	V_{DD_OB}	Power		Power supply for Bank B.
39	nQB1	Output		Bank B Differential Output. LVDS or LVPECL output levels.
40	QB1	Output		Bank B Differential Output. LVDS or LVPECL output levels.
41	nQB0	Output		Bank B Differential Output. LVDS or LVPECL output levels.
42	QB0	Output		Bank B Differential Output. LVDS or LVPECL output levels.
43	QB_CTRL0	Input	Pullup/Pulldown	Control input for bank B outputs QB0 to QB2 output type and OE status. LVCMOS interface levels.
44	V_{DD}	Power		Power supply.
45	QA_CTRL	Input	Pullup/Pulldown	Control input for bank A output type and OE status. LVCMOS interface levels.
46	V_{DD_OA}	Power		Power supply for Bank A.
47	nQA0	Output		Bank A Differential Output. LVDS or LVPECL output levels.
48	QA0	Output		Bank A Differential Output. LVDS or LVPECL output levels.
49	DIVSEL_A	Input	Pullup/Pulldown	Output divider selection for Bank A. LVCMOS interface levels.
50	QC_CTRL	Input	Pullup/Pulldown	Control input for bank C output type and OE status. LVCMOS interface levels.
51	V_{DD_OC}	Power		Power supply for Bank C.
52	nQC1	Output		Bank C Differential Output. LVDS or LVPECL output levels.
53	QC1	Output		Bank C Differential Output. LVDS or LVPECL output levels.
54	nQC0	Output		Bank C Differential Output. LVDS or LVPECL output levels.
55	QC0	Output		Bank C Differential Output. LVDS or LVPECL output levels.
56	V_{DD_OC}	Power		Power supply for Bank C.
E-PAD	GND	Power		Connect to ground; use thermal vias.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				3.5		pF
R_{PULLUP}	Input Pullup Resistor		SCLK, SDATA		50		kΩ
			DIVSEL_x, IN_SEL, IN_SEL, INPUT_DIVSEL, LVCMOS_CTRL, Qx_CTRL, QB_CTRL[1:0]		58		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				42		kΩ
			PLL_BYPASS, IIC_ADRX_SEL, Reserved, SLEW_LVCMOS		50		kΩ
C_{PD}	Power Dissipation Capacitance	QDO_S	V_{DD} = V_{DDO_ODS} = 3.63V		18		pF
		QDO_S	V_{DD} = V_{DDO_ODS} = 2.625V		16		pF
R_{OUT}	Output Impedance	QDO_S	V_{DDO_ODS} = 3.3V		24		Ω
		QDO_S	V_{DDO_ODS} = 2.5V		30		Ω

Function Tables

Table 3A. Input Frequency Select Table

INPUT_DIVSEL	
0	25MHz
1	125MHz
Float	156.25MHz

Table 3B. Slew Rate Control Table

SLEW_LVCMOS	
0 (default)	Normal
1	Slow

Table 3C. PLL Bypass Table

PLL_BYPASS	
0 (default)	Normal Operation
1	PLL Bypassed

Table 3D. I^2C Address Selection Table

IIC_ADRX_SEL	Address
0 (default)	DC (h)
1	DE (h)

Table 3E. Bank A Frequency Select Table

DIVSEL_A	Frequency
0	156.25MHz
1	125MHz
Float	312.5MHz

Table 3F. Bank B Frequency Select Table

DIVSEL_B	Frequency
0	156.25MHz
1	125MHz
Float	50MHz

Table 3G. Bank C Frequency Select Table

DIVSEL_C	Frequency
0	156.25MHz
1	125MHz
Float	100MHz

Table 3H. Bank D1 LVCMOS Control Table

LVCMOS_CTRL	State
0	High Impedance
1	125MHz
Float	f_{IN}

Table 3I. Bank D0 QD0 Frequency Select Table

DIVSEL_D0	Frequency
0	156.25MHz
1	125MHz
Float	f_{IN}

Table 3J. Clock Select Function Table

Control Input	Clock	
IN_SEL	Crystal	DIN, nDIN
0	Selected	De-selected
1	De-selected	Selected
Float	Selected (Doubler = ON)	De-selected

Table 3K. Qx_CTRL and QB_CTRL[1:0] Pin Table

Bank Mode Pin	Bank Mode	
	LVPECL	LVDS
0	Selected; Note 1, 2	De-selected
1	De-selected	Selected; Note 1, 2
Float	High Impedance; Note 3	High Impedance; Note 3

NOTE 1: QD_CTRL affects differential outputs ONLY.
NOTE 2: QB_CTRL0 affects outputs QB[0:2]. QB_CTRL1 affects outputs QB[3:5].
NOTE 3: High impedance mode: 100k pulldown on true output, 100k pullup on compliment output.

Serial Interface Configuration Description

The 8T49N4811 has an I^2C-compatible configuration interface to access any of the internal registers for frequency and PLL parameter programming. The 8T49N4811 acts as a slave device on the I^2C bus and has the address 0b1101110. The interface accepts byte-oriented block write and block read operations. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first, see Block Write/Read Operation tables).

Read and write block transfers can be stopped after any complete byte transfer.

For full electrical I^2C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 50kΩ typical.

Table 4A. Block Write Operation

Bit	1	2:08	9	10	11:18	19	20:27	28	...	...	...
Description	START	Slave Address	W(0)	ACK	Data Byte (P)	ACK	Data Byte (P+1)	ACK	Data Byte …	ACK	STOP
Length (bits)	1	7	1	1	8	1	8	1	8	1	1

Table 4B. Block Read Operation

Bit	1	2:08	9	10	11:18	19	20-27	28	...	...	...
Description	START	Slave Address	R(1)	ACK	Data Byte (P)	ACK	Data Byte (P+1)	ACK	Data Byte …	ACK	STOP
Length (bits)	1	7	1	1	8	1	8	1	8	1	1

Table 4C. DIVSEL_A Programming

00	156.25MHz
01	312.5MHz
10	125MHz
11	100MHz

Table 4D. DIVSEL_B Programming

00	156.25MHz
01	50MHz
10	125MHz
11	100MHz

Table 4E. DIVSEL_C Programming

00	156.25MHz
01	100MHz
10	125MHz
11	50MHz

Table 4F. DIVSEL_D0 Programming

00	156.25MHz
01	f_{IN}
10	125MHz
11	100MHz

Table 4G. LVCMOS_CTRL Programming

00	Output disabled
01	f_{IN}
10	125MHz
11	100MHz

Table 4H. INPUT_DIVSEL Programming

00	25MHz
01	156.25MHz
10	125MHz
11	100MHz

Table 4I. Frequency Selection Register, Output

Byte 0	Pin #	Control Function	Description	0	1	Default
Bit 0		Vendor ID				0
Bit 1		Vendor ID				0
Bit 2		DIVSEL_A(0)	Bank A Output Divider	See DIVSEL_A Table		0
Bit 3		DIVSEL_A(1)				0
Bit 4		DIVSEL_B(0)	Bank B Output Divider	See DIVSEL_B Table		0
Bit 5		DIVSEL_B(1)				0
Bit 6		DIVSEL_C(0)	Bank C Output Divider	See DIVSEL_C Table		0
Bit 7		DIVSEL_C(1)				0

Table 4J. Frequency Selection Register, Misc.

Byte1	Pin #	Control Function	Description	0	1	Default
Bit 0		DIVSEL_D0(0)	Bank D0 Output Divider	See DIVSEL_D0 Table		1
Bit 1		DIVSEL_D0(1)				1
Bit 2		LVCMOS_CTRL(0)	Bank D1 LVCMOS Output Divider and OE	See LVCMOS_CTRL Table		1
Bit 3		LVCMOS_CTRL(1)				1
Bit 4		INPUT_DIVSEL(0)	Input Mux Selection Frequency	See INPUT_DIVSEL Table		0
Bit 5		INPUT_DIVSEL(1)				0
Bit 6		IIC_ADRX_SEL	Selects IIC write address	DC (h)	DE (h)	0
Bit 7		IIC_Pin Control	Selects external pins or IIC control	external pin	IIC	0

Table 4K. Output Enable Bank A and B Register

Byte2	Pin #	Control Function	Description	0	1	Default
Bit 0		nOE QA0	Output Enable	Enable	Disable	0
Bit 1		nOE QB0	Output Enable	Enable	Disable	0
Bit 2		nOE QB1	Output Enable	Enable	Disable	0
Bit 3		nOE QB2	Output Enable	Enable	Disable	0
Bit 4		nOE QB3	Output Enable	Enable	Disable	0
Bit 5		nOE QB4	Output Enable	Enable	Disable	0
Bit 6		nOE QB5	Output Enable	Enable	Disable	0
Bit 7		N/A				

Note: unlike the external control pins, in IIC each output is individually controlled

Table 4L. Output Enable Bank C and D. Output Type Select Register

Byte3	Pin #	Control Function	Description	0	1	Default
Bit 0		nOE QC0	Output Enable	Enable	Disable	0
Bit 1		nOE QC1	Output Enable	Enable	Disable	0
Bit 2		nOE QD0	Output Enable	Enable	Disable	0
Bit 3		nOE QDO_S	Output Enable	Enable	Disable	0
Bit 4		Output Type Select QC0	LVPECL/LVDS Select	LVPECL	LVDS	0
Bit 5		Output Type Select QC1	LVPECL/LVDS Select	LVPECL	LVDS	0
Bit 6		Output Type Select QD0	LVPECL/LVDS Select	LVPECL	LVDS	0
Bit 7		N/A				

Table 4M. Output Type Select Bank A and B

Byte4	Pin #	Control Function	Description	0	1	Default
Bit 0		Output Type Select QA0	LVPECL/LVDS Select	LVPECL	LVDS	0
Bit 1		Output Type Select QB0	LVPECL/LVDS Select	LVPECL	LVDS	0
Bit 2		Output Type Select QB1	LVPECL/LVDS Select	LVPECL	LVDS	0
Bit 3		Output Type Select QB2	LVPECL/LVDS Select	LVPECL	LVDS	0
Bit 4		Output Type Select QB3	LVPECL/LVDS Select	LVPECL	LVDS	0
Bit 5		Output Type Select QB4	LVPECL/LVDS Select	LVPECL	LVDS	0
Bit 6		Output Type Select QB5	LVPECL/LVDS Select	LVPECL	LVDS	0
Bit 7		N/A				

Table 4N. Misc. Control

Byte5	Pin #	Control Function	Description	0	1	Default
Bit 0		IN_SEL	Select Xtal or mux input	Crystal	Clock	0
Bit 1		Reserved				0
Bit 2		SLEW_LVCMOS	Slew rate control for LVCMOS output	Normal	Slow	0
Bit 3		PLL_BYPASS	PLL Bypass	Active	Bypass	0
Bit 4		n_DOUBLER_EN	Turns 25MHz crystal input doubler circuit ON/OFF	ON	OFF	0
Bit 5		Reserved				0
Bit 6		Reserved				0
Bit 7		N/A				

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 8T49N4811. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, V_{DD}	3.63V
Inputs, V_I XTAL_IN Other Inputs	 0V to 2V -0.5V to V_{DDO_X} + 0.5V
Outputs, V_O (LVCMOS)	-0.5V to V_{DDO_A} + 0.5V
Outputs, V_O (LVDS) Continuous Current	10mA 15mA
Outputs, V_O (LVPECL)	-0.5V to V_{DDO_C} + 0.5V
Junction Temperature, T_J	125°C
Storage Temperature, T_{STG}	-65°C to 150°C

DC Characteristics

Table 5A. Power Supply DC Characteristics,

$V_{DD} = V_{DDA} = V_{DD\_XTAL} = V_{DD\_ODS} = V_{DD\_OA} = V_{DD\_OB} = V_{DD\_OC} = V_{DD\_OD}$ = 3.3V±10%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD_X}	Power Supply Voltage		2.97	3.3	3.63	V
V_{DDA}	Analog Supply Voltage		2.97	3.3	3.63	V
I_{DD_X}	Power Supply Current; NOTE 1			320	373	mA
I_{DDA}	Analog Supply Current			43	50	mA
I_{EE}	Core Supply Current; NOTE 2			275	326	mA

NOTE: V_{DD_X} denotes V_{DD}, V_{DD_XTAL}, V_{DD_ODS}, V_{DD_OA}, V_{DD_OB}, V_{DD_OC}, V_{DD_OD}.

NOTE: I_{DD_X} denotes I_{DD}, I_{DD_XTAL}, I_{DD_ODS}, I_{DD_OA}, I_{DD_OB}, I_{DD_OC}, I_{DD_OD}.

NOTE: Core supply voltage cannot be lower than the output supply voltage.

NOTE 1: Total power supply current with all differential outputs are set to LVDS output format and LVCMOS clock is running at 125MHz.

NOTE 2: Core power supply current with all differential outputs are set to LVPECL output format and LVCMOS clock is running at 125MHz.

Table 5B. Power Supply DC Characteristics,

$V_{DD} = V_{DDA} = V_{DD\_XTAL} = V_{DD\_ODS} = V_{DD\_OA} = V_{DD\_OB} = V_{DD\_OC} = V_{DD\_OD}$ = 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD_X}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
I_{DD_X}	Power Supply Current; NOTE 1			310	362	mA
I_{DDA}	Analog Supply Current			34	41	mA
I_{EE}	Core Supply Current; NOTE 2			251	293	mA

NOTE: V_{DD_X} denotes V_{DD}, V_{DD_XTAL}, V_{DD_ODS}, V_{DD_OA}, V_{DD_OB}, V_{DD_OC}, V_{DD_OD}.

NOTE: I_{DD_X} denotes I_{DD}, I_{DD_XTAL}, I_{DD_ODS}, I_{DD_OA}, I_{DD_OB}, I_{DD_OC}, I_{DD_OD}.

NOTE: Core supply voltage cannot be lower than the output supply voltage.

NOTE 1: Total power supply current with all differential outputs are set to LVDS output format and LVCMOS clock is running at 125MHz.

NOTE 2: Core power supply current with all differential outputs are set to LVPECL output format and LVCMOS clock is running at 125MHz.

Table 5C. LVCMOS Input DC Characteristics, V_{DD} = V_{DD_ODS} = 3.3V±10% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	Except SCLK, SDATA	V_{DD} = 3.3 V ±10%	2		V_{DD} + 0.3	V
			V_{DD} = 2.5 V ±5%	1.7		V_{DD} + 0.3	V
V_{IH}	Input High Voltage	SCLK, SDATA	V_{DD} = 3.3 V ±10%	2.4		V_{DD} + 0.3	V
			V_{DD} = 2.5 V ±5%	1.8		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3 V ±10%	-0.3		0.8	V
			V_{DD} = 2.5 V ±5%	-0.3		0.5	V
I_{IH}	Input High Current	Pullup Inputs	V_{DD} = V_{IN} = $V_{DD\ MAX}$			5	µA
		Pulldown Inputs				150	µA
I_{IL}	Input Low Current	Pullup Inputs	V_{DD} = $V_{DD\ MAX}$, V_{IN} = 0 V	-150			µA
		Pulldown Inputs		-5			µA
V_{OH}	Output High Voltage	LVCMOS Outputs	V_{DD_ODS} = 3.3V ±10%; I_{OH} = –12 mA	2.45			V
			V_{DD_ODS} = 2.5V± 5%; I_{OH} = –8 mA	1.8			V
V_{OL}	Output Low Voltage	LVCMOS Outputs	V_{DD_ODS} = 3.3V ±10%; I_{OL} = 12 mA			0.5	V
			V_{DD_ODS} = 2.5V± 5%; I_{OL} = 8 mA			0.5	V

NOTE: Core supply voltage cannot be lower than the output supply voltage.

Table 5D. Differential Input DC Characteristics, V_{DD} = 3.3V±10% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{PP}	Peak to Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.5		V_{DD} - 0.85	V
I_{IH}	Input High Current; NOTE 3	DIN, nDIN	nDIN = Open, V_{DD} = V_{IN} = $V_{DD\ MAX}$			175	µA
			DIN = Open, V_{DD} = V_{IN} = $V_{DD\ MAX}$			175	µA
I_{IL}	Input Low Current; NOTE 3	DIN, nDIN	nDIN = Open, V_{DD} = $V_{DD\ MAX}$, V_{IN} = 0 V	-225			µA
			DIN = Open, V_{DD} = $V_{DD\ MAX}$, V_{IN} = 0 V	-225			µA

NOTE: Core supply voltage cannot be lower than the output supply voltage.

NOTE 1: V_{IL} should not be less than -0.3V.

NOTE 2: Common mode input voltage is defined as the cross point.

NOTE 3: The differential inputs have internal 100Ω and biased to V_{DD} – 1.3V approximately.

Table 5E. LVPECL Output DC Characteristics, $V_{DD\_OA} = V_{DD\_OB} = V_{DD\_OC} = V_{DD\_OD}$ = 3.3V±10% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{DD_OX} –1.1		V_{DD_OX} – 0.7	V
V_{OL}	Output Low Voltage; NOTE 1		V_{DD_OX} –1.9		V_{DD_OX} – 1.6	V
V_{SWING}	Peak to Peak Output Voltage Swing		0.6		1.0	V

NOTE: V_{DD_OX} denotes V_{DD_OA}, V_{DD_OB}, V_{DD_OC}, V_{DD_OD}.
NOTE: Core supply voltage cannot be lower than the output supply voltage.
NOTE 1: Outputs terminated with 50Ω to V_{DD_OX} - 2V.

Table 5F. LVDS Output DC Characteristics, $V_{DD\_OA} = V_{DD\_OB} = V_{DD\_OC} = V_{DD\_OD}$ = 3.3V±10% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		0.25	0.325	0.454	V
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

NOTE: Core supply voltage cannot be lower than the output supply voltage.

Table 6. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of oscillation			Fundamental		
Frequency			25		MHz
Load Capacitance (C_L)			12	18	pF
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

AC Characteristics

Table 7. AC Output Characteristic.

$V_{DD} = V_{DDA} = V_{DD\_XTAL} = V_{DD\_ODS} = V_{DD\_OA} = V_{DD\_OB} = V_{DD\_OC} = V_{DD\_OD}$ = 3.3V±10% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		LVPECL, LVDS			312.5	MHz
			LVCMOS			125	MHz
t_R/t_F	Output Rise/Fall Time, Normal mode		LVPECL, LVDS; 20% - 80%		250	400	ps
			LVCMOS; 20% - 80%	150		850	ps
t_R/t_F	Output Rise/Fall Time, Slow mode		LVCMOS; 20% - 80%			2	ns
tjit(Ø)	Random Phase Jitter, RMS; NOTE 1		F_{OUT} = 50, 100, 125, 156.25, 312.5MHz, XTAL = 25MHz Integration Range: 10kHz - 20MHz		277	500	fs
			F_{OUT} = 25MHz (= f_{IN}) Crystal Input = 25MHz Integration Range: 10kHz - 5MHz		413	600	fs
f_N	Single-Side Band Phase Noise		156.25MHz, Offset 1kHz		-120		dBc/Hz
			156.25MHz, Offset 10kHz		-130		dBc/Hz
			156.25MHz, Offset 100kHz		-133		dBc/Hz
			156.25MHz, Offset 1MHz		-145		dBc/Hz
			156.25MHz, Offset 10MHz		-154		dBc/Hz
PSNR	Power Supply Noise Rejection	V_{DD}	50mVpp, 10k-1.5MHz		-61		dBc
		V_{DDA}	50mVpp, 10k-1.5MHz		-60		dBc
		V_{DD_Ox}	50mVpp, 10k-1.5MHz		-50		dBc
odc	Output Duty Cycle; NOTE 2		LVPECL, LVDS	48		52	%
			LVCMOS	45		55	%
t_{LOCK}	PLL Lock Time		Startup (Default Configuration Power-on Reset)		15		ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions

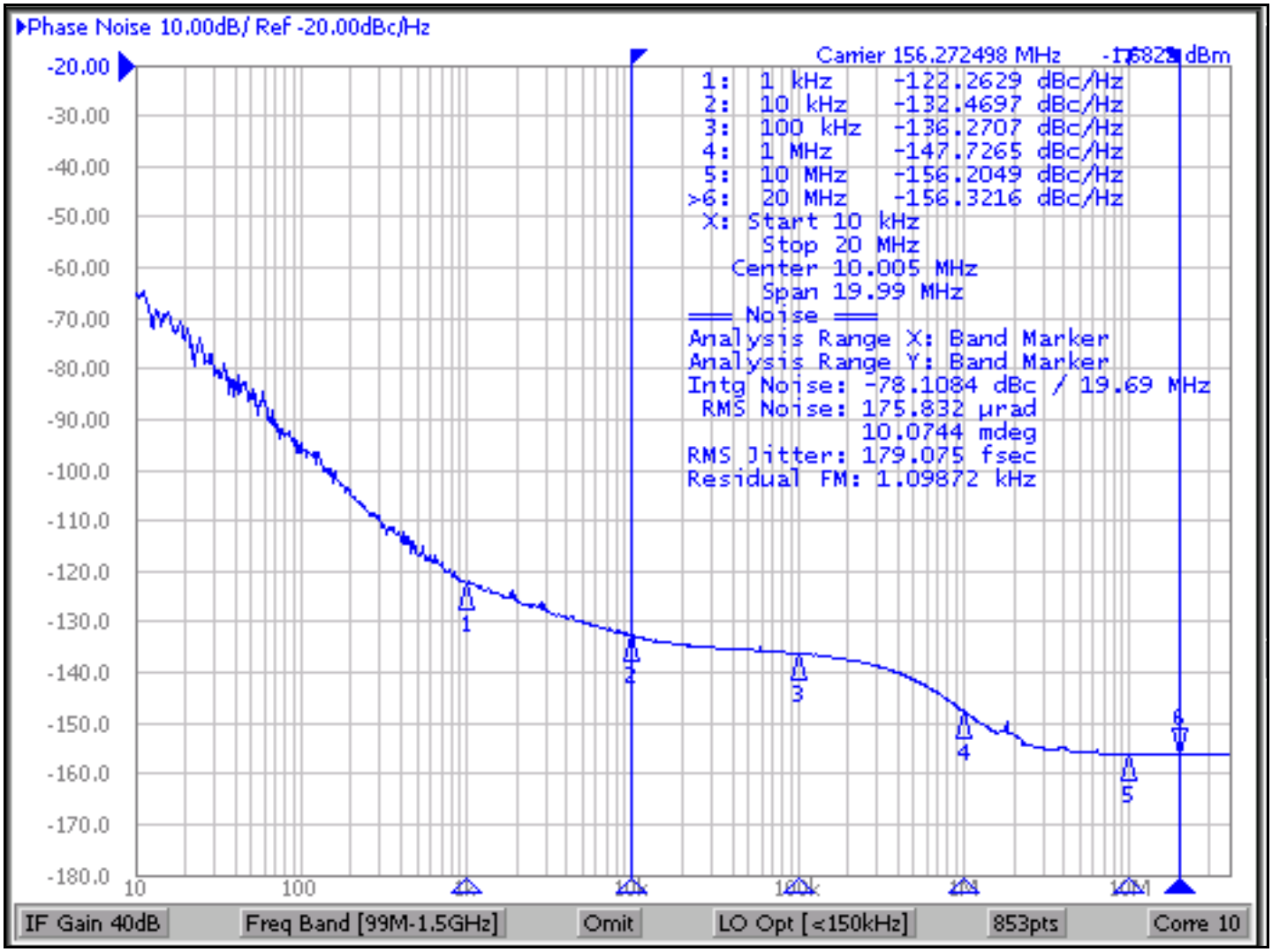
NOTE: V_{DD_OX} denotes V_{DD_OA}, V_{DD_OB}, V_{DD_OC}, V_{DD_OD}, V_{DD_ODS}.

NOTE: Core supply voltage cannot be lower than the output supply voltage.

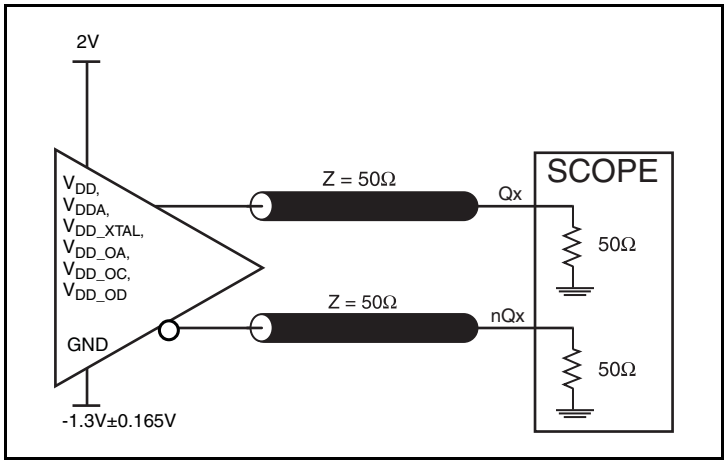
NOTE 1: QDO_S LVCMOS output is set to 125MHz. See Phase Noise plot on next page.

NOTE 2: In PLL Mode.

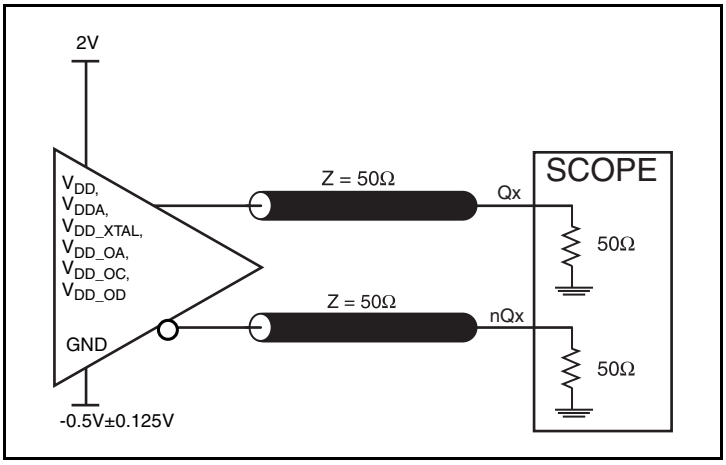
Typical Phase Noise at 156.25MHz (10kHz - 20MHz)



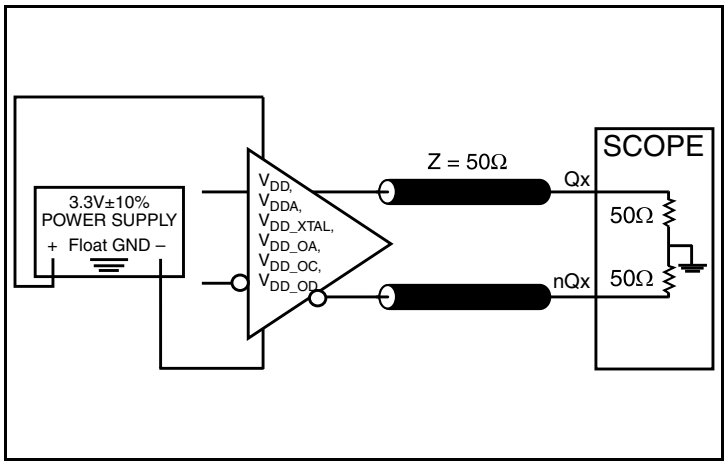
Parameter Measurement Information



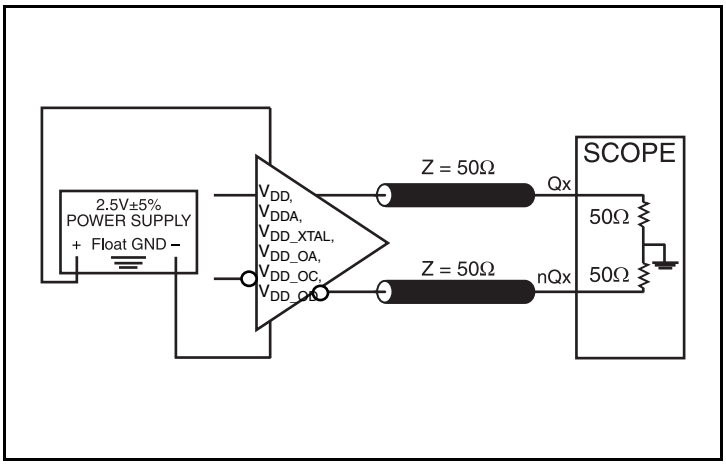
3.3V Core/3.3V LVPECL Output Load Test Circuit



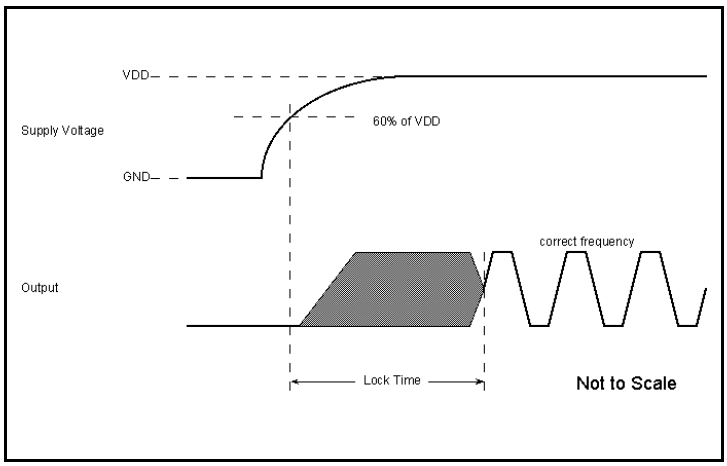
2.5V Core/2.5V LVPECL Output Load Test Circuit



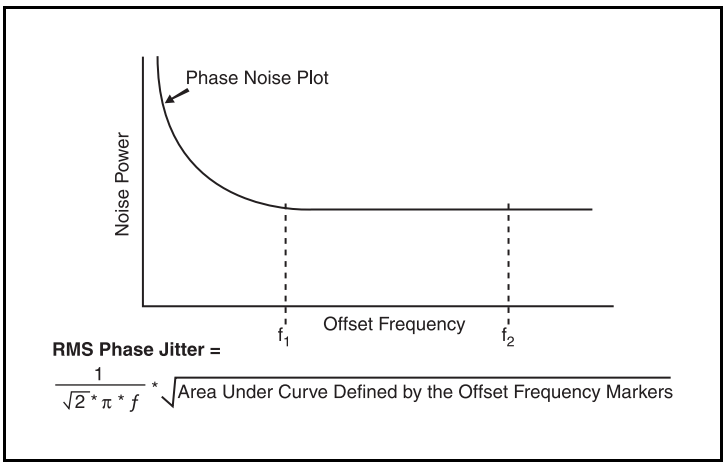
3.3V Core/3.3V LVDS Output Load Test Circuit



2.5V Core/2.5V LVDS Output Load Test Circuit

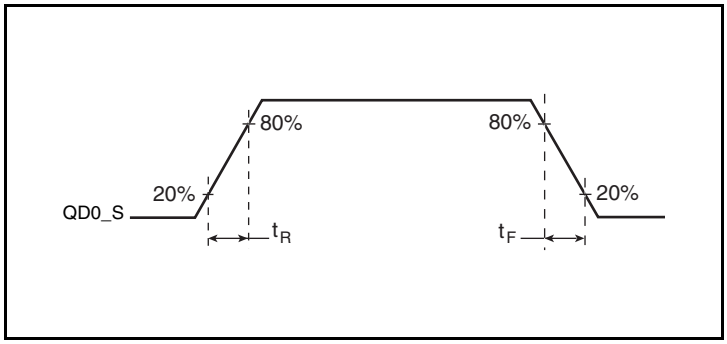


PLL Lock Time

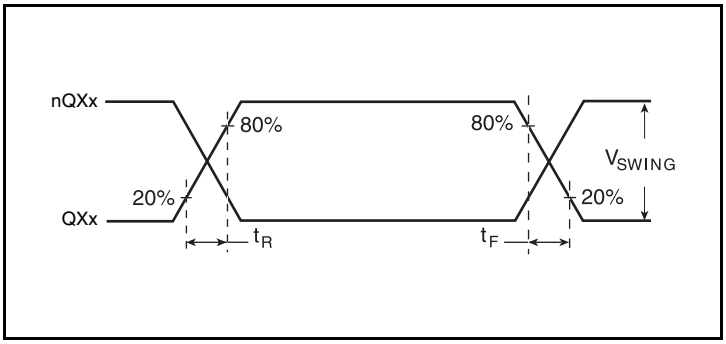


RMS Phase Jitter

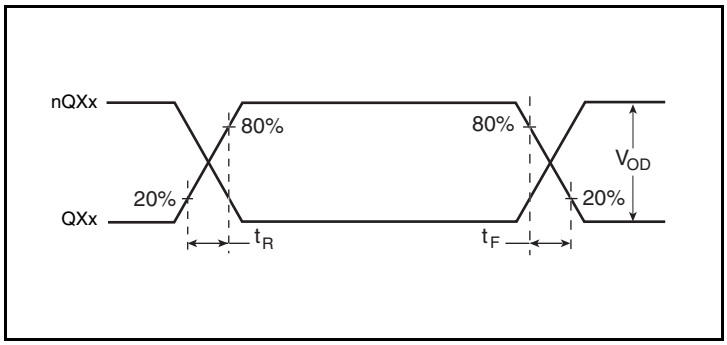
Parameter Measurement Information, continued



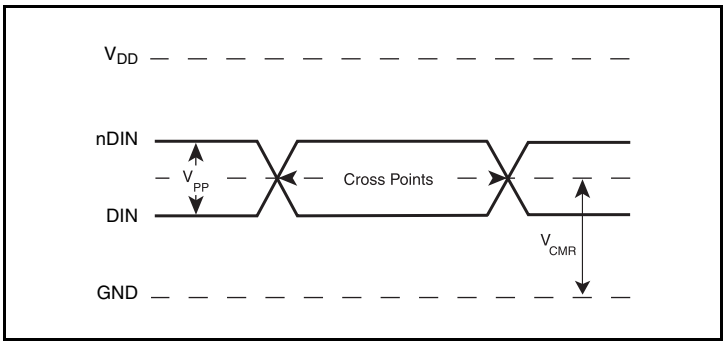
LVCMOS Output Rise/Fall Time



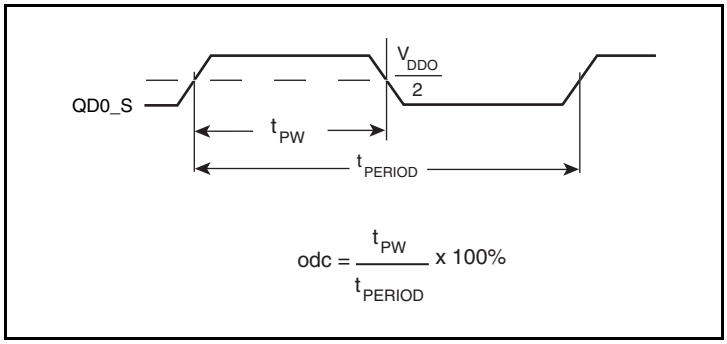
LVPECL Output Rise/Fall Time



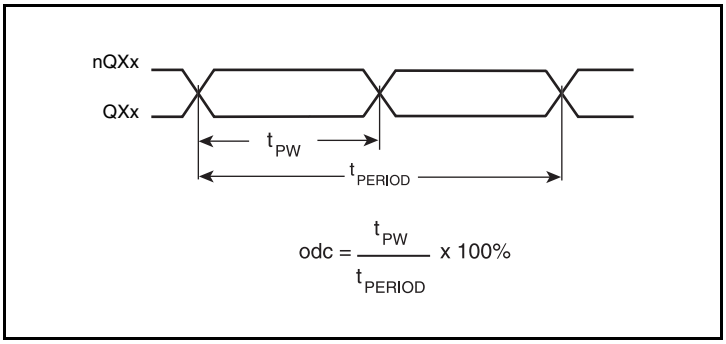
LVDS Output Rise/Fall Time



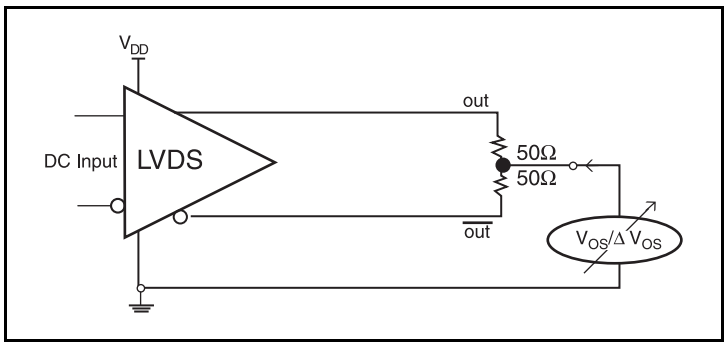
Differential Input Levels



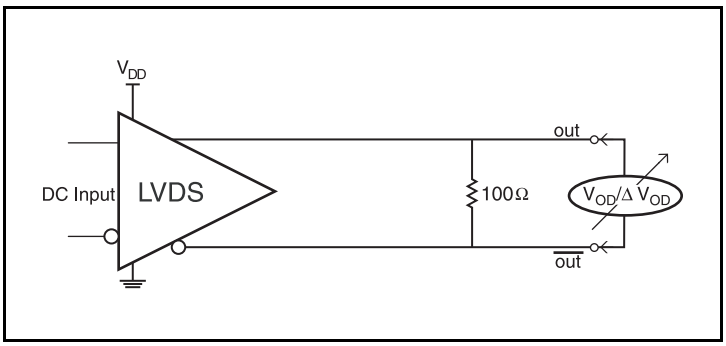
LVCMOS Output Duty Cycle/Output Pulse Width/Period



Differential Output Duty Cycle/Output Pulse Width/Period



Offset Voltage Setup



Differential Output Voltage Setup

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

DIN/nDIN Input

If the input buffer is not used, then connect DIN input to VDD and nDIN input to GND via 1kΩ resistors

XTAL Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS Control Pins

Some control pins have internal pullup or pulldown resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating there should be no trace attached.

LVCMOS Outputs

If the LVCMOS output is not used, then disable the output using control pin

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 1A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 1B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

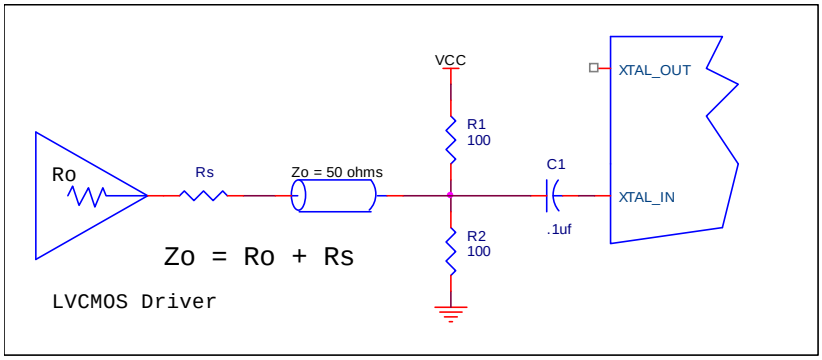


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

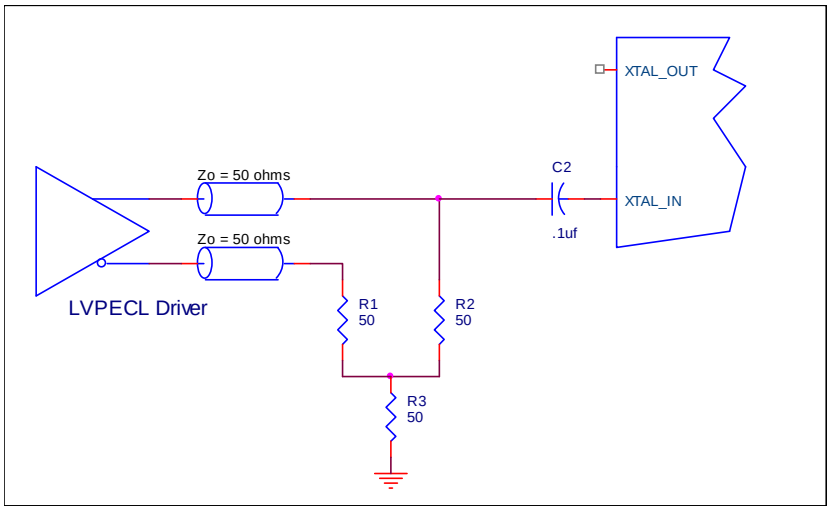


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 2A* can be used with either type of output structure. *Figure 2B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

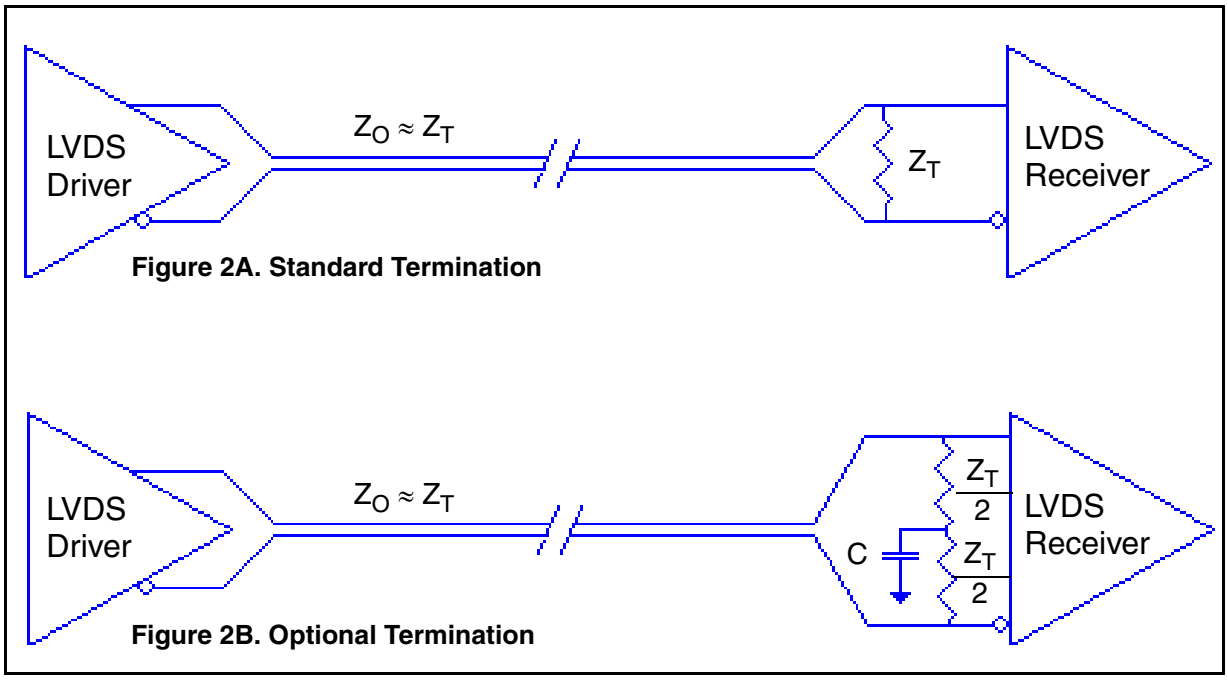


Figure 2A. Standard Termination

Figure 2B. Optional Termination

LVDS Termination

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figure 3A* and *Figure 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

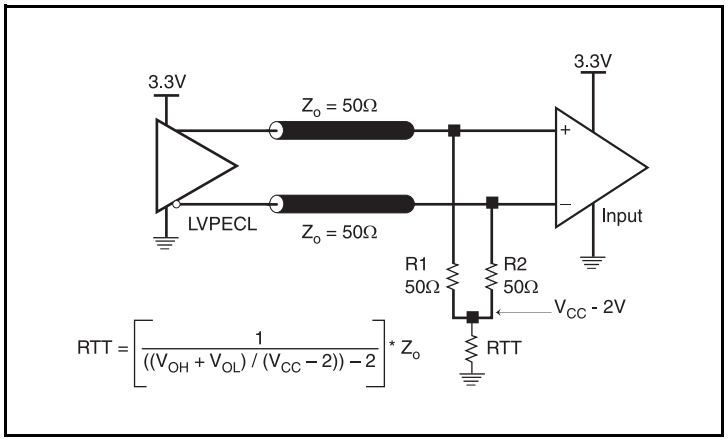


Figure 3A. 3.3V LVPECL Output Termination

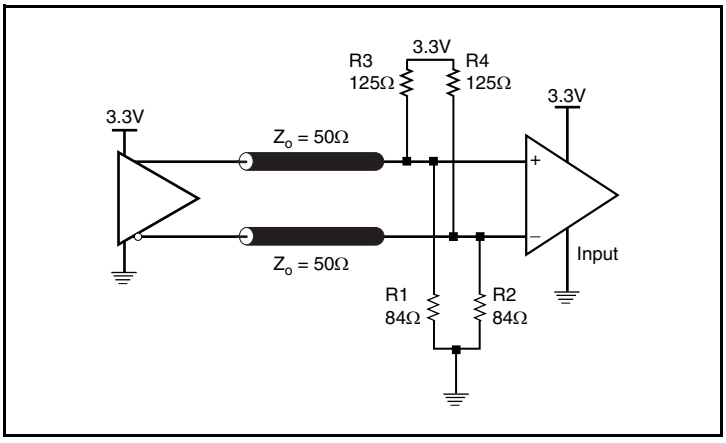


Figure 3B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 4A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{DDO} – 2V. For V_{DDO} = 2.5V, the V_{DDO} – 2V is very close to ground level. The R3 in *Figure 4B* can be eliminated and the termination is shown in *Figure 4B.*

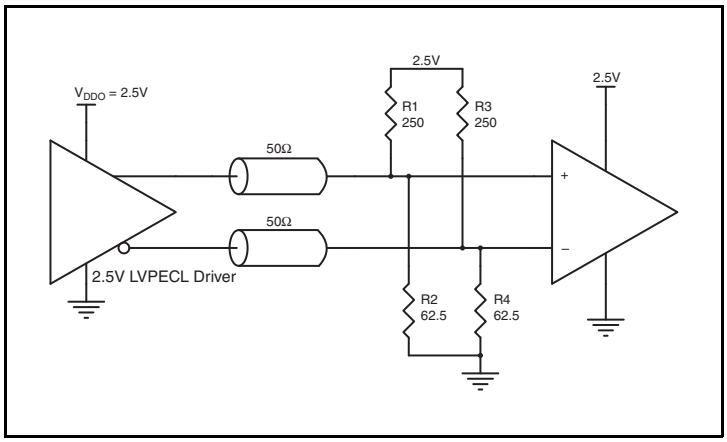


Figure 4A. 2.5V LVPECL Driver Termination Example

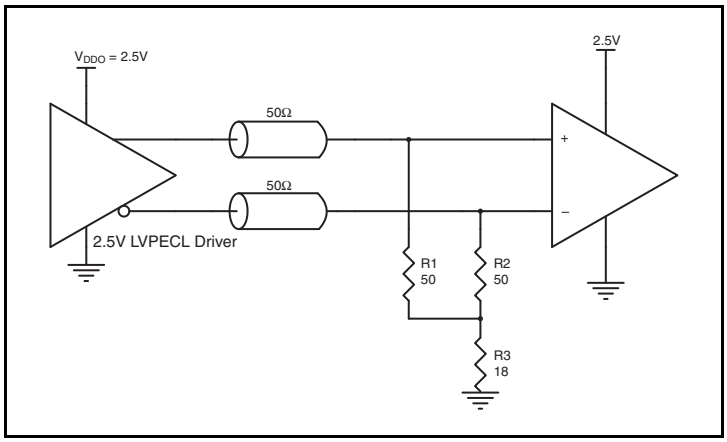


Figure 4B. 2.5V LVPECL Driver Termination Example

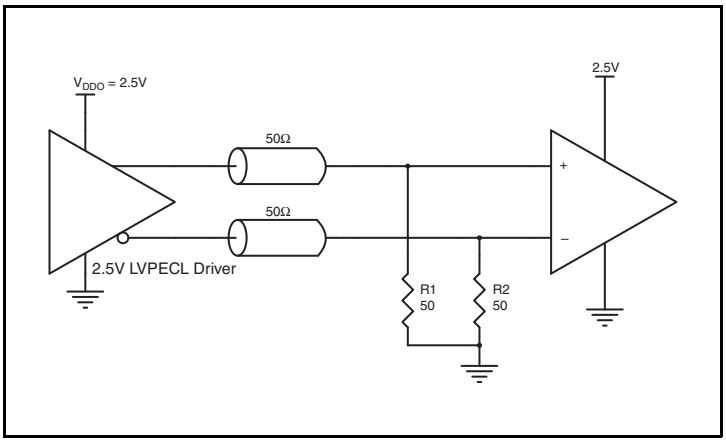


Figure 4C. 2.5V LVPECL Driver Termination Example

Schematic Example

Figure 5 (next page) shows an example 8T49N4811 application schematic in which the device is operated at V_{DD} = 3.3V.

This example focuses on functional connections and is not configuration specific. To illustrate the three level input control pins to configure the output banks, QA_CTRL and QB_CTRL0 are pulled to a logic 1 to enable LVDS outputs for Bank A and the first half of BankB, QB_CTRL1 is a No Connect to place the second half of Bank B into TriState and QC_CTRL and QD_CTRL are pulled to a logic 0 for enabled LVPELC outputs. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set for the application.

The 12pF parallel resonant Fox FX325BS 25MHz crystal is used with tuning capacitors C1 = C2 = 10pF recommended for frequency accuracy. Crystals with other load capacitance specifications can be used, for example, a CL=18pF crystal can be used with two 22pF tuning capacitors. Depending on the parasitics of the printed circuit board layout, the values of C1 and C2 might require a slight adjustment to optimize the frequency accuracy. For this device, the crystal tuning capacitors are required for proper operation.

Crystal layout is very important to minimize capacitive coupling between the crystal pads and leads and other metal in the circuit board. Capacitive coupling to other conductors has two adverse effects; it reduces the oscillator frequency leaving less tuning margin and noise coupling from power planes and logic transitions on signal traces can pull the phase of the crystal resonance, inducing jitter. Routing I^2C under the crystal is a very common layout error, based on the assumption that it is a low frequency signal and will not affect the crystal oscillation. In fact, I^2C transition times are short enough to capacitively couple into the crystal if they are routed close enough to the crystal traces.

In layout, all capacitive coupling to the crystal from any signal trace is to be minimized, that is to the XTAL_IN and XTAL_OUT pins, traces to the crystal pads, the crystal pads and the tuning capacitors. Using a crystal on the top layer as an example, void all signal and power layers under the crystal connections between the top layer and the ground plane used by the 8T49N4811. Then calculate the parasitic capacity to the ground and determine if it is large enough to preclude tuning the oscillator. If the coupling is excessive, particularly if the first layer under the crystal is a ground plane, a layout option is to void the ground plane and all deeper layers until the next ground plane is reached. The ground connection of the tuning capacitors should first be made between the capacitors on the top layer, then a single ground via is dropped to connect the tuning cap ground to the ground plane as close to the 8T49N4811 as possible as shown in the schematic.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8T49N4811 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µf capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10 kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

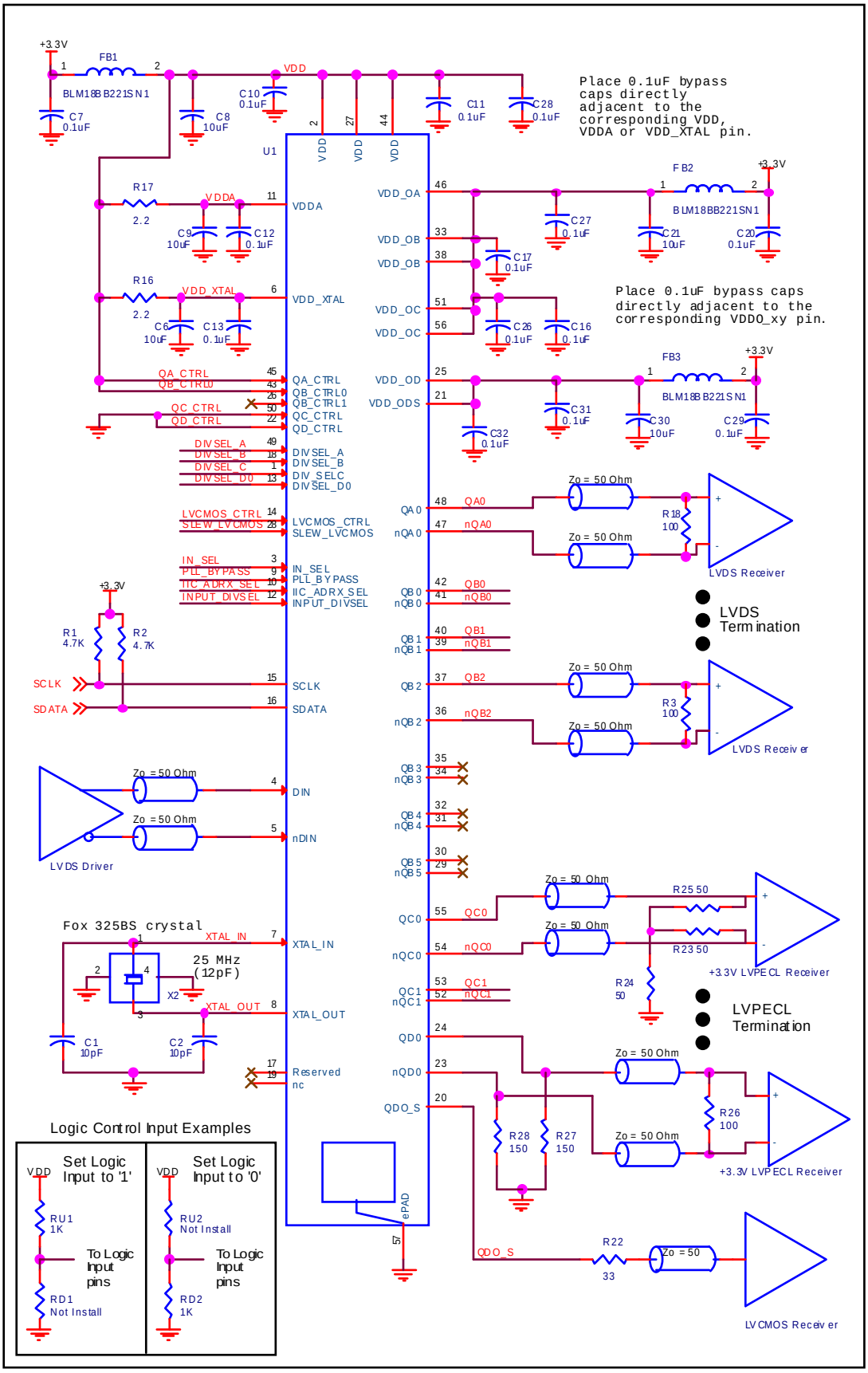


Figure 5. 8T49N4811 Schematic Example

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

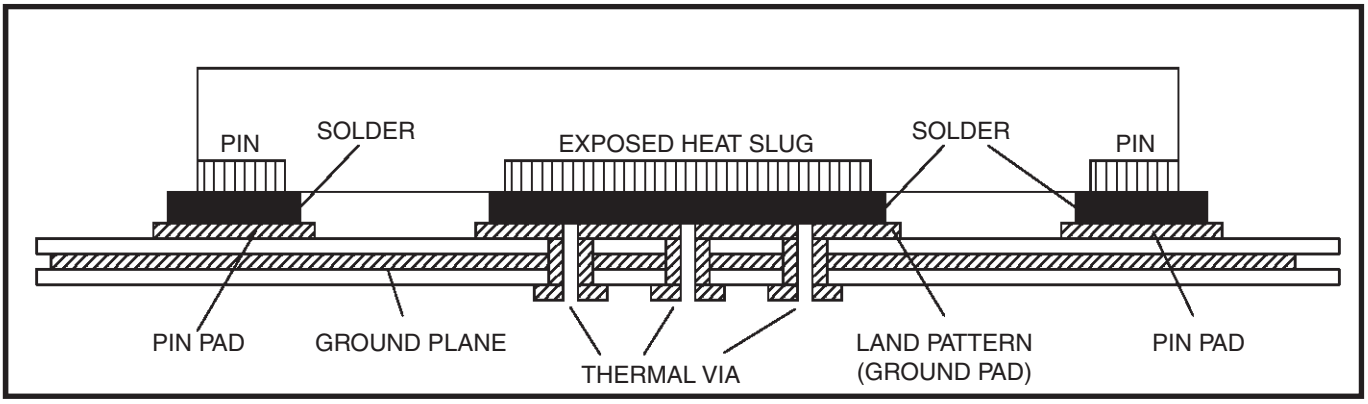


Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

LVPECL Power Considerations

This section provides information on power dissipation and junction temperature for the 8T49N4811.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8T49N4811 is the sum of the core power plus the power dissipated due to loading.
The following is the power dissipation for V_{DD} = 3.63V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to loading.

- Power (core)$_{MAX}$ = V_{DD_MAX} * I_{EE_MAX} = 3.63V * 326mA = **1183.38mW**
  NOTE: The current includes LVCMOS output running at 125MHz, ac-coupled and terminated.
- Power (outputs)$_{MAX}$ = **31mW/Loaded Output pair**
  If all outputs are loaded, the total power is 10 * 31mW = **310mW**
- Dynamic Power Dissipation at 125MHz
  Power (125MHz) = C_{PD} * Frequency * $(V_{DDO})^2$ = 18.1pF * 125MHz * $(3.63V)^2$ = **29.81mW per output**
- **Total Power**$_{\_MAX}$ (3.63V, with all outputs switching) = 1183.38W + 310mW + 29.81mW = **1523.19mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 25.6°C/W per Table 8 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.523W * 25.6°C/W = 124°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 8. Thermal Resistance θ_{JA} for 56-Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	25.6°C	19.8°C	18°C

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 7.*

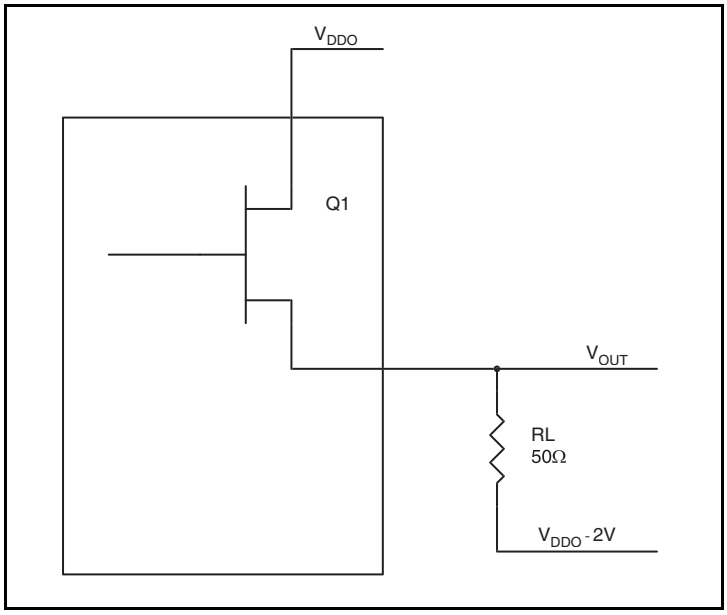


Figure 7. LVPECL Driver Circuit and Termination

To calculate power dissipation per output pair due to loading, use the following equations which assume a 50Ω load, and a termination voltage of V_{DD} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = V_{DD\_MAX}$ **– 0.7V**
  $(V_{DD\_MAX} – V_{OH\_MAX})$ = **0.7V**
- For logic low, $V_{OUT} = V_{OL\_MAX} = V_{DD\_MAX}$ **– 1.6V**
  $(V_{DD\_MAX} – V_{OL\_MAX})$ = **1.6V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{DD\_MAX} – 2V))/R_L] * (V_{DD\_MAX} – V_{OH\_MAX}) = [(2V – (V_{DD\_MAX} – V_{OH\_MAX}))/R_L] * (V_{DD\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.7V)/50Ω] * 0.7V =$ **18.2mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{DD\_MAX} – 2V))/R_L] * (V_{DD\_MAX} – V_{OL\_MAX}) = [(2V – (V_{DD\_MAX} – V_{OL\_MAX}))/R_L] * (V_{DD\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.6V)/50Ω] * 1.6V =$ **12.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **31mW**

LVDS Power Considerations

This section provides information on power dissipation and junction temperature for the 8T49N4811 for all outputs that are configured to LVDS. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8T49N4811 the sum of the core power plus the power dissipated due to loading. The following is the power dissipation for V_{DD} = 3.3V + 10% = 3.63V, which gives worst case results.

- The maximum current at 85°C is as follows: I_{DD_MAX} = 373mA, I_{DDA_MAX} = 43mA
- Dynamic Power Dissipation at 125MHz, (D1 LVCMOS output)
  Dynamic_Power(D1) = CPD * Frequency * $V_{DD\_ODS}^2$ = 18.1pF * 125MHz * 3.63V^2 = **29.81mW**
- **Total Power$_{_MAX}$** = (3.63V * (373mA + 43mA)) + Dynamic_Power(D1) = 1510.08mW + 29.81mW = **1539.89mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 25.6°C/W per Table 9 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.540W * 25.6°C/W = 124.4°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 9. Thermal Resistance θ_{JA} for 56-Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	25.6°C/W	19.8°C/W	18°C/W

Reliability Information

Table 10. θ_{JA} vs. Air Flow Table for a 56-Lead VFQFN

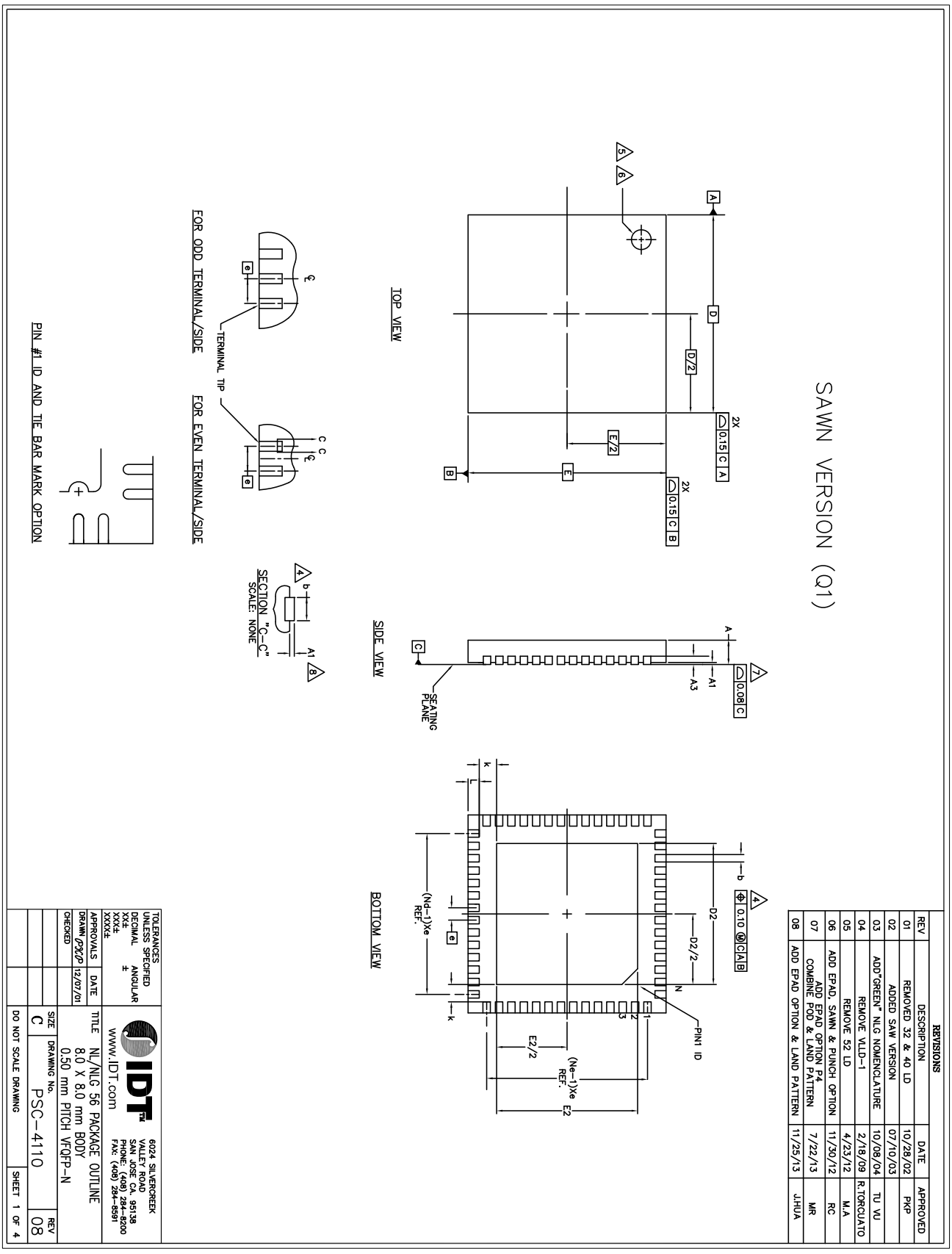
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	25.6°C/W	19.8°C/W	18°C/W

NOTE: Theta JA (θ_{JA}) values calculated using a 4-layer JEDEC PCB (114.3mm x 101.6mm), with 2oz. (70μm) copper plating on all four layers.

Transistor Count

The transistor count for 8T49N4811 is: 177,252

56-Lead VFQFN NL Package Outline



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
01	REMOVED 32 & 40 LD	10/28/02	PKP
02	ADDED SAW VERSION	07/10/03	
03	ADD"GREEN" NLG NOMENCLATURE	10/08/04	TU VU
04	REMOVE VLLD-1	2/18/09	R.TORCUATO
05	REMOVE 52 LD	4/23/12	M.A
06	ADD EPAD, SAWN & PUNCH OPTION	11/30/12	RC
07	ADD EPAD OPTION P4 COMBINE POD & LAND PATTERN	7/22/13	MR
08	ADD EPAD OPTION & LAND PATTERN	11/25/13	J.HUA

EPAD OPTION

SYMBOL	P1			P2			P3			P4		
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
E2	6.15	6.30	6.45	6.45	6.60	6.75	5.05	5.20	5.35	5.80	5.90	6.00
D2	6.15	6.30	6.45	6.45	6.60	6.75	4.35	4.50	4.65	5.80	5.90	6.00

8T49N4811 USES EPAD OPTION P4

SYMBOL	P5		
	MIN	NOM	MAX
E2	5.95	6.05	6.15
D2	5.95	6.05	6.15

COMMON DIMENSION

SYMBOL	DIMENSION			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		56		2
Nd		14		2
Ne		14		2
L	0.30	0.40	0.50	
b	0.18	0.25	0.30	4
D2		SEE EPAD OPTION		
E2		SEE EPAD OPTION		
A	0.80	0.9	1.00	
A1	0.00	0.02	0.05	
A3		0.20 REF.		
D		8.00 BSC		
E		8.00 BSC		
θ	–	–	12°	
k	0.20	–	–	

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. APPLIED TO EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY FOR TERMINALS.
9. NOT AN ACTUAL IO.

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX± ANGULAR ±

APPROVALS	DATE
DRAWN PSC/P	12/07/01
CHECKED	

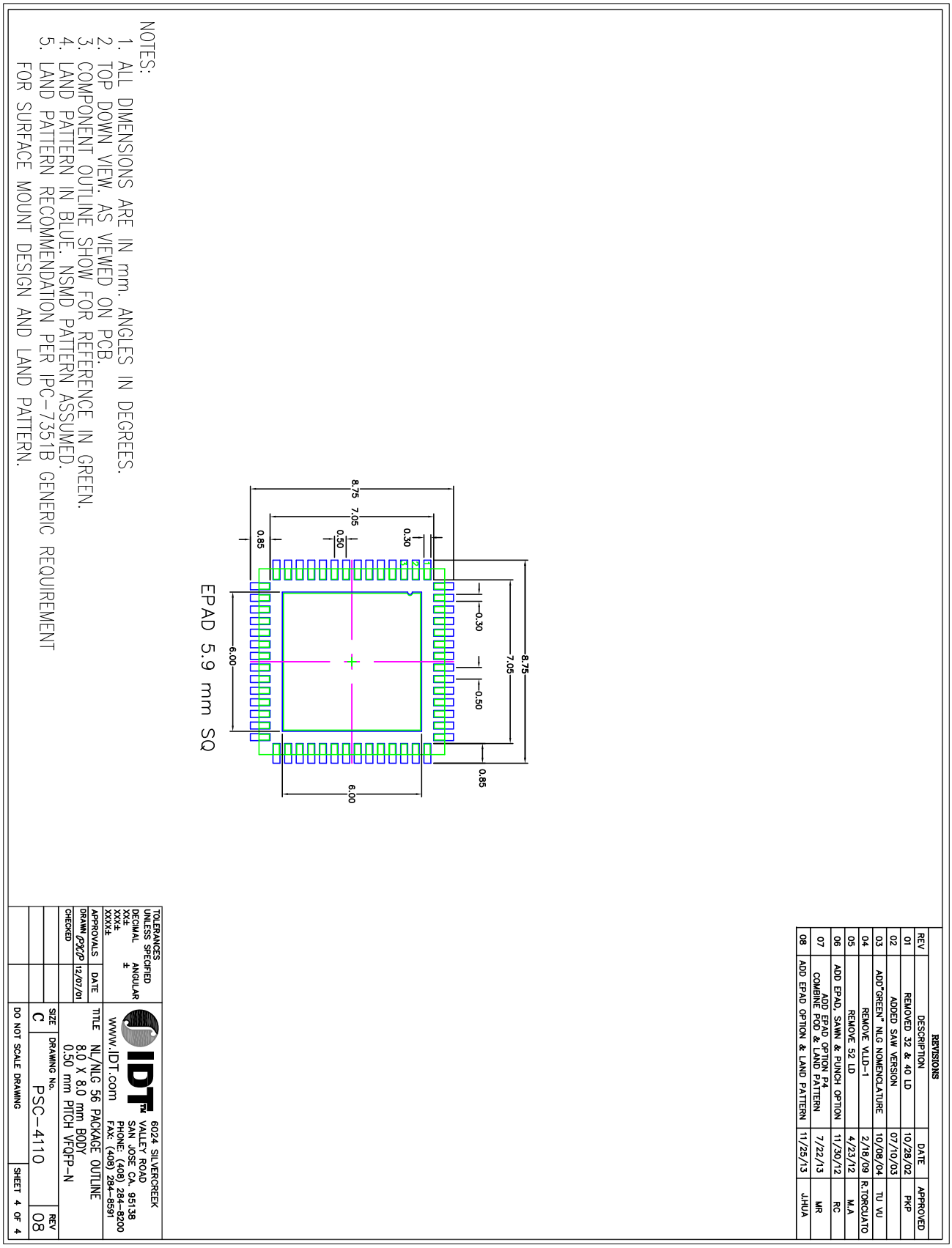
IDT™ www.IDT.com
6024 SILVERCREEK VALLEY ROAD
SAN JOSE CA. 95138
PHONE: (408) 284–8200
FAX: (408) 284–8591

TITLE NL/NLG 56 PACKAGE OUTLINE
8.0 X 8.0 mm BODY
0.50 mm PITCH VFQFP–N

SIZE	DRAWING No.	REV
C	PSC–4110	08

DO NOT SCALE DRAWING | SHEET 3 OF 4

56-Lead VFQFN NL Package Outline, continued



Ordering Information

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T49N4811NLGI	IDT8T49N4811NLGI	“Lead-Free” 56-Lead VFQFN	Tray	-40°C to +85°C
8T49N4811NLGI8	IDT8T49N4811NLGI	“Lead-Free” 56-Lead VFQFN	Tape & Reel	-40°C to +85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T5A & T5B	10	Datasheet error updated for I_{DDA} specification. I_{EE} is accurate and is inclusive of I_{DDA}. No changes to manufacturing test specification. Updated data sheet format.	3/30/15
B	T7	13 14	AC Characteristics Table - added maximum specs for *Random Phase Jitter, RMS.* Replaced *Typical Phase Noise* plot. Deleted “IDT” prefix and “I” suffix from part number.	11/12/15

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