

## Description

The F2976 is a single-pole double-throw (SP2T) reflective RF switch featuring high linearity and wide bandwidth. This device is optimized from 5MHz to 1.8GHz to support downstream cable modem future migration for DOCSIS 3.1 applications, and operates at up to 10GHz to support a multitude of wireless RF applications. Superb performance is achieved when used in either 50Ω or 75Ω terminating impedance applications.

The F2976 uses a single positive supply voltage of either +3.3V or +5.0V and is compatible with either 1.8V or 3.3V control logic.

## Competitive Advantage

The F2976 provides extremely low insertion loss across the entire bandwidth while providing superb distortion performance.

- Optimized for DOCSIS 3.1 applications up to 1.8GHz
- Optimized for Wi-Fi applications up to 5.9GHz
- Low insertion loss
- High isolation
- Fast switching
- No external matching required

## Typical Applications

- Broadband Cable DOCSIS 3.0 / 3.1
- Set top box
- CATV filter bank switching
- Wi-Fi
- Cellular BTS
- General purpose

## General Features

- Supply voltage: +2.5V to +5.25V
- 1.8V and 3.3V compatible control logic
- 2mm x 2mm, 12-pin TQFN package
- -40°C to +105°C operating temperature range

## Features (75Ω)

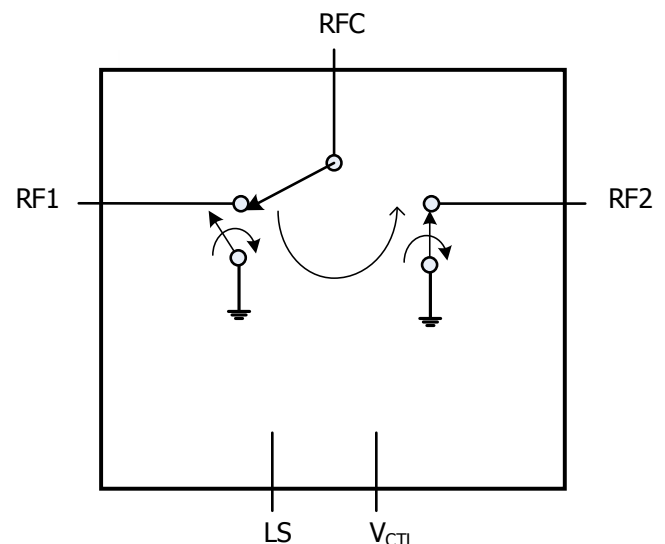
- Low insertion loss:
  - 0.23dB at 204MHz
  - 0.34dB at 1.8GHz
- High Isolation: 40dB at 1.8GHz
- P0.1dB compression of +37dBm at 204MHz
- Second Harmonic: -100dBc at 204MHz
- Third Harmonic: -120dBc at 204MHz
- Composite Second Order Distortion > 100dBc
- Composite Triple Beat Distortion > 100dBc

## Features (50Ω)

- Low insertion loss:
  - 0.40dB at 2.4GHz
  - 0.55dB at 8GHz
- High Isolation:
  - 34dB at 2.4GHz
- High Linearity:
  - IIP2 +125dBm at 2.4GHz
  - IIP3 +77dBm at 2.4GHz
- P0.1dB compression of +40dBm at 2.4GHz
- Second Harmonic: -100dBc at 2.4GHz
- Third Harmonic: -110dBc at 2.4GHz

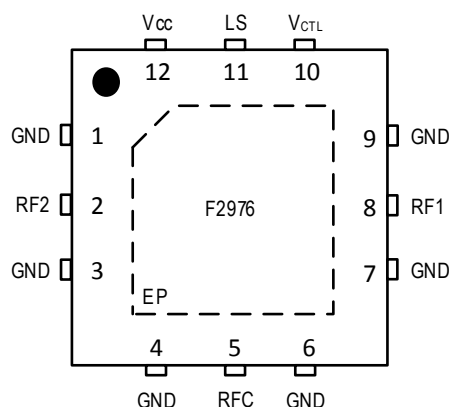
## Block Diagram

Figure 1. Block Diagram



## Pin Assignments

**Figure 2. Pin Assignments for 2mm x 2mm x 0.5mm 12-pin TQFN, NEG12 – Top View**



## Pin Descriptions

**Table 1. Pin Descriptions**

Number	Name	Description
1	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
2	RF2	RF2 Port. If this pin is not 0V DC, then an external coupling capacitor must be used.
3	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
4	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
5	RFC	RF Common Port. If this pin is not 0V DC, then an external coupling capacitor must be used.
6	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
7	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
8	RF1	RF1 Port. If this pin is not 0V DC, then an external coupling capacitor must be used.
9	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
10	V <sub>CTL</sub>	Logic control pin (see Table 9).
11	LS	Truth Table select pin. Defines V <sub>CTL</sub> logic for RF switching (see Table 9). Pin is internally pulled up to 2.5V through a 500kΩ resistor.
12	V <sub>CC</sub>	Power supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.
	EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

## Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 2. Absolute Maximum Ratings**

Parameter		Symbol	Minimum	Maximum	Units
$V_{CC}$ to GND		$V_{CC}$	-0.3	+5.5	V
$V_{CTL}$ , LS		$V_{LOGIC}$	-0.3	Lower of ( $V_{CC} + 0.3$ , 3.9)	V
RF1, RF2, RFC		$V_{RF}$	-0.3	+0.3	V
Maximum Input CW Power, 50 $\Omega$ , $T_{EP} = 25^{\circ}\text{C}$ , $V_{CC} = 5.25\text{V}$ (any port, insertion loss state) [a, b]	$5\text{MHz} \leq f_{RF} \leq 10\text{MHz}$	$P_{ABSCW1}$		30	dBm
	$10\text{MHz} < f_{RF} \leq 25\text{MHz}$	$P_{ABSCW2}$		32	
	$25\text{MHz} < f_{RF} \leq 200\text{MHz}$	$P_{ABSCW3}$		33	
	$200\text{MHz} < f_{RF} \leq 6000\text{MHz}$	$P_{ABSCW4}$		34	
	$f_{RF} > 6000\text{MHz}$	$P_{ABSCW5}$		33	
Maximum Peak Power, 50 $\Omega$ , $T_{EP} = 25^{\circ}\text{C}$ , $V_{CC} = 5.25\text{V}$ (any port, insertion loss state) [a, b, c]	$5\text{MHz} \leq f_{RF} \leq 10\text{MHz}$	$P_{ABSPK1}$		35	dBm
	$10\text{MHz} < f_{RF} \leq 25\text{MHz}$	$P_{ABSPK2}$		37	
	$25\text{MHz} < f_{RF} \leq 200\text{MHz}$	$P_{ABSPK3}$		38	
	$200\text{MHz} < f_{RF} \leq 6000\text{MHz}$	$P_{ABSPK4}$		39	
	$f_{RF} > 6000\text{MHz}$	$P_{ABSPK5}$		38	
Maximum Junction Temperature		$T_{JMAX}$		+140	$^{\circ}\text{C}$
Storage Temperature Range		$T_{ST}$	-65	+150	$^{\circ}\text{C}$
Lead Temperature (soldering, 10s)		$T_{LEAD}$		+260	$^{\circ}\text{C}$
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)		$V_{ESDHBM}$		2500 (Class 2)	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)		$V_{ESDCDM}$		1000 (Class C3)	V

- a. In a 50 $\Omega$  system,  $\text{dBmV} = \text{dBm} [50\Omega] + 47$ .  
In a 75 $\Omega$  system,  $\text{dBmV} = \text{dBm} [75\Omega] + 48.75$ .
- b.  $T_{EP}$  = Temperature of the exposed paddle.
- c. 5 % duty cycle of a 4.6ms period.

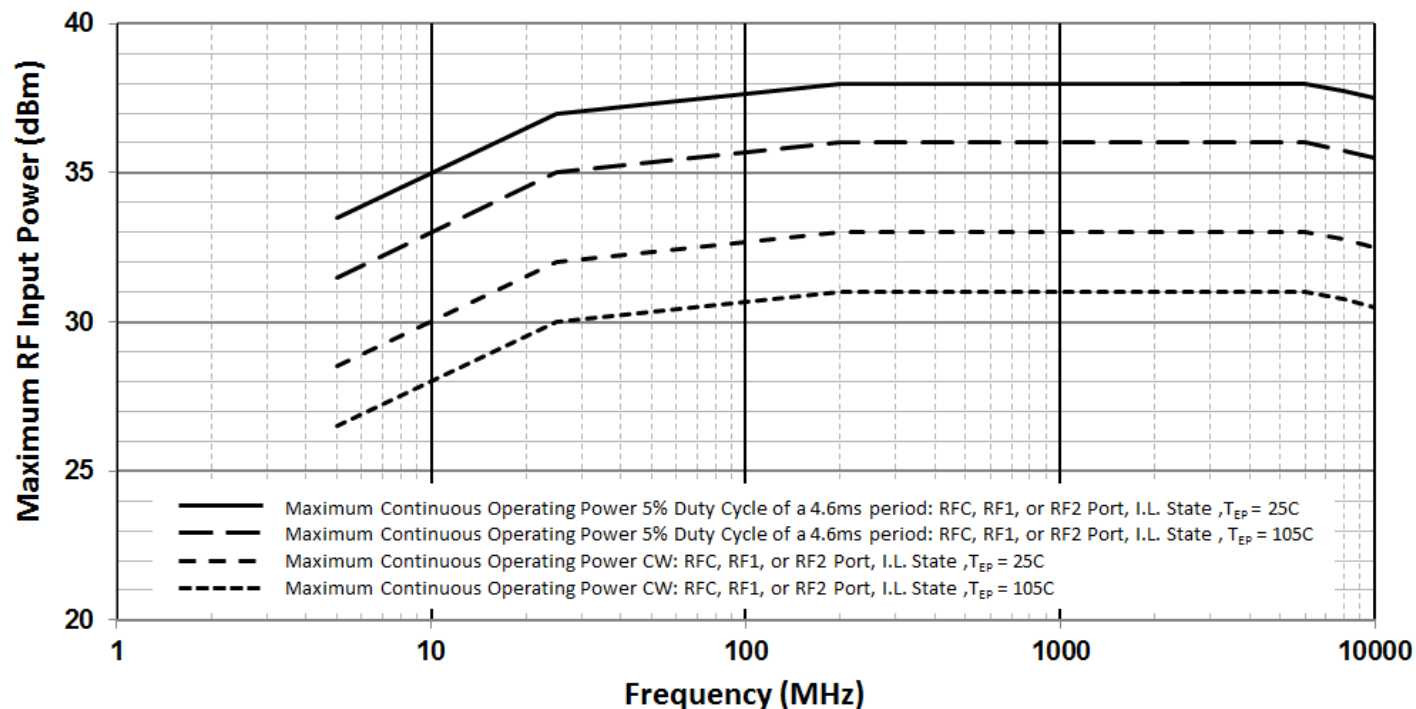
# Recommended Operating Conditions

**Table 3. Recommended Operating Conditions**

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Supply Voltage	$V_{CC}$		2.5	3.3	5.25	V
Operating Temperature Range	$T_{EP}$	Exposed Paddle	-40		+105	°C
RF Frequency Range	$f_{RF}$	75Ω	0.005		1.8	GHz
		50Ω	0.005		10	
Maximum Operating Input Power	$P_{MAX}$	Insertion Loss State $Z_S = Z_L = 50\Omega$			See Figure 3 [a]	dBm
Port Impedance (RFC, RF1, RF2)	$Z_{RF}$	75Ω System		75		Ω
		50Ω System		50		

a. In a 50Ω system, dBmV = dBm [50Ω] + 47. In a 75Ω system, dBmV = dBm [75Ω] + 48.75.

**Figure 3. Maximum Operating RF Input Power ( $Z_S = Z_L = 50\Omega$ )**



## General Specifications

**Table 4. General Specifications**

See F2976 Typical Application Circuit. Specifications apply when operated with  $V_{CC} = +3.3V$ ,  $T_{EP} = +25^{\circ}C$ , LS = HIGH, single tone signal applied at RF1 or RF2 and measured at RFC, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input High Threshold	$V_{IH}$	$V_{CTL}$ , LS pins	1.17 [b]		Lower of ( $V_{CC}$ , 3.6)	V
Logic Input Low Threshold	$V_{IL}$	$V_{CTL}$ , LS pins	-0.3		0.6	V
Logic Current	$I_{IH}$ , $I_{IL}$	$V_{CTL}$ , LS pins (each pin)	<b>-10</b> [a]		<b>+10</b>	$\mu A$
DC Current ( $V_{CC}$ )	$I_{CC}$			80	<b>150</b>	$\mu A$
Switching Rate	$SW_{RATE}$				25	kHz
Maximum Video Feed-Through, RFC Port	$VID_{FT}$	Peak transient during switching. $Z_S = Z_L = 75\Omega$ . Measured with 20ns rise time, 0V to 3.3V (3.3V to 0V) control pulse applied to $V_{CTL}$ .		5		mVp-p
Switching Time [c]	$SW_{TIME}$	50% $V_{CTL}$ to 90% or 10% RF		1.5	3	$\mu s$

- Items in min/max columns in **bold italics** are guaranteed by test.
- Items in min/max columns that are not bold italics are guaranteed by design characterization.
- Measured at  $f_{RF} = 1GHz$ .

## Electrical Characteristics

**Table 5. Electrical Characteristics - 75Ω SPECIFICATION**

See F2976 75Ω Application Circuit. Specifications apply when operated with  $V_{CC} = +3.3V$ ,  $T_{EP} = +25^{\circ}C$ .  $Z_S = Z_L = 75\Omega$ , LS = HIGH, single tone signal applied at RF1 or RF2 and measured at RFC, EVKit trace and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Insertion Loss (RFC to RF1, RF2)	IL	$f_{RF} = 5MHz$		0.20		dB
		$5MHz < f_{RF} \leq 204MHz$		0.23	0.43 [b]	
		$204MHz < f_{RF} \leq 1.2GHz$		0.32	0.52	
		$1.2GHz < f_{RF} \leq 1.8GHz$		0.34	0.54	
Isolation (All Paths)	ISO1	$f_{RF} = 5MHz$		77		dB
		$5MHz < f_{RF} \leq 204MHz$		60		
		$204MHz < f_{RF} \leq 1.2GHz$		44		
		$1.2GHz < f_{RF} \leq 1.8GHz$		40		
Return Loss (RFC, RF1, RF2) (Insertion Loss States)	RL	$f_{RF} = 5MHz$		35		dB
		$5MHz < f_{RF} \leq 204MHz$		30		
		$204MHz < f_{RF} \leq 1.2GHz$		17		
		$1.2GHz < f_{RF} \leq 1.8GHz$		16		
2 <sup>nd</sup> Harmonic	H2	$f_{IN} = 27MHz$ $P_{OUT} = 20dBm$ [c]		-80	-70	dBc
		$f_{IN} = 204MHz$ $P_{OUT} = 20dBm$		-100	-90	
		$f_{IN} = 800MHz$ $P_{OUT} = 20dBm$		-120	-110	
3 <sup>rd</sup> Harmonic	H3	$f_{IN} = 17MHz$ $P_{OUT} = 20dBm$		-95	-80	dBc
		$f_{IN} = 204MHz$ $P_{OUT} = 20dBm$		-120	-105	
		$f_{IN} = 800MHz$ $P_{OUT} = 20dBm$		-115	-100	
Input 0.1dB Compression Point [d] (RFC to RF1, RF2)	P0.1dB	$f_{RF} = 5MHz$		37		dBm
		$f_{RF} = 204MHz$		37		
		$f_{RF} = 1.8GHz$		38		
Composite Second Order	CSO	41dBmV / channel		>100		dBc
Composite Triple Beat	CTB	137 channels [e]		>100		

- Items in min/max columns in **bold italics** are guaranteed by test.
- Items in min/max columns that are not bold italics are guaranteed by design characterization.
- $dBmV = dBm [75\Omega] + 48.75$ .
- The input 0.1dB compression point is a linearity figure of merit. Refer to Figure 3 for the maximum operating RF input power levels.
- Total power =  $-7.75 dBm [75\Omega] + 10 \cdot \log(137) = +13.62 dBm [75\Omega]$ .

## Electrical Characteristics

**Table 6. Electrical Characteristics - 50Ω SPECIFICATION**

See F2976 50Ω Application Circuit. Specifications apply when operated with  $V_{CC} = +3.3V$ ,  $T_{EP} = +25^{\circ}C$ .  $Z_S = Z_L = 50\Omega$ , LS = HIGH, single tone signal applied at RF1 or RF2 and measured at RFC, EVKit trace and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Insertion Loss (RFC to RF1, RF2)	IL	$f_{RF} = 5MHz$		0.25	0.45 [b]	dB
		$5MHz < f_{RF} \leq 1GHz$		0.33	0.53	
		$1GHz < f_{RF} \leq 2GHz$ [c]		0.36	<b>0.56</b> [a]	
		$2GHz < f_{RF} \leq 3GHz$		0.40		
		$3GHz < f_{RF} \leq 6GHz$		0.45		
		$6GHz < f_{RF} \leq 8GHz$		0.55		
		$8GHz < f_{RF} \leq 9GHz$		0.65		
		$9GHz < f_{RF} \leq 10GHz$		0.80		
Isolation (RFC to RF1, RF2)	ISO1	$5MHz < f_{RF} \leq 1GHz$	43	48		dB
		$1GHz < f_{RF} \leq 2GHz$	36	42		
		$2GHz < f_{RF} \leq 3GHz$	31	37		
		$3GHz < f_{RF} \leq 6GHz$		27		
		$6GHz < f_{RF} \leq 8GHz$		22		
		$8GHz < f_{RF} \leq 10GHz$		18		
Isolation (RF1 to RF2, RF2 to RF1)	ISO2	$5MHz < f_{RF} \leq 1GHz$	40	45		dB
		$1GHz < f_{RF} \leq 2GHz$	33	38		
		$2GHz < f_{RF} \leq 3GHz$	29	34		
		$3GHz < f_{RF} \leq 6GHz$		26		
		$6GHz < f_{RF} \leq 8GHz$		21		
		$8GHz < f_{RF} \leq 10GHz$		18		
Return Loss (RFC, RF1, RF2) (Insertion loss states)	RL	$5MHz < f_{RF} \leq 1GHz$		28		dB
		$1GHz < f_{RF} \leq 2GHz$		26		
		$2GHz < f_{RF} \leq 3GHz$		26		
		$3GHz < f_{RF} \leq 6GHz$		25		
		$6GHz < f_{RF} \leq 8GHz$		23		
		$8GHz < f_{RF} \leq 9GHz$		18		
		$9GHz < f_{RF} \leq 10GHz$		16		

- Items in min/max columns in **bold italics** are guaranteed by test.
- Items in min/max columns that are not bold italics are guaranteed by design characterization.
- Minimum or maximum specification guaranteed by test at 2GHz and by design characterization over the whole frequency range.

# Electrical Characteristics

**Table 7. Electrical Characteristics - 50Ω SPECIFICATION**

See F2976 50Ω Application Circuit. Specifications apply when operated with  $V_{CC} = +3.3V$ ,  $T_{EP} = +25^{\circ}C$ .  $Z_S = Z_L = 50\Omega$ , LS = HIGH, single tone signal applied at RF1 or RF2 and measured at RFC, EVKit trace and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Input 0.1dB Compression [c]	P0.1dB	$f_{RF} = 2.4GHz$		40		dBm
		$f_{RF} = 6.0GHz$		40		
		$f_{RF} = 8.0GHz$		40		
Input IP3 (RF1, RF2 to RFC)	IIP3	$f_{RF} = 2.4GHz$ $P_{IN} = +24dBm/$ tone 100MHz spacing		77		dBm
Input IP2 (RF1, RF2 to RFC)	IIP2	$f_1 = 700MHz$ $f_2 = 1.7GHz$ $P_{IN} = +24dBm/$ tone Measure 2.4GHz product		125		dBm
		$f_1 = 2.4GHz$ $f_2 = 3.5GHz$ $P_{IN} = +24dBm/$ tone Measure 5.9GHz product		120		
Second Harmonic (RF1, RF2 to RFC)	H2	$f_{IN} = 2.4GHz$ , $P_{IN} = +24dBm$		-100	-90 [b]	dBc
		$f_{IN} = 5.9GHz$ , $P_{IN} = +24dBm$		-90	-80	
Third Harmonic (RF1, RF2 to RFC)	H3	$f_{IN} = 2.4GHz$ , $P_{IN} = +24dBm$		-110	-95	dBc
		$f_{IN} = 5.9GHz$ , $P_{IN} = +24dBm$		-100	-85	
Spurious Output (No RF Applied)	$P_{SPUR1}$	$f_{OUT} \geq 5MHz$ All unused ports terminated		-133		dBm
	$P_{SPUR2}$	$f_{OUT} < 5 MHz$ All unused ports terminated		-120		

- Items in min/max columns in ***bold italics*** are guaranteed by test.
- Items in min/max columns that are not bold italics are guaranteed by design characterization.
- The input 0.1dB compression point is a linearity figure of merit. Refer to Figure 3 for the maximum RF operating input power levels.



## Thermal Characteristics

**Table 8. Package Thermal Characteristics**

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance	$\theta_{JA}$	102	°C/W
Junction to Case Thermal Resistance (Case is defined as the exposed paddle)	$\theta_{JC\_BOT}$	56	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

## Typical Operating Conditions (TOCs)

Unless otherwise noted:

- $V_{CC} = +3.3V$
- LS = HIGH
- $Z_L = Z_S = 75\Omega$
- $Z_L = Z_S = 50\Omega$
- All temperatures are referenced to the exposed paddle
- Evaluation Kit traces and connector losses are de-embedded

## Typical Performance Characteristics - 75 $\Omega$ Performance

Figure 4. RF1 to RFC Insertion Loss

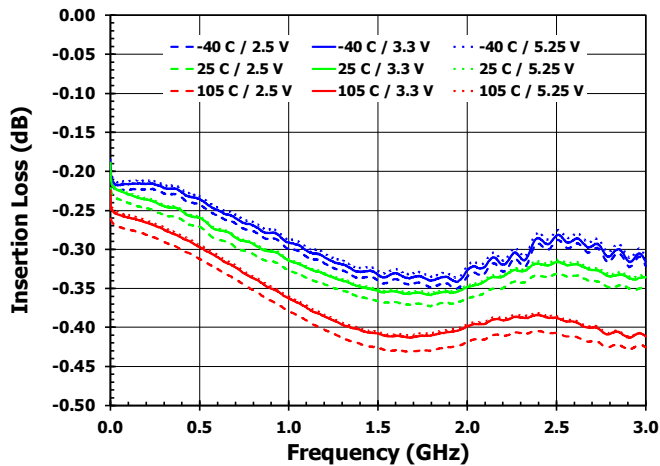


Figure 5. RF2 to RFC Insertion Loss

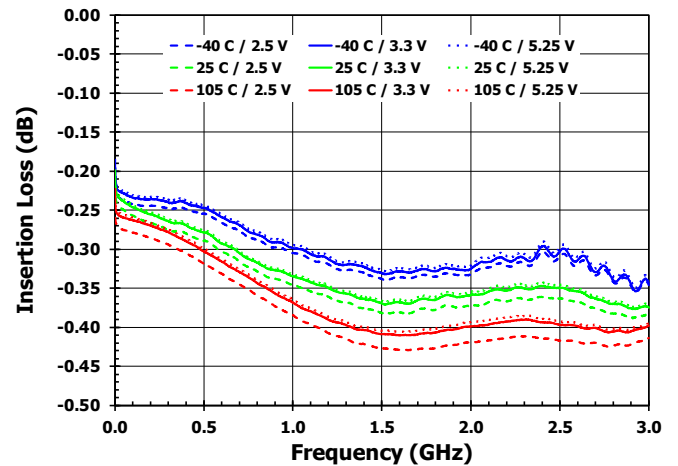


Figure 6. RF1 to RFC Isolation [RF2 On State]

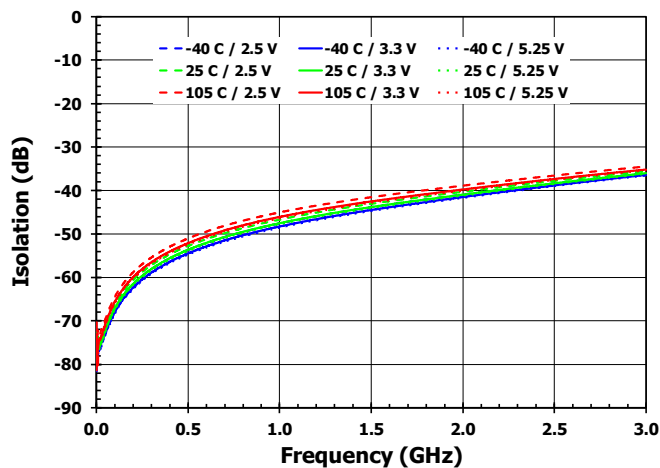


Figure 7. RF2 to RFC Isolation [RF1 On State]

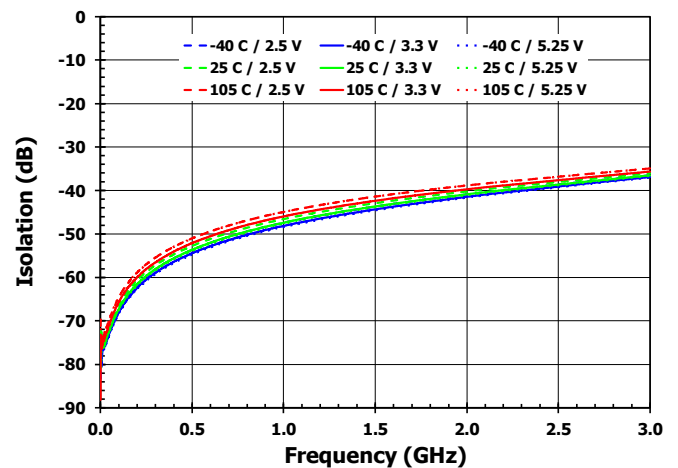


Figure 8. RF1 to RF2 Isolation [RF1 On State]

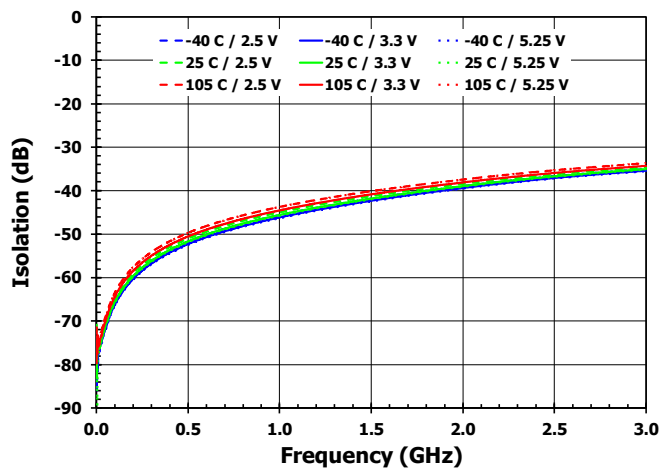
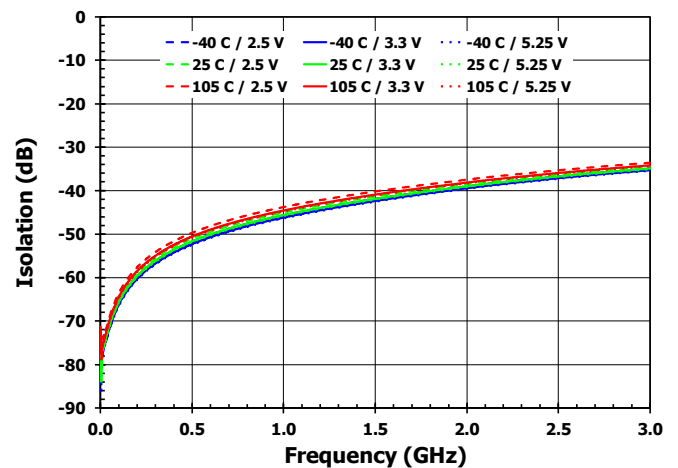


Figure 9. RF1 to RF2 Isolation [RF2 On State]



## Typical Performance Characteristics - 75 $\Omega$ Performance

Figure 10. RFC Return Loss [RF1 On State]

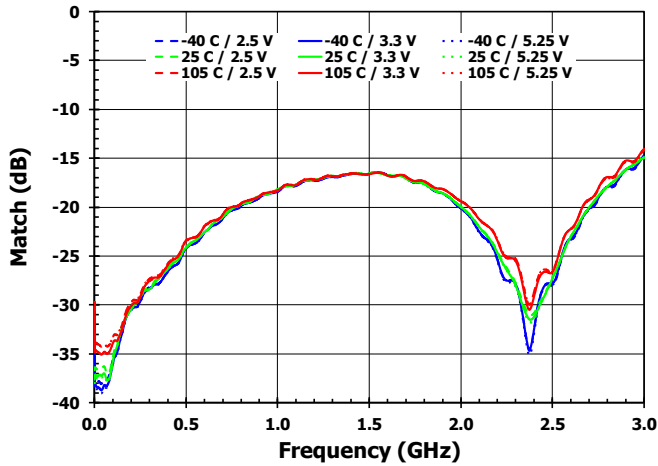


Figure 11. RFC Return Loss [RF2 On State]

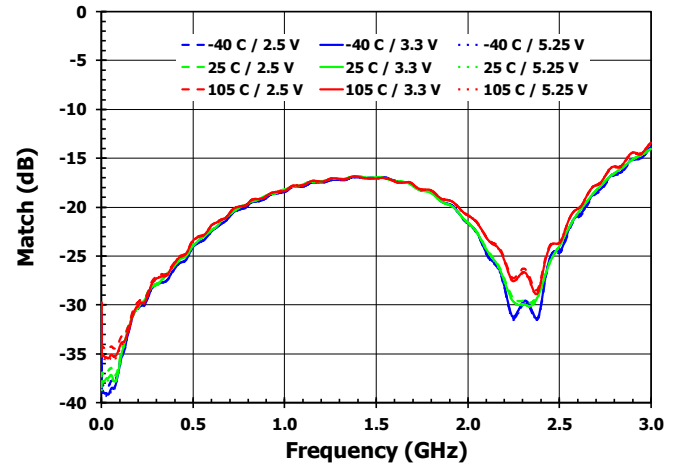


Figure 12. RF1 Return Loss [RF1 On State]

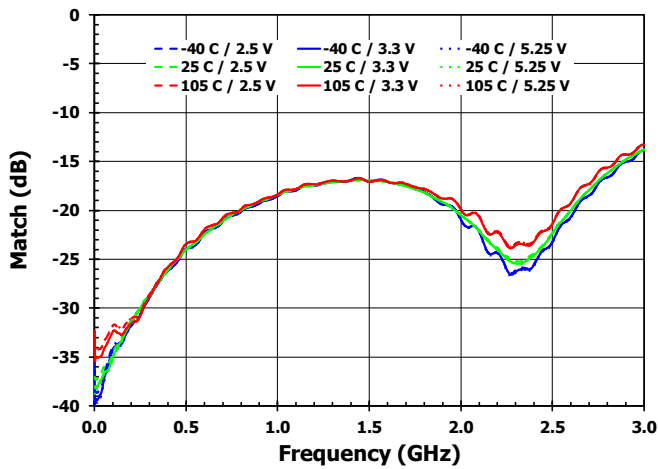
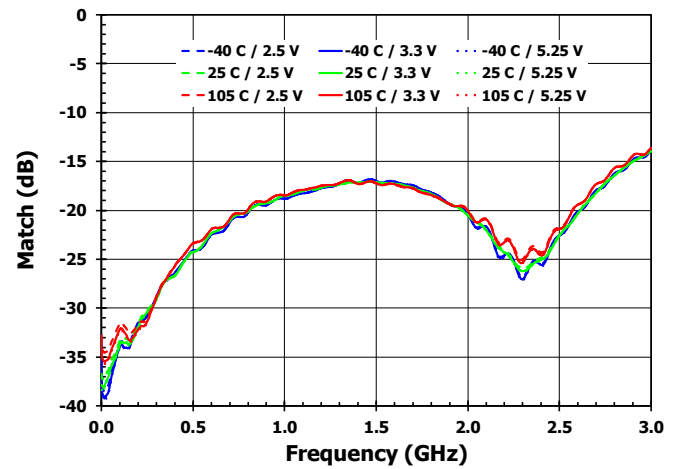


Figure 13. RF2 Return Loss [RF2 On State]



## Typical Performance Characteristics - 50 $\Omega$ Performance

Figure 14. RF1 to RFC Insertion Loss

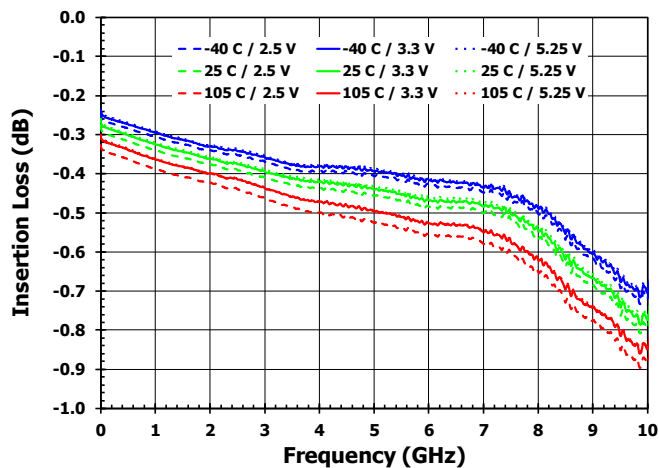


Figure 15. RF2 to RFC Insertion Loss

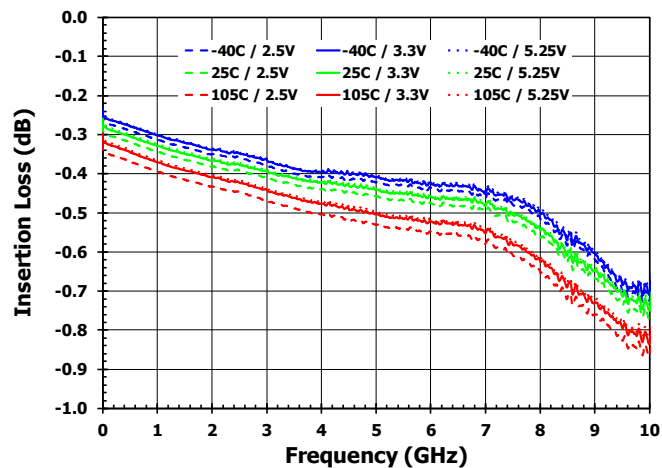


Figure 16. RF1 to RFC Isolation [RF2 On State]

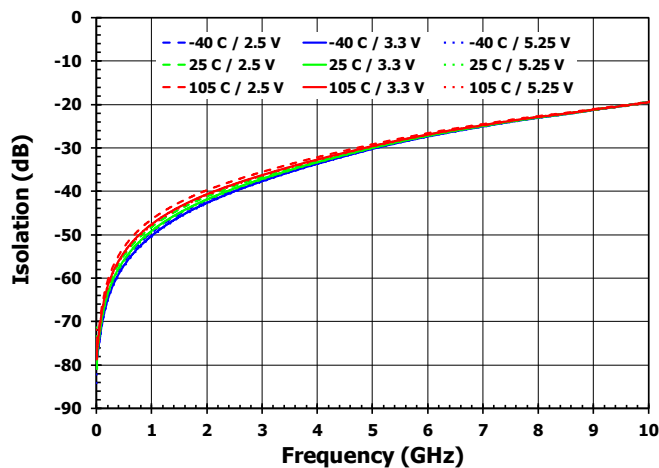


Figure 17. RF2 to RFC Isolation [RF1 On State]

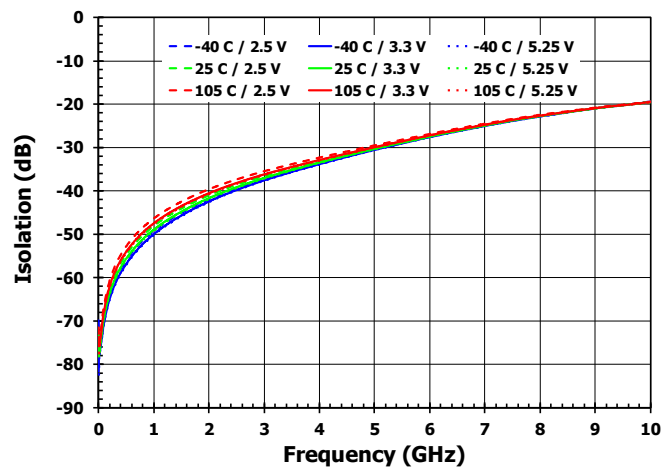


Figure 18. RF1 to RF2 Isolation [RF1 On State]

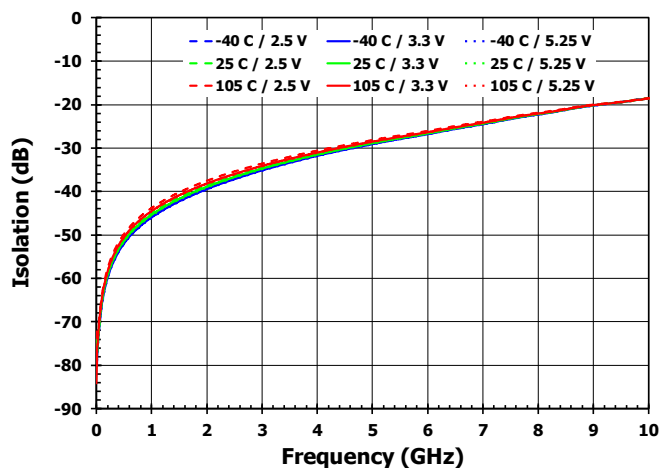
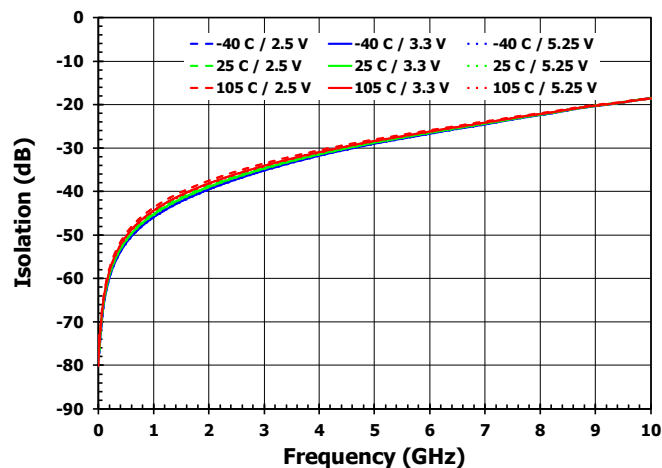


Figure 19. RF1 to RF2 Isolation [RF2 On State]



## Typical Performance Characteristics - 50 $\Omega$ Performance

Figure 20. RFC Return Loss [RF1 On State]

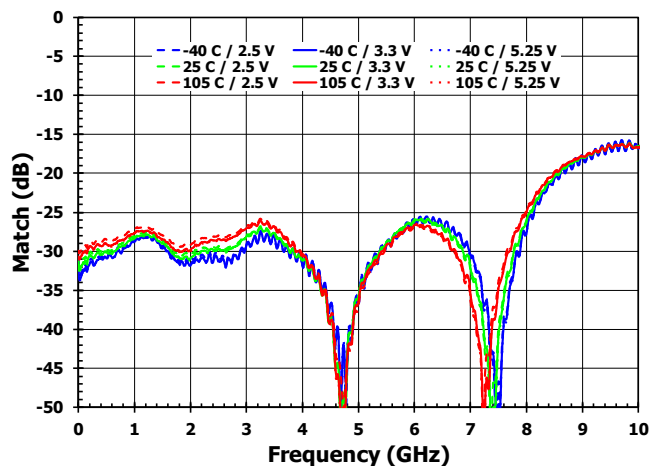


Figure 21. RFC Return Loss [RF2 On State]

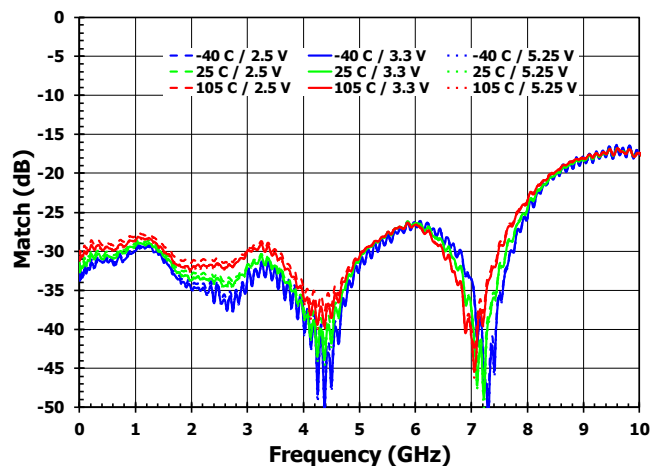


Figure 22. RF1 Return Loss [RF1 On State]

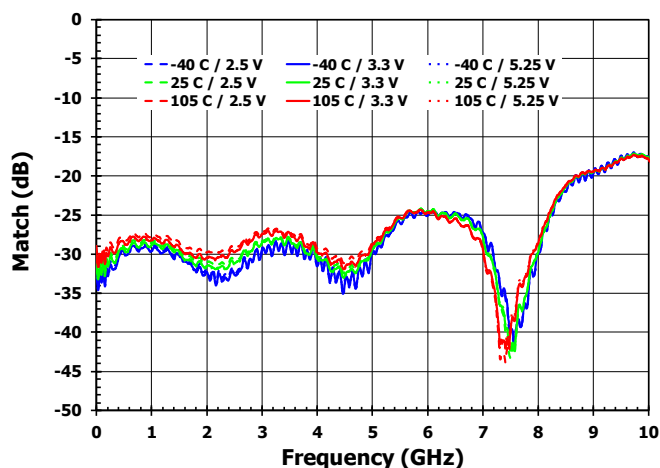


Figure 23. RF2 Return Loss [RF2 On State]

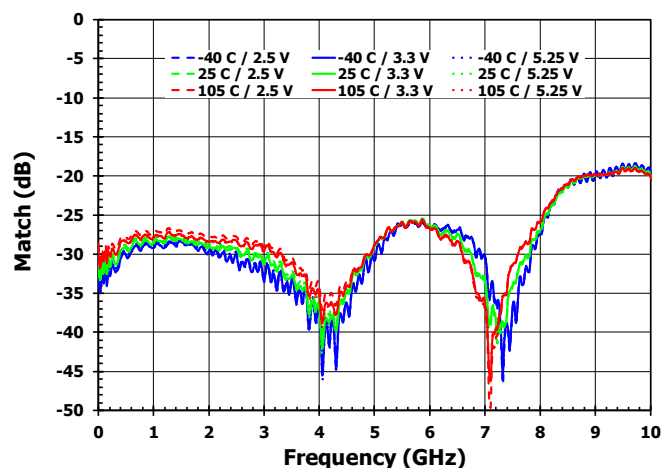


Figure 24. Switching Time  
[Isolation to Insertion Loss State]

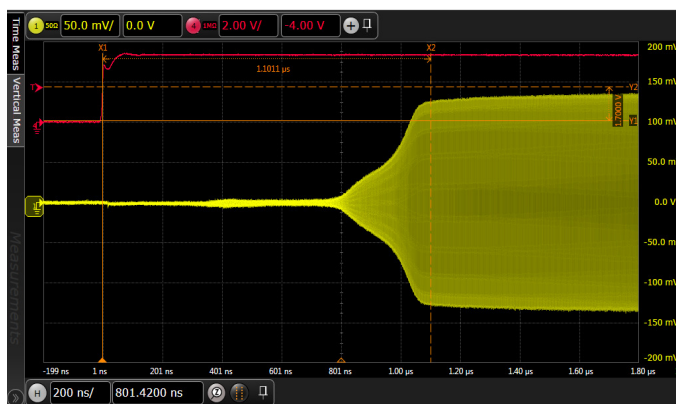
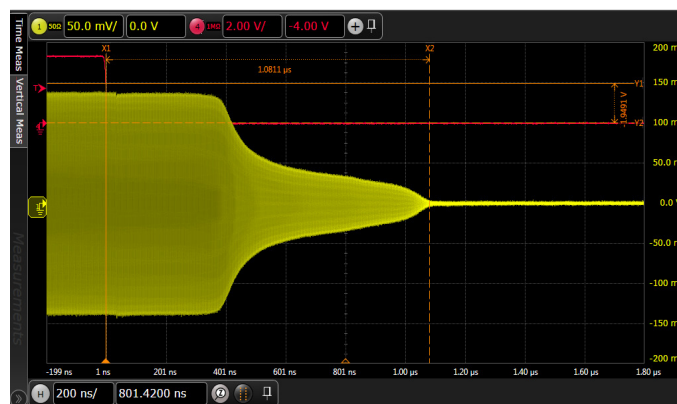


Figure 25. Switching Time  
[Insertion Loss to Isolation State]



## Control Mode

**Table 9. Switch Control Truth Table**

$V_{CTL}$ (pin 10)	LS (pin 11)	Switch State
HIGH	HIGH	RFC to RF2 Insertion Loss State
LOW	HIGH	RFC to RF1 Insertion Loss State
HIGH	LOW	RFC to RF1 Insertion Loss State
LOW	LOW	RFC to RF2 Insertion Loss State

## Application Information

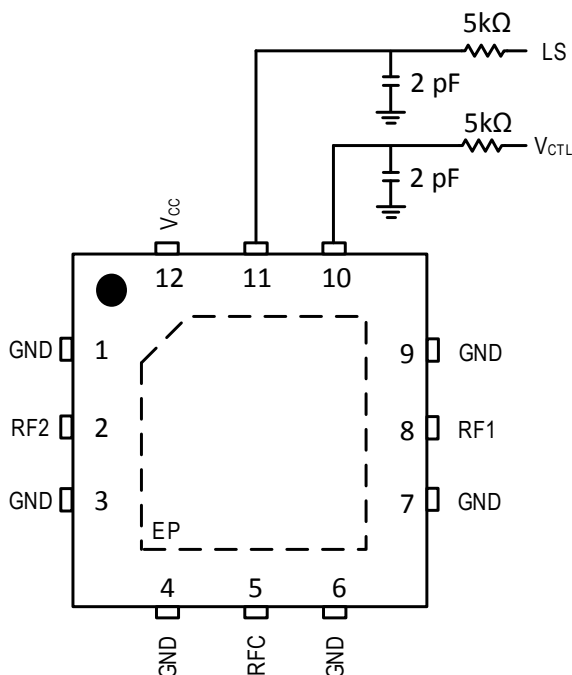
### Power Supplies

A common  $V_{CC}$  power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than  $1V / 20\mu s$ . In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps up or while it returns to zero.

### Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pins 7 and 8 as shown below.

**Figure 26. Control Pin Interface Schematic**



## 75Ω Evaluation Kit Picture

Figure 27. Top View (75Ω)

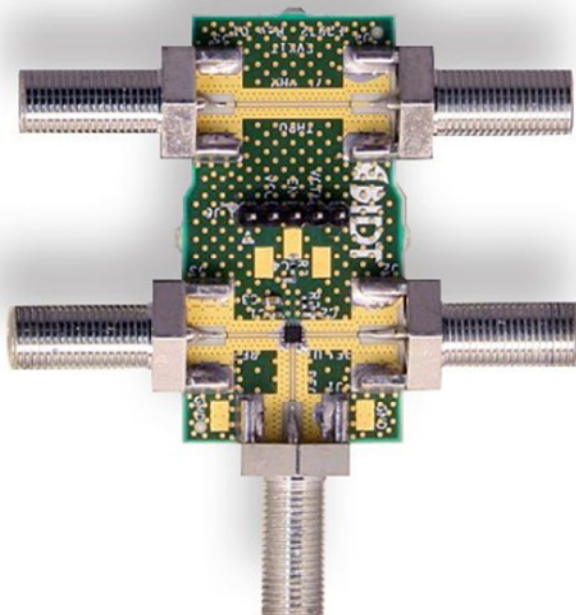
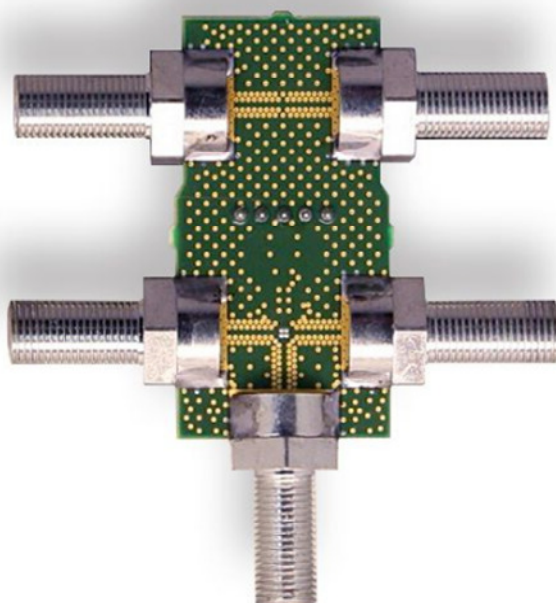


Figure 28. Bottom View (75Ω)



## 50 $\Omega$ Evaluation Kit Picture

Figure 29. Top View (50 $\Omega$ )

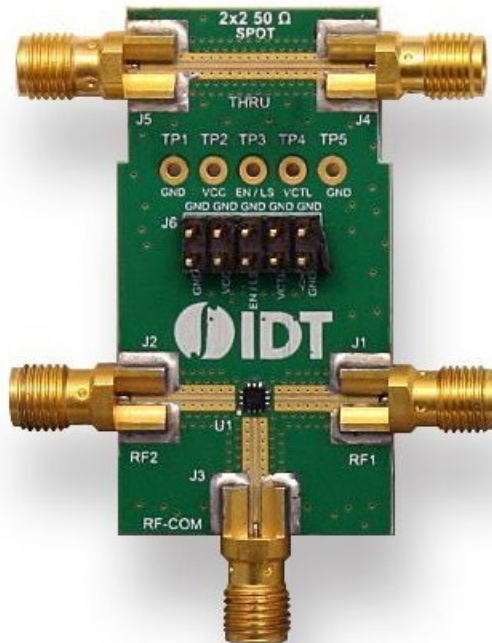
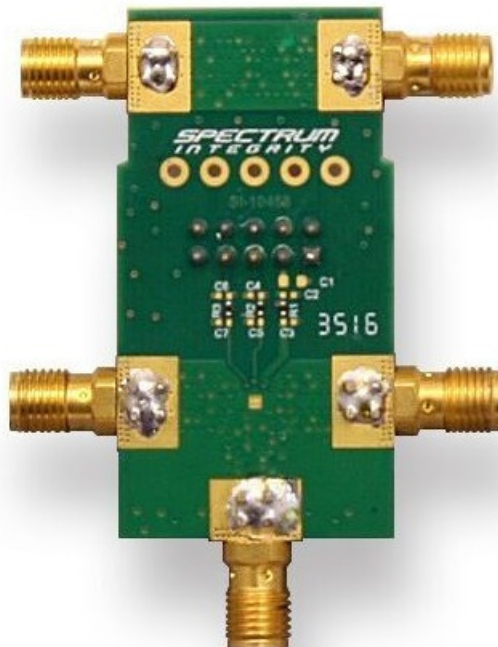


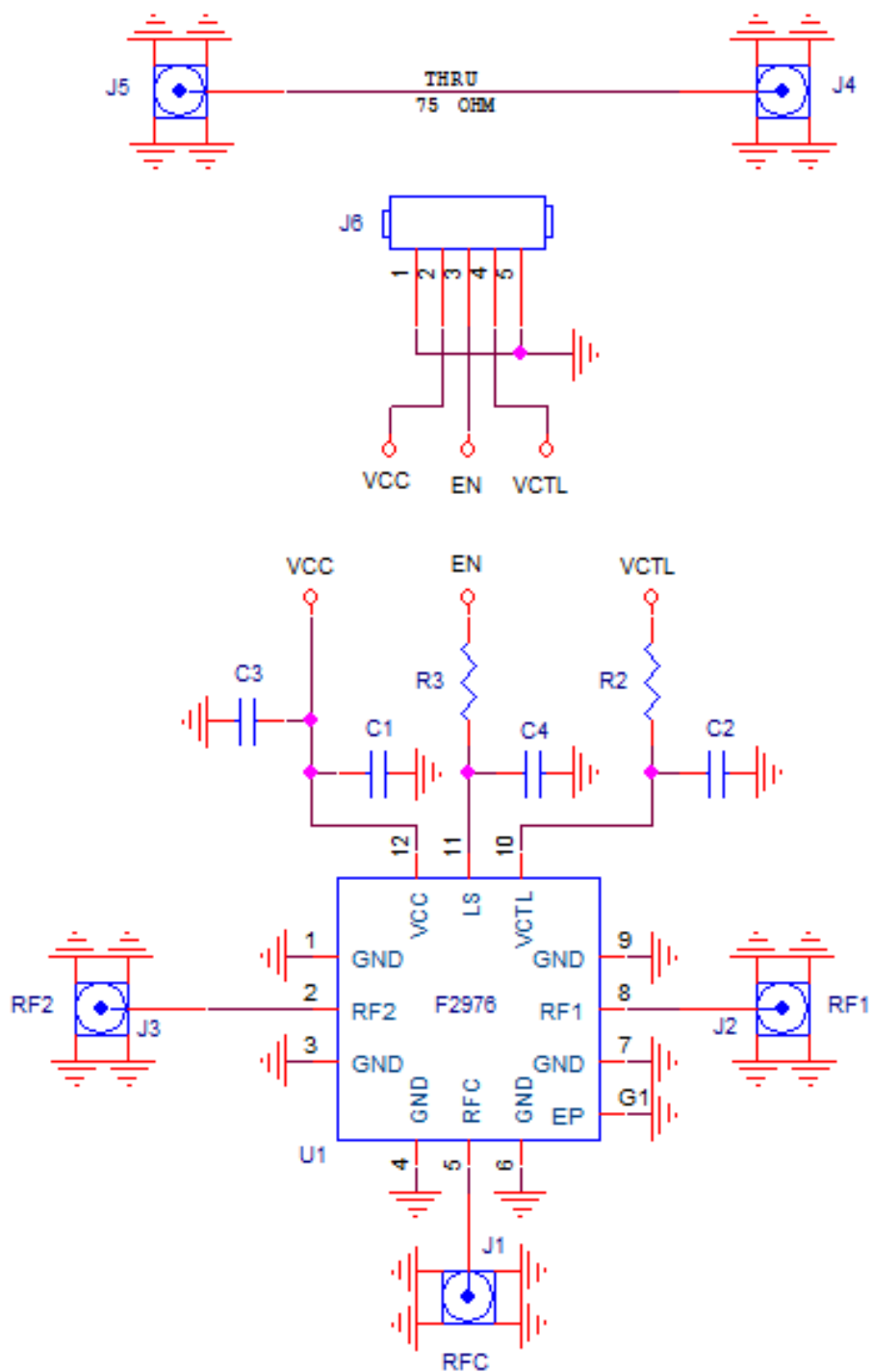
Figure 30. Bottom View (50 $\Omega$ )





## 75Ω Evaluation Kit / Applications Circuit

Figure 31. Electrical Schematic (75Ω)



Note: The F2976 75Ω EVKit reuses the 75Ω PCB from the F2972 and requires pin 1 of the F2976 to be rotated by 90 degrees clockwise from the F2972 PCB pin 1 marking, for proper assembly.



**Table 10. 75Ω Bill of Material (BOM)**

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1	1	0.1μF ±10%, 16V, X7R, Ceramic Capacitor (0402)	GRM155R71C104KA88D	Murata
C2, C4	2	100pF ±5% 50V, C0G, Ceramic Capacitor (0402)	GRM1555C1H101JA01D	Murata
C3	1	0.01μF ±5% 50V, X7R, Ceramic Capacitor (0603)	GRM188R71H103JA01D	Murata
R2, R3	2	100Ω 1/10W, Resistor (0402)	ERJ-2RKF1000X	Panasonic
J1 – J5	5	F-Type Edge Mount	222181	Amphenol RF
J6	1	Conn Header Vert 5x1 Pos Gold	68002-205HLF	Amphenol FCI
U1	1	SP2T Switch 2mm x 2mm 12-pin TQFN	F2976NEGK	IDT
	1	Printed Circuit Board <sup>[a]</sup>	F2972 75Ω PCB	IDT

- a. The F2976 75Ω EVKit reuses the 75Ω PCB from the F2972 and requires pin 1 of the F2976 to be rotated by 90 degrees clockwise from the F2972 PCB pin 1 marking, for proper assembly.

**Table 11. 50Ω Bill of Material (BOM)**

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1 – C7	0	Not Installed (0402)		
R1– R3	3	0Ω 1/10 W, Resistor (0402)	ERJ-2GE0R00X	Panasonic
J1 – J5	5	SMA Edge Mount	142-0761-881	Cinch Connectivity
J6	1	Conn Header 10 Pos 0.100" Str 15 Au	68602-210HLF	Amphenol FCI
TP1, TP2, TP3, TP4, TP5	0	Not Installed Test Point Loop		
U1	1	SP2T Switch 2mm x 2mm 12-pin TQFN	F2976NEGK	IDT
	1	Printed Circuit Board <sup>[a]</sup>	F2972 50Ω PCB	IDT

- a. The F2976 50Ω EVKit reuses the 50Ω PCB from the F2972 and requires pin 1 of the F2976 to be rotated by 90 degrees clockwise from the F2972 PCB pin 1 marking, for proper assembly.

## Evaluation Kit (EVKit) Operation

### External Supply Setup

Set up a  $V_{CC}$  power supply in the voltage range of 2.5V to 5.25V with the power supply output disabled.

For the 75 $\Omega$  EVKit, connect the disabled  $V_{CC}$  supply connection to J6 pin 2 and GND to J6 pins 1 or 5.

For the 50 $\Omega$  EVKit, connect the disabled  $V_{CC}$  supply connection to J6 pin 3 and GND to J6 pin 1, 2, 4, 6, 8, 9, or 10.

### Logic Control Setup

With the logic control lines disabled set the HIGH and LOW logic levels to satisfy the levels stated in the electrical specifications table.

For the 75 $\Omega$  EVKit, connect the disabled logic control lines to J6 EN (pin 3) and  $V_{CTL}$  (pin 4).

For the 50 $\Omega$  EVKit, connect the disabled logic control lines to J6 EN / LS (pin 5) and  $V_{CTL}$  (pin 7).

See Table 9 for the logic truth table.

### Turn On Procedure

Setup the supplies and EVKit as noted in the External Supply Setup and Logic Control Setup sections above.

Enable the  $V_{CC}$  supply.

Enable the logic control signals.

Set the logic settings to achieve the desired Table 9 configuration. Note that external control logic should not be applied without  $V_{CC}$  being present.

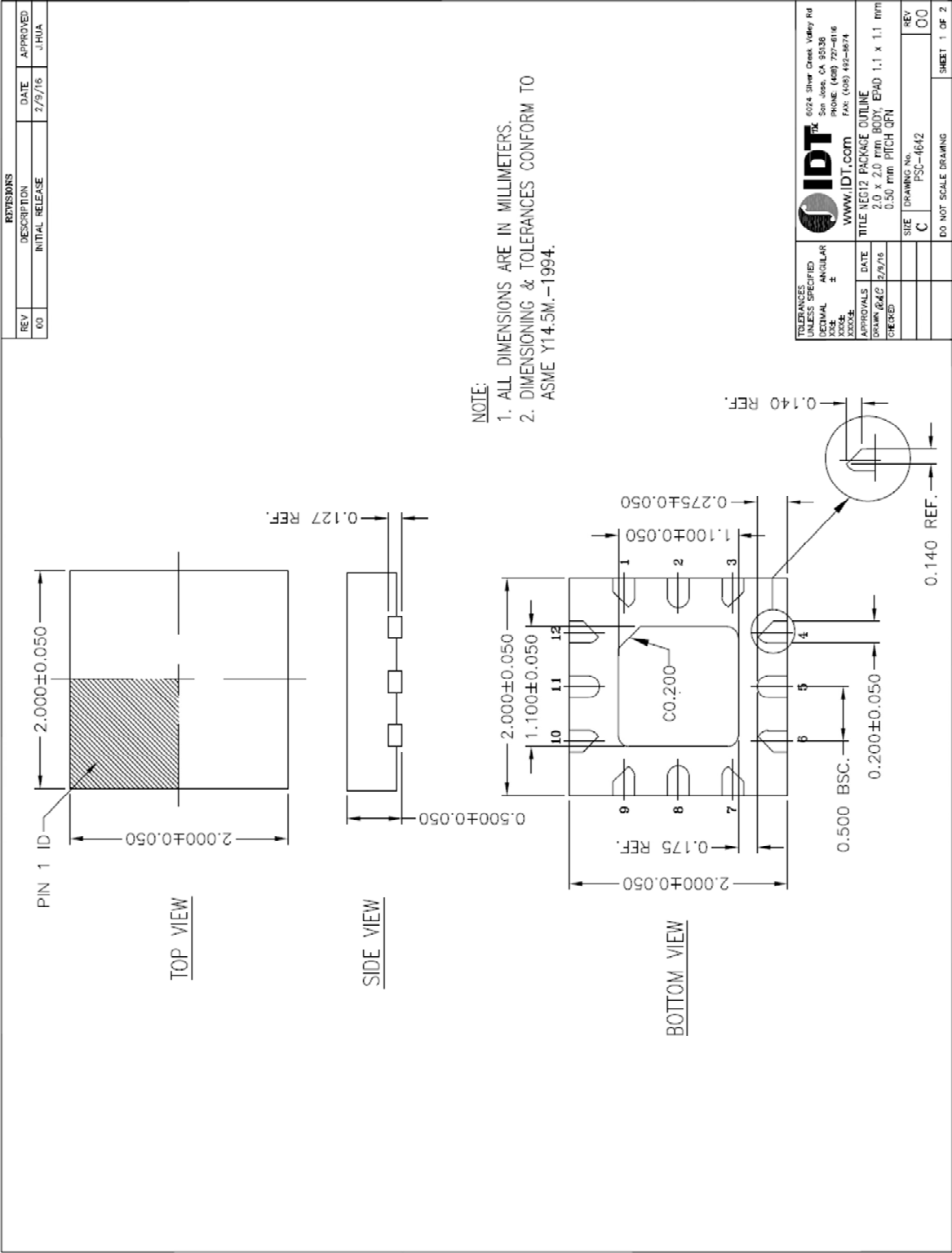
### Turn Off Procedure

Set the logic control pins to a logic LOW.

Disable the  $V_{CC}$  supply.

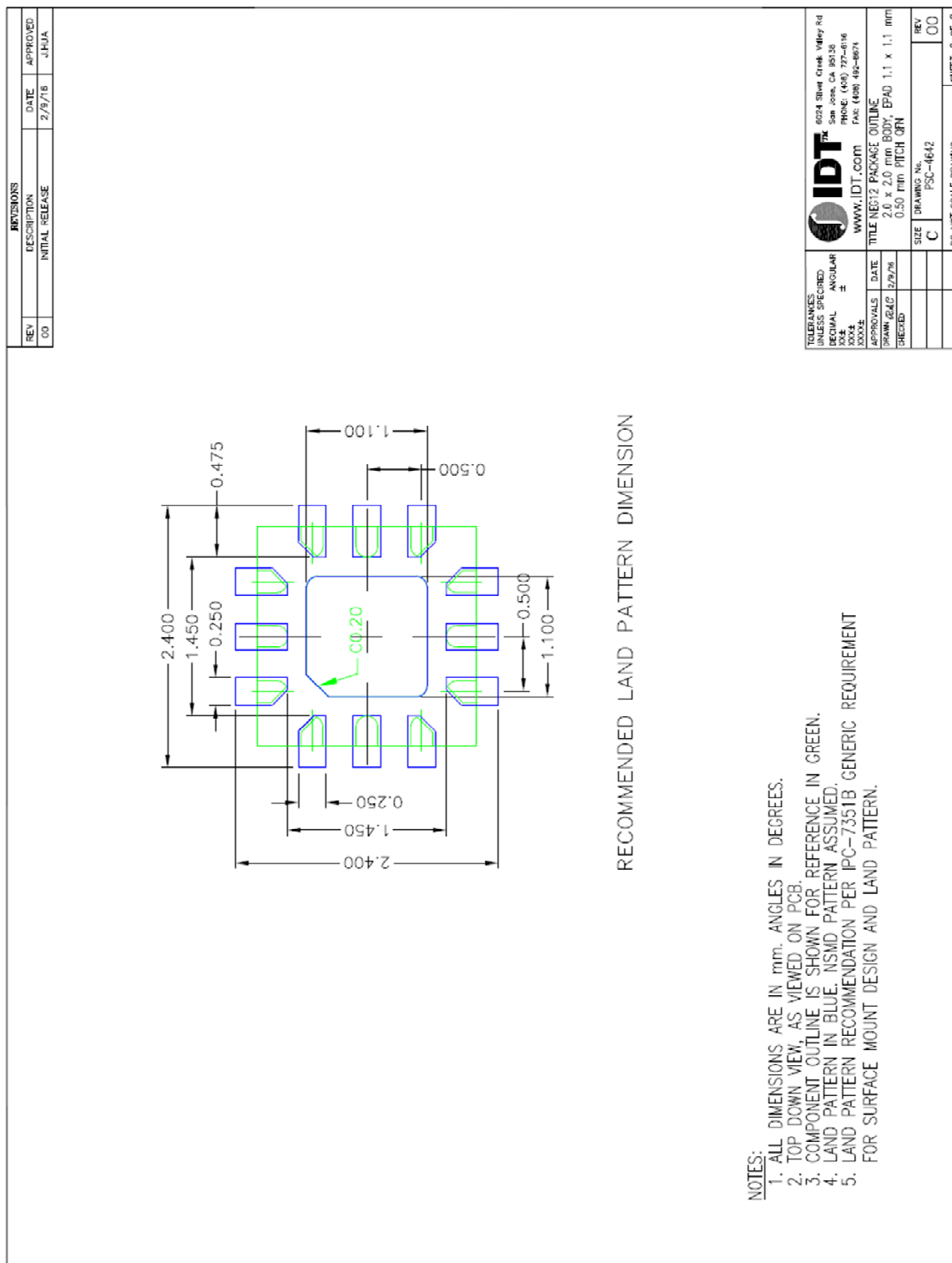
Package Drawings

Figure 33. Package Outline Drawing NEG12 PSC-4642

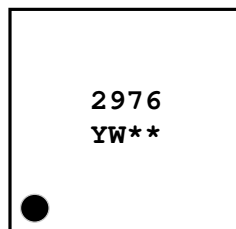


# Recommended Land Pattern

Figure 34. Recommended Land Pattern NEG12 PSC-4642



## Marking Diagram



Line 1 - 2976 = Abbreviated part number.  
 Line 2 - Y = Year code.  
 Line 2 - W = Work week code.  
 Line 2 - \*\* = Sequential alpha for lot traceability.

## Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F2976NEGK	2mm x 2mm x 0.5mm 12-VFQFP-N	MSL1	Cut Reel	-40°C to +105°C
F2976NEGK8	2mm x 2mm x 0.5mm 12-VFQFP-N	MSL1	Tape and Reel	-40°C to +105°C
F2976EVBI-75OHM	75Ω Evaluation Board			
F2976EVBI-50OHM	50Ω Evaluation Board			

Revision History

Revision	Revision Date	Description of Change
Rev 0	2017-Apr-19	Initial Release



## Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

## Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

## Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.