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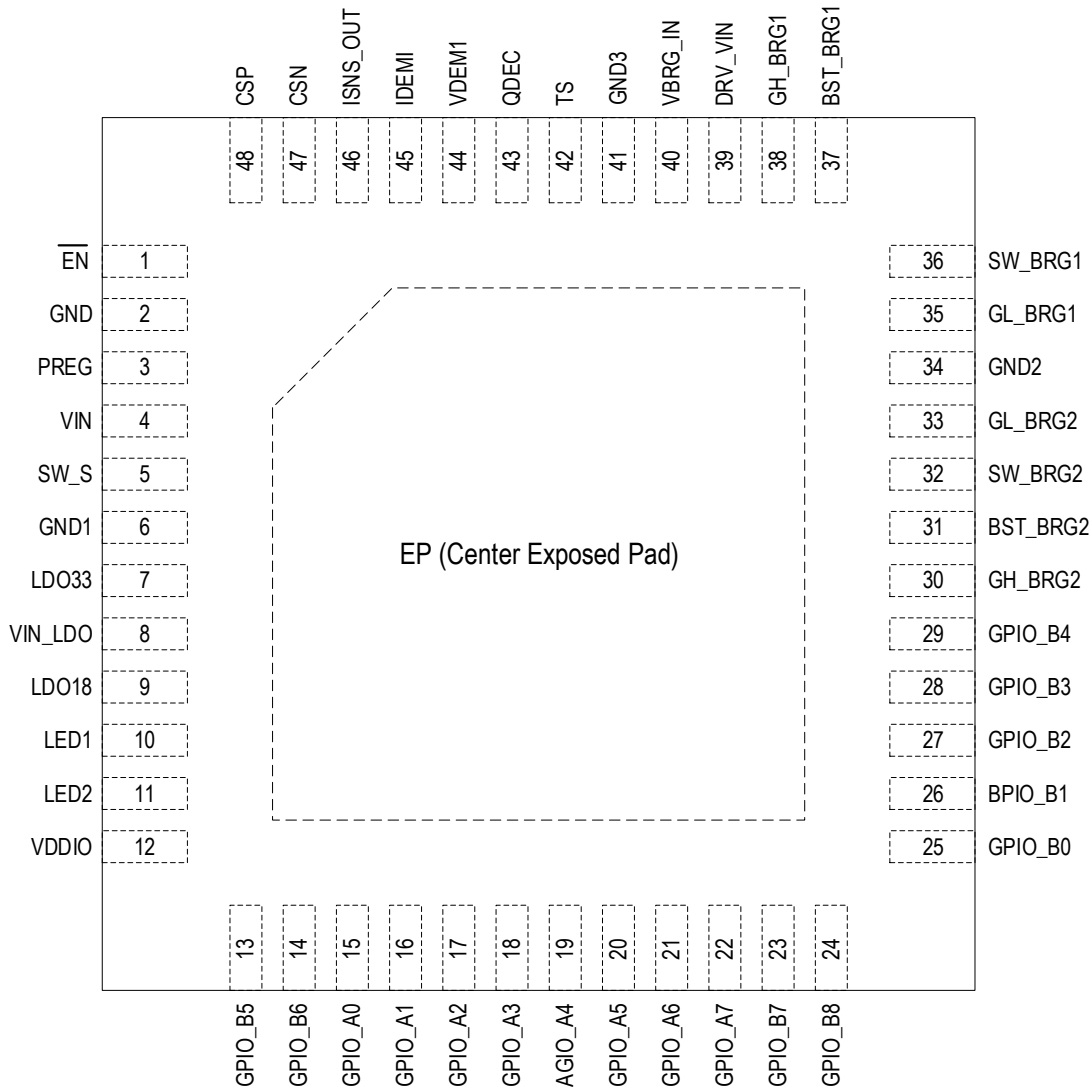
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1. Pin Assignments

Figure 1. Pin Assignments



2. Pin Descriptions

Table 1. Pin Descriptions

Note: See important table notes at the end of the table.

| Pins | Name | Type | Function |
|------|------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | $\overline{\text{EN}}$ | Input | Active-LOW enable pin. When connected to logic HIGH, the P9242-G enters the Shut Down Mode, which has a typical current consumption of 25 μ A. When connected to logic LOW, the device is in normal operation. |
| 2 | GND | – | Ground connection. |
| 3 | PREG | Output | Regulated 5V output used for internal device biasing. Connect a 1 μ F X5R or X7R ceramic capacitor from this pin to ground. This pin MUST NOT be externally loaded. |
| 4 | VIN | Input | Input power supply. Connect a 10 μ F X5R or X7R ceramic capacitor from this pin to ground. |
| 5 | SW_S | Output | Internal step-down regulator's switch node. Connect one of the terminals of a 4.7 μ H inductor to this pin. |
| 6 | GND1 | - | Ground connection. |
| 7 | LDO33 | Output | Regulated 3.3V output used for internal device biasing. Connect a 1 μ F X5R or X7R ceramic capacitor from this pin to ground. This pin MUST NOT be externally loaded. |
| 8 | VIN_LDO | Input | Linear regulator input power supply. Connected this pin to the 5V output of the step-down regulator. This pin MUST NOT be externally loaded. |
| 9 | LDO18 | Output | Regulated 1.8V output used for internal device biasing. Connect a 1 μ F X5R or X7R ceramic capacitor from this pin to ground. This pin MUST NOT be externally loaded. |
| 10 | LED1 | Output | Open-drain output. Connect an LED to this pin |
| 11 | LED2 | Output | Open-drain output. Connect an LED to this pin. |
| 12 | VDDIO | Input | Input power supply for internal biasing. This pin must be connected to LDO33. |
| 13 | GPIO_B5 | Input | Crystal input pin. Connect to GND when using external clock. |
| 14 | GPIO_B6 | Input | Crystal/clock input pin. |
| 15 | GPIO_A0 | Input | I2C interface clock input. Connect a 5.1k Ω pull-up resistor to the LDO33 rail. |
| 16 | GPIO_A1 | I/O | I2C interface data input and data output. Connect a 5.1k Ω pull-up resistor to the LDO33 rail. |
| 17 | GPIO_A2 ^[a] | Input | Programmable advanced qualify-factor threshold pin. Connect this pin to the center tap of a resistor divider to set the threshold. |
| 18 | GPIO_A3 ^[a] | Input | Programmable LED pattern selection and power loss FOD threshold pin. Connect the center tap of a resistor divider to this pin. For more information on setting the LED pattern and Q-factor enable/disable, see sections 9.9.7 and 9.9.2.2, respectively. |
| 19 | GPIO_A4 ^[a] | Output | Logic signal to bypass external buck regulator. |
| 20 | GPIO_A5 ^[a] | I/O | Connected to USB D- pin. |
| 21 | GPIO_A6 ^[a] | Output | Logic pin for detecting over-voltage for VCOIL in the power transfer. |
| 22 | GPIO_A7 ^[a] | I/O | Connected to USB D- pin. |
| 23 | GPIO_B7 | I/O | PWM control signal for regulating buck converter output voltage. |

| Pins | Name | Type | Function |
|------|----------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24 | GPIO_B8 | I/O | Connected to USB D+ pin. |
| 25 | GPIO_B0 | Output | Enable signal for external memory. |
| 26 | GPIO_B1 | I/O | Clock signal for external memory. |
| 27 | GPIO_B2 | I/O | Data output signal for external memory. |
| 28 | GPIO_B3 | I/O | Data input signal for external memory. |
| 29 | GPIO_B4 | Output | Enable signal for buck converter. |
| 30 | GH_BRG2 | Output | Gate driver output for the high-side FET of half bridge group 2. Connect this pin to a series 22Ω resistor to the respective bridge FET gate. |
| 31 | BST_BRG2 | Input | Bootstrap pin for half bridge group 2. Tie an external capacitor from this pin to the SW_BRG2 pin to generate a drive voltage higher than the input voltage. |
| 32 | SW_BRG2 | Output | Switch node for half bridge group 2. |
| 33 | GL_BRG2 | Output | Gate driver output for the low-side FET of half bridge group 2. Connect this pin to a series 22Ω resistor to the respective bridge FET gate. |
| 34 | GND2 | – | Ground connection. |
| 35 | GL_BRG1 | Output | Gate driver output for the low-side FET of half bridge group 1. Connect this pin to a series 22Ω resistor to the respective bridge FET gate. |
| 36 | SW_BRG1 | Output | Switch node for half bridge group 1. |
| 37 | BST_BRG1 | Output | Bootstrap pin for half bridge group 1. Tie an external capacitor from this pin to the SW_BRG1 to generate a drive voltage higher than the input voltage. |
| 38 | GH_BRG1 | Output | Gate driver output for the high-side FET of half bridge group 1. Connect this pin to a series 22Ω resistor to the respective bridge FET gate. |
| 39 | DRV_VIN | Input | Input power supply for the internal gate drivers. Connect a 10μF capacitor from this pin to ground. This pin MUST NOT be externally loaded. |
| 40 | VBRG_IN | Input | Bridge voltage input sense pin. |
| 41 | GND3 | – | Ground connection. |
| 42 | TS | Input | Remote temperature sensor for over-temperature shutdown. Connect this pin to the thermistor network. |
| 43 | QDEC | Input | Input signal for Q-factor measurement circuit. |
| 44 | VDEM1 | Input | High-pass filter input. Voltage demodulation pin for data packets based on coil voltage variation; transmitted by power receiver. |
| 45 | IDEMI | Input | High-pass filter input. Current demodulation pin for data packets based on coil current variation; transmitted by power receiver. |
| 46 | ISNS_OUT | Output | Input current sense output. |
| 47 | CSN | Input | Low-side input current sense. |
| 48 | CSP | Input | High-side input current sense. |
| – | EP | – | Ground connection. |

[a] GPIO_A2 to GPIO_A7 are multi-function pins. With a firmware (FW) change, GPIO_A5 can be set to ADC inputs.

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses beyond those listed under “Absolute Maximum Ratings” might cause permanent damage to P9242-G. Functional operation of P9242-G at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions for extended periods could affect long-term reliability.

Table 2. Absolute Maximum Ratings

| Pins [a] | Rating [b] | Units |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-------|
| EN, VIN, SW_S, VBRG_IN, SW_BRG1, SW_BRG2, CSP, CSN, BST_BRG1, BST_BRG2, GH_BRG1, GH_BRG2 [c] | -0.3 to 28 | V |
| PREG, LDO33, VIN_LDO, LED1, LED2, VDDIO, GL_BRG1, GL_BRG2, VDEM1, IDEMI, ISNS_OUT, DRV_VIN, TS, GPIO_A0, GPIO_A1, GPIO_A2, GPIO_A3, GPIO_A4, GPIO_A5, GPIO_A6, GPIO_A7, GPIO_B0, GPIO_B1, GPIO_B2, GPIO_B3, GPIO_B4, GPIO_B5, GPIO_B6, GPIO_B7, GPIO_B8 | -0.3 to 6 | V |
| LDO18 | -0.3 to 2 | V |

- [a] All voltages are referred to ground unless otherwise noted. All GND pins and the exposed pad (EP) are connected internally and must also be connected together.
- [b] During system application operation, pins SW_S, SW_BRG1, SW_BRG2, GH_BRG1, GH_BRG2, GL_BRG1, GL_BRG2 can momentarily go below ground by as much as -6.0V for no longer than 100ns.
- [c] When measuring the GL_BRG1 and GL_BRG2 pins' absolute maximum voltage, the current must be limited to within the “Absolute Peak” and “DC Drive” current specifications.

Table 3. Package Thermal Information

| Symbol | Description | VFQFN Rating | Units |
|---------------|------------------------------------------------------|--------------|-------|
| θ_{JA} | Thermal Resistance Junction to Ambient [a], [b], [c] | 27.2 | °C/W |
| θ_{JC} | Thermal Resistance Junction to Case [b], [c] | 18.8 | °C/W |
| θ_{JB} | Thermal Resistance Junction to Board [b], [c] | 1.36 | °C/W |
| T_J | Operating Junction Temperature [a], [b] | -40 to +125 | °C |
| T_A | Ambient Operating Temperature [a], [b] | -40 to +85 | °C |
| T_{STG} | Storage Temperature | -55 to +150 | °C |
| T_{LEAD} | Lead Temperature (soldering, 10s) | +300 | °C |

- [a] The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.
- [b] This thermal rating was calculated on a JEDEC 51-standard 4-layer board with the dimensions 76.2 x 114.3 mm in still air conditions.
- [c] Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

Table 4. ESD Information

| Test Model | Pins | Ratings | Units |
|----------------------------|----------|---------|-------|
| Human Body Model (HBM) | All pins | ±2000 | V |
| Charged-Device Model (CDM) | All pins | ±500 | V |

4. Electrical Characteristics

Table 5 Electrical Characteristics

Note: $V_{IN} = 5V$, $\overline{EN} = \text{LOW}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at 25°C .

| Symbol | Description | Conditions/Notes | Min | Typical | Max | Units |
|----------------------------------------------------------------------------------------------------------------------|------------------------------------------------|------------------------------------------------------|------|-----------|-----|---------------|
| Input Supplies and UVLO | | | | | | |
| V_{IN} | Input Operating Range ^[a] | | 4.25 | | 19 | V |
| V_{IN_UVLO} | Under-Voltage Lockout | V_{IN} rising | | 3.4 | 3.6 | V |
| | | V_{IN} falling | | 3.0 | | V |
| I_{IN} | Operating Mode Input Current | Power Transfer Phase, $V_{in} = 12V$ | | 10 | | mA |
| I_{STD_BY} | Standby Mode Current | Periodic ping | | 1 | | mA |
| I_{SHD} | Shut Down Current | | | 25 | 80 | μA |
| Enable Pin Threshold (\overline{EN}) | | | | | | |
| V_{IH} | Input Threshold HIGH | | 2.5 | | | V |
| V_{IL} | Input Threshold LOW | | | | 0.5 | V |
| I_{EN_LKG} | \overline{EN} Pin Input Leakage Current | $V_{\overline{EN}} = 0V$ | -1 | | 1 | μA |
| | | $V_{\overline{EN}} = 5V$ | | 2.5 | | μA |
| Step-Down Regulator ^[b] with $C_{OUT} = 33\mu\text{F}$; $L = 4.7\mu\text{H}$ | | | | | | |
| V_{OUT} | Step-Down Output Voltage | $V_{in} > 5.5V$ | | 5.1 | | V |
| I_{OUT} | Output Current | | | 50 | | mA |
| N-Channel MOSFET Drivers | | | | | | |
| $t_{LS_ON_OFF}$ | Low-Side Gate Driver Rise and Fall Times | $C_{LOAD} = 3nF$; 10% to 90%, 90% to 10% | | 50 | 150 | ns |
| $t_{HS_ON_OFF}$ | High-Side Gate Driver Rise and Fall Times | $C_{LOAD} = 3nF$; 10% to 90%, 90% to 10% | | 150 | 300 | ns |
| Input Current Sense | | | | | | |
| V_{SEN_OFST} | Amplifier Output Offset Voltage | Measured at the ISNS_OUT pin; $V_{CSP} = V_{CSN}$ | | 0.6 | | V |
| $I_{SEN_ACC_TYP}$ | Measured Current Sense Accuracy ^[c] | $V_{R_ISEN} = 25mV$, $I = 1.25A$ | | ± 3.5 | | % |
| Analog to Digital Converter | | | | | | |
| N | Resolution | | | 12 | | Bit |
| Channel | Number of Channels | | | 10 | | |
| V_{IN_FS} | Full Scale Input Voltage | | | 2.4 | | V |

| Symbol | Description | Conditions/Notes | Min | Typical | Max | Units |
|-------------------------------------------------------------------------------|------------------------------------|-----------------------------------------------------|-------------|---------|-------------|-------|
| LDO18^[b] (C_{OUT} = 1μF, V_{IN_LDO} = 5.5V) | | | | | | |
| V _{LDO18} | Output Voltage | | | 1.8 | | V |
| ΔV _{OUT} /V _{OUT} | Output Voltage Accuracy | | -5 | | +5 | % |
| I _{OUT18_MAX} | Maximum Output Current | | | 20 | 25 | mA |
| LDO33^[b] (C_{OUT} = 1μF, V_{IN_LDO} = 5.5V) | | | | | | |
| V _{LDO33} | | C _{OUT} = 1μF, V _{VIN_LDO} = 5.5V | 3.15 | 3.3 | 3.45 | V |
| ΔV _{OUT} /V _{OUT} | Output Voltage Accuracy | | -5 | | +5 | % |
| I _{OUT18_MAX} | Maximum Output Current | | | 10 | 25 | mA |
| PREG | | | | | | |
| V _{PREG} | 5V LDO Regulator | | | 5 | | V |
| Thermal Shutdown | | | | | | |
| T _{SD} | Thermal Shutdown | Threshold rising | | 140 | | °C |
| | | Threshold falling | | 120 | | °C |
| Analog Input Pins Input Current Leakage (TS, QDEC) | | | | | | |
| I _{LKG} | Leakage Current | | -1 | | 1 | μA |
| Open-Drain Pins Output Logic Levels (LED1, LED2, GPIO_A0, GPIO_A1) | | | | | | |
| V _{OH} | Output Logic HIGH | | 4 | | | V |
| V _{OL} | Output Logic LOW | I = 8mA | | | 0.5 | V |
| General Purpose Inputs/Outputs Pins Logic Levels | | | | | | |
| V _{IH} | Input Voltage HIGH Level | | 0.7 * VDDIO | | | V |
| V _{IL} | Input Voltage LOW Level | | | | 0.3 * VDDIO | V |
| I _{LKG} | Leakage Current | | | | 1 | μA |
| V _{OH} | Output Logic HIGH | I = 8mA, VDDIO = 3.3V | 2.4 | | | V |
| V _{OL} | Output Logic LOW | I = 8mA, VDDIO = 3.3V | | | 0.5 | V |
| I2C Interface (GPIO_A0, GPIO_A1) | | | | | | |
| f _{SCL_SLV} | Clock Frequency | As I2C slave | | | 400 | kHz |
| C _B | Capacitive Load | For each bus line | | | 100 | pF |
| C _{BIN} | GPIO_A0, GPIO_A1 Input Capacitance | | | 5 | | pF |
| I _{LKG} | Input Leakage Current | V = GND and 3.3V | -1 | | 1 | μA |

[a] The input voltage operating range is dependent upon the type of transmitter power stage (full-bridge, half-bridge) and transmitting coil inductance. WPC specifications should be consulted for appropriate input voltage ranges by end-product type.

[b] Do not externally load. For internal biasing only.

[c] A 20mΩ, 1% or better sense resistor and 10Ω, 1% input filter resistors are required to meet the FOD specification.

The following performance characteristics were taken using a P9221-R, 15W Wireless Power Receiver (RX) at $T_A = +25^\circ\text{C}$, $V_{IN} = 5\text{V to }19\text{V}$, and $\overline{\text{EN}} = \text{LOW}$ unless otherwise noted.

Figure 8. Internal Buck Load Regulation

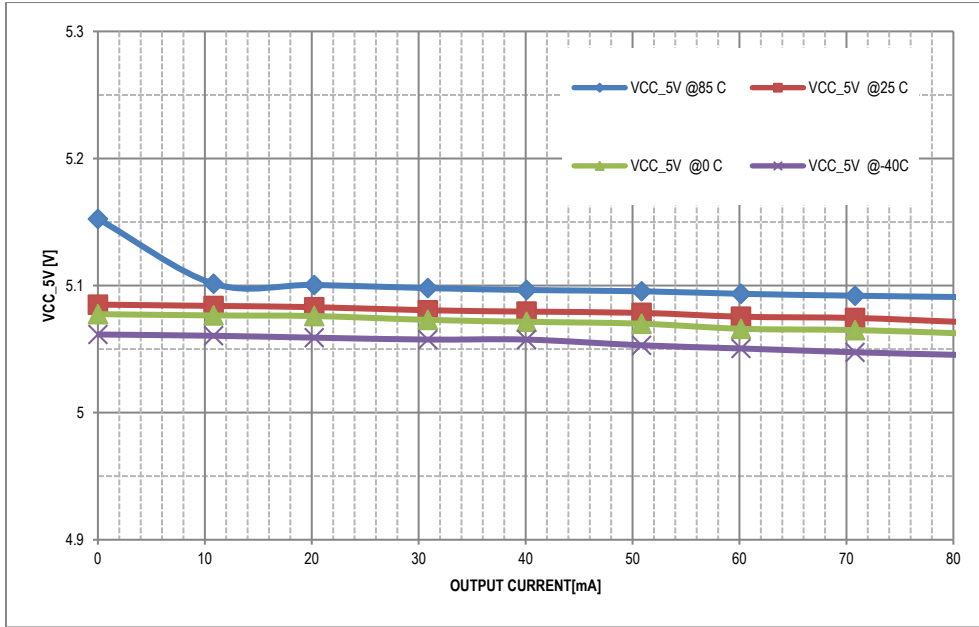
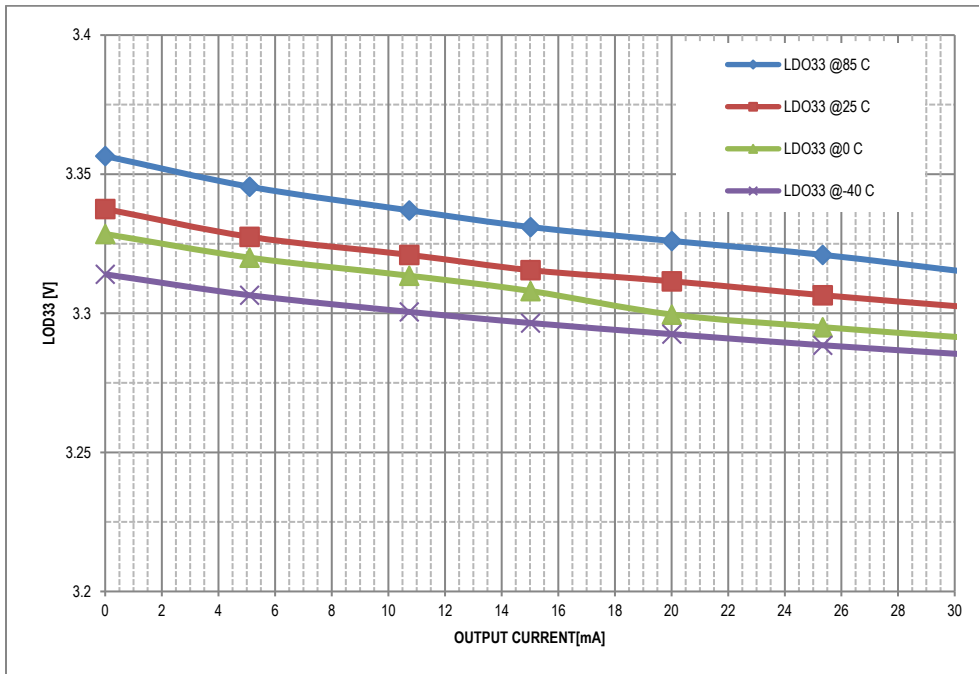


Figure 9. Load Regulation vs. Output Load: LD033



The following performance characteristics were taken using a P9221-R, 15W Wireless Power Receiver (RX) at $T_A = +25^\circ\text{C}$, $V_{IN} = 5\text{V}$ to 19V , and $\text{EN} = \text{LOW}$ unless otherwise noted.

Figure 10. Load Regulation vs. Output Load: LDO18

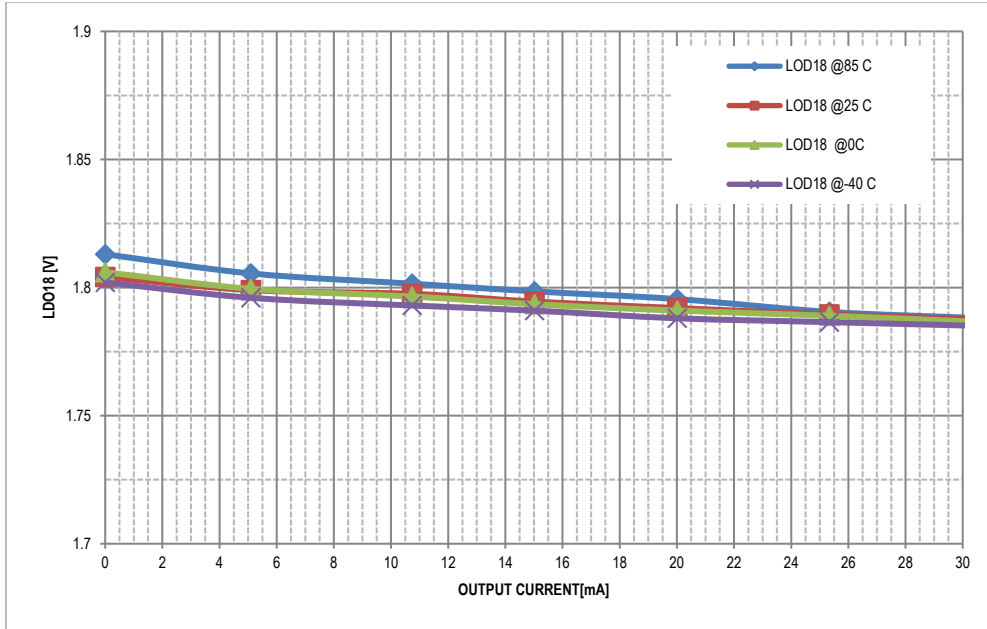


Figure 11. Voltage and Current Signal for Demodulation: Ch2 = VSNS, Ch3 = ISNS_IN



The following performance characteristics were taken using a P9221-R, 15W Wireless Power Receiver (RX) at $T_A = +25^\circ\text{C}$, $V_{IN} = 5\text{V}$ to 19V , and $\text{EN} = \text{LOW}$ unless otherwise noted. Note: See the schematic in Figure 28 for the location of the signals in these figures.

Figure 12. USB Adaptor Start-up: Ch1 = VBRIDGE, Ch2 = V_{in} , Ch3 = D-, Ch4 = D+

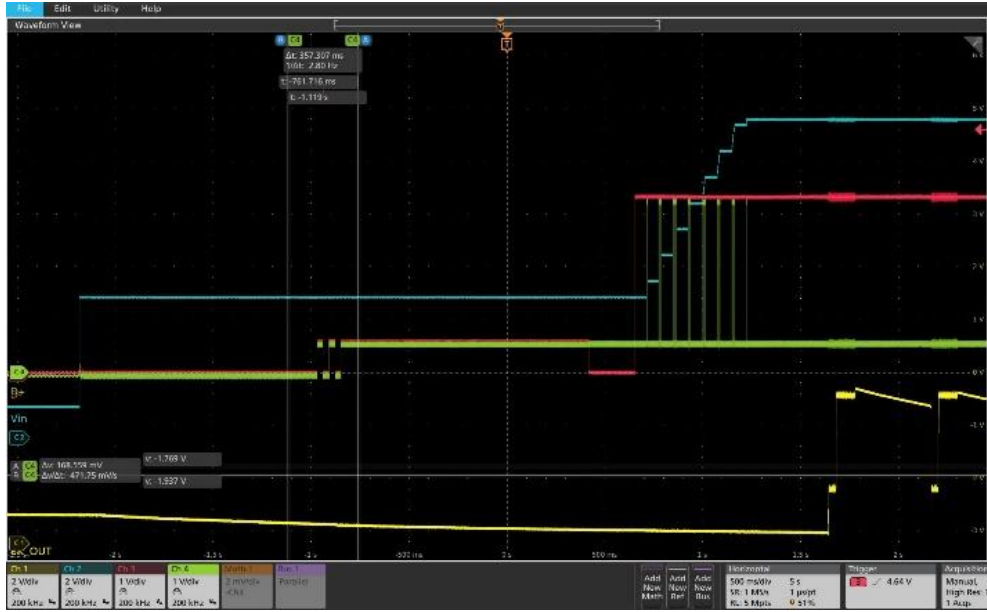
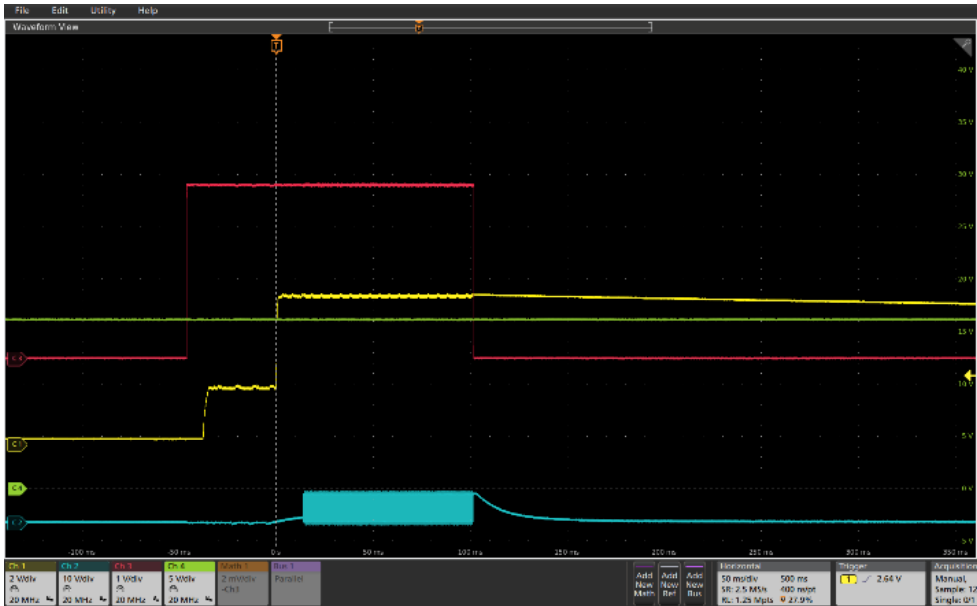


Figure 13. 19V Fixed Voltage Adaptor Start-up: Ch1 = VBRIDGE, Ch2 = V_{in} , Ch3 = GPIO_B4, Ch4 = i_{in}



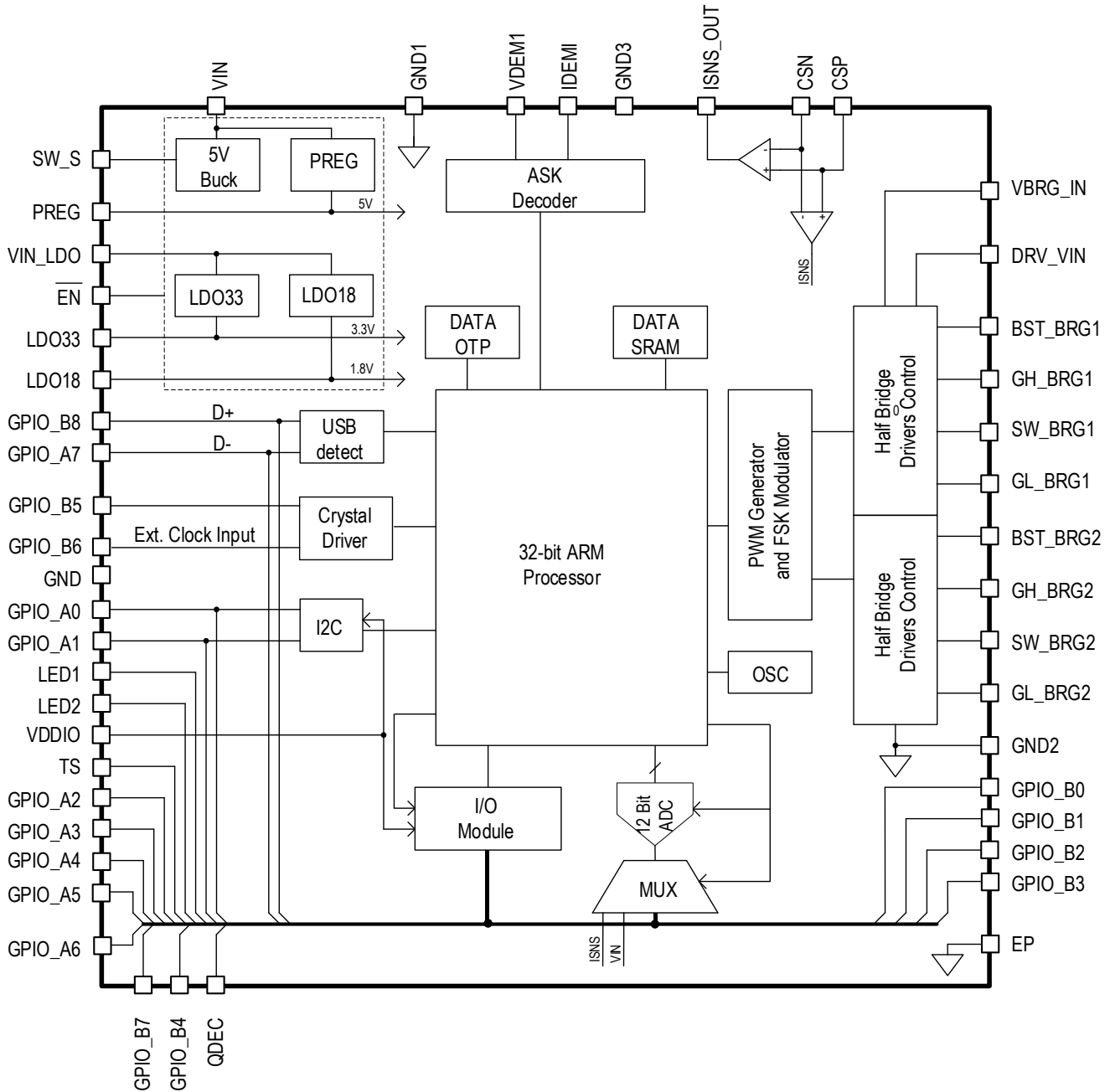
$V_{IN} = 5V$ to $19V$; $\overline{EN} = \text{LOW}$. The following performance characteristics were taken using a P9221-R, 15W Wireless Power Receiver (RX) at $T_A = +25^\circ\text{C}$ unless otherwise noted. Note: See the schematic in Figure 28 for the location of the signals in these figures.

Figure 14. Enable and Disable of External Buck Regulator: Ch1 = VBRIDGE, Ch2 = Tx_SW, Ch3 = GPIO_B4



6. Function Block Diagram

Figure 15 P9242-G Function Block Diagram



7. General Description

A wireless power charging system has a base station with one or more transmitters that make power available via DC-to-AC inverter(s) and transmit the power over a loosely-coupled inductor pair to a receiver in a mobile device. Before each transmitter and receiver pair starts transferring power, a power contract will be agreed upon and created by the RX and TX. The amount of power transferred to the mobile device is controlled by the wireless power receiver via sending communication packets to the transmitter to increase, decrease, or maintain the power level. If a fault is detected, the transmitter and receiver can also stop power transfer to protect the system. The communication packet from receiver to transmitter is purely digital and consists of logic 1's and 0's, which are added on top of the power link that exists between the transmitter (TX) and receiver (RX) coil. Amplitude shift keying (ASK) is used for the communication from receiver to transmitter; while communication from transmitter to receiver is achieved by frequency shift keying (FSK) modulation over the power signal frequency.

When the transmitter is not delivering power, it is in Standby Mode. The transmitter remains in Standby Mode and periodically pings until it detects the presence of a receiver. Once an Extended Power Profile (EPP) receiver is detected, such as the P9221-R or equivalent, the transmitter may provide up to 15W of output power depending on the power contract between the transmitter and receiver. If a Baseline Power Profile (BPP) receiver is present, the transmitter can deliver up to 5W of output power.

The P9242-G has features that ensure a high level of functionality and compliance with the WPC V1.2.4 specification requirements as illustrated in Figure 16, including a power path that efficiently achieves power transfer, a simple and robust communication demodulation circuit, safety and protection circuits, configuration, and status indication circuits.

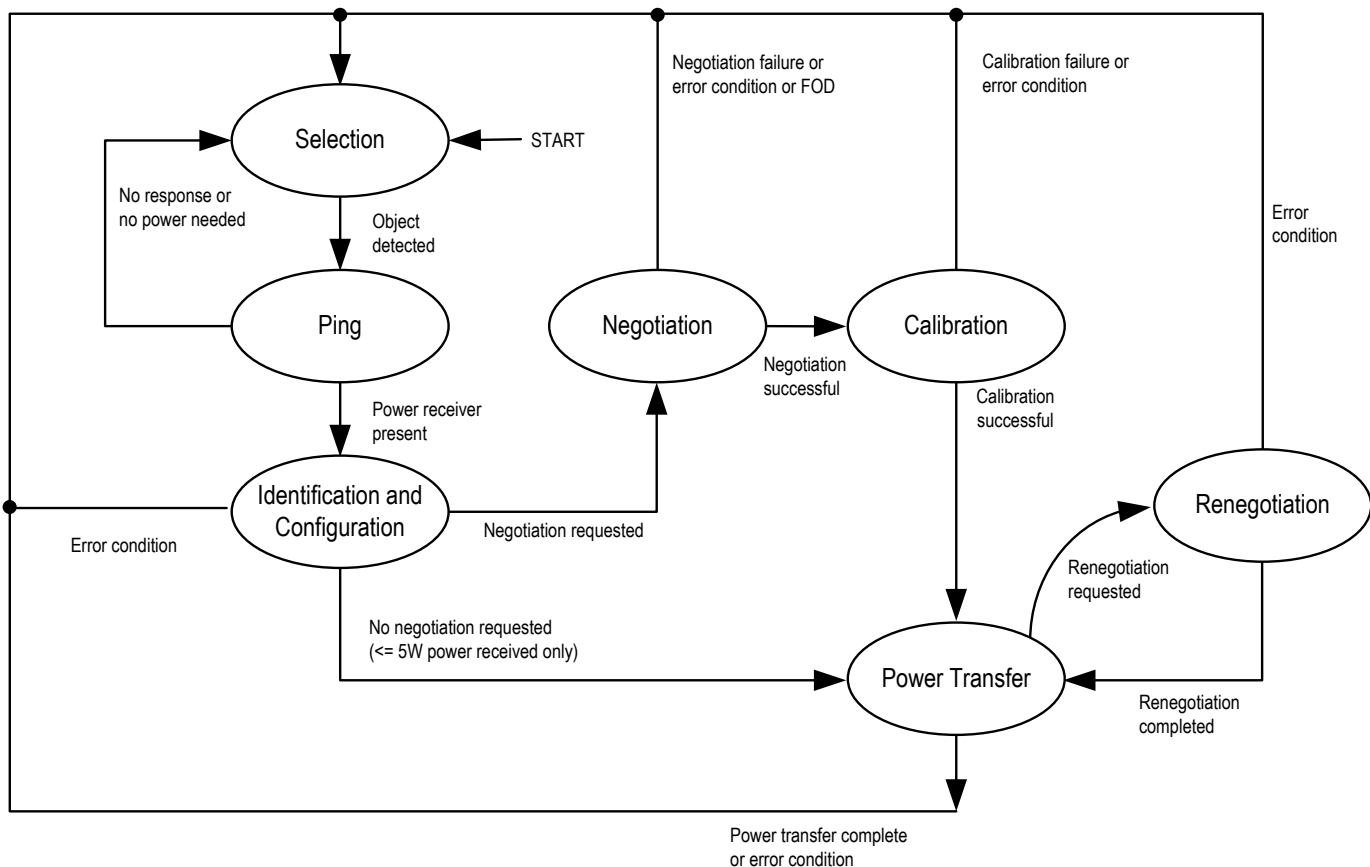
The P9242-G converges all popular wireless charging protocols including WPC Baseline Power Profile (BPP), Extended Power Profile (EPP), up to 7.5W charging for iPhones, and Android proprietary fast charging modes. Depending on the type and capability of the power supply, the P9242-G may operate in different modes. A USB adaptor detection circuit is also implemented in P9242-G by firmware. The P9242-G can detect input ports such as USB Standard Downstream Port (SDP), USB Charger Downstream Port (CDP), USB Dedicated Charging Port (DCP), and other AC/DC adaptors. When the connected power supply is limited at 5V, the P9242-G functions as a BPP transmitter and can deliver up to 5W at the Rx output.

The P9242-G supports constant and fixed frequency operation during power transfer. Under such application scenarios, the full-bridge input voltage is adjusted to control the P9242-G transmitted power, while its operating frequency is fixed at 127.7 kHz. The accuracy depends on that of the external clock or oscillator. If the IDT's clock IC is used, the accuracy of the operating frequency is guaranteed at 127.7 kHz, +/-6Hz. When using the Fixed-Frequency Operation Mode, an external step-down converter is employed in the P9242-G reference design to control the input voltage of the full-bridge inverter. Thus, the output of the step-down buck regulator is connected to the input of the P9242-G full-bridge inverter. A PWM signal from the P9242-G is employed to control the output of the buck regulator by adjusting its duty ratio. To respond to an increase or decrease in the power request from receiver, the P9242-G regulates the duty ratio of the PWM signal accordingly.

8. WPC Mode Characteristics

The WPC-1.2.4 extended power profile wireless power specification has a Selection Phase, Ping Phase, Identification and Configuration Phase, Negotiation Phase, Calibration Phase, Power Transfer Phase, and Renegotiation Phase, as shown in Figure 16.

Figure 16. WPC Power-Transfer Phases Flow Chart



8.1 Selection Phase

In the Selection Phase, the power transmitter determines if it will proceed to the Ping Phase after detecting the placement of an object. In this phase, the power transmitter typically monitors the interface surface for the placement and removal of objects using a measurement signal. This measurement signal is low level in order to not wake up a power receiver if it is positioned on the interface surface.

8.2 Ping Phase (Digital Ping)

In the Ping Phase, the power transmitter will start transmitting a power signal and will also detect the response from a possible power receiver. This response ensures that the power transmitter is linking to a power receiver rather than to some unknown object. When a WPC-compatible power receiver is placed on a WPC-compatible charging pad, it responds to the power signal by rectifying the power signal. When the receiver's internal bias voltage is greater than a specific threshold level, then the receiver is initiated, enabling the WPC communication protocol. If the power transmitter correctly receives a signal strength packet, the power transmitter proceeds to the Identification and Configuration Phase, maintaining the power signal output to the receiver.

8.3 Identification and Configuration Phase

This protocol extends the digital ping in order to enable the power receiver to communicate the relevant information in the Identification and Configuration Phase. The Identification and Configuration Phase is part of the WPC protocol so that the power transmitter and power receiver establish an initial default power transfer contract.

In the Configuration Phase, the power transmitter and receiver exchange information for a default power transfer contract as follows:

- The power transmitter receives the configuration packet.
- If the power transmitter does not acknowledge the request (does not transmit FSK modulation), power receiver will assume a BPP transmitter is present.

8.4 Negotiation Phase

Under the scenario that both transmitter and receiver support the EPP, the Negotiation Phase will be initiated by the receiver to further fine-tune the default power contract established in the Configuration Phase. The power receiver sends negotiation requests to the power transmitter, such as general requests and specific requests, which the power transmitter can grant or deny. In addition, to improve its initial assessment of whether foreign objects are present, the power transmitter compares the quality factor reported by the power receiver with its own measurement. If the power transmitter detects a foreign object, it will return to the Selection Phase.

8.5 Calibration Phase

During the Calibration Phase, the power receiver provides information that the power transmitter can use to improve its accuracy to detect foreign objects during power transfer. The calibration can be divided into two different modes. Mode 1 is defined as light load calibration of the transmitted power and received power difference; Mode 2 is defined as the heavy load calibration of the power difference. If the transmitter does not send an ACK to the receiver in either Mode 1 or Mode 2, the receiver remains in the same mode and will not move on to the next stage.

8.6 Power-Transfer Phase

In this phase, the power transmitter and power receiver control the power transfer by means of the following packets:

- Control Error Packets (CEP)
- Received Power Packet (RPP, FOD-related)
- End Power Transfer (EPT) Packet

Once a power contract is established, the transmitter initiates the Power Transfer Phase. The receiver's control and communication circuit sends control error packets to the transmitter to adjust the rectifier voltage to the level required to maximize the efficiency of the linear regulator, and to send to the transmitter the actual received power packet for foreign-object detection (FOD) to guarantee safe, efficient power transfer.

In the event of an EPT issued by the receiving device, the receiver will send an EPT packet to the transmitter and the transmitter can terminate the existing power transfer.

9. Application Information

9.1 Internal Power Supply and Internal Bias

The P9242-G has integrated internal buck regulators and internal LDOs to provide internal power.

9.1.1 Integrated Step-Down Regulator

To provide a power supply for the P9242-G internal circuitry as well as to reduce the power loss from a wide input voltage range, a step down buck regulator is integrated. It is internally compensated for the convenience of design. It takes the power from the input voltage to the P9242-G and regulates the DC voltage to 5V for use as an internal VCC_5V supply.

The internal step-down regulator supplies the power to the integrated MOSFET driver circuits, the internal LDO18, and the LDO33 linear regulators. It must not be used to power any external load.

9.1.2 Linear Regulators – PREG, LDO33, and LDO18

The P9242-G has three low-dropout (LDO) regulators. The 5V pre-regulator (PREG) provides voltage for the internal bias. The PREG requires a 1μF ceramic bypass capacitor connected from the PREG pin to GND. This capacitor must be placed very close to the PREG pin. The PREG voltage regulator must not be externally loaded.

The LDO33 and LDO18 are used to bias the internal analog and digital circuit. The regulator's input voltage is supplied through the VIN_LDO pin. Both regulators require a 1μF ceramic capacitor from the pin to GND. Both the LDO18 and LDO33 regulators must not be externally loaded.

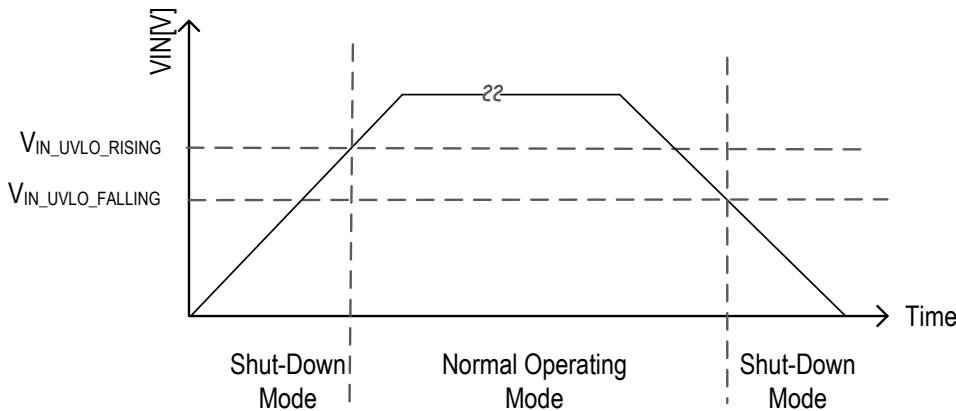
9.2 Enable Pin

The P9242-G device can be disabled by applying a logic HIGH to the \overline{EN} pin. When the voltage on the \overline{EN} pin is pulled HIGH, operation is suspended and the P9242-G is placed into the low-current Shut-Down Mode. If \overline{EN} is pulled LOW, the P9242-G is enabled and active. The rising and falling threshold for the \overline{EN} is specified in Table 5.

9.3 Software Under-Voltage Lock-Out (UVLO) Protection

The P9242-G has software UVLO features that protect the adaptor input port from being overloaded. For different adaptor voltages that are established, different UVLO levels are implemented. To guarantee proper functionality, the voltage on the VIN pin must be above the UVLO threshold. If the input voltage stays below the UVLO threshold, the P9242-G shuts down the system. If a software UVLO is triggered more than 3 times in a row, then the P9242-G will shut down, as an identified fault condition.

Figure 17. UVLO Threshold Definition



9.4 Die Temperature Protection

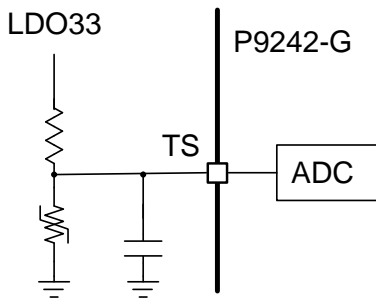
The P9242-G integrates die thermal shutdown circuitry to prevent damage resulting from excessive thermal stress that might be encountered under fault conditions. This circuitry will shut down or reset the P9242-G if the die temperature exceeds the threshold to prevent damage resulting from excessive thermal stress. An internal temperature protection block is enabled in the P9242-G that monitors the temperature inside the chip.

If the die temperature exceeds 140°C, the P9242-G shuts down and resumes when the internal temperature drops below 120°C.

9.5 External Temperature Sensing – TS

The P9242-G has a remote temperature sensor input, TS, which can be used to monitor an external temperature by using a thermistor. The built-in comparator's reference voltage is 0.6V with a 0.8V recovery voltage. Figure 18 below shows the temperature sensor circuits. Specific values for the thermistor and associated components are shown in Figure 28. Specific thermistor characteristics are included in the thermistor manufacturer's datasheet.

Figure 18. NTC Thermistor Connection to the TS Pin



To disable the thermistor, connect the TS pin to the LDO33 pin. Do not leave the TS pin floating.

9.6 Full-Bridge Driver

The transmitter switching frequency and duty cycle are controlled by the two groups of half-bridge drivers with bootstrap diodes that have been integrated into the P9242-G. Each driver is capable of driving a half bridge of two N-channel MOSFETs. The dead-time of each half-bridge can be set in the firmware to guarantee zero voltage switching as well as no risk of shoot-through. Each half-bridge driver can be controlled separately in the firmware, and thus the phase-shifted full-bridge or half-bridge can be enabled through the firmware.

The internal buck regulator provides 5V to both groups of half bridge driver circuits through the DRV_VIN pin. Applying any extra load on the internal buck regulator output is not recommended, since any extra load will compromise its loading capability and noise might be coupled into the half-bridge drivers.

9.7 LC Resonant Circuits

The LC resonant tank comprises a primary resonant coil (L_P) and series resonant capacitance (C_P). The LC resonant tank provides a resonant frequency at which it offers the minimum series resistance across the LC tank. The full-bridge or half-bridge inverter circuit drives the LC tank and operates above the LC resonant frequency to guarantee zero voltage switching at the transmitter side. The WPC-based transmitter is not specified to operate at the resonant frequency at any time.

The P9242-G is designed to support various Baseline Power Profile (BPP) and Extended Power Profile (EPP) coil configurations using half-bridge and full-bridge inverter topologies to drive the primary coil (L_P) and series resonant capacitors (C_P). Depending on the WPC coil configuration and specification, the coil inductance and series capacitance value can vary in a wide range. The transmitter coil specification must comply with the WPC definition. The WPC specification defines the transmitter coil self-inductance value, DC resistance (DCR), Q-factor, form factor, size, and number of turns. For the EPP coil configurations, MP-A11 and MP-A5 are supported by the P9242-G. For each WPC-specified transmitter coil configuration, the required resonant capacitance is also defined. High-voltage-rated, multi-layer ceramic capacitors that feature stable AC and DC characteristics (such as the C0G type) and stable temperature characteristics are highly recommended for this application.

9.8 WPC Communication Interface

9.8.1 Modulation/Communication

The WPC specification uses two-way communication for power transfer: receiver-to-transmitter and transmitter-to receiver.

Receiver-to-transmitter communication is accomplished by modulating the load applied to the receiver's coil; the communication is purely digital and logic 1's and 0's are modulated onto the power transfer signal waveform. Modulation is done with amplitude-shift keying (ASK) modulation with a bit-rate of 2Kbps. To the transmitter, this appears as an impedance change, which results in measurable variations of the transmitter's coil. The power transmitter demodulates this variation of the coil voltage to receive the packets.

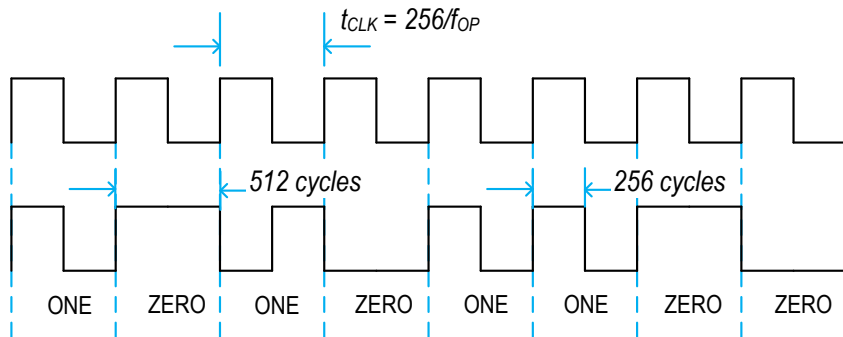
Transmitter-to-receiver communication is accomplished by frequency-shift keying (FSK) modulation over the power signal frequency. The power transmitter P9242-G has the capability to modulate FSK data onto the power transfer signal frequency and use it in order to establish the handshaking protocol with the power receiver.

9.8.2 Bit Decoding Scheme for FSK

The P9242-G implements FSK communication when used in conjunction with WPC-compliant receivers, such as the IDT P9221-R. The FSK communication protocol allows the transmitter to send data to the receiver using the power transfer link in the form of modulating the power transfer signal. This modulation appears in the form of a change in the base operating frequency (f_{OP}) of the modulated operating frequency (f_{MOD}) in periods of 256 consecutive cycles.

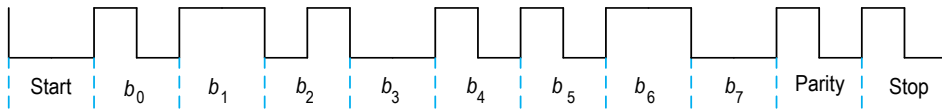
The FSK byte-encoding scheme and packet structure complies with the WPC specification revision 1.2.4. The FSK communication uses a bi-phase encoding scheme to modulate data bits into the power transfer signal. The start bit consists of 512 consecutive f_{MOD} cycles (or logic '0'). A logic 'ONE' value will be sent by sending 256 consecutive f_{OP} cycles followed by 256 f_{MOD} cycles or vice versa, and a logic 'ZERO' is sent by sending 512 consecutive f_{MOD} or f_{OP} cycles.

Figure 19. Example of Differential Bi-phase Encoding for FSK



Each byte will comply with the start, data, parity, and stop asynchronous serial format structure shown in Figure 20:

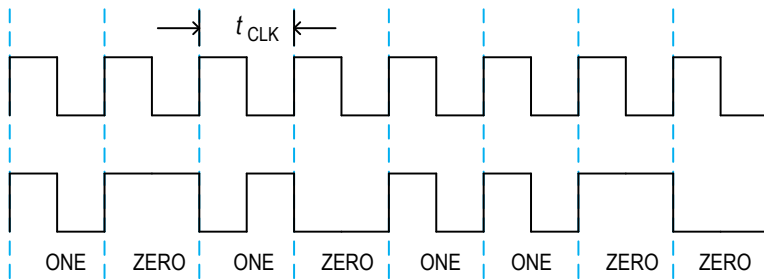
Figure 20. Example of Asynchronous Serial Byte Format for FSK



9.8.3 Bit Decoding Scheme for ASK

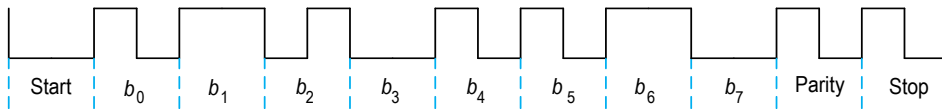
As required by the WPC specification, the P9242-G uses a differential bi-phase coding scheme to demodulate the data bits from the power transfer signal. A frequency of 2kHz is used for this purpose. A logic ONE bit is coded using two narrow transitions; a logic ZERO bit is encoded using one wider transition as shown below in Figure 21.

Figure 21. Bit Decoding Scheme



Each byte in the communication packet comprises 11 bits in an asynchronous serial format, as shown in Figure 22.

Figure 22. Byte Decoding Scheme



Each byte has a start bit, 8 data bits, a parity bit, and a single stop bit.

Each ASK communication packet has the following structure as shown in Figure 23.

Figure 23. Communication Packet Structure

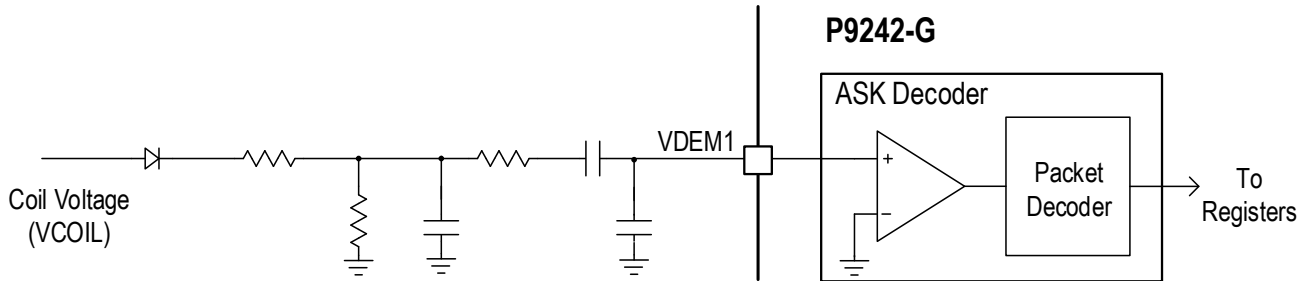
| | | | |
|----------|--------|---------|----------|
| Preamble | Header | Message | Checksum |
|----------|--------|---------|----------|

9.8.4 ASK Voltage Demodulation – VDEM1 Pin

In order to improve WPC ASK communication reliability under all loading conditions, the P9242-G has integrated two demodulation schemes: one based on input current information and the other based on coil voltage information. During the ASK communication initiated by the receiver, the envelope of the transmitter coil voltage reflects the ASK communication packet. The communication packet can be received by tracking the envelope of the coil voltage.

The voltage mode envelope detector is implemented using a combination of an RC-based filter as depicted on Figure 24 below. This simple implementation achieves the envelope detector function by combining a low-pass filter as well as a DC rejection filter.

Figure 24. Voltage Mode Envelope Detector



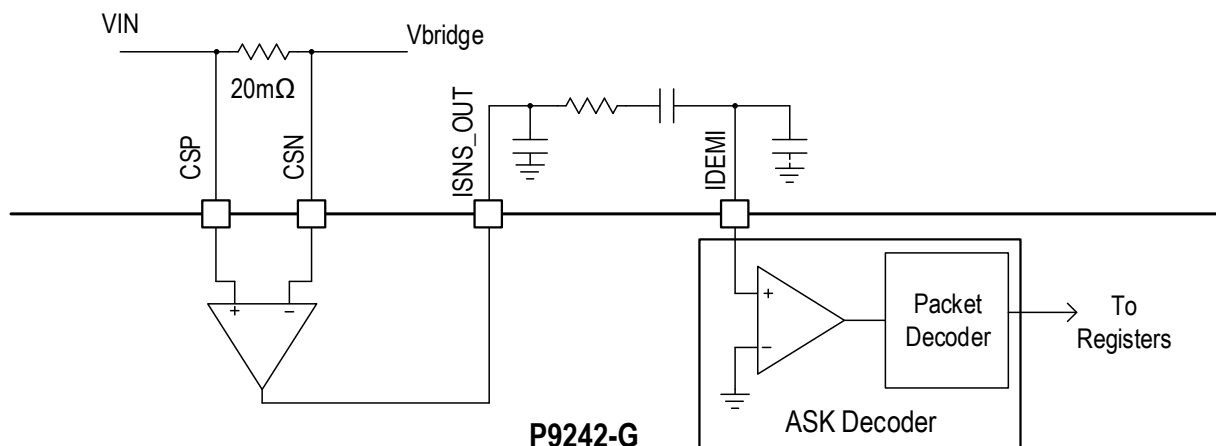
The filtered signal from the transmitter coil voltage will be processed by the P9242-G internal ASK decoder circuit, which includes an operational amplifier to automatically condition the filtered signals, and then a digital packet decoder to translate the signal into communication packets.

9.8.5 ASK Current Demodulation – IDEMI Pin

The ASK current demodulation scheme receives input current information from the current sense resistor, which carries the coil current modulation information on top of the averaged input current as shown in Figure 25. Similar to voltage demodulation circuits, an external discrete low-pass filter and DC filter between the ISNS_OUT and IDEMI pins provide additional filtering.

The packet decoder block is shared between the voltage and current detectors. The packet decoder selects either voltage information or current information from the filtered signals, depending upon which produces the better demodulated signal.

Figure 25. Current Mode Envelope Detector



9.9 General Purpose Input/output – GPIO Pins

The P9242-G has 11 GPIOs, some of which can be repurposed in the firmware to perform functions such as setting the advanced Q-factor thresholds and changing the LED patterns, etc.

9.9.1 Input Port Detection and Receiver Support – GPIO_A5, GPIO_A7, and GPIO_B8

The P9242-G supports input voltages in a wide range, such as a 5V, 9V, 12V, and 16V to 19V fixed DC power supply. Depending on the reference design and WPC coil configuration selection, the P9242-G can support a variety of receivers based on the input voltage as shown in Table 6.

When an AC/DC adaptor is connected to the P9242-G, it will detect if this is a USB port, based on the D+ and D- signals. In the case that a USB port is detected, the P9242-G will identify the type of USB port by executing the USB Battery Charging (BC 1.2) protocol on the D+ and D- signals. The P9242-G can adjust the input voltage to the highest level possible that enables as many receiver types as possible, as shown in Table 6. The GPIO_A5 and GPIO_A7 pins are used for D- detection and communication; GPIO_B8 is used for D+ detection and communication.

If the AC/DC adaptor is connected through a DC barrel jack or a fixed DC voltage, the P9242-G will set up the operation mode and support the corresponding receivers listed in Table 6.

When the DC source is 5V fixed, the P9242-G operates in the BPP Mode only and supports up to 5W. In this operation mode, the P9242-G disables the external power-stage buck regulator and enables an external MOSFET to bypass the buck regulator.

Table 6. Input Voltage vs. Receiver Supported

| Input Voltage/Current Rating | Receiver Supported |
|------------------------------|--------------------------------------|
| 5V/2A | BPP (Bypass External Buck Regulator) |
| 9V/1.67A | BPP 5W |
| | EPP, up to 8W |
| | Up to 7.5W charging for iPhones |
| 12V/2A | BPP 5W |
| | EPP, up to 10W |
| | Samsung AFC |
| | Up to 7.5W charging for iPhones |
| 16V to 19V/1.8A | BPP 5W |
| | EPP, up to 15W |
| | Samsung AFC |
| | Up to 7.5W charging for iPhones |

9.9.2 Foreign Object Detection – GPIO_A2 and GPIO_A3

When metallic objects, such as coins, keys, and paperclips, are exposed to alternating magnetic fields, the eddy current flowing through such objects will cause a power loss and the metallic object will exhibit a temperature increase. The amount of heat generated is a function of the strength and frequency of the magnetic field, as well as the characteristics of the object, such as resistivity, size, and shape. In a WPC-based wireless power system, the heat generated by the eddy current manifests itself as a power loss reducing the overall system efficiency. If appropriate actions are not taken, the heating could lead to unsafe conditions.

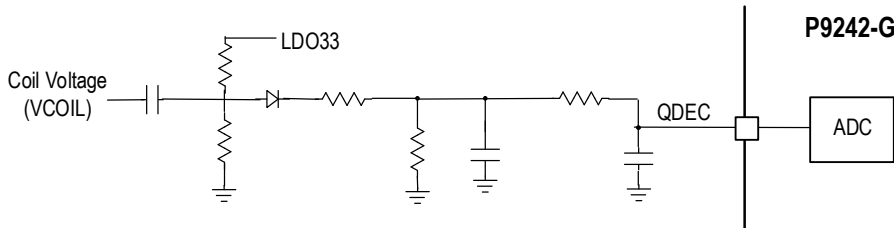
In the Extended Power Profile, there are two stages of foreign object detection (FOD). One stage is the measurement of the transmitter coil quality factor (Q-factor) prior to entering the Digital Ping Phase, and the other is a measurement of the power loss between the received power and the transmitted power during the Power Transfer Phase.

9.9.2.1 Quality Factor in the Digital Ping Phase – GPIO_A2

Prior to each digital ping, the P9242-G detects and measures the coil's quality factor (Q-factor). If an EPP receiver is present, the transmitter compares its own measured Q-factor with the reference Q-factor provided by EPP receiver. If the difference is considerably large, the P9242-G will identify this situation as a WPC-defined FOD being present and cannot move on to the Power Transfer Phase for the purpose of system protection. For BPP receivers, the P9242-G still detects and measures the Q-factor prior to each digital ping, but it does not do the compare since there is no reported Q-factor reference from BPP receivers.

The method implemented by P9242-G to detect the Q-factor is completely based on the nature of the LC resonant circuit. The transmitter LC resonant tank is first charged by a low voltage DC source to ensure that the Rx will not be powered up by using a small amount of energy. Until there is no AC current flowing from the DC source to the LC tank, the DC source voltage will be removed and the LC tank will be shorted. The energy previously stored in the LC resonant tank circulates between the coil and capacitors and generates resonant ringing naturally. The frequency and envelope of the resonant ringing are directly related to the Q-factor. Thus, the Q-factor can be calculated by detecting the envelope of the ringing with the circuit in in Figure 26 below.

Figure 26. Q-Factor Detection



To extend this feature and add Q-factor-based protection for BPP receivers as well, IDT has implemented a proprietary advanced open Q-factor detection and protection mechanism, which is different from the WPC-defined Q-factor. Even with no reference Q-factor from the receiver, the P9242-G still uses this advanced open Q-factor for BPP receivers, and it cannot move forward to the Power Transfer Phase if the advanced Q-factor is lower than the user pre-defined threshold. The pre-defined advanced open Q-factor threshold can be set up based on the voltage across the GPIO_A2 pin as shown below in Table 7.

Table 7. Voltage on GPIO_A2 vs. Advanced Q-Factor Threshold

Note: Do not set the GPIO_A2 voltage close to the endpoints of the selected range.

| Voltage on GPIO_A2 | Advanced Open Q-Factor Threshold |
|-------------------------------|----------------------------------|
| $0V \leq V_{GPIO_A2} < 0.4V$ | Feature Disabled |
| $0.4V < V_{GPIO_A2} < 0.5V$ | 13 |
| $0.5V < V_{GPIO_A2} < 0.6V$ | 16 |
| $0.6V < V_{GPIO_A2} < 0.7V$ | 19 |
| $0.7V < V_{GPIO_A2} < 0.8V$ | 22 |

| Voltage on GPIO_A2 | Advanced Open Q-Factor Threshold |
|------------------------------|----------------------------------|
| $0.8V < V_{GPIO_A2} < 0.9V$ | 25 |
| $0.9V < V_{GPIO_A2} < 1V$ | 28 |
| $1V < V_{GPIO_A2} < 1.1V$ | 31 |
| $1.1V < V_{GPIO_A2} < 1.2V$ | 34 |
| $1.2V < V_{GPIO_A2} < 1.3V$ | 37 |
| $1.3V < V_{GPIO_A2} < 1.4V$ | 40 |
| $1.4V < V_{GPIO_A2} < 1.5V$ | 43 |
| $1.5V < V_{GPIO_A2} < 1.6V$ | 46 |
| $1.6V < V_{GPIO_A2} < 1.7V$ | 49 |
| $1.7V < V_{GPIO_A2} < 1.8V$ | 52 |
| $1.8V < V_{GPIO_A2} < 1.9V$ | 55 |
| $1.9V < V_{GPIO_A2} < 2V$ | 58 |
| $2V < V_{GPIO_A2} < 2.1V$ | 61 |
| $2.1V < V_{GPIO_A2} < 2.2V$ | 64 |
| $2.2V < V_{GPIO_A2} < 2.3$ | 67 |
| $2.3V < V_{GPIO_A2} < 2.4V$ | 70 |

9.9.2.2 Power Difference in the Power Transfer Phase – GPIO_A3

The second stage of the foreign object detection is achieved during the Power Transfer Phase. The power loss is calculated between the reported received power and the transmitted power, which is constantly measured and compared with the WPC-specified thresholds. In normal power transfers, the power difference between received power and transmitted power (power loss) is constantly lower than the pre-set threshold. However, if a foreign object has been placed on its surface and is able to be coupled with the magnetic flux, this can generate additional power loss, which can become significantly large. If the loss is higher than the threshold set by the WPC-specification, the power loss FOD protection mechanism will be triggered and the transmitter will shut down the whole system to avoid over-heating and a potentially unsafe situation.

The power loss can be different based on the component selection, PCB layout, and end-product casing. Therefore, it must be adjusted according to each design. The P9242-G has a set of default power-loss FOD thresholds loaded in the firmware. It can be modified based on the voltage across GPIO_A3 as shown in Table 8.

Note: GPIO_A3 is a multi-function pin, which also used to set the LED pattern. Refer to section 9.9.7 for the LED pattern settings.

Table 8. Voltage on GPIO_A3 vs. FOD Threshold

Note: Do not set the GPIO_A3 voltage close to the endpoints of the selected range.

| Voltage on GPIO_A3 (V) | Power Difference FOD Threshold |
|-------------------------------|--------------------------------|
| $0V \leq V_{GPIO_A3} < 0.7V$ | Default values |
| $0.7V < V_{GPIO_A3} < 1.4V$ | 2 x default values |
| $1.4V < V_{GPIO_A3} < 2.1V$ | 3 x default values |
| $2.1V < V_{GPIO_A3} < 2.4V$ | 4 x default values |

9.9.3 Control of External Power Stage DC/DC Buck Regulator – GPIO_B4 and GPIO_B7

To regulate the receiver output voltage, as well as to regulate the system's delivered power, the transmitter adjusts the DC/AC inverter switching frequency, duty cycle, or DC/AC inverter input voltage. For the WPC coil configurations that operate at a fixed frequency and require adjusting the inverter bridge input voltage, the P9242-G supports these coil configurations by employing an external front-end DC/DC stage. The external DC/DC is part of the power stage, which connects between the input voltage and the DC/AC inverter.

For Apple 7.5W charging mode, the P9242-G supports fixed and precise switching frequency at 127.7kHz, and thus its bridge input voltage must be adjusted. Another stage of the external buck regulator is added to regulate the input voltage of the full bridge LC circuits. GPIO_B4 is employed to enable/disable this external DC/DC buck regulator. GPIO_B7 generates a PWM signal that is applied on top of the feedback pin of the buck regulator through a low-pass filter to fine-tune the output voltage of the buck regulator. The resolution of the buck regulator output depends on the buck IC's internal reference voltage, output voltage range, buck regulator compensation design, and resolution of the PWM signal from GPIO_B7.

9.9.4 Bypass External DC/DC Buck Regulator– GPIO_A4

When the input voltage is 5V only, the P9242-G operates in the BPP Mode to support legacy adaptors, as shown in Table 6. However, enabling the external power stage buck regulator at this time compromises the efficiency, thermal performance, and maximum power that can be delivered to the receiver. Under such an application scenario, the P9242-G will disable the external power stage buck regulator and enable another power path for the input voltage (5V) to be directly applied to the DC/AC inverter. GPIO_A4 is used to bypass the external power stage buck regulator. In this mode, the P9242-G operates in a mode for a fixed input voltage with variable frequency. The operating frequency range depends on the WPC coil configuration specification.

9.9.5 Coil Over-Voltage Control – GPIO_A6

Under the EPP working mode, the voltage across the transmitter coil could be excessive as the bridge input and frequency changes. Some unprotected receivers might risk being damaged or malfunction if placed on top of the transmitter coil immediately after another receiver is removed. When the voltage across the transmitter coil is too high, the P9242-G will open an additional switch via GPIO_A6 and cause a reduction in the coil voltage.

9.9.6 External Oscillator– GPIO_B5 and GPIO_B6

To guarantee that the operating frequency is precisely at 127.7kHz within a tolerance of +/-50 ppm under different temperature conditions, the P9242-G requires an external oscillator to provide accurate frequency operation. The PLL and crystal driver circuits inside the P9242-G guarantee that the internal clock for the ARM® Cortex®-M0 core is synchronized with the external oscillator frequency.

GPIO_B6 is used as the external oscillator frequency synchronization input. Either a clock IC or another oscillator can be used to generate 6.16791MHz. GPIO_B5 must be connected to GND and cannot be used for other applications if GPIO_B6 is used as the external frequency synchronization pin.

9.9.7 LED Pattern Selection – GPIO_A3

The P9242-G uses two LED outputs to indicate the power transfer status, faults, and operating modes depending on the voltage level on the GPIO_A3 pin. The GPIO_A3 pin also programs the power difference FOD thresholds (see section 9.9.2.2). The LEDs are connected to the LED1 and LED2 pins as shown in the typical application schematic in Figure 28. The LED pattern can be selected using the external resistor divider based on Table 9.

Table 9. Resistors for Setting the LED Pattern

Note: Do not set the GPIO_A3 voltage close to the endpoints of the selected range.

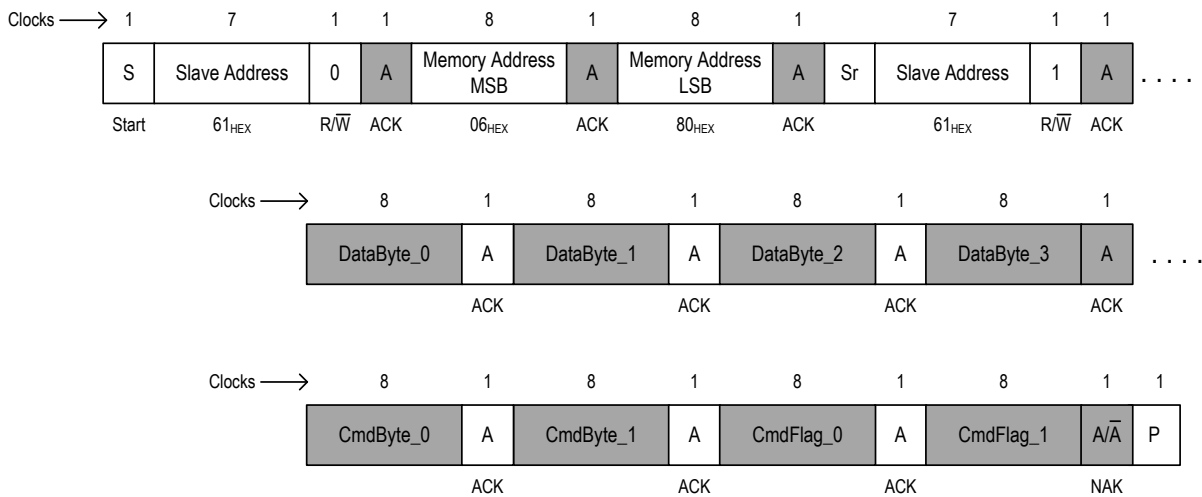
| Option | Voltage on GPIO_A3 Pin | LED1/LED2 Pin | Status | | | |
|--------|-------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|-----------|----------|-----------|
| | | | Standby | Transfer | Complete | Fault |
| 1 | $0V \leq V_{GPIO_A3} < 0.1V$; $0.7V < V_{GPIO_A3} < 0.8V$; $1.4V < V_{GPIO_A3} < 1.5V$; $2.1V < V_{GPIO_A3} < 2.4V$ | LED2 | Off | On | Off | Off |
| | | LED1 | Off | Off | Off | Blink 4Hz |
| 2 | $0.1V < V_{GPIO_A3} < 0.2V$; $0.8V < V_{GPIO_A3} < 0.9V$; $1.5V < V_{GPIO_A3} < 1.6V$ | LED2 | On | On | Off | Off |
| | | LED1 | On | Off | Off | Blink 4Hz |
| 3 | $0.2V < V_{GPIO_A3} < 0.3V$; $0.9V < V_{GPIO_A3} < 1.0V$; $1.6V < V_{GPIO_A3} < 1.7V$ | LED2 | Off | Blink 1Hz | On | Blink 4Hz |
| | | LED1 | Off | Off | Off | Off |
| 4 | $0.3V < V_{GPIO_A3} < 0.4V$; $1.0V < V_{GPIO_A3} < 1.1V$; $1.7V < V_{GPIO_A3} < 1.8V$ | LED2 | Off | On | Off | Blink 4Hz |
| | | LED1 | Off | Off | Off | Off |
| 5 | $0.4V < V_{GPIO_A3} < 0.5V$; $1.1V < V_{GPIO_A3} < 1.2V$; $1.8V < V_{GPIO_A3} < 1.9V$ | LED2 | On | Blink 1Hz | On | Off |
| | | LED1 | On | Off | Off | Blink 4Hz |
| 6 | $0.5V < V_{GPIO_A3} < 0.6V$; $1.2V < V_{GPIO_A3} < 1.3V$; $1.9V < V_{GPIO_A3} < 2.0V$ | LED2 | Off | Off | On | Off |
| | | LED1 | Off | On | Off | Blink 4Hz |
| 7 | $0.6V < V_{GPIO_A3} < 0.7V$; $1.3V < V_{GPIO_A3} < 1.4V$; $2.0V < V_{GPIO_A3} < 2.1V$ | LED2 | Off | Blink 1Hz | On | Off |
| | | LED1 | Off | Off | Off | Blink 4Hz |

9.9.8 I2C Communication Interface – GPIO_A0 and GPIO_A1

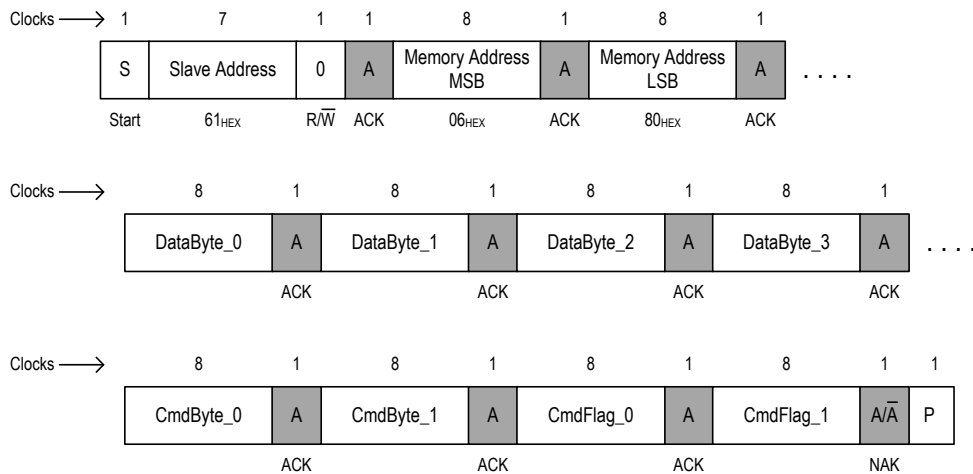
The P9242-G supports the standard I2C interface. The default I2C slave address is 61_{HEX}. GPIO_A0 serves as the I2C clock line, and GPIO_A1 serves as the I2C data line. Figure 27 shows the READ and WRITE protocol structure that the external I2C master must use to communicate with the P9242-G.

Figure 27. I2C Access Read Protocol and Write Protocol

Read Protocol



Write Protocol



| | | |
|---------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|------------------------------|
| From Master | A = Acknowledge (SDA LOW) | LSB = Least Significant Byte |
| From Slave | Ā = Not Acknowledge (SDA HIGH) | MSB = Most Significant Byte |
| | S = Start Condition | |
| | Sr = Restart Condition | |
| | P = Stop Condition | |

9.9.9 External Memory – GPIO_B0, GPIO_B1, GPIO_B2, and GPIO_B3

The P9242-G requires an external flash memory in which the firmware must be programmed during the development stage. The P9242-G accesses external flash memory using the SPI interface to upload the firmware into the internal SRAM. The Winbond W25X20CLUXIG is the recommended external flash memory.

The GPIO_B0, GPIO_B1, GPIO_B2, and GPIO_B3 pins are used for the external flash memory read and write.

10. Register Addresses and Definitions

The tables in this section provide a comprehensive list of address locations, field names, available operations (R or RW), default values, and functional descriptions of all internally accessible registers in the P9242-G. The default I2C slave address is 61_{HEX}. The address of each register is 16 bits. Note that some values require multiple registers and therefore span multiple addresses. For example, the address of the device ID high byte is 0001_{HEX} and the low byte address is 0000_{HEX}.

Table 10. Read Register – Device ID Register

| Address and Bit | Register Field Name | R/W | Default | Function and Description |
|---------------------|---------------------|-----|-------------------|--------------------------|
| 0000 _{HEX} | Device_ID [7:0] | R | 42 _{HEX} | Device ID low byte |
| 0001 _{HEX} | Device_ID [15:8] | R | 92 _{HEX} | Device ID high byte |

Table 11. Read Register – Firmware Revision

| Address and Bit | Register Field Name | R/W | Default | Function and Description |
|----------------------|---------------------|-----|-------------------|-----------------------------------|
| 00004 _{HEX} | FW_Major_Rev [7:0] | R | 18 _{HEX} | Major firmware revision low byte |
| 00005 _{HEX} | FW_Major_Rev [15:8] | R | 00 _{HEX} | Major firmware revision high byte |
| 00006 _{HEX} | FW_Rev [7:0] | R | 01 _{HEX} | Project code firmware version |
| 00007 _{HEX} | FW_Rev [15:8] | R | 00 _{HEX} | Customer code firmware version |

Table 12. Read Register – State Register

| Address and Bits | Register Field Name | R/W | Default | Function and Description |
|---------------------|---------------------|-----|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0707 _{HEX} | System State | R | - | 0 _{DEC} = Detection Phase 1 _{DEC} = Selection Phase 2 _{DEC} = Ping Phase 3 _{DEC} = ID Phase 5 _{DEC} = Configuration Phase 6 _{DEC} = Negotiation Phase 7 _{DEC} = Calibration Phase 8 _{DEC} = Power Transfer Phase 9 _{DEC} = Renegotiation Phase 10 _{DEC} = Remove Power |

Table 13. Read Register – Error Code Register

| Address and Bits | Register Field Name | R/W | Default | Function and Description |
|---------------------|----------------------|-----|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0614 _{HEX} | System Error [7:0] | R | 00 _{HEX} | Bit 0 = <i>End Power Transfer</i> command from receiver Bit 6 = Signal strength Bit 7 = WPC packager timeout |
| 0615 _{HEX} | System Error [15:8] | R | 00 _{HEX} | Bit 0 = Control Error Packet timeout Bit 1 = Received Power Packet timeout Bit 2 = Over-current protection during the Digital Ping Phase Bit 3 = Over-voltage Bit 4 = Under-voltage Bit 5 = FOD in power transfer Bit 6 = Over-temperature |
| 0616 _{HEX} | System Error [23:16] | R | 00 _{HEX} | Bit 1 = Over-current Bit 5 = Buck error Bit 6 = Q-factor FOD |

Table 14. Read Register – Adaptor Type Register

| Address and Bits | Register Field Name | R/W | Default | Function and Description |
|---------------------|---------------------|-----|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 070E _{HEX} | Adaptor Type | R | - | 0 _{DEC} = None 1 _{DEC} = USB SDP 2 _{DEC} = USB DCP 3 _{DEC} = USB CDP 4 _{DEC} = QC 2.0 5 _{DEC} = Other QC 12 _{DEC} = Adaptor detect error |

Table 15. Read Register – Potential Power Register

| Address and Bits | Register Field Name | R/W | Default | Function and Description |
|---------------------|---------------------|-----|---------|-----------------------------------|
| 083E _{HEX} | Potential_Power | R | - | Transmitter potential power in W. |

Table 16. Read Register – Input Current

| Address and Bits | Register Field Name | R/W | Default | Function and Description |
|---------------------|-----------------------------|-----|---------|-----------------------------------|
| 0664 _{HEX} | Bridge_input_current [7:0] | R | - | LSB of input current value in mA. |
| 0665 _{HEX} | Bridge_input_current [15:8] | R | - | MSB of input current value in mA. |

Table 17. Read Register – Input Voltage

| Address and Bits | Register Field Name | R/W | Default | Function and Description |
|---------------------|----------------------|-----|---------|----------------------------------|
| 0668 _{HEX} | Input_voltage [7:0] | R | – | LSB of coil voltage value in mV. |
| 0669 _{HEX} | Input_voltage [15:8] | R | – | MSB of coil voltage value in mV. |

Table 18. Read Register – Remote Temperature Sensing Voltage

| Address and Bits | Register Field Name | R/W | Default | Function and Description |
|---------------------|-------------------------------|-----|---------|----------------------------------|
| 06A4 _{HEX} | Thermistor pin voltage [7:0] | R | – | LSB of thermistor voltage value. |
| 06A5 _{HEX} | Thermistor pin voltage [15:8] | R | – | MSB of thermistor voltage value. |

Table 19. Read Register – Operating Frequency

$$f_{OP} = \frac{61.6791\text{MHz}}{FRE_CNT[15:0] + 2}$$

| Address and Bits | Register Field Name | R/W | Default | Function and Description |
|---------------------|---------------------|-----|---------|-----------------------------------|
| 0632 _{HEX} | FRE_CNT [7:0] | R | – | LSB of operating frequency count. |
| 0633 _{HEX} | FRQ_CNT [15:8] | R | – | MSB of operating frequency count. |

Table 20. Read Register – Transmitter Duty Cycle

$$D = \frac{FRE_CNT[7:0]}{511}$$

| Address and Bits | Register Field Name | R/W | Default | Function and Description |
|---------------------|---------------------|-----|---------|--------------------------|
| 05CF _{HEX} | Transmitter_Duty | R | – | Transmitter duty cycle. |

Table 21. Read Register – Receiver Reported Q-factor

| Address and Bits | Register Field Name | R/W | Default | Function and Description |
|---------------------|---------------------|-----|---------|--------------------------|
| 083D _{HEX} | Reported_Q | R | – | Reported Q value. |

Table 22. Read Register – Transmitter Detected WPC Q-Factor

| Address and Bits | Register Field Name | R/W | Default | Function and Description |
|---------------------|---------------------|-----|---------|-----------------------------|
| 06FA _{HEX} | Q_factor_1 [7:0] | R | – | LSB of first-time Q-factor |
| 06FB _{HEX} | Q_factor_1 [15:8] | R | – | MSB of first-time Q-factor |
| 06FC _{HEX} | Q_factor_2 [7:0] | R | – | LSB of second-time Q-factor |
| 06FD _{HEX} | Q_factor_2 [15:8] | R | – | MSB of second-time Q-factor |

Table 23. Read Register – Transmitter Detected Advanced Q-Factor

| Address and Bits | Register Field Name | R/W | Default | Function and Description |
|---------------------|-----------------------|-----|---------|--------------------------------------|
| 06F4 _{HEX} | Adv_Q_factor_1 [7:0] | R | – | LSB of first-time advanced Q-factor |
| 06F5 _{HEX} | Adv_Q_factor_1 [15:8] | R | – | MSB of first-time advanced Q-factor |
| 06F6 _{HEX} | Adv_Q_factor_2 [7:0] | R | – | LSB of second-time advanced Q-factor |
| 06F7 _{HEX} | Adv_Q_factor_2 [15:8] | R | – | MSB of second-time advanced Q-factor |

Table 24. Read Register – Transmitter Power 32 Bit

| Address and Bits | Register Field Name | R/W | Default | Function and Description |
|---------------------|---------------------|-----|---------|-------------------------------------------|
| 0880 _{HEX} | Tx_Power [7:0] | R | – | LSB of transmitter power, low byte in mW |
| 0881 _{HEX} | Tx_Power [15:8] | R | – | MSB of transmitter power, low byte in mW |
| 0882 _{HEX} | Tx_Power [23:16] | R | – | LSB of transmitter power, high byte in mW |
| 0883 _{HEX} | Tx_Power [31:24] | R | – | MSB of transmitter power, high byte in mW |

Table 25. Read Register – Received Power Packet Value 32 Bit

| Address and Bits | Register Field Name | R/W | Default | Function and Description |
|---------------------|---------------------|-----|---------|----------------------------------------------|
| 0884 _{HEX} | RPP_Value [7:0] | R | – | LSB of received power value, low byte in mW |
| 0885 _{HEX} | RPP_Value [15:8] | R | – | MSB of received power value, low byte in mW |
| 0886 _{HEX} | RPP_Value [23:16] | R | – | LSB of received power value, high byte in mW |
| 0887 _{HEX} | RPP_Value [31:24] | R | – | MSB of received power value, high byte in mW |

Table 26. Read Register – FOD Threshold 16 Bit

| Address and Bits | Register Field Name | R/W | Default | Function and Description |
|---------------------|---------------------|-----|---------|----------------------------------------------|
| 088C _{HEX} | FOD_TH [7:0] | R | – | LSB of current FOD threshold, low byte in mW |
| 088D _{HEX} | FOD_TH [15:8] | R | – | MSB of current FOD threshold, low byte in mW |

11. Power Dissipation and Thermal Requirements

The P9242-G is offered in a 48-pin QFN package that has a maximum power dissipation capability of approximately 1.47W. The maximum power dissipation of the package is determined by the number of thermal vias between the package and the printed circuit board (PCB). The maximum power dissipation of the package is defined by the die's specified maximum operating junction temperature, $T_{J(MAX)}$ of 125°C. The junction temperature rises when the heat generated by the device's power dissipation flow is impeded by the package-to-PCB thermal resistance.

The VFQFPN package offers a typical thermal resistance, junction to ambient (θ_{JA}), of 27.2°C/W when the PCB layout design is optimized as described in the *P9242-G Layout Guide* document. The techniques noted in the PCB layout section must be followed when designing the printed circuit board layout. Take into consideration possible proximity to other heat-generating devices when placing the P9242-G and the bridge FET packages in a given application design. The ambient temperature around the power IC will also have an effect on the thermal limits of an application. The main factors influencing θ_{JA} (in the order of decreasing influence) are PCB characteristics, the size of the thermal pad attached to the die/package (QFN), the thermal vias, and the final system hardware construction. Board designers should keep in mind that the package thermal metric θ_{JA} is impacted by the characteristics of the PCB. Changing the design or configuration of the PCB changes the overall thermal resistivity and the board's heat-sinking efficiency.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design.
- Improving the thermal coupling of the component to the PCB.
- Introducing airflow into the system.

First, the maximum power dissipation for a given situation should be calculated using Equation 1:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{AMB})}{\theta_{JA}} \tag{Equation 1}$$

Where: $P_{D(MAX)}$ = Maximum power dissipation

θ_{JA} = Package thermal resistance (°C/W)

$T_{J(MAX)}$ = Maximum device junction temperature (°C)

T_{AMB} = Ambient temperature (°C)

The maximum recommended operating junction temperature ($T_{J(MAX)}$) for the P9242-G is 125°C. The thermal resistance of the 48-pin QFN package is optimally $\theta_{JA} = 27.2^\circ\text{C/W}$. Operation is specified to a maximum steady-state ambient temperature (T_{AMB}) of 85°C. Therefore, the maximum recommended power dissipation is given by Equation 2.

$$P_{D(MAX)} = \frac{(125^\circ\text{C} - 85^\circ\text{C})}{27.2^\circ\text{C/W}} \cong 1.47\text{W} \tag{Equation 2}$$

All the previously mentioned thermal resistances are the values found when the P9242-G is mounted on a standard board of the dimensions and characteristics specified by the JEDEC 51 standard.

11.1 Typical Application Schematic

The typical application schematic provides a basic guideline for understanding and building a functional medium-power wireless power transmitter type MP-A11 as described in the WPC specifications. Other components, not shown on the typical application schematic might be needed in order to comply with other requirements, such as EMC/EMI or thermal specifications.

11.2 Bill of Materials (BOM)

Table 27. P9242-G Evaluation Kit v3.8 Bill of Materials

| Item | Quantity | Reference | Value | Description | Part Number | PCB Footprint |
|------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|-------------------------------------|-------------------------|---------------------------|
| 1 | 8 | VIN1, GND1, GND2, GND3, GND4, BK_VIN, VIN_SEL, GND | TP | TEST POINT PC MINIATURE SMT | 5015 | test_pt_s m_135x7 0 |
| 2 | 36 | V_BRIDGE1, VSNS_IN1, VDEM1, VCOIL1, SW_BRG1, IO_B1, ENB1, CSP1, CSN1, BRG1_LG, BRG1_HG, SW_BRG2, IO_B2, IO_A2, BRG2_LG, BRG2_HG, IO_B3, IO_A3, IO_B4, IO_A4, IO_B5, IO_A5, IO_A6, IO_B7, LDO18, LDO33, VCC5V1, SDA, SCL, Q_DEC, OTP, IO_B0, IDEM, EX_CLK, D-, D+ | NP | 30 GAUGE WIRE PAD | | TEST_PT 30DPAD |
| 3 | 1 | C1 | 0.1 μ F | CAP CER 0.1 μ F 25V X7R 0603 | GCM188R71E104KA5 7D | 0603 |
| 4 | 9 | C2, C7, C31, C32, C35, C42, C45, C55, C56 | 10 μ F | CAP CER 10 μ F 25V X5R 0603 | C1608X5R1E106M080 AC | 0603 |
| 5 | 19 | C3, C5, C8, C9, C11, C15, C16, C30, C33, C34, C38, C40, C46, C57, C62, C64, C66, C67, C68 | 0.1 μ F | CAP CER 0.1 μ F 25V X7R 0402 | C1005X7R1E104K050 BB | 0402 |
| 6 | 7 | C4, C6, C10, C22, C23, C24, C25 | 22 μ F | CAP CER 22 μ F 25V X5R 1206 | GRT21BR61E226ME1 3L | 1206 |
| 7 | 1 | C12 | 0.1 μ F | CAP CER 100nF 50V X5R 0402 | GRM155R71H104KE1 4J | 0402 |
| 8 | 11 | C13, C14, C17, C41, C52, C60, C61, C63, C65, C70, C71 | NP | | | 0402 |
| 9 | 2 | C18, C69 | 22nF | CAP CER 0.022 μ F 100V X7R 0603 | GCM188R72A223KA3 7D | 0603 |
| 10 | 1 | C19 | 5.6nF | CAP CER 5600pF 100V NPO 0603 | GRM188R72A562KA0 1D | 0603 |
| 11 | 2 | C20, C29 | 680pF | CAP CER 680pF 50V X7R 0402 | CL05B681KB5NNNC | 0402 |
| 12 | 1 | C21 | 22nF | CAP CER 22nF 25V X7R 0402 | GRM155R71E223JA61 D | 0402 |
| 13 | 1 | C26 | 1nF | CAP CER 1nF 100V X7R 0603 | GCM188R72A102KA3 7D | 0603 |
| 14 | 1 | C27 | 2.2nF | CAP CER 2.2nF 50V X7R 0402 | 04025C222KAT2A | 0402 |
| 15 | 1 | C28 | 56pF | CAP CER 56pF 50V NP0 0402 | CL05C560JB5NNNC | 0402 |

| Item | Quantity | Reference | Value | Description | Part Number | PCB Footprint |
|------|----------|--------------------|----------------|-----------------------------|----------------------|----------------------------------|
| 16 | 1 | C29 | 680pF | CAP CER 680pF 50V X7R 0402 | CL05B681KB5NNNC | 0402 |
| 17 | 1 | C36 | 47pF | CAP CER 47pF 50V X7R 0402 | 04025C470KAT2A | 0402 |
| 18 | 4 | C37, C43, C50, C53 | 1µF | CAP CER 1µF 25V X5R 0402 | C1005X5R1E105M050 BC | 0402 |
| 19 | 2 | C39, C59 | 22nF | CAP CER 22nF 50V X7R 0603 | GCM188R71H223KA3 7D | 0603 |
| 20 | 2 | C44, C47, | 100nF | CAP CER 100nF 100V C0G 1206 | GRM31C5C2A104JA0 1L | 1206 |
| 21 | 3 | C48, C49, C51 | 100nF | CAP CER 100nF 250V X7R 1206 | GRM31CR72E104KW 03L | 1206 |
| 22 | 1 | D1 | DDZ22ASF-7DICT | DIODE 300mW Zener | DDZ22ASF-7DICT-ND | sod123 |
| 23 | 2 | D2, D3 | BAV21W | DIODE 80V 125mA | BAV21W | sod123 |
| 24 | 1 | D4 | 1N4148 | DIODE 75V 200mA | 1N4148WX-TP | sod-323 |
| 25 | 2 | D5, D6 | SMAJ20CA-13-F | DIODE 300mW Zener | SMAJ20CA-13-F | SMAJ20 CA |
| 26 | 1 | D7 | NP | DIODE 80V 125MA | BAV21W | sod123 |
| 27 | 1 | D8 | BAT54S | DIODE ARRAY SCHOTTKY 30V | BAT54S | SOT-23 |
| 28 | 1 | J1 | AC_Adapter | CONN POWER JACK 2.5X5.5MM | PJ-002AH | CONN_P OWER_J ACK5_5 MM |
| 29 | 1 | J2 | USB Type C | CONN USB-C | 12401610E4#2ACT-ND | USB- C124016 10E4 |
| 30 | 1 | J3 | SIP con | 4 Pin Header | 961104-6404-AR | SIP-4 |
| 31 | 1 | J4 | 68000-105HLF | 5 Pin Header | 68000-105HLF | SIP-5 |
| 32 | 1 | J11 | 5P | CONN USB Micro | 90080004 | usb_micr o_ab |
| 33 | 3 | J13, J14, J15 | JUMPER | BERGSTIK STRAIGHT | 68000-102HLF | sip2 |
| 34 | 1 | LED1 | LED | LED RED | 150060RS75000 | 0603_dio de |
| 35 | 1 | LED2 | LED | LED GREEN | 150060GS75000 | 0603_dio de |
| 36 | 2 | LX1, LX2 | PTH_TP | 30 GAUGE WIRE PAD | NP | TP_TXCo il |
| 37 | 1 | L1 | NP | Common mode EMI choke | ACM4520-901-2P-T-000 | EMI_TDK _ACM452 0L |

| Item | Quantity | Reference | Value | Description | Part Number | PCB Footprint |
|------|----------|-----------------------------------------------------------------------------------------------|------------------|--------------------------------------|-----------------------------------------------|-------------------------|
| 38 | 1 | L2 | 0 | 0 | 0 | 1206 |
| 39 | 1 | L3 | 10 μ H | FIXED IND 10uH 3.6A 29mOhm | SWPA8040S100MT | 8 x 8 |
| 40 | 1 | L4 | 4.7 μ H | FIXED IND 4.7uH 620mA 500 m Ω | CIG10W4R7MNC | L0603 |
| 41 | 1 | L5 | 6.3 μ H | MP-A11 coil 6.3uH | MQQTC505030S6R3/ WTCL05054F- 6R3ABKS-70 | |
| 42 | 1 | Q1 | SIA453EDJ-T1_GE3 | MOSFET P-CH 30V | SIA453EDJ-T1-GE3 | Powerdi33 33_8ld_fet |
| 43 | 1 | Q2 | Si3417 | MOSFET P-CH 30 V | Si3417DV-T1-GE3 | SOT-23-6 |
| 44 | 2 | Q4, Q9 | 2N7002 | MOSFET N-CH 60V | 2N7002KT1G | SOT23_3 |
| 45 | 4 | Q5, Q6, Q7, Q8 | DMG7430L FG | MOSFET N-CH 30V | DMG7430LFG-7 | powerdi33 33_8ld_fet |
| 46 | 1 | Q10 | MMBT4403/SOT | TRANS PNP 40V 0.6A | SMMBT4403LT1G | SOT-23 |
| 47 | 1 | Q11 | 2N3904/TO | TRANS NPN 40V 0.2A | MMBT3904 | SOT-23 |
| 48 | 1 | Q12 | NP | MOSFET N-CH 60V | 2N7002KT1G | SOT-23 |
| 49 | 3 | R1,R2,R9 | 0 | RES SMD 0.0 OHM 1% 1/4W 1206 | RC1206JR-070R | 1206 |
| 50 | 1 | R3 | 150 Ω | RES SMD 150 OHM 1% 1/4W 0603 | RC0603FR-07150RL | 0603 |
| 51 | 3 | R4, R8, R87 | 100k Ω | RES SMD 100K OHM 1% 1/10W 0402 | RC0402FR-07100KL | 0402 |
| 52 | 12 | R5, R19, R28, R32, R53, R54, R59, R60, R61, R62, R65, R95 | 10k Ω | RES SMD 10K OHM 1% 1/10W 0402 | RC0402FR-0710KL | 0402 |
| 53 | 1 | R6 | 91k Ω | RES SMD 91K OHM 1% 1/10W 0402 | RC0402FR-0791K | 0402 |
| 54 | 3 | R7, R22, R25 | 10 Ω | RES SMD 10 OHM 1% 1/10W 0402 | RC0402FR-0710RL | 0402 |
| 55 | 1 | R11 | 150k Ω | RES SMD 150K OHM 1% 1/10W 0402 | RC0402FR-07150K | 0402 |
| 56 | 2 | R12, R15 | 30k Ω | RES SMD 30K OHM 1% 1/10W 0402 | RC0402FR-0730KL | 0402 |
| 57 | 1 | R13 | 18k Ω | RES SMD 18K OHM 0.1% 1/10W 0402 | RP73PF1E1K18BTD | 0402 |
| 58 | 1 | R14 | 3.3k Ω | RES SMD 3.3K OHM 1% 1/16W 0402 | RC0402FR-073K3P | 0402 |
| 59 | 4 | R16, R31, R50, R52 | 5.1k Ω | RES SMD 5.1K OHM 1% 1/10W 0402 | ERJ-2RKF5101X | 0402 |
| 60 | 2 | R17, R70 | NP | RES SMD 1% 1/10W 0402 | | 0402 |
| 61 | 19 | R18, R21, R39, R49, R67, R68, R69, R73, R76, R77, R80, R81, R82, R86, R88, R90, R93, R96, R97 | 0 | RES SMD 0.0 OHM 1% 1/16W 0402 | RC0402JR-070RL | 0402 |

| Item | Quantity | Reference | Value | Description | Part Number | PCB Footprint |
|------|----------|-----------------------------------------------------------------------------------------------|---------------|----------------------------------|----------------------|---------------|
| 62 | 1 | R20 | 2.4k Ω | RES SMD 2.4K OHM 5% 1/16W 0402 | RC0603FR-072K4L | 0603 |
| 63 | 1 | R23 | 200k Ω | RES SMD 200K OHM 1% 1/10W 0603 | RC1608F204CS | 0603 |
| 64 | 19 | R24, R33, R34, R37, R38, R51, R56, R66, R71, R72, R75, R78, R79, R84, R85, R89, R91, R92, R94 | NP | | | 0402 |
| 65 | 1 | R26 | 0.02 Ω | RES SMD 0.02 OHM 1% 1/3W 0805 | UCR10EVHFSR020 | 0805 |
| 66 | 1 | R27 | 51k Ω | RES SMD 51K OHM 1% 1/16W 0402 | RC0402FR-0751K | 0402 |
| 67 | 1 | R29 | 510 Ω | RES SMD 510 OHM 1% 1/16W 0402 | RC0402FR-07510RL | 0402 |
| 68 | 1 | R30 | 47k Ω | RES SMD 47K OHM 1% 1/5W 0402 | RCS040247K0FKED | 0402 |
| 69 | 4 | R35, R40, R44, R47 | 22 Ω | RES SMD 22 OHM 1% 1/16W 0402 | RC0402FR-0722RL | 0402 |
| 70 | 5 | R36, R42, R45, R48, R57 | 100k Ω | RES SMD 100K OHM 5% 1/10W 0402 | ERJ-2GEJ104X | 0402 |
| 71 | 2 | R41, R43 | 1k Ω | RES SMD 1K OHM 5% 1/16W 0402 | RC0402JR-071KL | 0402 |
| 72 | 1 | R46 | 680 Ω | RES SMD 680 OHM 5% 1/16W 0402 | RC0402JR-07680RL | 0402 |
| 73 | 1 | R55 | 33 Ω | RES SMD 33 OHM 0.5% 1/16W 0402 | ERA-2AKD330X | 0402 |
| 74 | 1 | R58 | 20k Ω | RES SMD 20K OHM 1% 1/10W 0402 | RC0402FR-0710KL | 0402 |
| 75 | 1 | R98 | 100 Ω | RES SMD 100 OHM 1% 1/10W 0402 | TNPW0402100RBEED | 0402 |
| 76 | 1 | TH_Coil1 | NP | | | 0805 |
| 77 | 1 | U1 | MP2229 | Buck Converter Chip | MP2229GQ | QFN-14 |
| 78 | 1 | U3 | P9242-G | Medium Power Transmitter | P9242-G | QFN-48 |
| 79 | 1 | U4 | MCP6021 | OPA, 10MHz R2R | MCP6021 | SOT23-5 |
| 80 | 1 | U5 | 6P40369 | Clock Generator | 6P40369NDGI | 5X2503 |
| 81 | 1 | U6 | NP | Oscillator | DSC6111MI2A-006.1679 | ASTMLP A-33 |
| 82 | 1 | U7 | W25X40CL UXIG | SPIFLASH 4M-BIT 4KB UNIFORM SECT | W25X40CLUXIG | uson_2x3_8LD |

12. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

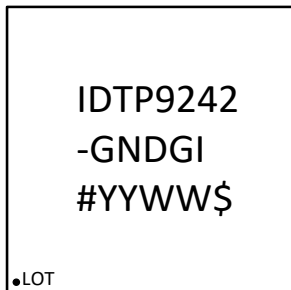
<https://www.idt.com/document/psc/48-vfqfn-package-outline-drawing-60-x-60-x-090-mm-body-epad-42-x-42-mm-040mm-pitch-ndg48p2>

13. Special Notes: P9242-G 48-VFQFPN Package Assembly

Unopened dry packaged parts have a one-year shelf life.

The HIC indicator card for newly-opened dry packaged parts should be checked. If there is any moisture content, the parts must be baked for a minimum of 8 hours at 125°C within 24 hours prior to the assembly reflow process.

14. Marking Diagram



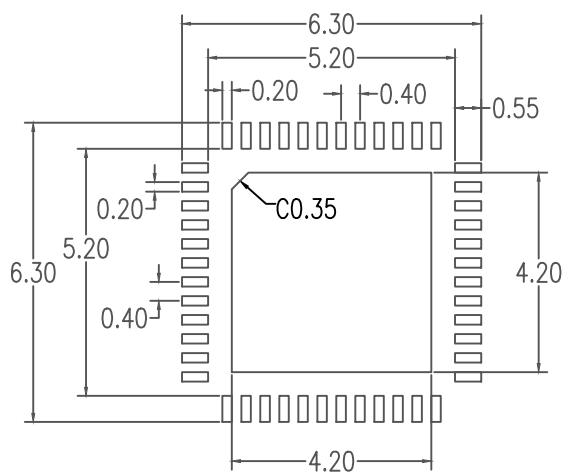
1. Line 1: Company name and part number.
2. Line 2: -G is part of the part number, which is followed by the package code.
3. Line 3: "YYWW" is the last two digits of the year and two digits for the week that the part was assembled. # is the device step. "\$" denotes the mark code.

15. Ordering Information

| Orderable Part Number | Description and Package | MSL Rating | Carrier Type | Ambient Temperature |
|-----------------------|------------------------------------------------------------------------------------|------------|--------------|---------------------|
| P9242-GNDGI | P9242-G Wireless Power Receiver for 15W Applications, 48-VFQFPN (6 x 6 mm) package | MSL3 | Tray | -40°C to +85°C |
| P9242-GNDGI8 | P9242-G Wireless Power Receiver for 15W Applications, 48-VFQFPN (6 x 6 mm) package | MSL3 | Reel | -40°C to +85°C |

16. Revision History

| Revision Date | Description of Change |
|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| February 17, 2019 | <ul style="list-style-type: none"> ▪ Updated the description of Item 59 in “Bill of Materials (BOM)” |
| November 19, 2018 | <ul style="list-style-type: none"> ▪ Revision of input voltage range given in previous version of the P9242-G Short-Form Datasheet. ▪ Revision of package-outline drawing. ▪ Revision of part codes. ▪ Revised LDO max current rating. ▪ Minor edits. |
| September 6, 2018 | Updates. |
| August 15, 2018 | Updates. |
| July 6, 2018 | Updates. |
| May 10, 2018 | Initial release. |
| February, 12, 2019 | Updates. |



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| Package Revision History | | |
|--------------------------|---------|-----------------------------------------------------------|
| Date Created | Rev No. | Description |
| July 24, 2018 | Rev 02 | New Format Change QFN to VFQFPN, Recalculate Land Pattern |
| Feb 25, 2020 | Rev 03 | Tolerance Format Change |

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