8-Channel 6.25Gbps Serial RapidIO™ Signal Repeater

89HP0608R
Data Sheet

Device Overview

The IDT 89HP0608R (P0608R) is a 1.25Gbps to 6.25Gbps Repeater IC that reconditions high-speed serial data streams. The device features IDT EyeBoost™ technology that compensates for cable and board trace attenuations and ISI jitter, thereby extending connection reach. The device is optimized for Serial RapidIO (SRIO) high-speed, serial differential data streams and contains eight data channels, each able to process up to 6.25Gbps transmission rates. Each channel consists of an input equalizer and amplifier, signal detection with glitch filter, as well as programmable output swing, slew rate, and de-emphasis with delay control. Since all of these features are user programmable, they allow for application specific optimization.

Besides the per channel programmable features, the P0608R provides global programmable settings - termination resistance values and transfer modes. The P0608R, with its many programmable receiver and transmitter features, is ideal for applications using any combination of cables and board trace materials.

All modes of active data transfer are designed with minimized power consumption. Also, a wide selection of power reducing modes allows the user to eliminate power of unused blocks, including a shutdown mode. In full shutdown mode, the part consumes less than 80mW in worst case environmental conditions.

Applications

- ATCA, µTCA
- Military, industrial, and imaging systems
- Open VPX and VITA 41/46 systems

Features

- Compensates for cable and PCB trace attenuation and ISI jitter
- Programmable receiver equalization up to 30db
- Programmable de-emphasis up to -8.5dB
- Minimized in-out latency of 300ps typical
- Recovers data stream even when the differential signal eye is completely closed due to trace attenuation and ISI jitter
- Full SRIO protocol support
- Configurable via I^2C interface
- Supports automatic download of configuration from external EEPROM with a single or multiple repeaters on I2C bus
- Leading edge power minimization in active and shutdown modes
- No external bias resistors or reference clocks required
- Channel mux mode, demux mode, 1 to 2 channels multicast, and Z-switch function mode
- Available in a 9x9mm 100-ball FPBGA package

Benefits

- Extends maximum cable length to over 10 meters and trace length over 65 inches in SRIO applications (short/medium/ long range and beyond long range)
- Speeds up system design time by allowing usage of longer trace and cable lengths
- Minimizes BER

Typical Application

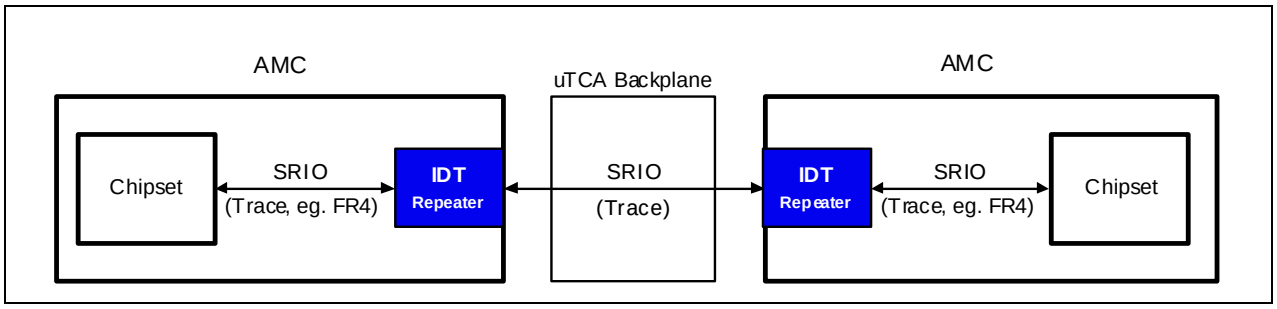


Figure 1 IDT Repeaters in µTCA

P0608R SRIO Compliance

The device was designed to provide end users with features needed to comply with SRIO system application requirements. It meets SRIO 2.1 specifications for DC and AC requirements as detailed in the Electrical Specifications section.

P0608R Block Diagram

The P0608R contains eight high speed channels as shown in Figure 2. Each channel can routed to different outputs. Depending on user configuration via mode selections, input traffic can be muxed, demuxed, or looped back. Please, refer to modes of operation chapter for details. To facilitate buffering of system clocks, the repeater provides 1:2 clock buffer as shown in the figure below. Powerdown (PDB) and Channel Enable (AEN0, etc.) pins are provided for easy state and channel control. Status output pins are available for monitoring critical states, such as the detection of high speed input signals (A0SIGDET, etc.).

Each channel's configuration and performance can be optimized via the I^2C interface (SCL, SDA). The programming option allows the user to optimize the repeater's performance in a wide range of applications, making it an ideal solution for most applications requiring cancellation of trace or cable attenuation and ISI jitter.

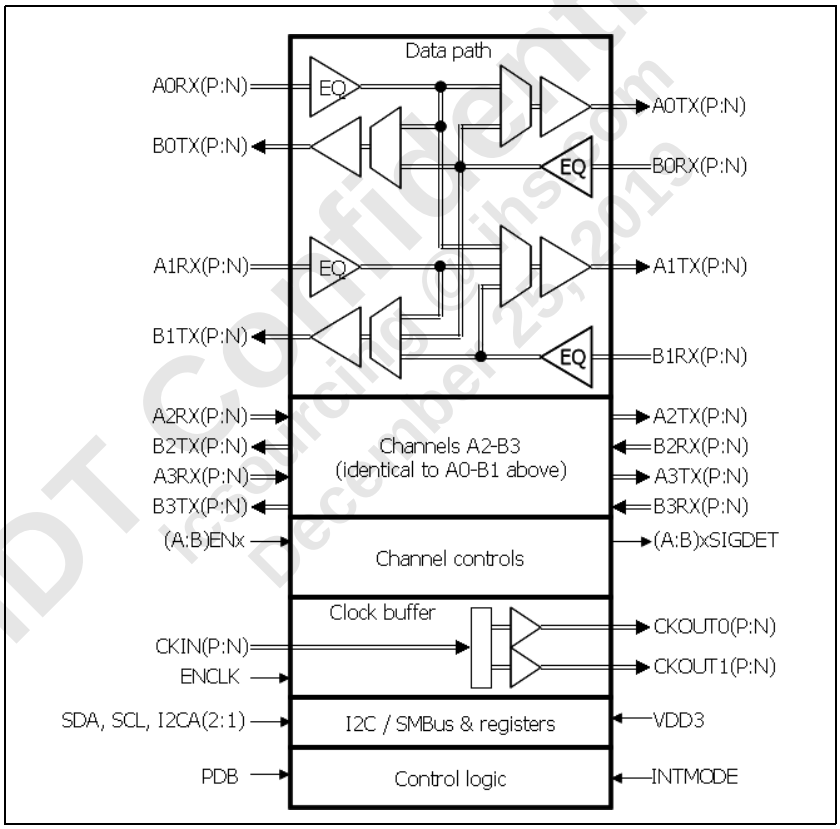


Figure 2 P0608R Block Diagram

Table of Contents

PAGE INTENTIONALLY LEFT BLANK

Data Units

The following data unit terminology is used in this document.

Term	Words	Bytes	Bits
Byte	1/2	1	8
Word	1	2	16
Doubleword (DWord)	2	4	32

Table 1 Data Unit Terminology

In doublewords, bit 31 is always the most significant bit and bit 0 is the least significant bit. In words, bit 15 is always the most significant bit and bit 0 is the least significant bit. In bytes, bit 7 is always the most significant bit and bit 0 is the least significant bit.

Register Terminology

Software in the context of this register terminology refers to modifications made by PCI Express root configuration writes, writes to registers made through the slave SMBus interface, or serial EEPROM register initialization. See Table 2.

Type	Abbreviation	Description
Hardware Initialized	HWINIT	Register bits are initialized by firmware or hardware mechanisms such as pin strapping or serial EEPROM. (System firmware hardware initialization is only allowed for system integrated devices.) Bits are read-only after initialization and can only be reset (for write-once by firmware) with reset.
Read Only and Clear	RC	Software can read the register/bits with this attribute. Reading the value will automatically cause the register/bit to be reset to zero. Writing to a RC location has no effect.
Read Clear and Write	RCW	Software can read the register/bits with this attribute. Reading the value will automatically cause the register/bits to be reset to zero. Writes cause the register/bits to be modified.
Reserved	Reserved	The value read from a reserved register/bit is undefined. Thus, software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. In addition to reserved registers, some valid register fields have encodings marked as reserved. Such register fields must never be written with a value corresponding to an encoding marked as reserved. Violating this rule produces undefined operation in the device.
Read Only	RO	Software can only read registers/bits with this attribute. Contents are hardwired to a constant value or are status bits that may be set and cleared by hardware. Writing to a RO location has no effect.

Table 2 Register Terminology (Part 1 of 2)

Type	Abbreviation	Description
Read and Write	RW	Software can both read and write bits with this attribute.
Read and Write Clear	RW1C	Software can read and write to registers/bits with this attribute. However, writing a value of zero to a bit with this attribute has no effect. A RW1C bit can only be set to a value of 1 by a hardware event. To clear a RW1C bit (i.e., change its value to zero) a value of one must be written to the location. An RW1C bit is never cleared by hardware.
Read and Write when Unlocked		Software can read the register/bits with this attribute. Writing to register/bits with this attribute will only cause the value to be modified if the REGUNLOCK bit in the SWCTL register is set. When the REGUNLOCK bit is cleared, writes are ignored and the register/bits are effectively read-only.

Table 2 Register Terminology (Part 2 of 2)

Functional Description

The P0608R has 8 channels, each with the individually programmable features listed below. Figure 3 diagrams the channel and Tables 3 and 4 summarize key configuration options.

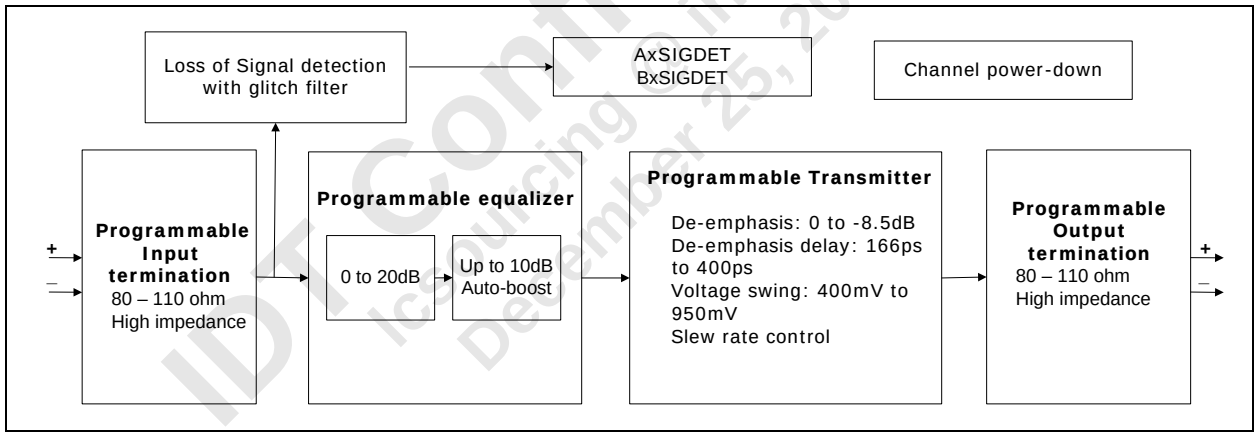


Figure 3 Channel Block Diagram with Channel Features

- Per-channel programmable features used at the RX side (ranges refer to I^2C programming method).
  - Input equalization with 11 levels: 0 to 20dB compensation for high frequency signal attenuation due to cables and board traces. Additionally, up to 10dB boost is added automatically by the equalizer for applications using long cables. The total equalization range is between 0dB and 30dB.
  - Input amplifier DC gain with 7 levels: -2dB to -14dB plus 4 levels for further tuning: -3db to 3dB. The total DC gain is the sum of 7-level gain and 3-level gain controls. This function can be useful for input signals with large swing.
  - Input loss of signal detection with 8 levels: 50mV pk-pk to 170mV pk-pk. Measures the envelope of the incoming differential signal (peak-to-peak) and puts the device in loss of signal mode when the envelope has fallen below a programmable threshold. In loss of signal mode, the transmitter stops toggling, and maintains its common-mode voltage level.

    Note: It is recommended to disable the Loss of Signal for typical SRIO applications not requiring loss-of-signal detection by programming both SIG_PD_TRANDET and SIG_PD_LVLDET bits to 1.
  - Input loss of signal detection glitch filter with 4 levels: 2.6ns to 4ns negative glitch removal avoids detection of extremely short spurious signal losses. This is an advanced feature with suggested default setting for most users.
  - Input high impedance control via channel enable: disabled (active mode) and hi-Z (power-down).

- Per-channel programmable features used at the TX side.
  - Output de-emphasis with 8 levels: 0 to -8.5dB. The de-emphasis boosts the magnitude of higher frequencies sent by the transmitter to compensate for high frequency losses travelling through output side cable or output side board traces. This ensures that the final received signal has a wider eye opening.
  - Output differential swing with 8 levels: 0.4V to 0.95V (peak-to-peak).
  - Output slew rate with 4 levels: 45ps to 150ps.
  - Output de-emphasis delay control with 4 levels: 166ps to 400ps. When used, this feature should be set to a value of 1UI, which is 166ps for 6Gbps rate, 200ps for 5Gbps rate, 333ps for 3Gbps rate, and 400ps for 2.5Gbps.
  - Individual channel power-down (includes Rx and Tx power-down).

In addition, the device contains global programmable settings:

- Input and output differential termination resistance with 4 levels: 80 ohm, 90 ohm, 100 ohm, 110 ohm.
- Transfer modes: direct connect, cross-connect, multicast, and loopback.

Power-Up

After the power supplies reach their minimum required levels, the P0608R powers up by setting all input and output pins to known states:

- All the device's input configuration pins are set internally to VSS or VDD for 2-level pins and to VDD/2 for 3-level pins.
- High speed differential input and output pins, status output pins indicating signal detection at high speed inputs, and signal detection outputs depend on various conditions described below:
  - High speed differential input and output pins are in high impedance if any of the following conditions is true:
    - Powerdown is set (PDB pin = 0V) or
    - Channels containing high speed differential inputs are disabled via pins (eg. A0EN) or

    In all other cases, high speed differential input and output pins are set to 50 ohms per pin, with 100 ohms differential impedance. Also refer to Table 5, Power Reducing Modes.
  - Status output pins indicating signal detection at high speed inputs (A0SIGDET, A1SIGDET, etc.) are at 0V if:
    - Corresponding (A0, A1, etc.) channel inputs do not swing or swing below the programmed threshold levels or
    - Corresponding channel enable pins (A0EN, A1EN, etc.) are at 0V or
    - Powerdown is set (PDB pin = 0V)

    In all other cases, these output pins are at VDD level.
- Other power-up settings:
  - If INTMODE=VSS then the programming pins are ignored and the register values are used for programming P0608R settings (I^2C slave mode).
  - If INTMODE=VDD then the P0608R is in I^2C master mode (used when external EEPROM is needed).

Power-Up/Power-Down Sequencing

To avoid potential damage to the part, adhere to the following sequence during power supply ramp-up:

- VDD3 supply must be ramped-up and stable at 3.3V prior to VDD supply reaching 1.2V
- Power ramp-up time for VDD should be less than 1ms to avoid potential I^2C reset issues.

Note: VDD3 supply should be common to all devices communicating on the same I^2C bus.

The power-down sequence can occur in any order.

IDT EyeBoost™ Technology

IDT EyeBoost™ technology is a method of data stream recovery of data stream even when the differential signal eye is completely closed due to cable or trace attenuation and ISI jitter. With IDT EyeBoost™ technology™, the system designer can both recover the incoming data and retransmit it to target device with a maximized eye width and amplitude. An example of IDT EyeBoost™ technology usage in a system application and eye diagram results are shown in Figure 4. In this figure, the (a) diagram shows incoming differential signal (closed eye) after 62 inch FR4 connection from signal source and the (b) diagram shows differential signal at the output of repeater maximized eye opening with IDT EyeBoost™ technology.

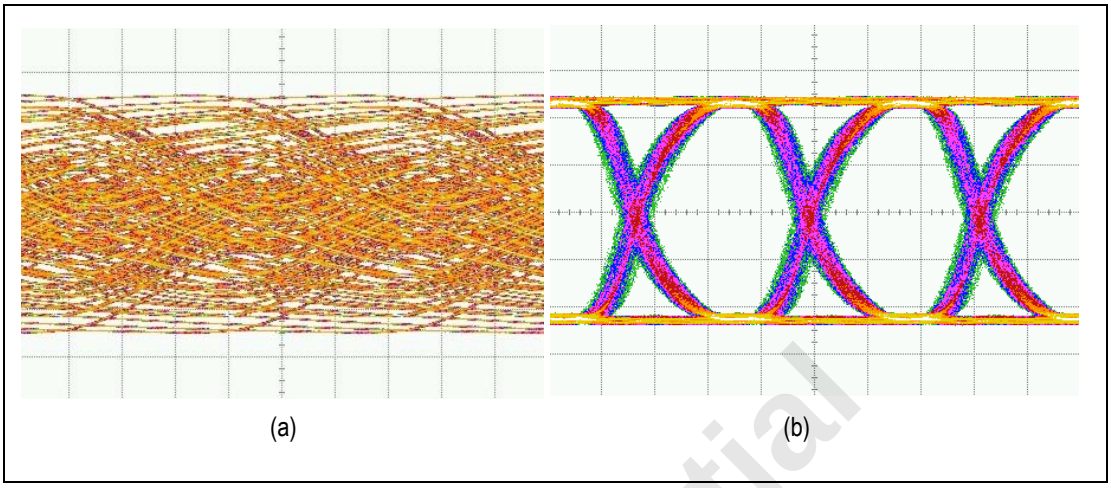


Figure 4 Eye Diagram

Eye Diagram Parameters

Feature	Feature Type	Parameter Names for Programming via I^2C
Input equalization	Main eye optimization	EQ Range: 0dB to 20dB (plus additional auto-boost up to 10dB for long connections)
Input equalization data rate	Main eye optimization	EQDATARATE Range: 2.5Gbps to 8Gbps
Output de-emphasis	Main eye optimization	TX_DEEMP Range: 0dB to -8.5dB
Output differential signal swing (peak-to-peak)	Main eye optimization	TX_SWING Range: *0.4V to 0.95V*
Output slew rate	Main eye optimization	TX_SLEW Range: 45ps to 150ps
Output de-emphasis delay	Main eye optimization	TX_EMP_DELAY Range: 166ps to 400ps
DC gain of Input amplifier	Eye optimization for large swing inputs	DC_GAIN Range: -2dB to -14dB
Equalizer DC gain	Eye optimization for large swing inputs	EQDCGAIN Range: -3dB to 3dB
Limiting Amplifier swing (intermediate stage)	Fine optimization	LA_SWING Range: 560mV to 840mV
Output de-emphasis delay cell offset cancellation loop control	Fine optimization	TX_OC_ENA Range: enable / disable
Channel speed control optimization	Fine optimization	CHEN Range: Disable and 3Gpbs to 6Gbps

Table 3 Quick Reference: Parameters Used for Eye Optimization

Feature	Feature Type	Parameter Names for Programming via I^2C
Rx loss of signal detection threshold used for loss of signal mode, differential peak-to-peak	NA	SIG_THRESH Range: 50mV to 170mV
Input and output differential termination resistance	NA	TERM_CTL Range: 80 ohm to 110 ohm
Minimum loss of signal detection glitch removal	NA	SIG_GLITCHRM Range: 2.6ns to 4ns
Channel transfer mode	NA	CTRL options: multicast, direct-connect, cross-connect, loopback

Table 4 Quick Reference: Parameters Used for Functions other than Eye Optimization

Modes of Operation

The device supports several data transfer modes, loss of signal mode, loopback mode, and several power reducing modes.

Loss of Signal Mode

In loss of signal mode, the transmitter stops toggling and maintains its common-mode voltage level. The device enters loss of signal mode when the envelope of the incoming signal on a given channel has fallen below a programmable threshold level. This feature is not required for typical SRIO applications and should be disabled via Global Control register (address offset=12h) by setting bits 21 and 22 to 1.

Power Reducing Modes

The Repeater supports three power-down states and one active state as shown in Table 5. The user can choose between full chip power-down, channel based power-down, and one loss of signal mode. Power reducing modes can be selected via PDB and channel enable pins (A0EN, A1EN, etc.).

Power Reducing Mode	Required Signal Values			State Description
	Power-Down Control		Signal Detect Status	
	Global	Per Channel	A[1:0]SIGDET, B[1:0]SIGDET	
	PDB	A[1:0]EN, B[1:0]EN		
Full IC power-down	0	X	X	All channels are powered-down Rx termination is set to Hi-Z Tx termination is set to 1kΩ Tx common-mode is at VDD
Individual channel power-down	X	0	X	Rx termination is set to Hi-Z Tx termination is set to 1kΩ Tx common-mode is at VDD
Channel enabled but inactive (loss of signal). Rx and Tx set to 50 Ohms	1	1	0	Tx output is squelched if loss of signal is detected Receiver terminations set to 50Ω Output common-mode is held at its active value Tx termination is set to 50Ω
Channel enabled and active. No power-down	1	1	1	Tx output is active Receiver terminations set to 50Ω Transmitter terminations set to 50Ω

Table 5 Power Reducing Modes

Loopback Mode

The P0608R fully supports data loopbacks on all channels via I^2C using the CTRL register. Refer to Table 13 for this parameter setting. While the device is in the loopback mode, all channels are enabled regardless of the A0/B0/A1/B1EN setting. Signal detect signals can also be looped back.

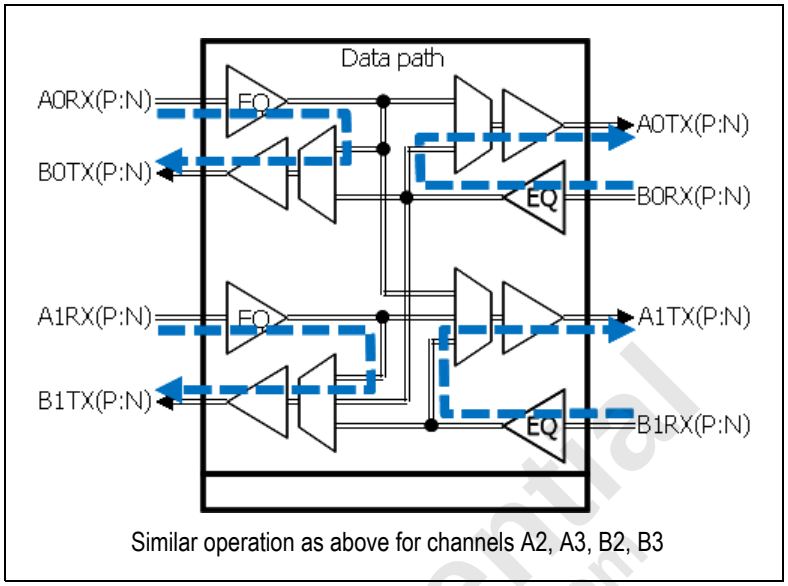


Figure 5 Diagram of P0608R Configuration in Loopback Mode

Channel Muxing

The P0608R repeater permits a variety of muxing, demuxing, and switching configurations. These configurations require the selection of specific pins for input and output ports. In the following sections, each configuration is described in terms of pin connectivity to external upstream and downstream devices. The configurations shown are those often used in system designs:

- Uni-directional 2:1 Mux (1 or 2 instances)
- Uni-directional 1:2 De-Mux (1 or 2 instances)
- Bi-directional 2:1 Mux/De-Mux
- Bi-directional Z-function (also called Partial Cross Function)

Channels A0, A1, B0, B1 programming via CTRL requires setting I2CA0=0 in the slave I2C address. Channels A2, A3, B2, B3 programming via CTRL requires setting I2CA0=1. Refer to the Serial Interface section for details.

The P0608R supports channel muxing in both upstream and downstream channel directions via the mode control bits, CTRL, in the Global Control Register (address offset=12h). Figure 6 shows the channel/reference muxing modes and Tables 6 and 7 show how CTRL bits allow for various modes of data transfers: Multicast mode, Direct-connect, and Cross-connect. Both Direct-connect, and Cross-connect modes are used to build uni-directional and bi-directional 2:1 mux and Z-switch functions.

While the part is in Multicast or Cross-connect mode, all channels are enabled regardless of the A0/B0/A1/B1EN setting.

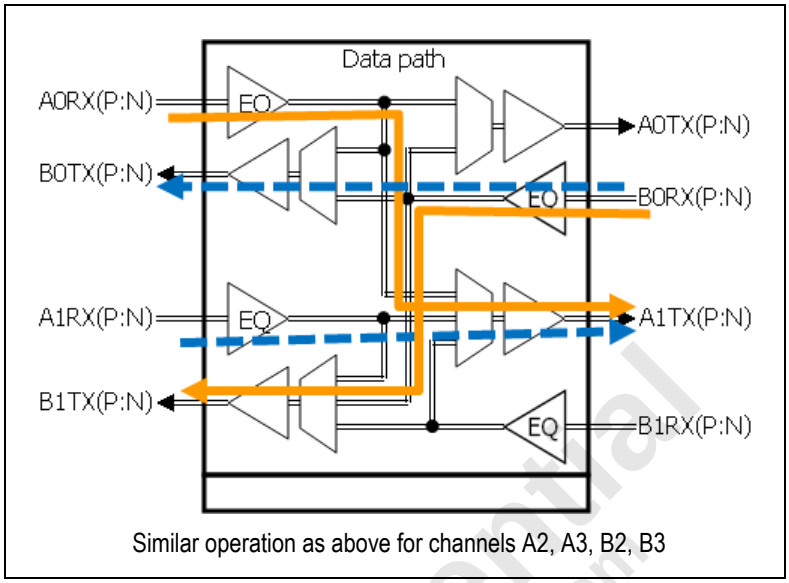


Figure 6 Diagram of Channel/Reference Muxing Modes

Input Pins					Output Pins			
CTRL	A0RX[P,N]	A1RX[P,N]	B0RX[P,N]	B1RX[P,N]	A0TX[P,N]	A1TX[P,N]	B0TX[P,N]	B1TX[P,N]
CTRL=0010 (Multicast Mode)	A0 DATA	X	B0 DATA	X	A0 DATA	A0 DATA	B0 DATA	B0 DATA
CTRL=0001 (Direct-Connect Mode)	A0 DATA	A1 DATA	B0 DATA	B1 DATA	A0 DATA	A1 DATA	B0 DATA	B1 DATA
CTRL=0100 (demux Mode)	A0 DATA	X	B0 DATA	X	Squelched	A0 DATA	Squelched	B0 DATA

Table 6 Description of Channel Muxing/De-Muxing Functionality — Channels A0, A1, B0, B1

Input Pins					Output Pins			
CTRL	A2RX[P,N]	A3RX[P,N]	B2RX[P,N]	B3RX[P,N]	A2TX[P,N]	A3TX[P,N]	B2TX[P,N]	B3TX[P,N]
CTRL=0010 (Multicast Mode)	A2 DATA	X	B2 DATA	X	A2 DATA	A2 DATA	B2 DATA	B2 DATA
CTRL=0001 (Direct-Connect Mode)	A2 DATA	A3 DATA	B2 DATA	B3 DATA	A2 DATA	A3 DATA	B2 DATA	B3 DATA
CTRL=0100 (demux Mode)	A2 DATA	X	B2 DATA	X	Squelched	A2 DATA	Squelched	B2 DATA

Table 7 Description of Channel Muxing/De-Muxing Functionality — Channels A2, A3, B2, B3

The signal detect output pins support the functionality shown in Tables 8 and 9.

Input Pins					Output Pin Value			
CTRL	A0RX[P,N]	A1RX[P,N]	B0RX[P,N]	B1RX[P,N]	A0SIGDET	A1SIGDET	B0SIGDET	B1SIGDET
CTRL=0010 (Multicast Mode)	A0 Data	A1 Data	B0 Data	B1 Data	Based on A0RX Swing	0	Based on B0RX Swing	0
CTRL=0001 (Direct-Connect Mode)	A0 Data	A1 Data	B0 Data	B1 Data	Based on A0RX Swing	Based on A1RX Swing	Based on B0RX Swing	Based on B1RX Swing
CTRL=0100 (demux Mode)	A0 Data	X	B0 Data	X	Based on A0RX Swing	0	Based on B0RX Swing	0

Table 8 Description of Signal Detect Muxing/De-Muxing Functionality — Channels A0, A1, B0, B1

Input Pins					Output Pin Value			
CTRL	A2RX[P,N]	A3RX[P,N]	B2RX[P,N]	B3RX[P,N]	A2SIGDET	A3SIGDET	B2SIGDET	B3SIGDET
CTRL=0010 (Multicast Mode)	A2 Data	A3 Data	B2 Data	B3 Data	Based on A2RX Swing	0	Based on B2RX Swing	0
CTRL=0001 (Direct-Connect Mode)	A2 Data	A3 Data	B2 Data	B3 Data	Based on A2RX Swing	Based on A3RX Swing	Based on B2RX Swing	Based on B3RX Swing
CTRL=0100 (demux Mode)	A2 Data	X	B2 Data	X	Based on A2RX Swing	0	Based on B2RX Swing	0

Table 9 Description of Signal Detect Muxing/De-Muxing Functionality — Channels A2, A3, B2, B3

The following sections describe a system implementation of mux, demux, and Z-switch functions for channels A0, A1, B0, B 1. Analogous implementations can be applied to channels A2, A3, B2, B3 by programming those channels to the desired function via CTRL bits. For example, 2:1 mux from Figure 7 would have A2RX(P,N) and A3RX(P,N) ports on the left side and A3TX(P,N) port on the right side.

Uni-directional 2:1 Mux or Two Instances of Unidirectional 2:1 Mux

This function can be achieved by using the CTRL bits in the Global Control Register. The ports should be configured as indicated in Figure 7.

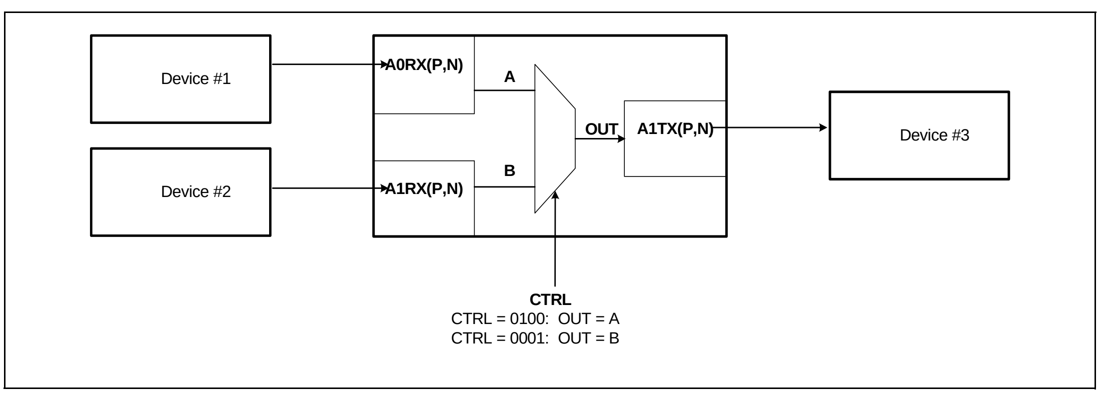


Figure 7 Implementation of Unidirectional 2:1 Mux

As an alternative, different chip channels can also be selected as shown in Figure 8. This solution can be combined with the previous one to obtain two instances of Uni-directional 2:1 Mux.

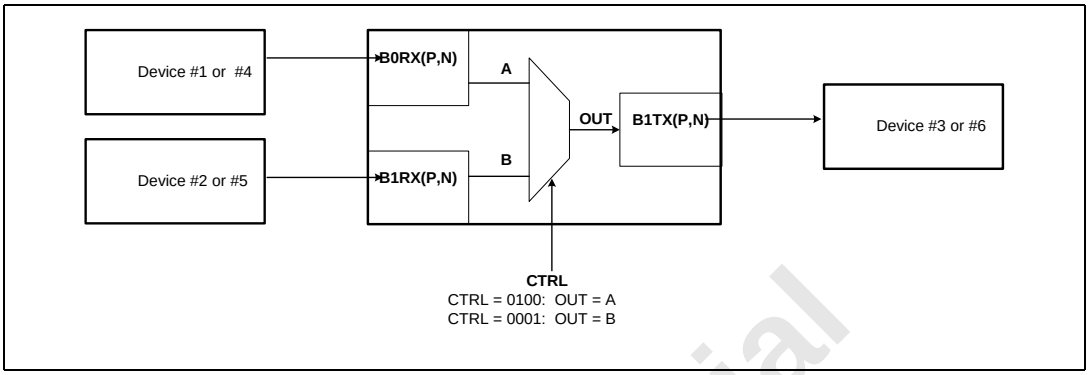


Figure 8 Implementation of Second Instance of Unidirectional 2:1 Mux

Uni-directional 1:2 De-mux or Two Instances of Unidirectional 1:2 De-Mux

This function can be achieved by using CTRL pin as a de-mux control signal. CTRL should be set to either 0001 or 0100. The ports should be configured as shown in Figure 9.

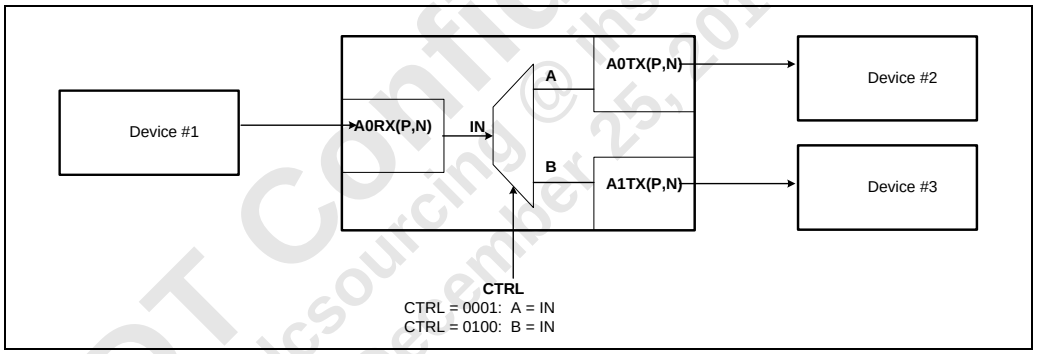


Figure 9 Implementation of Unidirectional 1:2 De-Mux

As an alternative, different chip channels can also be selected as shown in Figure 10. This solution can be combined with the previous one to obtain two instances of Uni-directional 1:2 De-Mux.

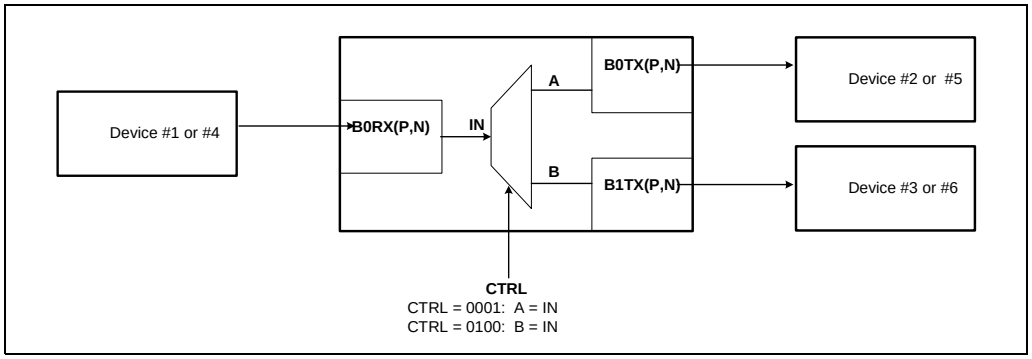


Figure 10 Implementation of Second Instance of Unidirectional 1:2 De-Mux

Bi-directional 2:1 Mux/De-Mux

The bi-directional Mux and De-Mux function can also be achieved by using the CTRL bits. The ports should be configured as shown in Figure 11.

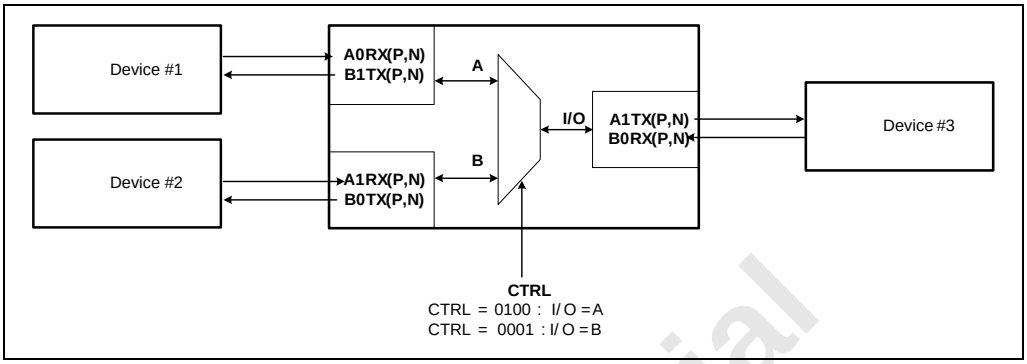


Figure 11 Implementation of Bi--directional 2:1 Mux/De-Mux

Bi-directional Z-function (also called Partial Cross Function)

This function can also be achieved by using the CTRL bits. The ports should be configured as shown in Figure 12.

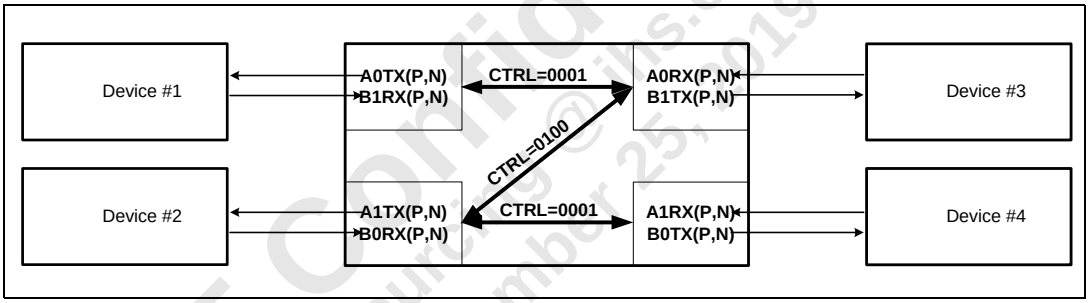


Figure 12 Implementation of Z-function

I²C Registers

I²C Register Description Summary

Table 10 provides a summary of the P0608R register set. Registers are organized as 4-bytes (Dword). Channel-specific parameters are assigned one byte for each channel within the Dword. The following sections describe the serial slave and master/EEPROM modes of operation.

Note: Two identical register sets are implemented in the P0608R: one set for channels A0, A1, B0, B1 as shown in Table 10 and one set for channels A2, A3, B2, B3 as shown in Table 11. To program values for channels A0, A1, B0, B1, set I2CA[0] to 0 in the P0608R I²C address. To program values for channels A2, A3, B2, B3, set I2CA[0] to 1 in the P0608R I²C address.

	Bits			
	[31:24]	[23:16]	[15:08]	[07:00]
Address Offset (hex)	Channel B1	Channel B0	Channel A1	Channel A0
00	Vendor ID (VID)			
01	Device ID (DID)			
02	Revision ID (RID)			
03	DC_GAIN	DC_GAIN	DC_GAIN	DC_GAIN
04	EQDATARATE	EQDATARATE	EQDATARATE	EQDATARATE
05	EQDCGAIN	EQDCGAIN	EQDCGAIN	EQDCGAIN
06	EQ	EQ	EQ	EQ
07	LA_SWING	LA_SWING	LA_SWING	LA_SWING
08	SIG_THRESH	SIG_THRESH	SIG_THRESH	SIG_THRESH
09	SIG_GLITCHRM	SIG_GLITCHRM	SIG_GLITCHRM	SIG_GLITCHRM
0A	SIG_FORCESIGDET	SIG_FORCESIGDET	SIG_FORCESIGDET	SIG_FORCESIGDET
0B	TX_SWING	TX_SWING	TX_SWING	TX_SWING
0C	TX_DEEMP	TX_DEEMP	TX_DEEMP	TX_DEEMP
0D	TX_SLEW	TX_SLEW	TX_SLEW	TX_SLEW
0E	TX_EMP_DELAY	TX_EMP_DELAY	TX_EMP_DELAY	TX_EMP_DELAY
0F	TX_OC_ENA	TX_OC_ENA	TX_OC_ENA	TX_OC_ENA
10	DET_STATUS	DET_STATUS	DET_STATUS	DET_STATUS
11	CHEN	CHEN	CHEN	CHEN
12	Global control register			
13	Reserved			
14	I2CSTS register			
15	I2CCTL register			
16	EEPROM control register			

Table 10 I²C Register Description Summary for Channels A0, A1, B0, B1

	Bits			
	[31:24]	[23:16]	[15:08]	[07:00]
Address Offset (hex)	Channel B3	Channel B2	Channel A3	Channel A2
00	Vendor ID (VID)			
01	Device ID (DID)			
02	Revision ID (RID)			
03	DC_GAIN	DC_GAIN	DC_GAIN	DC_GAIN
04	EQDATARATE	EQDATARATE	EQDATARATE	EQDATARATE
05	EQDCGAIN	EQDCGAIN	EQDCGAIN	EQDCGAIN
06	EQ	EQ	EQ	EQ
07	LA_SWING	LA_SWING	LA_SWING	LA_SWING
08	SIG_THRESH	SIG_THRESH	SIG_THRESH	SIG_THRESH
09	SIG_GLITCHRM	SIG_GLITCHRM	SIG_GLITCHRM	SIG_GLITCHRM
0A	SIG_FORCESIGDET	SIG_FORCESIGDET	SIG_FORCESIGDET	SIG_FORCESIGDET
0B	TX_SWING	TX_SWING	TX_SWING	TX_SWING
0C	TX_DEEMP	TX_DEEMP	TX_DEEMP	TX_DEEMP
0D	TX_SLEW	TX_SLEW	TX_SLEW	TX_SLEW
0E	TX_EMP_DELAY	TX_EMP_DELAY	TX_EMP_DELAY	TX_EMP_DELAY
0F	TX_OC_ENA	TX_OC_ENA	TX_OC_ENA	TX_OC_ENA
10	DET_STATUS	DET_STATUS	DET_STATUS	DET_STATUS
11	CHEN	CHEN	CHEN	CHEN
12	Global control register			
13	Reserved			
14	I2CSTS register			
15	I2CCTL register			
16	EEPROM control register			

Table 11 I^2C Register Description Summary for Channels A2, A3, B2, B3

The I^2C registers are implemented in 32-bit wide format (DWord).

Note: The following register descriptions apply to both the A0, A1, B0, B1 and the A2, A3, B2, B3 register sets.

Vendor Identification Register

Address Offset (hex)	Field Name	Type	Default Value	Description
00h	VID	R0	111Dh	16 bit Vendor ID for IDT

Device Identification Register

Address Offset (hex)	Field Name	Type	Default Value	Description
01h	DID	R0	80AAh	16 bit Device ID for P0608R

Revision Identification Register

Address Offset (hex)	Field Name	Type	Default Value	Description
02h	RID	R0	08h	Revision ID for device version

Channel Based Register

The I^2C register shown below is implemented in a 32-bit wide format. For each register, bits 31:24 are for channel B1, 23:16 for B0, 15:8 for A1, and 7:0 for A0.

Address Offset (hex)	Register Name	Type	Default Value	Description
03h	DC_GAIN	RW	01h	DC Gain of Input Amplifier. Used for reducing input signal swings to adapt them better to internal RX circuits.[1] 00h: -2dB 04h: -8dB 01h: -4dB(default) 05h: -10dB 02h: -6dB 06h: -12dB 03h: -8dB 07h: -14dB Usage details: Settings between -6db and -14db might reduce output jitter if input swing is larger than 800mVpp diff. Corresponding programming pins: N/A
04h	EQDATARATE	RW	02h	Input Equalization Data Rate 00h: 2.5 to 3 Gbps data rate 01h: 5 Gbps data rate 02h: 6 Gpbs data rate (default) 03h: 8 Gpbs data rate Usage details: Set to the data rate used in end application. Sometimes, a minor improvement can be seen by setting 5Gbps at 6Gbps speeds (or vice versa). This depends on the number of connectors and line length. Corresponding programming pins: N/A
05h	EQDCGAIN	RW	01h	Equalizer DC Gain Control. Used for large swing input signals. 00h: -3dB 01h: -1dB (default) 02h: 1dB 03h: 3dB Usage details: Typically left at default, but might need to be set to -3db if the input swing is above 1000mVppdiff. Corresponding programming pins: N/A
06h	EQ	RW	03h	Input Equalization at selected F=EQDATARATE/2 00h: +0dB 08h: +16dB 01h: +2dB 09h: +18dB 02h: +4dB 0Ah: +20dB 03h: +6dB 0Bh: Reserved 04h: +8dB 0Ch: Reserved 05h: +10dB 0Dh: Reserved 06h: +12dB 0Eh: Reserved 07h: +14dB 0Fh: Reserved Usage details: Set to 0dB - 10db for traces and cables based on input channel length. Can also be set to higher dB values for very long input cables. Corresponding programming pins: N/A

Table 12 P0608R I^2C Register (Part 1 of 3)

Address Offset (hex)	Register Name	Type	Default Value	Description
07h	LA_SWING	RW	02h	Internal Limiting Amplifier Programmable Swing. Used for fine optimization. 00h: 700mV$_{diff-pkpk}$ - 20% 01h: 700mV$_{diff-pkpk}$ 02h: 700mV$_{diff-pkpk}$(default) 03h: 700mV$_{diff-pkpk}$+ 20% Usage details: Typically left at default. Used for fine optimization. May slightly reduce jitter for some combinations of connectors and line lengths. Does not interact with TX_SWING settings. Corresponding programming pins: N/A
08h	SIG_THRESH	RW	03h	Rx Loss of Signal Detection Threshold 00h: 50mV$_{diff-pkpk}$ 01h: 70mV$_{diff-pkpk}$ 02h: 90mV$_{diff-pkpk}$ 03h: 110mV$_{diff-pkpk}$ (default) 04h: 120mV$_{diff-pkpk}$ 05h: 140mV$_{diff-pkpk}$ 06h: 150mV$_{diff-pkpk}$ 07h: 170mV$_{diff-pkpk}$ Usage details: Set to desired value based on end application. Loss of signal can be disabled completely via SIG_PD_TRANDET and SIG_PD_LVLDET bits. Corresponding programming pins: N/A
09h	SIG_GLITCHRM	RW	00h	Minimum Loss of Signal Detection Glitch Removal. Advanced feature. 00h: 2.6n (default) 01h: 3.1n 02h: 3.5n 03h: 4.0n Usage details: Typically left at default (2.6ns). Corresponding programming pins: N/A
0Ah	SIG_FORCESIGDET	RW	00h	Force Output of Signal Detection 00h: Normal operation 01h: Force RX_SIGNALDET to 1 Usage details: Not used.
0Bh	TX_SWING	RW	04h	Transmitter Differential Swing Peak-to-Peak (typical) (see $V_{TX-DIFF-PP}$ and $V_{TX-DIFF-PP-LOW}$ transmitter specifications) 00h - 0.4Vdiff-pkpk 01h - 0.5Vdiff-pkpk 02h - 0.6Vdiff-pkpk 03h - 0.7Vdiff-pkpk 04h - 0.8Vdiff-pkpk 05h - 0.85Vdiff-pkpk 06h - 0.90Vdiff-pkpk 07h - 0.95Vdiff-pkpk Usage details: Set to desired TX driver amplitude. Typically, higher values are recommended when TX has to drive over longer distances. Corresponding programming pins: N/A

Table 12 P0608R I^2C Register (Part 2 of 3)

Address Offset (hex)	Register Name	Type	Default Value	Description
0Ch	TX_DEEMP	RW	02h	Output De-emphasis. Defined as 20log($V_{TX-DE-EMP}$ / $V_{TX-DIFF}$) [dB] 00h: +0dB 01h: -2.5dB 02h: -3.5dB (default) 03h: -4.5dB 04h: -5.5dB 05h: -6.5dB 06h: -7.5dB 07h: -8.5dB Usage details: Typically, value should be more negative when TX has to drive over longer distances. Corresponding programming pins: N/A
0Dh	TX_SLEW	RW	00h	Output Rise/Fall (20% - 80% levels) 00h: 45ps (default) 01h: 50ps 02h: 70ps 03h: 150ps Usage details: Set to desired TX slew rate Corresponding programming pins: N/A
0Eh	TX_EMP_DELAY	RW	00h	Output De-emphasis Delay 00h: 166ps, 6Gbps mode (default) 01h: 200ps, 5Gbps mode 02h: 333ps, 3Gbps mode 03h: 400ps, 2.5Gbps mode Usage details: Needed only when de-emphasis is used. Select delay closest to data rate period (example: 5Gb->200ps). See Figure 22. Corresponding programming pins: N/A
0Fh	TX_OC_ENA	RW	01h	Transmitter De-emphasis Delay Cell Offset Cancellation Loop Control. Used for fine optimization. 00h: disable the loop 01h: enable the loop (default) Usage details: Left at default (enabled). Corresponding programming pins: N/A
10h	DET_STATUS	R	00h	Input Loss of Signal Detection Bit 0: 1 = input has signal Bit 1: 1 = reserved
11h	CHEN	RW	03h	Channel Enable and Speed Control Bit 0: 1 = enable, 0 = disable Bit 1: 1 = 6Gbps and below, 0 = 3Gbps and below Usage details: Based on channel usage and frequencies of operation required in end applications. Corresponding programming pins: bit 0 = A0EN, A1EN, etc.; bit 1 = NA

Table 12 P0608R I^2C Register (Part 3 of 3)

1. During the readout of this register for channels A0 and A2 only: Readout value = (Last value written into DC-GAIN register) + 08h (e.g. 00h setting reads out as 08h).

Global Control Register (address offset=12h)

Bit Field	Field Name	Type	Default Value	Description
1:0	TERM_CTL	RW	10	Input and Output Differential Termination (typical) 00 – 80Ω differential impedance 01 – 90Ω differential impedance 10 – 100Ω differential impedance (default) 11 – 110Ω differential impedance Usage details: Set to value 2 times higher than line impedance. Corresponding programming pins: N/A
5:2	CTRL	RW	0001	Data Transfer Control 0001: direct connect (default) 0010: multicast mode 0100: cross connect mode 1000: loopback mode Usage details: Set to desired mode of transfer. Corresponding programming pins: N/A
11:6	Reserved	RO	000000	Reserved bits
12	RXDET_EXT	RW	0	Write 1 to this bit to extend the time allowed for Tx common mode voltage negative step from 800µs to 1.2ms. Advanced feature.
20:13	Reserved	RO	00h	Reserved bits
21	SIG_PD_TRANDET	RW	0	Transition Detection in Input Signal Detector 0: enable 1: disable Usage details: Typically left at default. Signal detection can be disabled completely via SIG_PD_TRANDET and SIG_PD_LVLDET bits. Corresponding programming pins: N/A
22	SIG_PD_LVLDET	RW	0	Level Detection in Input Signal Detector 0: enable 1: disable Usage details: Typically left at default. Signal detection can be disabled completely via SIG_PD_TRANDET and SIG_PD_LVLDET bits. Corresponding programming pins: N/A
23	LA_EQ_ENA	RW	1	Limiting Amplifier Equalization Peaking Control. Advanced feature. 0: disable 1: enable Usage details: Typically left at default. Corresponding programming pins: N/A
24	Reserved	RW	1	Reserved bit
31:25	Reserved	RO	0000000	Reserved bits

Table 13 Global Control Register (OFFSET = 12h)

Test Control Register — Reserved (address offset=13h)

I²C Status Register (I2CSTS) (address offset=14h)

Bit Field	Field Name	Type	Default Value	Description
0	Reserved	RO	0	Reserved
7:1	SI2CADDR	RO	HWINIT	Slave I²C address
8	Reserved	RO	0	Reserved
15:9	MI2CADDR	RO	HWINIT	Master I²C address
16	MODE	RO	HWINIT	This field specifies the mode that the device's I²C master interface initialize in. 0x0: talking mode 0x1: listening mode
21:17	Reserved	RO	00000	Reserved
22	BLANK	RW1C	0	Blank Serial EEPROM
23	ROLLOVER	RW1C	0	EEPROM rolled over
24	EEPROMDONE	RO	0	EEPROM_DONE
25	NAERR	RW1C	0	No Acknowledge Error
26	Reserved	RO	0	Reserved
27	OTHERERR	RW1C	0	Other Error
28	CSERR	RW1C	0	Checksum Error
29	URIA	RW1C	0	Unmapped register initialization attempt
31:30	Reserved	RO	0	Reserved

Table 14 I²C Status Register (OFFSET=14h)

I²C Control Register (I2CCTL) (address offset=15h)

Bit Field	Field Name	Type	Default Value	Description
15:0	MI2CCP	RO		Master I²C clock prescaler Final Master I²C clk freq = msmbcp x 8 x oscillator_clk_period
16	Reserved	RO	0	Reserved
17	ICHECKSUM	RW	0	Ignore checksum error
19:18	SI2CMODE	RW	01	Slave I²C mode 00: Glitch counters operate with 1 us delay 01: Glitch counters operate with 100 ns delay 10: Disabled

Table 15 I²C Control Register (OFFSET=15h)

Bit Field	Field Name	Type	Default Value	Description
21:20	MI2CMODE	RW	00	Master I^2C mode Same encodings as Slave I^2C mode
22	I2CDTO	RW	0	I^2C disable timeout
31:23	Reserved	RO	000000000	Reserved

Table 15 I^2C Control Register (OFFSET=15h)

EEPROM Control Register (address offset=16h)

Bit Field	Field Name	Type	Default Value	Description
7:0	SIZE	HWINIT	00h	This field sets the size of each partition in EEPROM, according to 64*2^SIZE: 00h: 64 bytes 01h: 128 bytes 02h: 256 bytes 03h: 512 bytes 04h: 1024 bytes 05h: 2048 bytes 06h: 4096 bytes 07h: 8192 bytes 08h: 16384 bytes others: reserved This field, and the other fields in this register are critical for external EEPROM operation and must be stored at the address 0 of EEPROM memory space using single Double-word format. Other register configurations must be stored in EEPROM space after this register configuration.
15:8	VECTOR	HWINIT	FFh	This field indicates which P0608Rs are present on the shared I2C bus. Bit 8: P0608R(0) is present (I2CA[2:1]=00) channels A0, A1, B0, B1 Bit 9: P0608R(0) is present (I2CA[2:1]=00) channels A2, A3, B2, B3 Bit10: P0608R(1) is present (I2CA[2:1]=01) channels A0, A1, B0, B1 … Bit 15: P0608R(3) is present (I2CA[2:1]=11) channels A2, A3, B2, B3 Note: 2 bits must be set for every P0608R present. This field, and the other fields in this register are critical for external EEPROM operation and must be stored at the address 0 of EEPROM memory space using single Double-word format. Other register configurations must be stored in EEPROM space after this register configuration.
31:16	Reserved	RO	0000h	Reserved

Table 16 External EEPROM Control Register (OFFSET=16h)

Serial Interface

The P0608R interface supports I^2C interfaces. The P0608R has two interface operating modes, slave and master. The slave I^2C mode provides full access to all software-visible registers, allowing every register in the device to be read or written by an external I^2C master. The master I^2C mode provides connection for an optional external serial EEPROM used for initialization. Once initialized, the P0608R switches to slave mode. I^2C interfaces contain an I^2C clock pin and an I^2C data pin. The master and slave interfaces share the same set of address pins I2CA[2:1].

The pin INTMODE controls if the I^2C is in the master or the slave mode. When INTMODE=low, the interface is in the slave mode, when INTMODE=high, it is in the master mode.

Note that the register array is not fully contiguous for all registers. The register array appears as two identical blocks, each identified by the state of the I^2C A0 address bit. For I2CA0=0, the lower four channels (A0, A1, B0, B1) are accessed. When I2CA0=1, the upper four channels (A2, A3, B2, B3) are accessed.

I^2C Slave Mode

The slave I^2C mode provides the P0608R with a configuration, management, and debug interface. Using the slave I^2C mode, an external master can read or write any software-visible register in the device.

Initialization

Slave I^2C initialization occurs during a switch fundamental reset. During the switch fundamental reset initialization sequence, the slave I^2C address is initialized. The address is specified by the I2CA[2:1] signals as shown in Table 17. The I2CA[0] bit is used to select programming for A0, A1, B0, B1 channels when I2CA0=0 or to select programming for A2, A3, B2, B3 channels when I2CA0=1.

Address Bit	Address Bit Value
1	I2CA0=0: selects access to A0, A1, B0, B1 channels I2CA0=1: selects access to A2, A3, B2, B3 channels
2	I2CA1
3	I2CA2
4	0
5	1
6	1
7	1

Table 17 Slave I^2C Address

I^2C Transactions

The slave I^2C interface responds to the following I^2C transactions initiated by an I^2C master. Refer to the I^2C 2.0 specification for a detailed description of these transactions.

- Byte and Word Write/Read
- Block Write/Read

Initiation of any I^2C transaction other than those listed above to the slave I^2C interface produces undefined results. Associated with each of the above transactions is a command code. The command code format for operations supported by the slave I^2C interface is shown in Table 18 and described in Table 19.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PEC	SIZE		FUNCTION			START	END

Table 18 Slave I^2C Command Code Format

Bit Field	Name	Description
0	END	End of transaction indicator. Setting both START and END signifies a single transaction sequence 0 - Current transaction is not the last read or write sequence. 1 - Current transaction is the last read or write sequence.
1	START	Start of transaction indicator. Setting both START and END signifies a single transaction sequence 0 - Current transaction is not the first of a read or write sequence. 1 - Current transaction is the first of a read or write sequence.
4:2	FUNCTION	This field encodes the type of I^2C operation. 0 - CSR register read or write operation 1 - 7 Reserved
6:5	SIZE	This field encodes the data size of the I^2C transaction. 0 - Byte 1 - Word 2 - Block 3 - Reserved
7	PEC	This bit controls whether packet error checking is enabled for the current I^2C transaction. 0 - Packet error checking disabled for the current I^2C transaction. 1 - Packet error checking enabled for the current I^2C transaction.

Table 19 Slave I^2C Command Code Fields

The FUNCTION field in the command code indicates if the I^2C operation is a system address register read/write or a serial EEPROM read/write operation, since the format of these transactions is different. Both operations are described in the following sections. If a command is issued while one is already in progress or if the slave is unable to supply data associated with a command, then the command is NACKed. This indicates to the master that the transaction should be retried.

CSR Register Read or Write Operation

Table 20 indicates the sequence of data as it is presented on the slave I^2C following the byte address of the Slave I^2C interface.

Byte Position	Field Name	Description
0	CCODE	Command Code. Slave Command Code field described in Table 19.
1	BYTCNT	Byte Count. The byte count field is only transmitted for block type I^2C transactions. I^2C word and byte accesses do not contain this field. The byte count field indicates the number of bytes following the byte count field when performing a write or setting up for a read. The byte count field is also used when returning data to indicate the number of following bytes (including status). *Note that the byte count field does not include the PEC byte if PEC is enabled.*
2	CMD	Command. This field encodes fields related to the CSR register read or write operation.
3	ADDRL	Address Low. Lower 8-bits of the double-word system address of register to access.
4	ADDRU	Address Upper. Upper 8-bits of the double-word system address of register to access.
5	DATALL	Data Lower. Bits [7:0] of data double-word.
6	DATALM	Data Lower Middle. Bits [15:8] of data double-word.
7	DATAUM	Data Upper Middle. Bits [23:16] of data double-word.
8	DATAUU	Data Upper. Bits [31:24] of data double-word.

Table 20 CSR Register Read or Write Operation Byte Sequence

The format of the CMD field is shown in Table 21 and described in Table 22.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WERR	RERR	0	OP	Fh			

Table 21 CSR Register Read or Write CMD Field Format

Bit Field	Name	Type	Description
0	1	1	Reserved. Must be One.
1	1	1	Reserved. Must be One.
2	1	1	Reserved. Must be One.

Table 22 CSR Register Read or Write CMD Field Description (Part 1 of 2)

Bit Field	Name	Type	Description
3	1	1	Reserved. Must be One.
4	OP	Read/Write	CSR Operation. This field encodes the CSR operation to be performed. 0 - CSR write 1 - CSR read
5	0	0	Reserved. Must be zero
6	RERR	Read-Only and Clear	Read Error. This bit is set if the last CSR read I^2C transaction was not claimed by a device. Success indicates that the transaction was claimed and not that the operation completed without error.
7	WERR	Read-Only and Clear	Write Error. This bit is set if the last CSR write I^2C transaction was not claimed by a device. Success indicates that the transaction was claimed and not that the operation completed without error.

Table 22 CSR Register Read or Write CMD Field Description (Part 2 of 2)

Sample Slave I^2C Operation

This section illustrates sample Slave I^2C operations. Shaded items are driven by the P0608R's slave I^2C interface and non-shaded items are driven by an I^2C host.

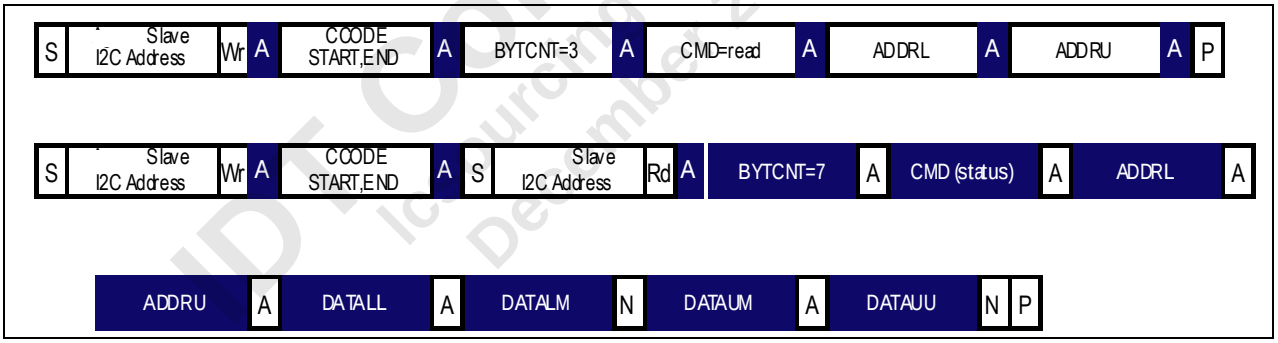


Figure 13 CSR Register Read Using I^2C block Write/Read Transactions with PEC Disabled

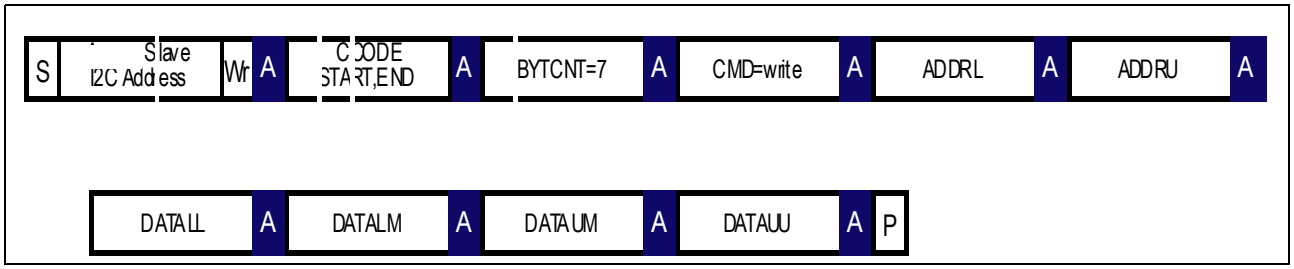


Figure 14 CSR Register Write Using I^2C Block Write transactions with PEC Disabled

I2C Master Interface

The P0608R master interface is used to read and download the contents of EEPROM into the P0608R configuration registers. The master interface can be used in two modes: standalone mode (single repeater) and shared mode (up to 4 repeaters). The master interface does not support I2C arbitration. As a result, when the P0608R I2C interface is in master mode, either standalone or shared mode, care needs to be taken to avoid any potential bus contention with other masters on the bus. During the transfer from EEPROM, no other master can be active on the bus. Once the configuration is read and loaded from EEPROM, the P0608R master automatically enters slave mode. If there are other masters, they can then take control of the bus if needed.

Figure 15 shows a standalone application of a single P0608R with a dedicated EEPROM. In this mode, the P0608R acts as a master and can be set to any address via I2CA[2:1] pins.

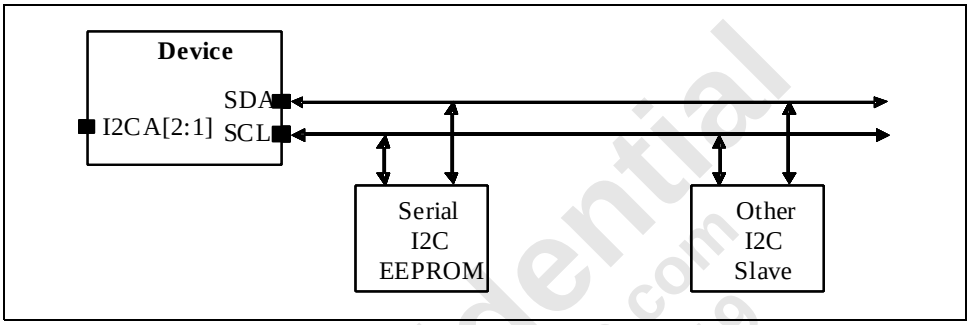


Figure 15 Single P0608R Implementation

Figure 16 shows an example of a shared mode implementation where multiple P0608Rs are connected on the I2C bus. This allows a single EEPROM to be shared across all P0608Rs in the system. In this configuration, P0608R(0) = I2CA[2:1] = 0 is the only master on the bus. There must be a P0608R(0) in shared mode, otherwise download behavior is undefined. P0608R(0) is responsible for reading all initialization data for all devices from the external EEPROM. As the master P0608R device reads the configuration data from EEPROM, the other P0608Rs connected to the bus will only listen to the initialization data and extract and apply register configuration data relevant to them. Each slave device can recognize its portion of configuration data stored in EEPROM, because EEPROM mapping is based on a slave address as shown in Figure 17.

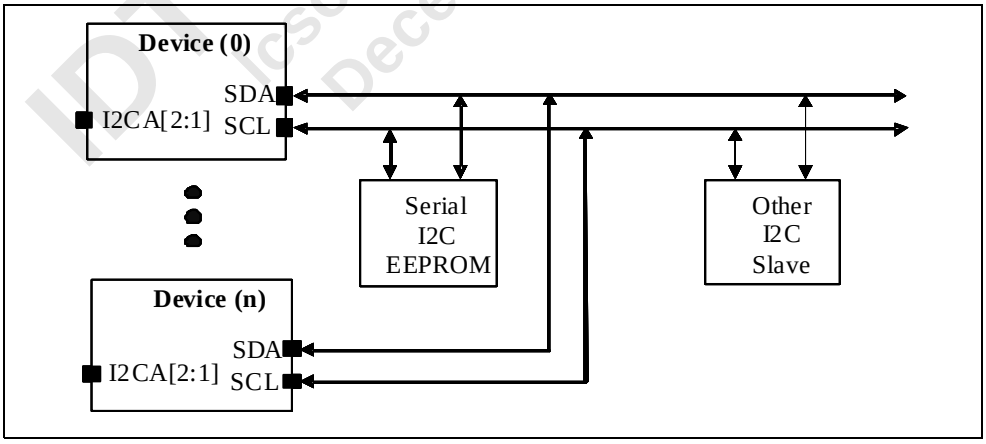


Figure 16 Multiple P0608Rs Implementation

Serial EEPROM Access

At power-up, if EEPROM is present on the I2C bus, it is used to initialize P0608R configuration registers in the device. The address used by the I2C interface is set to default 1010b for the upper four bits. The address used by the I2C interface to access the serial EEPROM is specified by the I2CA[2:0] signals as shown in Table 23.

Address Bit	Address Bit Value
1	I2CA0
2	I2CA1
3	I2CA2
4	0
5	1
6	0
7	1

Table 23 Serial EEPROM I2C Address

Creating and Saving EEPROM Device Configuration

There are two ways to create/save the desired configuration content into EEPROM:

- Create the EEPROM content manually by following the guidelines in the EEPROM Content Format section of this document.
- Create a working copy of the desired register settings in a live system and save these settings into the EEPROM by using the Device Management (GUI) software provided by IDT.

Serial EEPROM Compatibility

Any serial EEPROM equivalent to those listed in Table 24 may be used to store initialization values.

Serial EEPROM	Size
24C32	4 KB
24C64	8 KB
24C128	16 KB
24C256	32 KB
24C512	64 KB

Table 24 P0608R Compatible Serial EEPROMs

Initialization from Serial EEPROM

At power-up, the P0608R master waits 5ms (max) after de-assertion of the internally-generated power on reset to make sure all P0608Rs on the bus come out of reset before starting to read EEPROM data. When the P0608R slave devices come out of reset, they immediately start listening to the bus and internally write the configuration data into their configuration registers as it becomes available on the bus during master-controlled EEPROM reading (download).

If there is only one P0608R on the bus (standalone mode) with I2CA[2:1] address different from zero, it will wait up to a maximum of 10ms after de-assertion of the internally-generated power on reset at power-up before starting to act as the master and read EEPROM data.

EEPROM Content Format

The P0608R master begins reading bytes starting at serial EEPROM address zero. The content of bytes starting from EEPROM address 0 must define the value in the P0608R EEPROM Control Register settings (register offset = 16h, SIZE and VECTOR fields, see Table 16 for details). The P0608R EEPROM Control Register is used to set up the EEPROM start addresses for each P0608R and to define which P0608R I^2C addresses are present via SIZE and VECTOR. Refer to Figure 17. The EEPROM Control Register can only be set up in EEPROM via single double-word format

described later in this section. The user has an option to store any number of P0608R configuration register values in EEPROM. The registers, whose configurations are not stored in the EEPROM, will be initialized to their default values as shown in the I^2C Registers section.

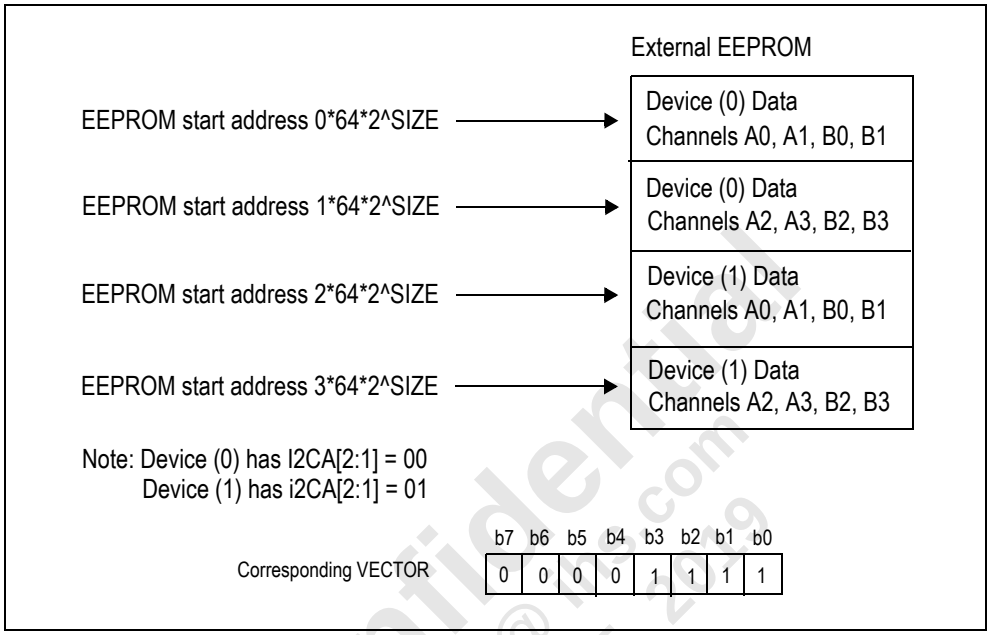


Figure 17 EEPROM Start Address

The P0608R contains 8 channels and each EEPROM-initialized configuration register needs to be defined two times in EEPROM: once for A0, A1, B0, B1 channels, and once for A2, A3, B2, B3 channels. Refer to Figure 17 showing the mapping of 8 channels in EEPROM space.

There are three allowable configuration formats that can be stored in the serial EEPROM. These 3 formats are recognizable by P0608R devices during the download process. Allowable formats are:

- Single double-word format: used to store one P0608R configuration register (32 bits of configuration + header).
- Sequential double-word format: used to store multiple P0608R configuration registers (n*32 bits of configuration + header). This format can be used in combination with the single double-word format.
- Configuration-done format: must be placed right after configuration space used by the formats described above. If there are multiple P0608R devices, the configuration-done format also needs to be placed multiple times, once for every block shown in the example in Figure 17.

The first format type, a single double-word initialization sequence, occupies seven bytes in the serial EEPROM. A single double-word format consists of three fields and is shown in Table 25. The TYPE field indicates the type of the configuration format. For a single double-word format, this value is 00 by definition. The SYSADDR field is the address offset of a P0608R configuration register as defined in the I^2C Registers section. The final DATA field contains the value that defines the P0608R configuration register with address offset SYSADDR.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 0	TYPE 00		Reserved (must be zero)					
Byte 1	SYSADDR[7:0]							
Byte 2	SYSADDR[15:8]							
Byte 3	DATA[7:0]							
Byte 4	DATA[15:8]							
Byte 5	DATA[23:16]							
Byte 6	DATA[31:24]							

Table 25 Single Double-word Initialization Sequence Format

The second type of configuration format is the sequential double-word format. It consists of a header (TYPE, SYSADDR, NUMDW) and one to 65535 double-word initialization data fields. The format of a sequential double-word format is shown in Table 26.

The TYPE field indicates the type of the configuration block. For a sequential double-word initialization format, this value is always 01 by definition. The SYSADDR field contains the starting address offset of a P0608R configuration register. The NUMDW field specifies the number of P0608R configuration registers to be sequentially stored. This is followed by the number of DATA fields specified in the NUMDW field. The DATA fields define the content of the P0608R configuration registers starting from address offset SYSADDR.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 0	TYPE 01		Reserved (must be zero)					
Byte 1	SYSADDR[7:0]							
Byte 2	SYSADDR[15:8]							
Byte 3	NUMDW[7:0]							
Byte 4	NUMDW[15:8]							
Byte 5	DATA[7:0]							
Byte 6	DATA[15:8]							
Byte 5	DATA[23:16]							
Byte 6	DATA[31:24]							
	. . . . . .							
Byte 4n+ 5	DATAn[7:0]							
Byte 4n+ 6	DATAn[15:8]							
Byte 4n+7	DATAn[23:16]							
Byte 4n+ 8	DATAn[31:24]							

Table 26 Sequential Double-word Initialization Sequence Format

The third type of configuration format is the configuration-done sequence which consists of two fields as shown in Table 27. The TYPE field is 11 by definition for the configuration-done format. The CHECKSUM field is done per 4 channels — A0, A1, B0, B1 and A2, A3, B2, B3 — of every P0608R device present (2 checksums for each P0608R in the system). This field contains the 1's complement of the sum of all the bytes in all of the

fields stored in the serial EEPROM for its corresponding channel set — A0, A1, B0, B1 or A2, A3, B2, B3 — of the corresponding P0608R device present in the system. The counting starts from the first configuration byte to the last byte of the configuration-done format. All bytes from all 3 types of configuration formats need to be counted.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte 0	TYPE 11		Reserved (must be zero)					
Byte 1	CHECKSUM[7:0]							

Table 27 Configuration-Done Sequence Format

The checksum in the configuration-done sequence enables the integrity of the serial EEPROM initialization to be verified. The checksum is verified in the following manner. An 8-bit counter is cleared and the 8-bit sum is computed over the bytes read from the serial EEPROM during the initialization process, including the entire contents of the configuration-done sequence. The correct result should always be FF (i.e., all ones). Checksum checking may be disabled by setting the Ignore Checksum Errors (ICHECKSUM) bit in the I^2C Control (I2CCTL) register.

Troubleshooting EEPROM Download Issues

The P0608R has a built-in I^2C Status Register (address offset = 14h) that stores flags if certain error events occur during configuration downloads from EEEPROM. By reading this register, a user can verify which errors, if any, occurred during the reading from EEPROM. If an error is detected during loading of the serial EEPROM, then loading of the serial EEPROM is aborted. Once serial EEPROM initialization completes, is aborted, or when an error is detected, the EEPROM Done (EEPROMDONE) bit is set in the I^2C Status (I2CSTS) register. Table 28 summarizes possible error types and the associated flag bits.

Error	Action Taken
Configuration-Done Sequence checksum mismatch with that computed	- CSERR bit is set in the I2CSTS register - Abort initialization, set EEPROMDONE bit in the I2CSTS register
Invalid configuration block type (only invalid type is 0x2)	- CSERR bit is set in the I2CSTS register - Abort initialization, set EEPROMDONE bit in the I2CSTS register
An unexpected NACK is observed during a master I^2C transaction	- NAERR bit is set in the I2CSTS register - Abort initialization, set EEPROMDONE bit in the I2CSTS register
A misplaced START or STOP condition is detected by the master I^2C interface	- OTHERERR bit is set in the I2CSTS register - Abort initialization, set EEPROMDONE bit in the I2CSTS register
Serial EEPROM address rollover error detected	- ROLLOVER bit is set in the I2CSTS register - Abort initialization, set EEPROMDONE bit in the I2CSTS register
Blank serial EEPROM detected	- BLANK bit is set in the I2CSTS register - Abort initialization, set EEPROMDONE bit in the I2CSTS register
Checksum error detected	- CSERR bit is set in the I2CSTS register - Abort initialization, set EEPROMDONE bit in the I2CSTS register
Unmapped register initialization attempt	- URIA bit is set in the I2CSTS register - Abort initialization, set EEPROMDONE bit in the I2CSTS register

Table 28 Serial EEPROM Initialization Errors

Rollover Flag Details

During serial EEPROM initialization, the master I^2C interface begins reading bytes starting at serial EEPROM address zero. These bytes are interpreted as configuration blocks and sequential reading of the serial EEPROM continues until the end of a configuration-done block is reached or the serial EEPROM address rolls over from 0xFFFF to 0x0 due to insufficient EEPROM memory. When a serial EERPROM address roll over is detected, loading of the serial EEPROM is aborted and the Serial EEPROM Rollover (ROLLOVER) bit is set in the I2C Status (I2CSTS) register.

Blank Flag Details

A blank serial EEPROM contains 0xFF in all data bytes. When the P0608R is configured to initialize from serial EEPROM and the first 256 bytes read from the EEPROM all contain the value 0xFF, then loading of the serial EEPROM is aborted, the computed checksum is ignored, the Blank Serial EEPROM (BLANK) bit is set in the I^2C Status Register (I2CSTS), and normal device operation begins (i.e., the device operates in the same manner as though it were not configured to initialize from the serial EEPROM). This behavior allows a board manufacturing flow that utilizes uninitialized serial EEPROMs.

Unmapped Register Initialization Attempt Flag Details

All register initialization performed by the serial EEPROM is done in DWord (32-bit) quantities. Byte values may be modified by writing the entire DWord. If during serial EEPROM initialization an attempt is made to initialize a register that is not defined in a configuration space, then the Unmapped Register Initialization Attempt (URIA) bit is set in the I2CSTS register and the write is ignored. This bit is only set in the device when the start address is such that it would write this block into its register space.

Electrical Specifications

Absolute Maximum Ratings

Note: All voltage values, except differential voltages, are measured with respect to ground pins.

Parameter	Value	Unit
Supply voltage range VDD	–0.5 to 1.35	V
Supply voltage range VDD3	–0.5 to 4.0	V
Voltage range Differential I/O	–0.5 to VDD +0.5	V
Control I/O	–0.5 to VDD + 0.5	V
ESD requirements: Electrostatic discharge Human body model	±2000	V
ESD requirements: Charged-Device Model (CDM)	±500	V
ESD requirements: Machine model	±125	V
Storage ambient temperature	-55 to 150	°C

Table 29 Absolute Maximum Ratings

Warning: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Notes	Min	Typical	Max	Unit
Power Supply Pin Requirements					
VDD	1.2V DC analog supply voltage (specified at bump pins)	1.14	1.2	1.26	V
VDD3	3.3V DC supply voltage for I^2C interface	3.0	3.3	3.6	V
Temperature Requirements					
TA	Ambient operating temperature - Commercial	0	—	70	°C
	Ambient operating temperature - Industrial	-40	—	85	°C
TJUNCTION	Junction operating temperature	-40	—	125	°C

Table 30 P0608R Operating Conditions

Power Consumption

Table 31 below lists power consumption values under typical and maximum operating conditions.

Parameter	Notes	Min	Typical	Max	Unit
Active Mode					
I_{VDD}	Current into VDD supply	—	660	1000	mA
I_{VDD3}	Current into VDD3 supply		80	150	µA
P_D	Full chip power[1]		800	1200	mW
P_{D-ch}	Power per channel[1]		100	150	mW
Standby Mode	Full chip standby		60	80	mW

Table 31 P0608R Power Consumption

1. Maximum power under all conditions. Power is reduced by selecting smaller de-emphasis settings (closer or equal to 0dB).

Package Thermal Considerations

The data in Table 32 below contains information that is relevant to the thermal performance of the 100-pin FPBGA package.

Parameter	Description	Value	Conditions	Units
$T_{J(max)}$	Junction Temperature	125	Maximum	^{o}C
$T_{A(max)}$	Ambient Temperature	70	Maximum for commercial-rated products	^{o}C
		85	Maximum for industrial-rated products	^{o}C
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	46.4	Zero air flow	$^{o}C/W$
		41.3	1 m/S air flow	$^{o}C/W$
		40.5	2 m/S air flow	$^{o}C/W$
		39.2	3 m/S air flow	$^{o}C/W$
		30.9	4 m/S air flow	$^{o}C/W$
		31.0	5 m/S air flow	$^{o}C/W$
θ_{JB}	Thermal Resistance, Junction-to-Board	31.6	NA	$^{o}C/W$
θ_{JC}	Thermal Resistance, Junction-to-Case	26.7	NA	$^{o}C/W$

Table 32 Thermal Specifications for P0608R, 9x9mm FPBGA100 Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 32. Consequently, the effective junction to ambient thermal resistance (θ_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired θ_{JA} becomes a known entity to the system designer. How to achieve the desired θ_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of θ_{JC} (value provided in Table 32), thermal resistance of the chosen adhesive (θ_{CS}), that of the heat sink (θ_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board).

DC Specifications

Parameter	Description	Min	Typical	Max	Unit
1.2V, 2-Level Input and Output Pin Requirements					
V_{IL}	Digital Input Signal Voltage Low Level[1]	- 0.3		0.6	V
V_{IH}	Digital Input Signal Voltage High Level[1]	1.1		VDD + 0.3	V
V_{OL}	Digital Output Signal Voltage Low Level, I_{OL}=3mA[2]			0.4	V
V_{OH}	Digital Output Signal Voltage High Level, I_{OH}=3mA[2]	VDD - 0.4			V
V_{HYS}	Hysteresis of Schmitt Trigger Input	0.1			V
I_{IL}	Input current with internal pull-up resistor[3]			100	µA
I_{IH}	Input current with internal pull-down resistor[4,5]			100	µA
$R_{WEAK\_PD\_2L}$	Internal weak pull-down resistor at 2-level input pads[4,5.]	11			K ohm
$R_{WEAK\_PU\_2L}$	Internal weak pull-up resistor at 2-level input pads[3]	11			K ohm
3.3V Pin Requirements					
V_{IL_VDD3}	Digital Input Signal Voltage Low Level[6]	-0.3		0.8	V
V_{IH_VDD3}	Digital Input Signal Voltage High Level[6]	2.1		VDD3 + 0.3	V
$V_{OL\_VDD3\_HP}$	Digital Output Signal Voltage Low Level, High Power, IOL=4mA[7,8]			0.4	V
$V_{OL\_VDD3\_LP}$	Digital Output Signal Voltage Low Level, Low Power, IOL=350uA[7,8]			0.4	V
1.2V, 3-Level Input Pin Requirements					
V_{IL}	Digital Input Signal Voltage Low Level	-0.3		0.25*VDD-0.1	V
V_{IM}	Digital Input Signal Voltage Mid Level	0.25*VDD+0.1		0.75*VDD-0.1	V
V_{IH}	Digital Input Signal Voltage High Level	0.75*VDD+0.1		VDD+0.3	V
I_{IL}	Input Current for V_{IL}			180	µA
I_{IH}	Input Current for V_{IH}			180	µA
$R_{WEAK\_PD\_3L}$	Internal weak pull-down resistor at all 3-level input pads	6.3			K ohm
$R_{WEAK\_PU\_3L}$	Internal weak pull-up resistor at all 3-level input pads	6.3			K ohm

Table 33 DC Specification

1. Applies to input pins.
2. Applies to output pins.
3. Applies only to 2-level input pins with default values set to VDD in the Pin Description table (Table 41).
4. Applies only to 2-level input pins with default values set to VSS in the Pin Description table (Table 41).
5. Applies to I2CA pins in the Pin Description table (Table 41).
6. Applies to I2C interface pins.
7. VOL low power and high power state is controlled via an external pull-up design in the end-application.
8. Applies to SDA and SCL pins.

AC Specifications

Latency Specification

Parameter	Description	Min	Typical	Max	Unit
Latency	Input to output signal propagation device		300		ps

Table 34 P0608R Latency Specification

Receiver Specifications

Parameter	Description	Min	Typical	Max	Unit
Receiver Input Jitter Specifications					
T_{RX-DDJ}	Receive Input Signal Data Dependent Jitter (Inter-Symbol Interference. Levels 1 and 2.)[1]			>1	UI
$R_{\_JT}$	Receive Input Signal Total Jitter Tolerance (Levels 1 and 2)[1]			>1	UI
T_{RX-EYE}	Receiver eye time opening (can recover from closed eye due to trace attenuation and ISI jitter) (Levels 1 and 2)	0			UI
Receiver Input Voltage and Eye Specification					
R_Vin	Absolute Input Voltage (measured at device pins)	-0.1		VDD + 0.1	V
$R_{\_Vdiff}$	Receiver Differential Peak-Peak Voltage[2]	0		2000	mV
$V_{RX-CM-AC-P}$	Receiver AC Common Mode Voltage			150	mV
Receiver Return Loss					
$R_{\_SDD11}$	Receiver Differential Return Loss (0 - 3.125GHz)			-8	dB
$R_{\_SCC11}$	Receiver Common Mode DC Return Loss			-6	dB
Receiver DC Impedance					
$R_{\_Rdin}$	DC Differential Impedance[3]	80		120	Ohm
$Z_{RX-HIGH-IMP-DC-POS}$	DC Input Common Mode Receive High Impedance for Input Voltage from 0V to 200mV	50k			Ohm
$Z_{RX-HIGH-IMP-DC-NEG}$	DC Input Common Mode Receive High Impedance for Input Voltage from 0V to -200mV	1k			Ohm
$Z_{DIFF-HIZ-POS}$	Differential Receive High Impedance for Input Voltage from 0V to 200mV	200k			Ohm
$Z_{DIFF-HIZ-NEG}$	Differential Receive High Impedance for Input Voltage from 0V to -200mV	4k			Ohm
Receiver Signal Detection					
$V_{RX-LOS-DET-DIFFp-p}$	Loss of Signal Detect Threshold (Programmable)[4,5]	50		175	mV
$T_{SIGDET-ATTACK}$	Signal Detect Valid Signal Attack Time (Turn-on time)			15	ns
$T_{SIGDET-DECAY}$	Signal Detect Valid Signal Decay Time (Turn-off time)			15	ns
$T_{SIGDET-ATT-DECAY-MIS}$	Signal Detect Attack / Decay Time Mismatch			5	ns

Table 35 P0604R Receiver Electrical Specifications

1. PRBS-7 pattern used.

2. The minimum value of 0 mV represents the case when Eye is completely closed.

3. When TERM_CTL bit is set to 100Ω.

4. The value can be programmed from 50mV to 170mV via the SIG_THRESH register.

5. This feature should be disabled for typical SRIO applications not requiring loss-of-signal detection by programming both SIG_PD_TRANDET and SIG_PD_LVLDET bits to 1.

Transmitter Specifications

Parameter	Description	Min	Typical	Max	Unit
Output Eye and Common Voltage Specification					
T_Vdiff_1	Differential Transmitter Swing (Short run, Level 1)[1]	800		1100	mVppd
T_Vdiff_2	Differential Transmitter Swing (Long run: Levels 1 and 2. Medium run: Level 2)[1]	800		1100	mVppd
T_Vdiff_3	Differential Transmitter Swing (Short run, Level 2)[2]	400		750	mVppd
V_O	Absolute Output Voltage	-0.40		VDD+0.3	V
$D_{TX-DEEMP}$	Output De-emphasis (programmable). Defined as $20\log(V_{TX-DE-EMP} / V_{TX-DIFF})$ [dB] [3]	-9.5		0	dB
$V_{TX-DE-RATIO-3.5dB}$	Tx de-emphasis level ratio[4] (default)	-4.0		-3.0	dB
T_tr, T_tf	Rise/Fall Time (20% to 80%) (programmable)	25			ps
T_Diffpair-skew	Transmitter Differential Pair Skew			15	ps
$T_{RF-MISMATCH}$	Tx Rise/Fall Mismatch			0.1	UI
$T_{\_X1}$	Eye Mask (Level 1)[5,6]			0.17	UI
$T_{\_X2}$	Eye Mask (Level 1)[5,6]			0.39	UI
$T_{\_Y1}$	Eye Mask (Short run, Level 1)[6]	250			mV
$T_{\_Y2}$	Eye Mask (Short run, Level 1)[6]			500	mV
$T_{\_Y1}$	Eye Mask (Long run, Level 1)[6]	400			mV
$T_{\_Y2}$	Eye Mask (Long run, Level 1)[6]			800	mV
$T_{\_TJ}$	Total Jitter (Level 2)			0.30	UIpp
$T_{\_X1}$	Eye Mask (Level 2)[6,7]			0.15	UI
$T_{\_X2}$	Eye Mask (Level 2)[6,7]			0.40	UI
$T_{\_Y1}$	Eye Mask (Short run, Level 2)[6]	200			mV
$T_{\_Y2}$	Eye Mask (Short run, Level 2)[6]			375	mV
$T_{\_Y1}$	Eye Mask (Medium and Long run, Level 2)[6]	200			mV
$T_{\_Y2}$	Eye Mask (Medium and Long run, Level 2)[6]			600	mV
$T_{RES-DJ-6.25GBPS-1}$	Residual Deterministic Jitter at output pins (1 inch FR4 trace before receiver input pins, 6.25Gbps)[8]	—	—	<0.05	UI
$T_{RES-DJ-6.25GBPS-2}$	Residual Deterministic Jitter at output pins (62 inch FR4 trace before receiver input pins, 6.25Gbps)[8]	—	0.2	0.28	UI
$T_{\_Vcm}$	Transmitter DC Common Mode Voltage	0		VDD	V
C_{TX}	AC Coupling Capacitor	75		200	nF

Table 36 P0604R Transmitter Electrical Requirements (Part 1 of 2)

Parameter	Description	Min	Typical	Max	Unit
Transmitter DC Impedance					
$T_{\_Rd}$	Transmitter Output Differential DC Impedance[9]	80	100	120	Ohm
$T_{\_Ishort}$	Transmitter Short-circuit Current Limit			100	mA
Transmitter Return Loss					
$T_{\_SDD22}$	Transmitter Differential Return Loss (0 - 3.125GHz)			-10	dB
$T_{\_SCC22}$	Transmitter Common-Mode DC Return Loss			-6	dB
Loss of Signal					
V_{TX-LOS}	Loss of Signal Output Voltage			20	mV
$V_{CM-DELTA-SQUELCH}$	Maximum Common-Mode Step Entering/Exiting Loss of Signal Mode			50	mV
$V_{TX-CM-DC-ACTIVELOS-DELTA}$	Absolute Delta of DC Common Mode Voltage during L0 and Loss of Signal.	0		100	mV
$V_{TX-LOS-DIFF-AC-p}$	Loss of Signal Differential Peak Output Voltage	0		20	mV
$V_{TX-LOS-DIFF-DC}$	DC Loss of Signal Differential Output Voltage	0		5	mV
Lane Skew					
L_{TX-SMO}	Lane-to-Lane Output Skew		10	50	ps

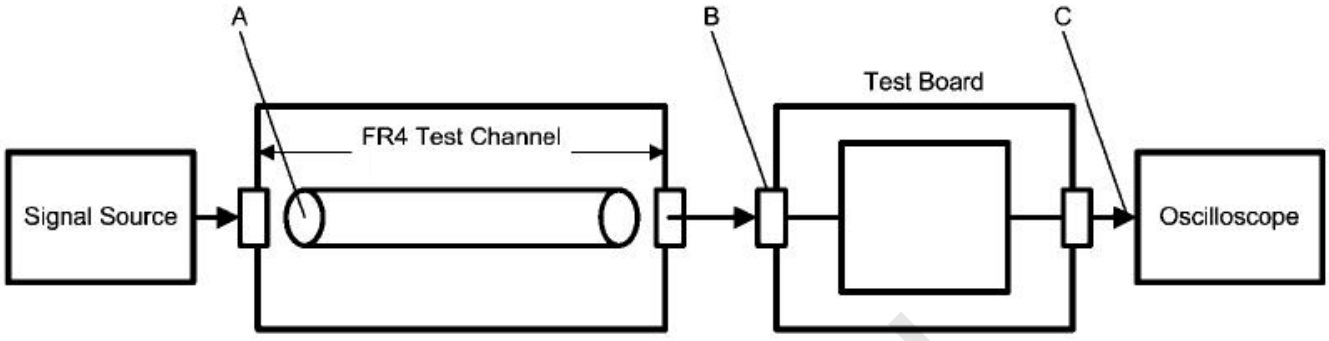
Table 36 P0604R Transmitter Electrical Requirements (Part 2 of 2)

1. When the TX_SWING register is set to 0.95V.
2. When the TX_SWING register is set to 0.5V or 0.6V.
3. Programmable via the TX_DEEMP register or via pin A0TXDE, A1TXDE, etc.
4. When the TX_DEEMP register is set to 3.5dB.
5. With 62-inch FR4 trace at device inputs.
6. Transmit Eye Mask is shown in Figure 19.
7. With 100cm FR4 trace at device inputs.
8. Refer to Figure 18.
9. When TERM_CTL bit is set to 100Ω.

Repeater Additive Jitter

Parameter	Description	Min	Typical	Max	Unit
D_J	Repeater Data Dependent Jitter			<0.05	UI
R_J	Random Jitter			1	psrms

Table 37 P0608R Repeater Additive Jitter



A — FR4 Trace B — SMA Connector C — Measurement Point

Note: FR4 test channel is bypassed for 1-inch input trace case.

Figure 18 Residual Jitter Characterization Test Setup

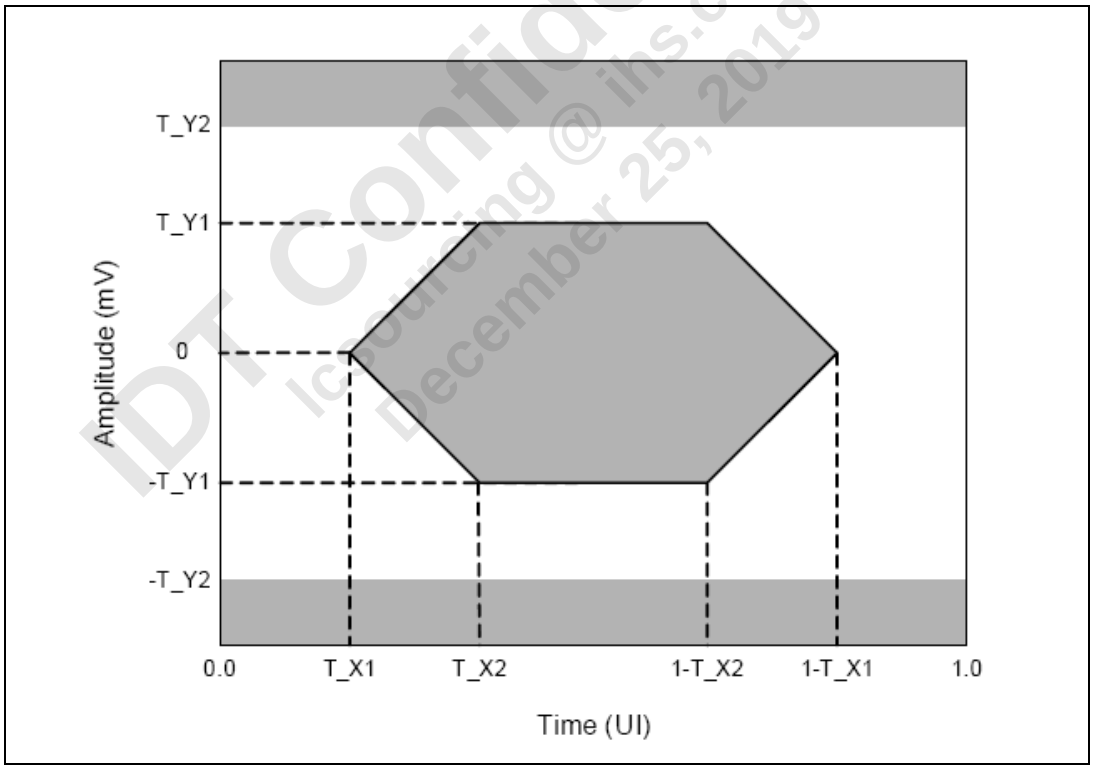


Figure 19 Transmit Eye Mask

Reference Clock Specifications

The P0608R includes a single differential input buffer and two output reference clock buffers. The single reference clock input can be multiplexed to either output buffer, or can be multi-casted onto both output buffers simultaneously.

Note: The input and output reference clocks must be AC-coupled on the PCB using a capacitor between 10nF and 100nF.

The input reference clock electrical specifications are shown in Table 38. Note that the P0608R does not require a reference clock.

Parameter	Description	Min	Typ	Max	Unit
Input Clock Electrical Specifications					
P_{REF_IN}	Clock Frequency	30	100	125	MHz
$V_{REF\text{-}DIFF\text{-}PKPK\_IN}$	Clock Input Amplitude	400		2400	mV
$T_{REF\text{-}RISE\text{-}FALL\_IN}$	Clock Input Rise/Fall Time	350	500	650	ps
$T_{REF\text{-}DUTY\_IN}$	Clock Input Duty-Cycle	40	50	60	%
R_{IN}	Clock Input Internal Termination to Ground (on both P and N pins)	40	50	60	Ohm

Table 38 Input Reference Clock Buffer Electrical Specifications

The output reference clock uses low voltage swing and low power differential CML signaling. The electrical specifications are shown in Table 39.

Parameter	Description	Min	Typ	Max	Unit
Output Clock Electrical Specifications					
P_{REF_OUT}	Clock Frequency	30	100	125	MHz
$V_{REF\text{-}DIFF\text{-}PKPK\_OUT}$	Clock Output Amplitude	450	600	750	mV
$V_{REF\text{-}CM\_OUT}$	Clock Output Common-Mode Voltage (before capacitor)		VDD - 150		mV
$T_{REF\text{-}RISE\text{-}FALL\_OUT}$	Clock Rise/Fall Time	300		1200	ps
$T_{REF\text{-}DUTY\_OUT}$	Clock Duty-Cycle	40	50	60	%
$R_{DIFFOUT}$	Differential Output Impedance	80	100	120	Ohm

Table 39 Output Reference Clock Buffer Electrical Specifications

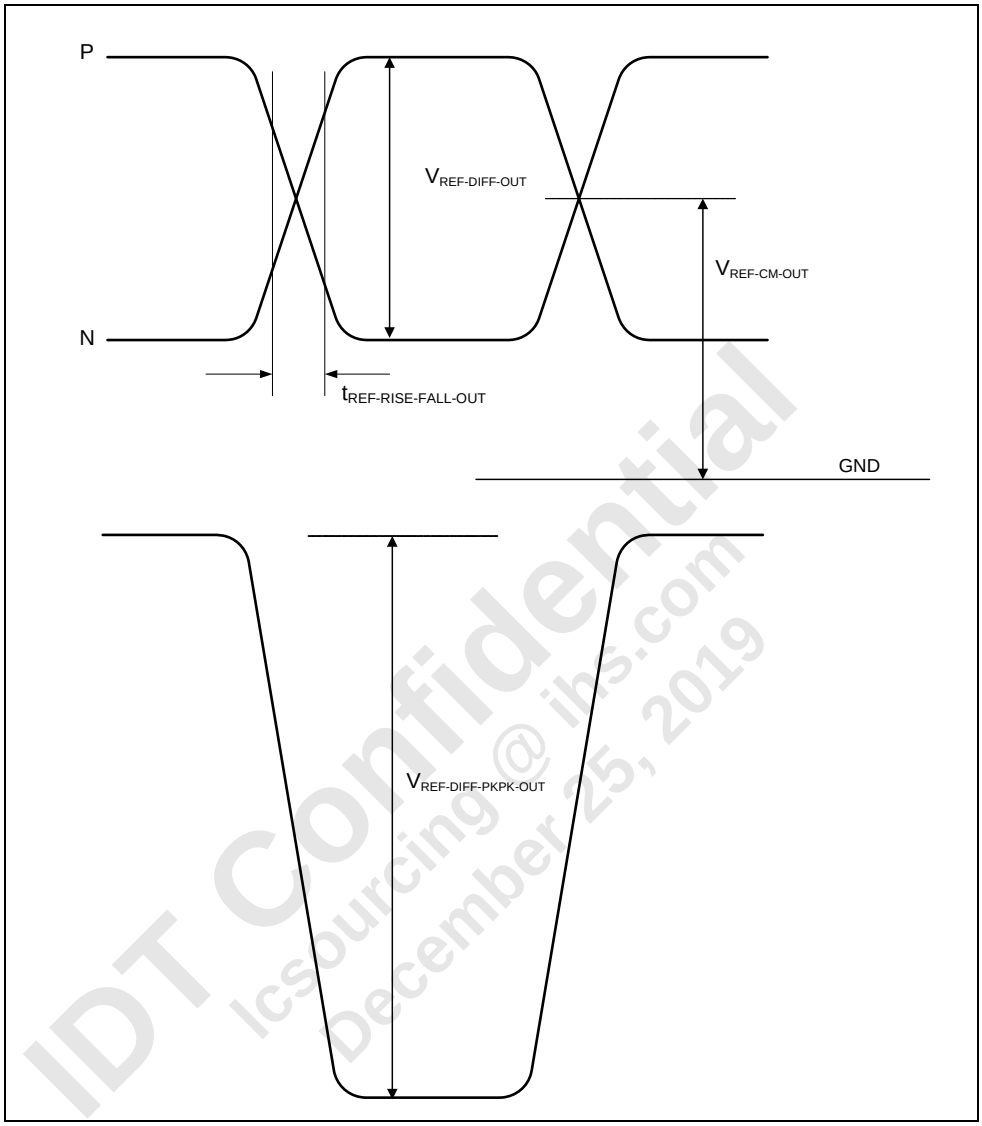


Figure 20 Output Reference Clock Buffer Parameters

I2C Specifications

Parameter	Description	Min	Typ	Max	Unit
f_{SCL}	Clock frequency	10		400	kHz
t_{HIGH}	Clock pulse width high time	600			ns
t_{LOW}	Clock pulse width low time	1300			ns
$t_{TIMEOUT(L)}$	Detect clock low timeout	24		40	ms
$t_{TIMEOUT(H)}$	Detect clock high timeout	40		66	us
t_R	SDA rise time	20		300	ns
t_F	SDA fall time	20		300	ns
$t_{SU:DAT}$	Data in setup time	100			ns
$t_{HD:DI}$	Data in hold time	0			ns
$t_{HD:DAT}$	Data out hold time	200		900	ns
$t_{SU:STA}$	Start condition setup time	600			ns
$t_{HD:STA}$	Start condition hold time	600			ns
$t_{SU:STO}$	Stop condition setup time	600			ns
t_{BUF}	Time between Stop Condition and next Start Condition	1300			ns
t_{GLITCH_FILTER}	SDA and SCL glitch removal time	80		130	ns

Table 40 I2C AC Timing Specifications

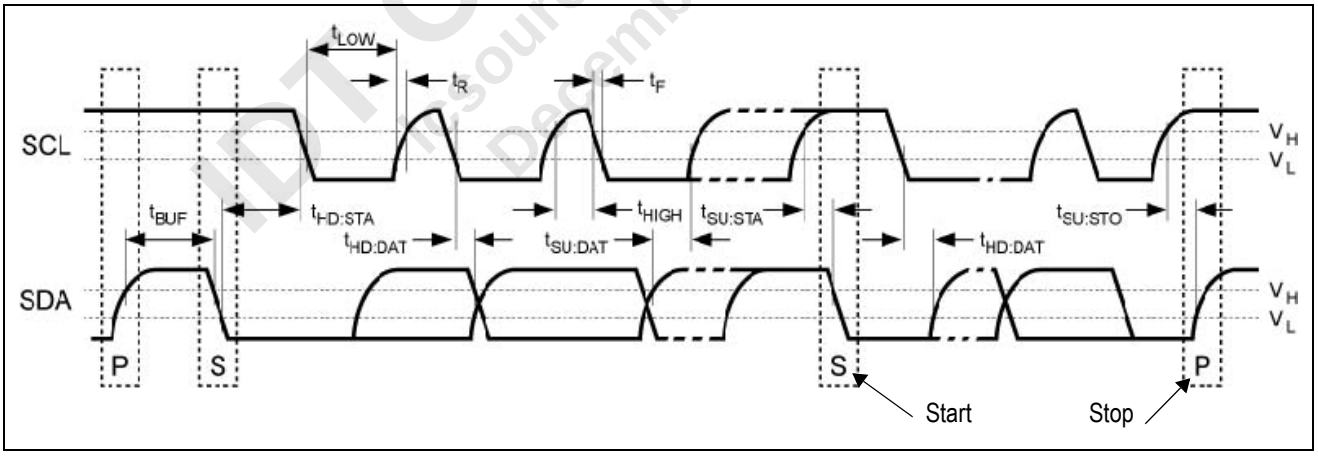


Figure 21 I2C AC Waveforms

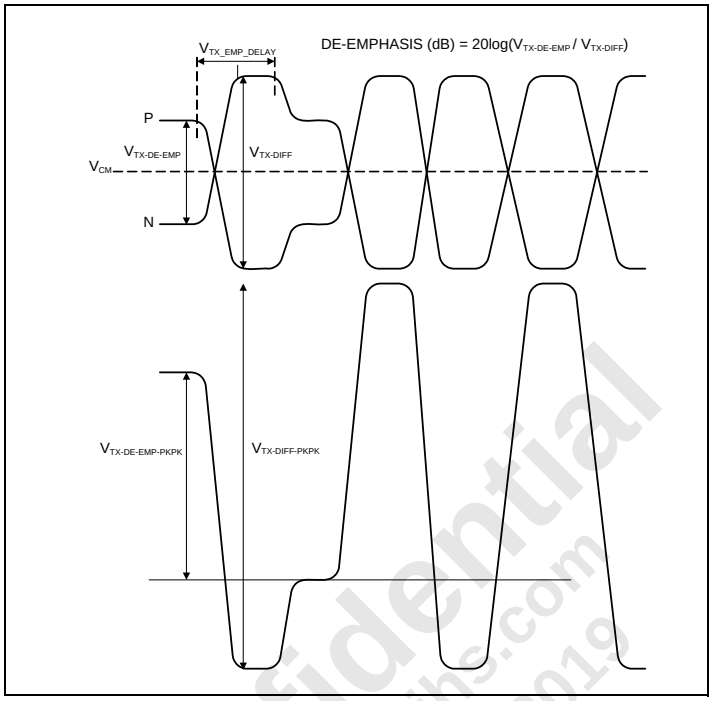


Figure 22 Transmitter Swing Levels With and Without De-emphasis

Note: $V_{TX\text{-}DIFF\text{-}PKPK}$ Peak to Peak voltage is twice as large as voltage difference between P pins and N pins of differential pairs. For example, if the P pin swings from 0.8V to 1.4V while the N pin swings from 1.4V to 0.8V, then:$V_{TX\text{-}DIFF\text{-}PKPK}$ = 2*(1.4-0.8)=1.2V.

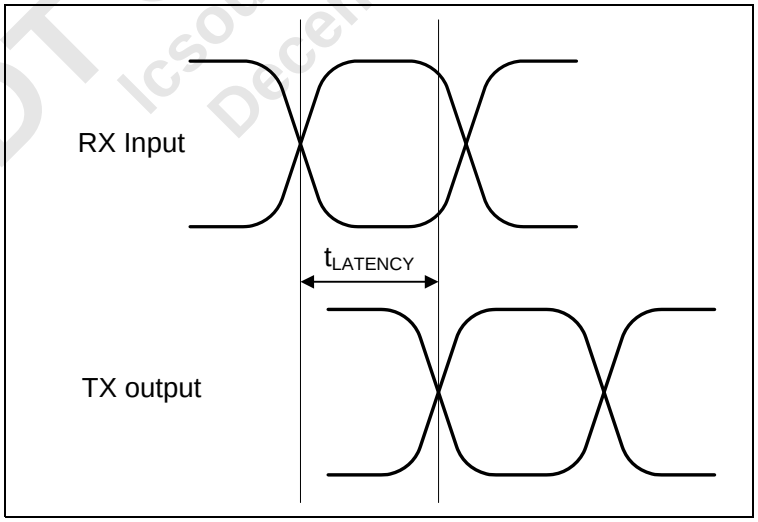


Figure 23 Definition of Latency Timing

Pin Description

Note: Unused pins can be left floating except when a Note in this table specifies otherwise (see VDD3, CKINN/P, SCL, and SDA below).

Pin Name	Pin #	Description	Input/ Output/ Power 2 or 3 Level
Power			
VDD	A1,A4,A7,A10,D1,D4, D7,D10,G1,G4,G7, G10,K1,K4,K7,K10	1.2V (typ) Power supply for Repeater high speed channels and internal logic. Each VDD pin should be connected to the VDD plane through a low inductance path, with a via located as close as possible to the landing pad of VDD pins. It is recommended to have a 0.01 µF or 0.1 µF, X7R, size-0402 bypass capacitor from each VDD pin to ground plane.	Power
VDD3	E1	3.3V (typ) Power supply for Repeater I^2C interface signals It is recommended to have a 0.01 µF or 0.1 µF, X7R, size-0402 bypass capacitor from this pin to ground plane. Note: If not used, tie to VDD.	Power
VSS	B2,B3,B8,B9,C2,C3, C8,C9,E2,H2,H3,H8, H9,J2,J3,J8,J9	VSS reference. Each VSS pin should be connected to the ground plane through a low inductance path, with a via located as close as possible to the landing pad of the VSS pin.	Power
Data Signals			
A0RXN A0RXP	A3 A2	Upstream Channel A0 Receive Data Ports	Input
A0TXN A0TXP	A9 A8	Upstream Channel A0 Transmit Data Ports	Output
B0RXN B0RXP	C7 B7	Downstream Channel B0 Receive Data Ports	Input
B0TXN B0TXP	C1 B1	Downstream Channel B0 Transmit Data Ports	Output
A1RXN A1RXP	D3 D2	Upstream Channel A1 Receive Data Ports	Input
A1TXN A1TXP	D9 D8	Upstream Channel A1 Transmit Data Ports	Output
B1RXN B1RXP	C10 B10	Downstream Channel B1 Receive Data Ports	Input
B1TXN B1TXP	C4 B4	Downstream Channel B1 Transmit Data Ports	Output
A2RXN A2RXP	G3 G2	Upstream Channel A2 Receive Data Ports	Input
A2TXN A2TXP	G9 G8	Upstream Channel A2 Transmit Data Ports	Output
B2RXN B2RXP	J7 H7	Downstream Channel B2 Receive Data Ports	Input

Table 41 P0608R Pin Description (Part 1 of 3)

Pin Name	Pin #	Description	Input/ Output/ Power 2 or 3 Level
B2TXN B2TXP	J1 H1	Downstream Channel B2 Transmit Data Ports	Output
A3RXN A3RXP	K3 K2	Upstream Channel A3 Receive Data Ports	Input
A3TXN A3TXP	K9 K8	Upstream Channel A3 Transmit Data Ports	Output
B3RXN B3RXP	J10 H10	Downstream Channel B3 Receive Data Ports	Input
B3TXN B3TXP	J4 H4	Downstream Channel B3 Transmit Data Ports	Output
Input Control and Output Status			
A0EN (Channel A0) A1EN (Channel A1) A2EN (Channel A2) A3EN (Channel A3)	E3 E4 K6 K5	Channel A0 Enable. Programming channel A0 via pins is shown below. To program other channels, use pins for those channels. A0EN — Setting VSS — Disabled and RX terminations are in Hi-Z, TX is disabled Open — Enabled and optimized for data rates 3.125Gbps and below (Default) VDD — Enabled and optimized for data rates 6.25Gbps and below Programming is also available via I^2C. Refer to parameter CHEN in section I2C Slave Mode.	Input - 3 level
B0EN (Channel B0) B1EN (Channel B1) B2EN (Channel B2) B3EN (Channel B3)	B6 B5 F9 F8	Channel B0 Enable. Programming channel B0 via pins is shown below. To program other channels, use pins for those channels. A0EN — Setting VSS — Disabled and RX terminations are in Hi-Z, TX is disabled Open — Enabled and optimized for data rates 3.125Gbps and below (Default) VDD — Enabled and optimized for data rates 6.25Gbps and below Programming is also available via I^2C. Refer to parameter CHEN in section I2C Slave Mode.	Input - 3 level
Other Control Signals			
ENCLK	E8	Reference Clock Output Enable Pin. Default tied-off value in the IO = VSS via internal weak pull-down. Programming this channel via pins is shown below. ENCLK — Setting VSS — Clock outputs disabled to Hi-Z (internal 11K ohm minimum pull-down applied) VDD — Clock outputs enabled	Input - 2 level

Table 41 P0608R Pin Description (Part 2 of 3)

Pin Name	Pin #	Description	Input/ Output/ Power 2 or 3 Level
CKINN CKINP	E7 F7	Reference Clock Input Port Note: An input clock is not required for repeater/data path operation. When not used, set ENCLK=0 to reduce power. Note: If not used, tie to ground.	Input
CKOUT0N CKOUT0P	E6 F6	Reference Clock Output Port #1	Output
CKOUT1N CKOUT1P	E5 F5	Reference Clock Output Port #2	Output
A0SIGDET (Channel A0) A1SIGDET (Channel A1) A2SIGDET (Channel A2) A3SIGDET (Channel A3)	C5 D5 H5 J5	Indicates that Signal was detected at the channel's input. A0SIGDET Setting VSS No signal VDD Signal detected	Output - 2 level
B0SIGDET (Channel B0) B1SIGDET (Channel B1) B2SIGDET (Channel B2) B3SIGDET (Channel B3)	C6 D6 J6 H6	Indicates that Signal was detected at the channel's input. B0SIGDET Setting VSS No signal VDD Signal detected	Output - 2 level
I2CA[1] I2CA[2]	E10 F10	I^2C Address Identifier Pins. Must be shorted on the board to a distinct, unique address. Default Tied Off Value in the IO = VSS via internal 11K ohm minimum weak pull-down. Note: Use 1.2V VDD supply to set these pins to 1.	Input - 2 level
INTMODE	A5	Interface Control Mode. 3 Level Input Pin. INTMODE Setting VSS I^2C slave mode with register programming Open Pin programming is enabled (Default) VDD I^2C master mode	Input - 3 level
PDB	F3	Power-down Enable. Default tied-off value in the IO = VDD via internal weak pull-up. PDB Setting VSS Powerdown IC. RX terminations are in Hi-Z, TX is disabled. Recommended resistance to ground with value between 0 ohms and 1k ohm. VDD Normal operation (internal 11K ohm minimum pull-up applied). No external termination is required.	Input - 2 level
SCL	F1	I^2C Clock Pin (Open Drain) Note: If not used, tie to ground.	I/O
SDA	F2	I^2C Data Pin (Open Drain) Note: If not used, tie to ground.	I/O
RSVD	A6, E9, F4 G5, G6	Reserved. Do not connect.	

Table 41 P0608R Pin Description (Part 3 of 3)

Package Pinout — 100-BGA Signal Pinout for the P0608R

Table 42 lists the pin numbers and signal names for the P0608R device.

Function	Pin	Function	Pin	Function	Pin
A0EN	E3	B1SIGDET	D6	VDD	A10
A0RXN	A3	B1TXN	C4	VDD	D1
A0RXP	A2	B1TXP	B4	VDD	D4
A0SIGDET	C5	B2EN	F9	VDD	D7
A0TXN	A9	B2RXN	J7	VDD	D10
A0TXP	A8	B2RXP	H7	VDD	G1
A1EN	E4	B2SIGDET	J6	VDD	G4
A1RXN	D3	B2TXN	J1	VDD	G7
A1RXP	D2	B2TXP	H1	VDD	G10
A1SIGDET	D5	B3EN	F8	VDD	K1
A1TXN	D9	B3RXN	J10	VDD	K4
A1TXP	D8	B3RXP	H10	VDD	K7
A2EN	K6	B3SIGDET	H6	VDD	K10
A2RXN	G3	B3TXN	J4	VDD3	E1
A2RXP	G2	B3TXP	H4	VSS	B2
A2SIGDET	H5	CKINN	E7	VSS	B3
A2TXN	G9	CKINP	F7	VSS	B8
A2TXP	G8	CKOUT0N	E6	VSS	B9
A3EN	K5	CKOUT0P	F6	VSS	C2
A3RXN	K3	CKOUT1N	E5	VSS	C3
A3RXP	K2	CKOUT1P	F5	VSS	C8
A3SIGDET	J5	ENCLK	E8	VSS	C9
A3TXN	K9	I2CA1	E10	VSS	E2
A3TXP	K8	I2CA2	F10	VSS	H2
B0EN	B6	INTMODE	A5	VSS	H3
B0RXN	C7	PDB	F3	VSS	H8
B0RXP	B7	RSVD	A6,E9,F4, G5,G6	VSS	H9
B0SIGDET	C6			VSS	J2
B0TXN	C1	SCL	F1	VSS	J3
B0TXP	B1	SDA	F2	VSS	J8
B1EN	B5	VDD	A1	VSS	J9
B1RXN	C10	VDD	A4	—	—
B1RXP	B10	VDD	A7		

Table 42 P0608R Alphabetical Pin List

P0608R Pin Diagram

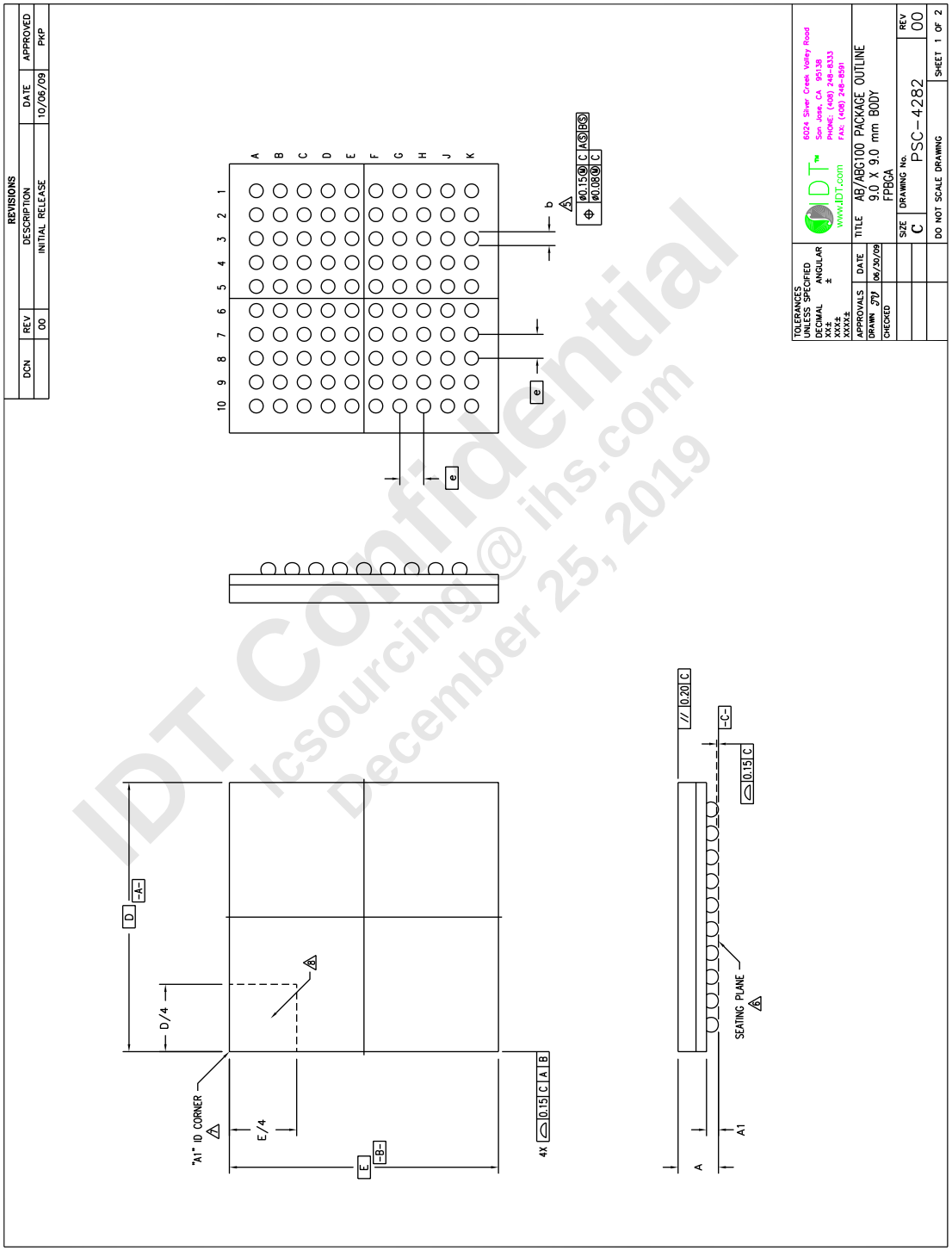
The following figure lists the pin numbers and the signal names for the P0608R 100-Ball BGA package.

	1	2	3	4	5	6	7	8	9	10	
A	VDD	A0RXP	A0RXN	VDD	INTMODE	RSVD	VDD	A0TXP	A0TXN	VDD	A
B	B0TXP	VSS	VSS	B1TXP	B1EN	B0EN	B0RXP	VSS	VSS	B1RXP	B
C	B0TXN	VSS	VSS	B1TXN	A0SIGDET	B0SIGDET	B0RXN	VSS	VSS	B1RXN	C
D	VDD	A1RXP	A1RXN	VDD	A1SIGDET	B1SIGDET	VDD	A1TXP	A1TXN	VDD	D
E	VDD3	VSS	A0EN	A1EN	CKOUT1N	CKOUT0N	CKINN	ENCLK	RSVD	I2CA1	E
F	SCL	SDA	PDB	RSVD	CKOUT1P	CKOUT0P	CKINP	B3EN	B2EN	I2CA2	F
G	VDD	A2RXP	A2RXN	VDD	RSVD	RSVD	VDD	A2TXP	A2TXN	VDD	G
H	B2TXP	VSS	VSS	B3TXP	A2SIGDET	B3SIGDET	B2RXP	VSS	VSS	B3RXP	H
J	B2TXN	VSS	VSS	B3TXN	A3SIGDET	B2SIGDET	B2RXN	VSS	VSS	B3RXN	J
K	VDD	A3RXP	A3RXN	VDD	A3EN	A2EN	VDD	A3TXP	A3TXN	VDD	K
	1	2	3	4	5	6	7	8	9	10	

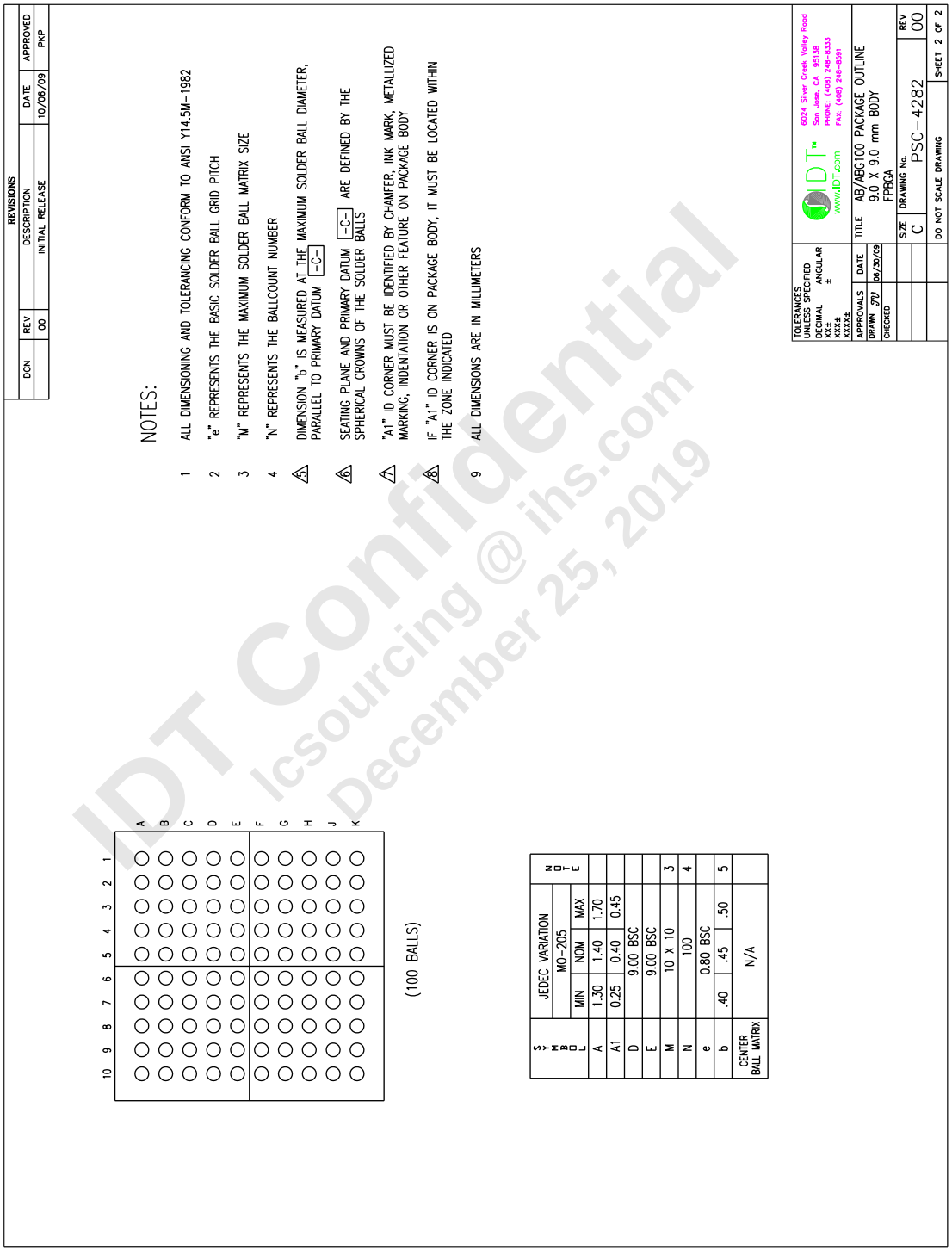
Figure 24 P0608R Pin Diagram — Top View

Note: Data positive (P) and negative (N) pins may be switched without any protocol impact provided channel polarity from host to target is maintained. Example: pins A0RXN (A3) and A0RXP (A2) may be switched provided that pins A0TXN (A9) and A0TXP (A8) are also switched; pins B1RXN (C10) and B1RXP (B10) may be switched provided that pins B1TXN (C4) and B1TXP (B4) are also switched.

FPBGA Package Dimension



FPBGA Package Dimension — Page Two



REVISIONS

DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	10/06/09	PKP

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH
3. "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE
4. "N" REPRESENTS THE BALLCOUNT NUMBER
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C-
6. SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS
7. "A1" ID CORNER MUST BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKING, INDENTATION OR OTHER FEATURE ON PACKAGE BODY
8. IF "A1" ID CORNER IS ON PACKAGE BODY, IT MUST BE LOCATED WITHIN THE ZONE INDICATED
9. ALL DIMENSIONS ARE IN MILLIMETERS

(100 BALLS)

SYMBOL	JEDEC VARIATION MO-205			NOTE
	MIN	NOM	MAX	
A	1.30	1.40	1.70	
A1	0.25	0.40	0.45	
D		9.00 BSC		
E		9.00 BSC		
M		10 X 10		3
N		100		4
e		0.80 BSC		
b	.40	.45	.50	5
CENTER BALL MATRIX	N/A			

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

APPROVALS DATE
DRAWN JTJ 06/30/09
CHECKED

IDT™ 6024 Silver Creek Valley Road San Jose, CA 95138 PHONE: (408) 248-8333 FAX: (408) 248-8591 www.IDT.com

TITLE AB/ABG100 PACKAGE OUTLINE 9.0 X 9.0 mm BODY FPBGA

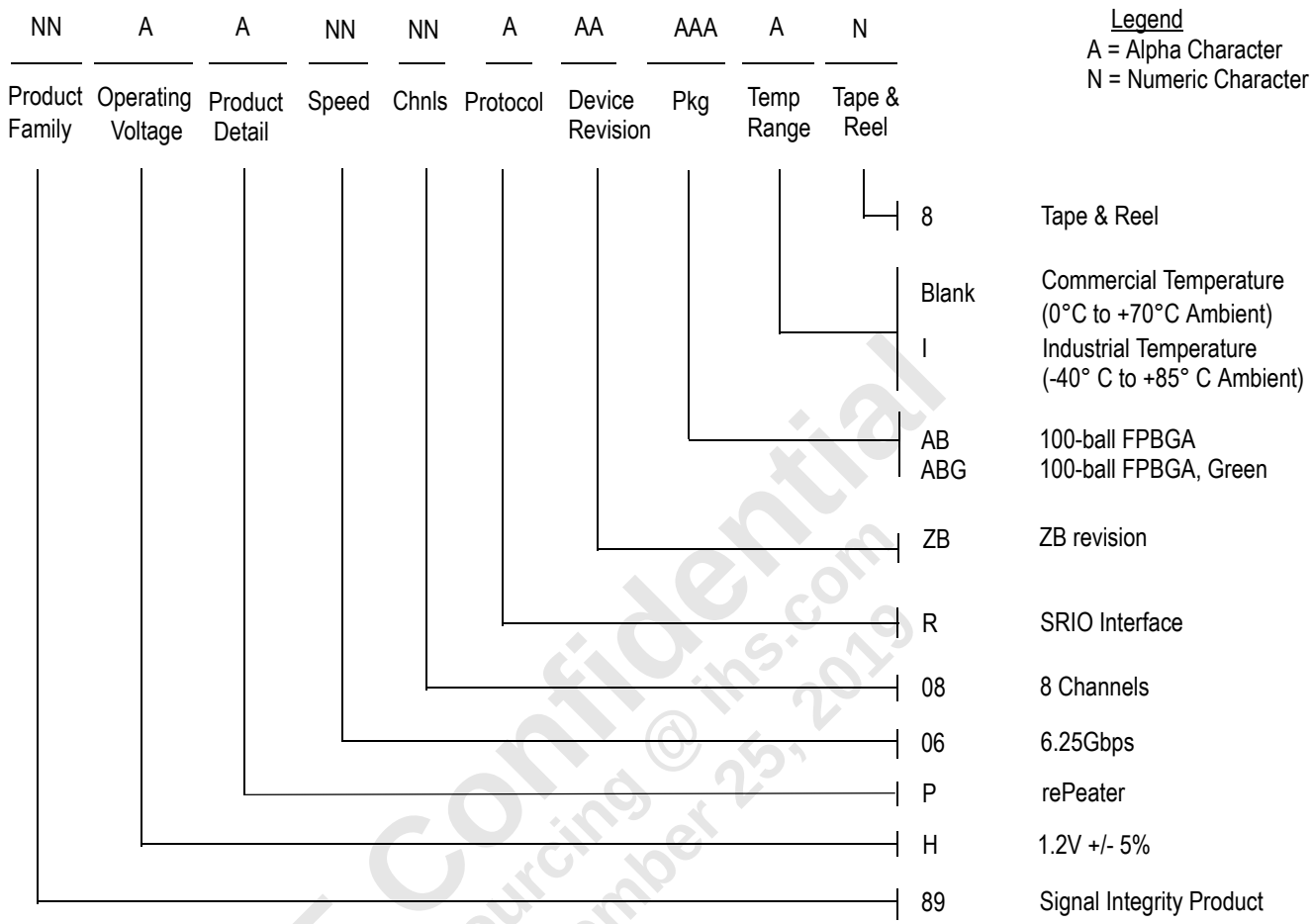
SIZE C DRAWING No. PSC-4282 REV 00

DO NOT SCALE DRAWING SHEET 2 OF 2

Revision History

October 1, 2014: Initial publication.

Ordering Information



Legend
A = Alpha Character
N = Numeric Character

Valid Combinations

89HP0608RZBAB / 89HP0608RZBAB8	100-ball FPBGA package, Commercial Temperature
89HP0608RZBABG / 89HP0608RZBABG8	100-ball Green FPBGA package, Commercial Temperature
89HP0608RZBABI / 89HP0608RZBABI8	100-ball FPBG package, Industrial Temperature
89HP0608RZBABGI / 89HP0608RZBABGI8	100-ball Green FPBG package, Industrial Temperature

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.IDT.com/go/support

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.