High and Low Side N-Channel Gate Driver

Product Datasheet

IDTP9090

Features

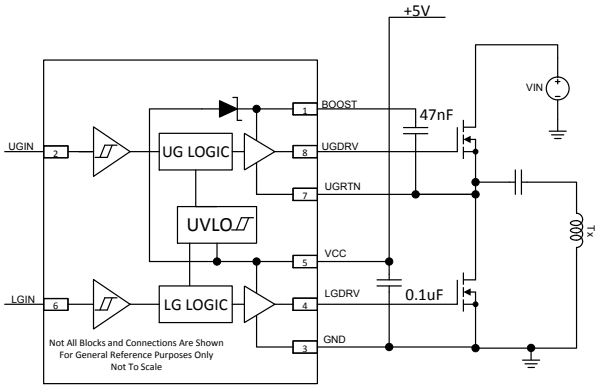
- Input Voltage Range: 4.5 to 5.5
- Output Voltage Range: Control Range 0-30V
- Peak MOSFET Drive current into 3nF
  - LGDRV Sink 3A
  - LGDRV Source 1A
  - UGDRV Sink 1A
  - UGDRV Source 0.8A
- Static Current (inputs at 0V) 175 µA
- No-load, 250kHz current 1.3mA
- On-chip boost Schottky diode
- Dual Independent Schmitt trigger inputs with ~2V hysteresis and 28 µA pull downs
- 3.4V UVLO with 0.4V of hysteresis for sequencing with controller
- 24ns nominal propagation delays

Description

The IDTP9090 is a high-performance dual-PWM-input MOSFET driver for wireless power and general-purpose applications. It is designed to interface directly with a power controller IC and provide a 5V gate drive to two separately-controlled power MOSFETs. The IDTP9090 contains one ground-referred MOSFET driver and one floating MOSFET driver capable of floating up to 30V.

The IDTP9090 is available in an 8-lead 3mm x 3mm QFN package.

Typical Application Circuit



Applications

- Wireless Power Gate Driver
- General Purpose MOSFET driver
- Custom ASIC Power Logic Buffer
- Motor Driver

Package: NLG8 – QFN-8 3x3-8 QFN

(See page 9)

Ordering Information

PART NUMBER	MARKING	PACKAGE	AMBIENT TEMP. RANGE	SHIPPING CARRIER	QUANTITY
P9090-0NLGI	P9090I	NLG8 - QFN-8 3x3x1mm	-40°C to +125°C	Tube	25
P9090-0NLGI8	P9090I	NLG8 - QFN-8 3x3x1mm	-40°C to +125°C	Tape and Reel	2,500

Absolute Maximum Ratings

These absolute maximum ratings are stress ratings only. Stresses greater than those listed below (Table 1 and Table 2) may cause permanent damage to the device. Functional operation of the IDTP9090 at maximum ratings is not implied. Continuous application of the absolute maximum rating conditions affects device reliability.

Table 1. Absolute Maximum Ratings. All voltages are referred to ground, unless otherwise noted.

PINS	RATING	UNITS
VCC, UGIN, LGDRV, LGIN,	-0.3 to 6	V
UGRTN	-0.3 to 30	V
BOOST, UGDRV	-0.3 to 35	V
BOOST to UGRTN	-0.3 to 6	V
UGDRV to UGRTN	-0.3 to 6	V

Table 2. Package Thermal Information

SYMBOL	DESCRIPTION	RATING	UNITS
θ_{JA}	Thermal Resistance Junction to Ambient (NLG8 - QFN)	119.6	°C/W
θ_{JC}	Thermal Resistance Junction to Case (NLG8 - QFN)	131.84	°C/W
θ_{JB}[2]	Thermal Resistance Junction to Board (NLG8 - QFN)	13.4	°C/W
T_J	Junction Temperature	-40 to +150	°C
T_A	Ambient Operating Temperature	-40 to +125	°C
T_{STG}	Storage Temperature	-55 to +150	°C
T_{LEAD}	Lead Temperature (soldering, 10s)	+300	°C

Note 1: The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 150°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

Note 2: This thermal rating was calculated on the JEDEC 51 standard 4-layer board with dimensions 3" x 4.5" in still air conditions.

Note 3: Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

Note 4: For the NTG8 package, connecting the 1.1 mm X 1.1 mm EP to internal/external ground planes with a 2x2 matrix of PCB plated-through-hole (PTH) vias, from top to bottom sides of the PCB, is recommended for improving the overall thermal performance.

Table 3. ESD Information

TEST MODEL	PINS	RATINGS	UNITS
HBM	All	±1500	V
CDM	All	±500	V

Electrical Specifications

V_{CC} = 5V, T_A = -40°C to +125°C, typical values are at T_A =+25°C, unless otherwise noted. All voltages are referred to ground, unless otherwise noted.

Table 4. Device Characteristics

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
BIAS						
V_{CC}	VCC Input Voltage Range		4.5	-	5.5	V
$UGDRV_{MCM}$	UGDRV Max Common Mode		-	-	35	V
IQ_{DC}	Operating Supply Current, Not Switching		-	150	200	µA
IQ_{SW}	Operating Supply Current, Switching	UGDRV & LGDRV = Open, F_S = 250 kHz	-	300	500	µA
UVLO						
VCC_{THR}	VCC Rising		3.2	3.4	3.7	V
VCC_{HYST}	VCC Hysteresis		-	400	-	mV
UGIN and LGIN Inputs						
IN_{ISINK}	Input Current	UGIN = LGIN = V_{CC}	15	28	50	µA
V_{FLP}	Pull Down Voltage	UGIN = LGIN = Open	-	50	100	mV
$VUGIN_{ON}$	Input Threshold UGDRV Rising		-	3.5	3.8	V
$VUGIN_{OFF}$	Input Threshold UGDRV Falling		1	1.3	-	V
$VUGIN_{HYST}$	Input Hysteresis UGDRV	$VUGIN_{ON}$ - $VUGIN_{OFF}$	-	2.4	-	V
$VLGIN_{ON}$	Input Threshold LGDRV Rising		-	2.8	3.3	V
$VLGIN_{OFF}$	Input Threshold LGDRV Falling		1	1.2	-	V
$VLGIN_{HYST}$	Input Hysteresis LGDRV	$VLGIN_{ON}$ - $VLGIN_{OFF}$	-	1.6	-	V
UGDRV						
$UGDRV_{RSRC}$	Source Impedance	Source = 100 mA	-	1.4	2	Ω
$UGDRV_{RSINK}$	Sink Impedance	Sink = 100 mA	-	1.3	1.8	Ω
$UGDRV_{TR}$	Rise Time	1.0 nF Load 10 % to 90 %	-	6	-	ns
$UGDRV_{TF}$	Fall Time	1.0 nF Load 90 % to 10 %	-	5	-	ns
LGDRV						
$LGDRV_{RSRC}$	Source Impedance	Source = 100 mA	-	1.2	1.9	Ω
$LGDRV_{RSINK}$	Sink Impedance	Sink = 100 mA	-	0.6	1.1	Ω
$LGDRV_{TR}$	Rise Time	3.0 nF Load 10 % to 90 %	-	10	-	ns
$LGDRV_{TF}$	Fall Time	3.0 nF Load 90 % to 10 %	-	8	-	ns
Propagation Delays						
$UGDLY_{ON}$	UGIN Rising to UGDRV Rising	3.0 nF load LGIN = 50 % to LGDRV at 90 %, Vin = 5 V	-	24	-	ns
$UGDLY_{OFF}$	UGIN Falling to UGDRV Falling	3.0 nF load LGIN = 50 % to LGDRV at 10 %, Vin = 5 V	-	24	-	ns
$LGDLY_{ON}$	LGIN Rising to LGDRV Rising	3.0 nF load LGIN = 50 % to LGDRV at 90 %	-	10	-	ns
$LGDLY_{OFF}$	LGIN Falling to LGDRV Falling	3.0 nF load LGIN = 50 % to LGDRV at 10 %	-	10	-	ns
Boost Diode						
BD_{FV}	Forward Voltage	I = 10 mA	-	600	800	mV
BD_{RL}	Reverse Leakage	V_{BOOST} =5V, V_{CC}=0	-	0.1	-	µA

Pin Configuration

IDTP9090 is packaged in an 8-lead 3mm x 3mm QFN package.

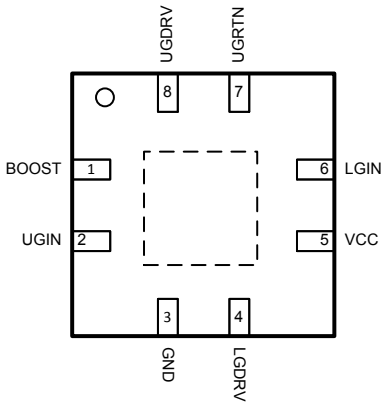


Figure 1. IDTP9090 Pin Configuration

Pin Descriptions

Table 5. IDTP9090 Package Pin Functions by Pin Number

PIN #	PIN	DESCRIPTION
1	BOOST	BOOST pin for Upper Gate N Chanel Drive. An internal Schottky diode is connected between this pin and VCC. A minimum 16V X7R ceramic capacitor must be connected from the BOOST pin to the UGRTN pin
2	UGIN	Control input signal for the UGDRV output. The pin has a 28µA pull-down.
3	GND	Digital & signal ground, as well as the Power Ground for LG driver.
4	LGDRV	Lower-side MOSFET gate driver output controlled by the LGDRV pin (no logic inversion).
5	VCC	Power for the LGDRV and BOOST pins, and for the bias current for the IDTP9090.
6	LGIN	Control input signal for the LGDRV output. The pin has a 28µA pull-down.
7	UGRTN	Return for UGDRV drive. Connect this pin to the source of the high-side FET/drain of the low-side FET.
8	UGDRV	Upper-side MOSFET gate driver output controlled by the UGDRV pin (no logic inversion).
	EP	Exposed pad, must be connected to ground. Do not use as the IC ground connection.

Block Diagram

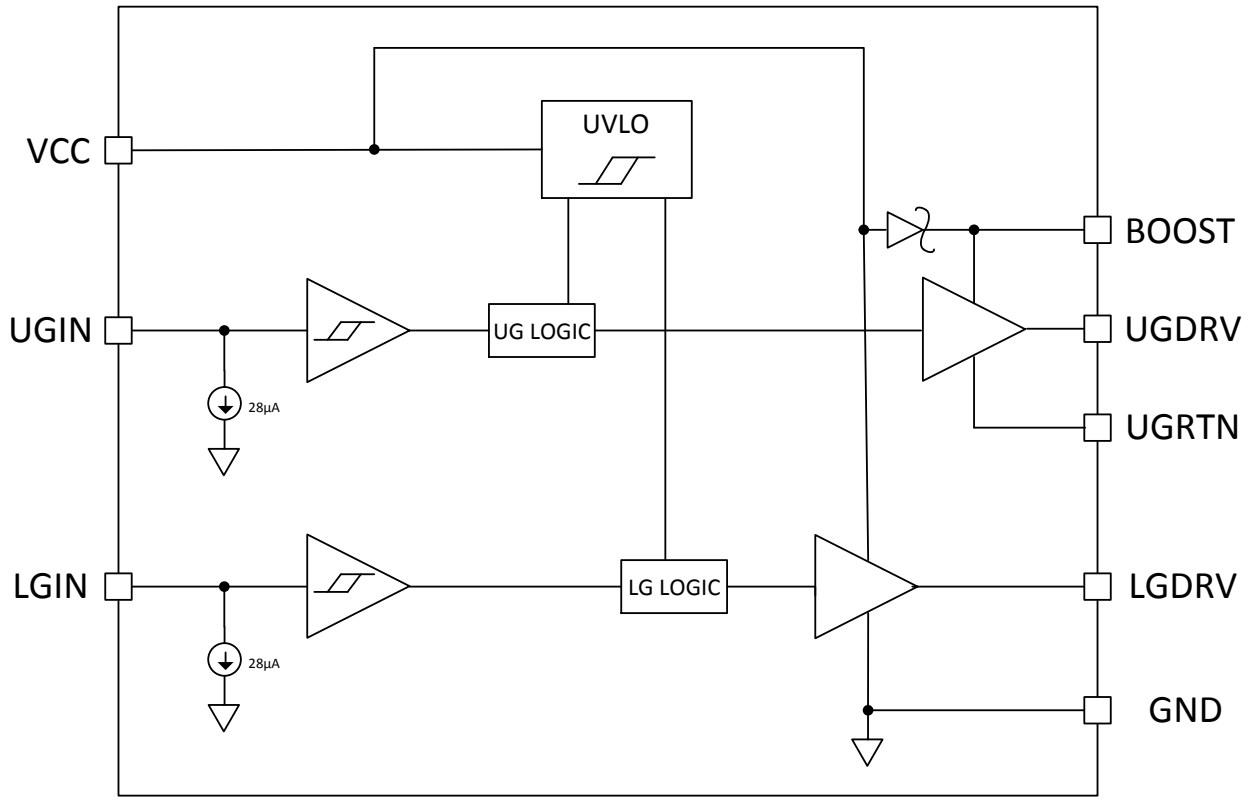


Figure 2. IDTP9090 Functional Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 3. Quiescent Current vs Vin

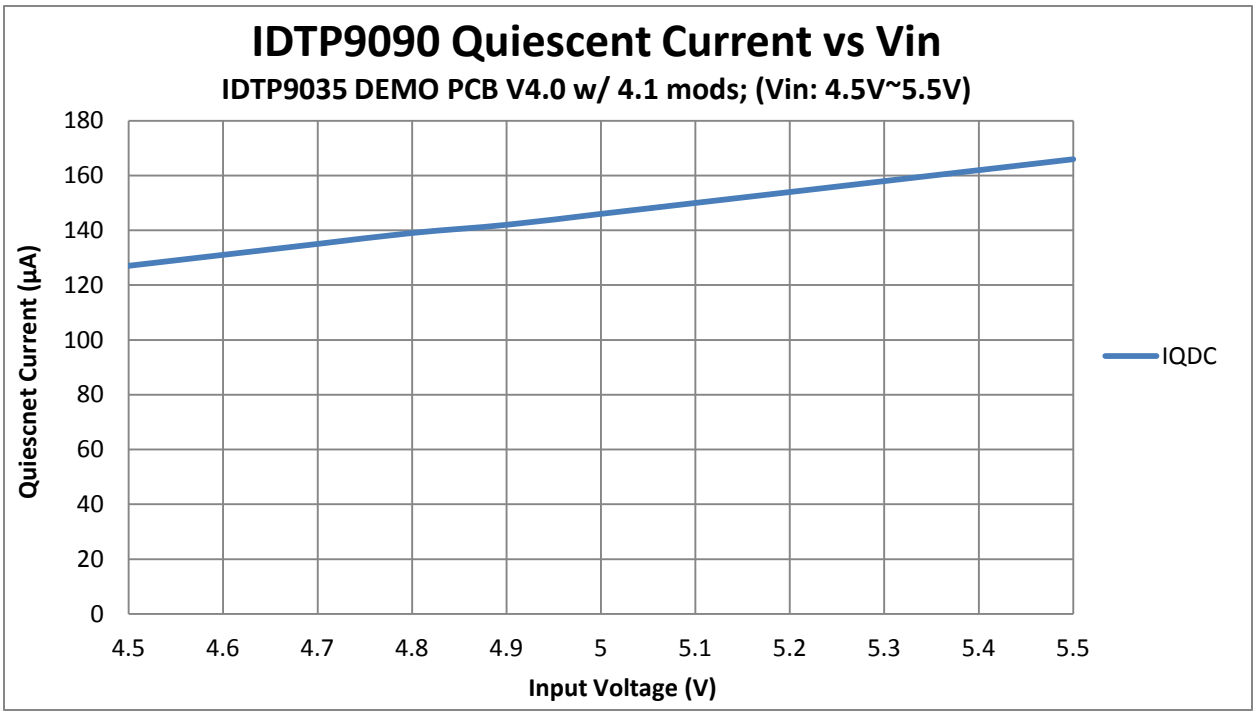


Figure 4. Quiescent Current vs Frequency

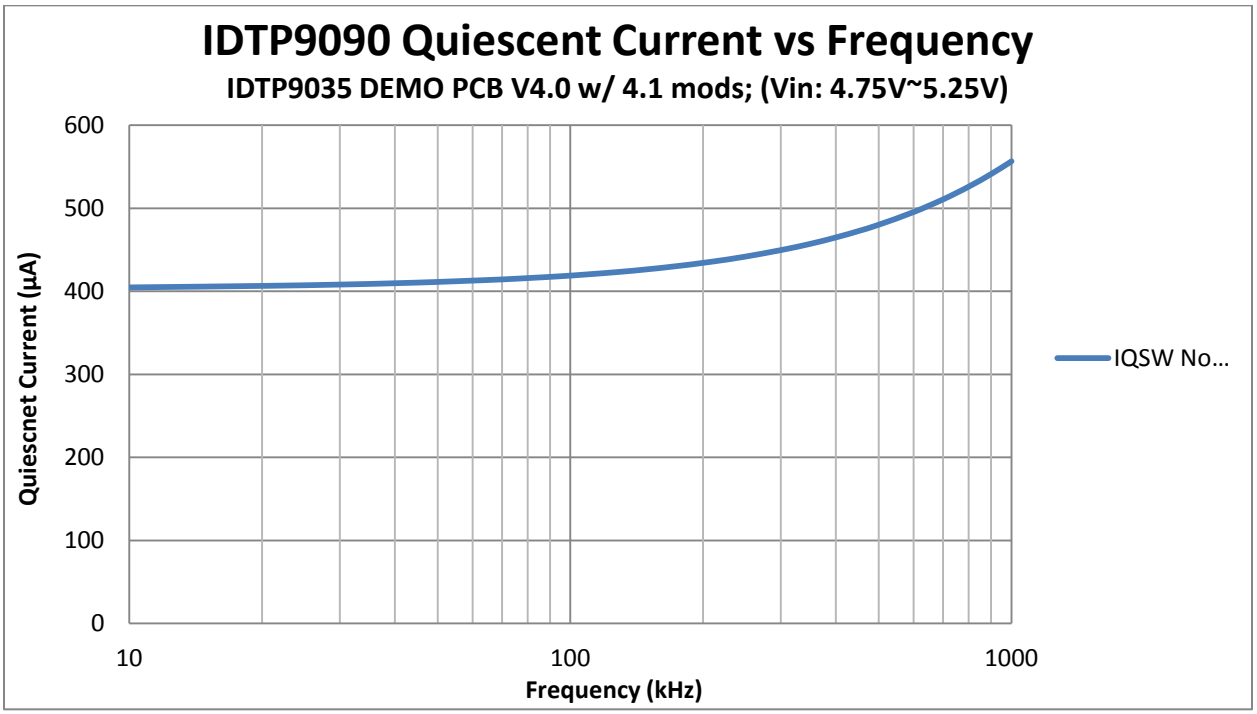
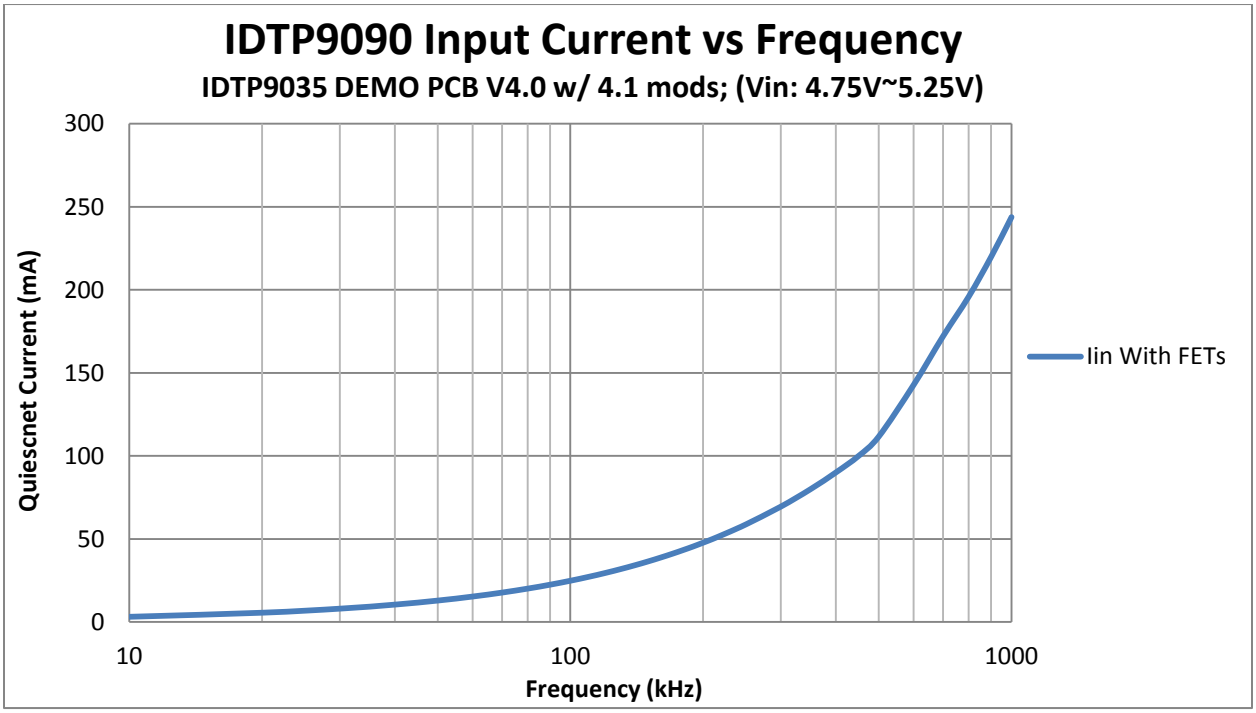


Figure 5. Input Current vs Frequency



Application Schematics

Half-Bridge Wireless Power Inverter Driver

The following diagram shows an IDTP9090 being used to drive a Wireless Power Solution Transmitter Coil.

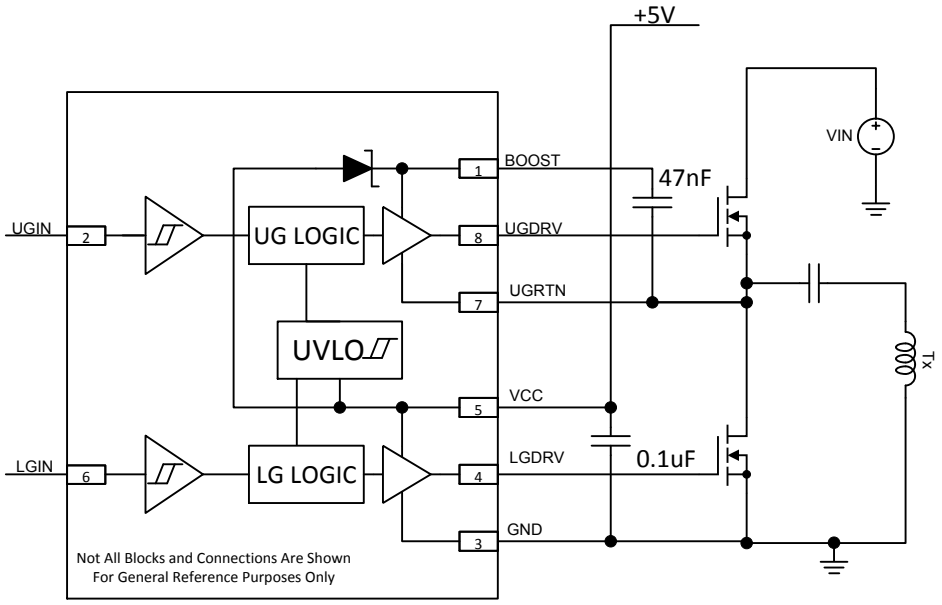


Figure 6. Application Diagram – Half Bridge Wireless Power Driver

Full Bridge Wireless Power Inverter Driver

The following diagram shows two IDTP9090s driving a Wireless Power Solution Transmitter Coil.

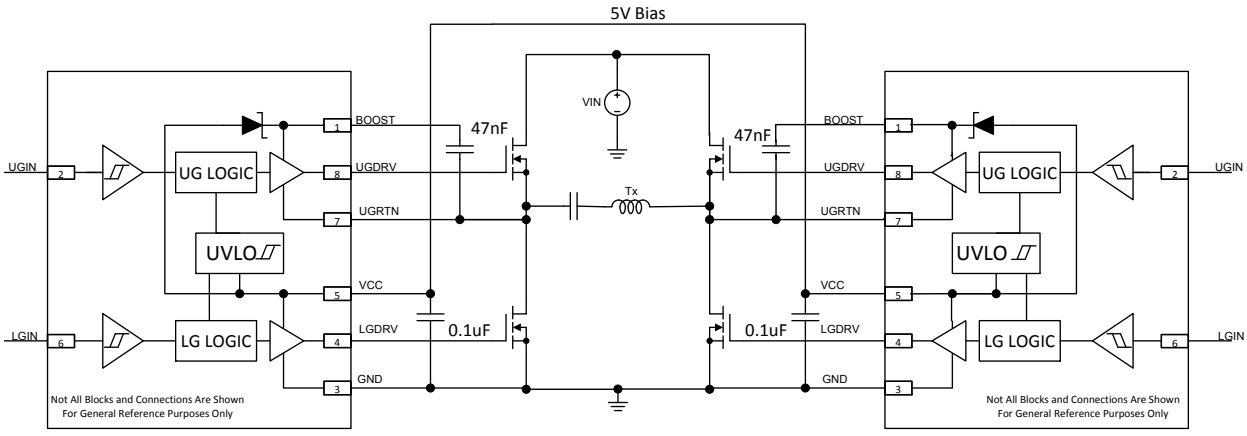


Figure 7. Application Diagram – Full Bridge Wireless Power Driver

Functional Description

The IDTP9090 is a high-performance dual-PWM-input MOSFET driver for wireless power and general purpose applications. It is designed to interface directly with a power controller IC and provide a 5V gate drive to two separately-controlled N-channel power MOSFETs. The IDTP9090 contains one ground-referred MOSFET driver and one floating MOSFET driver capable of floating up to 30V.

Active Input Pull Down

Each drive signal input has a Schmitt trigger and a 28µA (nominal) pull down. This prevents a high impedance input from causing an indeterminate state on the output DRV signals.

VCC UVLO

The IDTP9090 will be kept disabled until the voltage on the VCC pin exceeds VCC_{THR}, as specified in Table 4.

Independent UGIN and LGIN signals

The IDTP9090 utilizes two independent non-inverting gate drive signal paths for controlling the respective output drive pins. This provides the customer maximum flexibility in choosing a control architecture.

30V Floating Drive with Integral Boost Diode

The IDTP9090 UGDRV provides a 5V signal referred to UGRTN for driving a high efficiency N-Channel MOSFET with up to 30V on the UGRTN pin. An internal Boost Diode is connected between the VCC pin and the BOOST pin to recharge the boost capacitor when the UGDRV pin is at or near 0V.

Package Outline Drawing

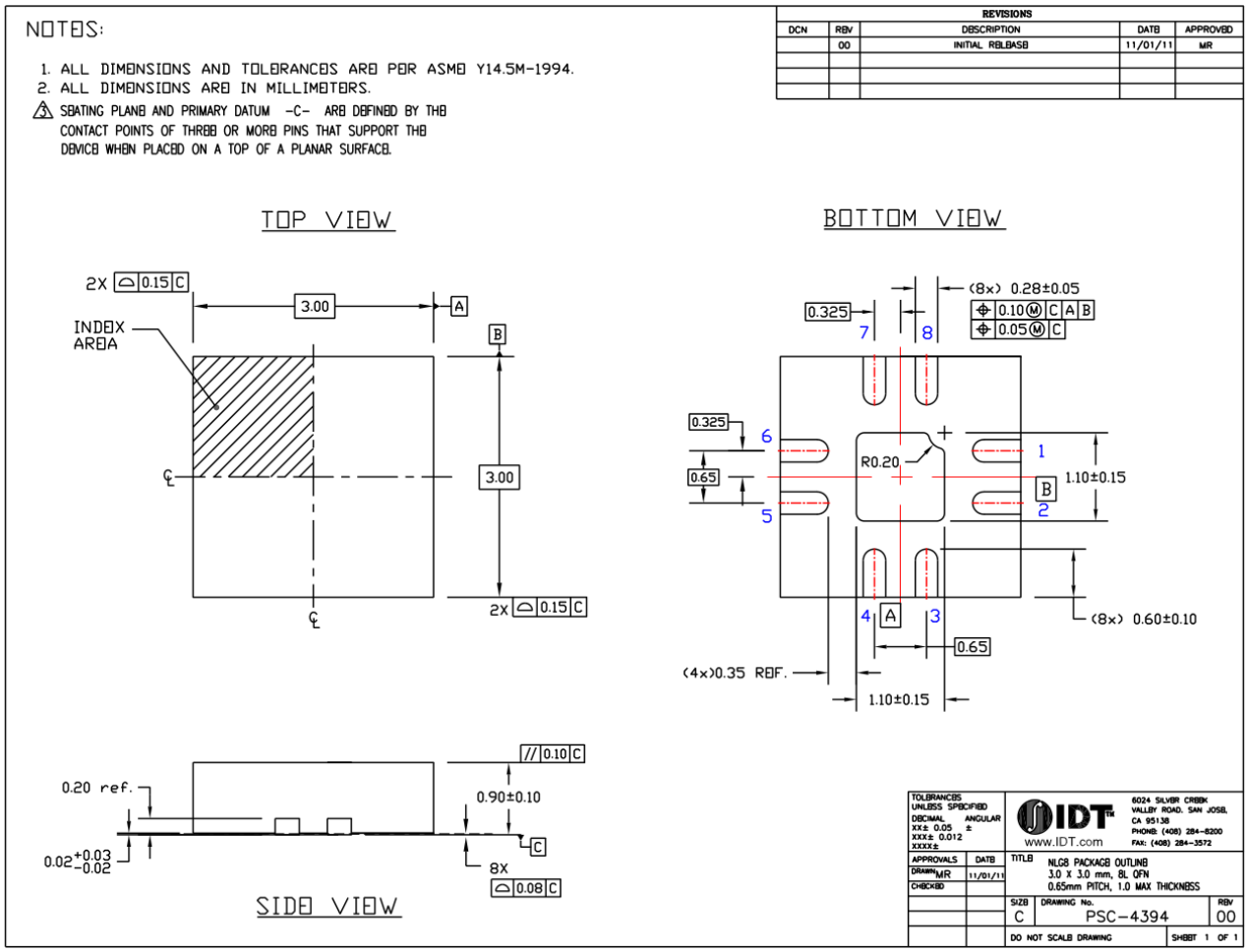


Figure 8. Package Outline Drawing (NLG8 QFN-8 3.0mmx3.0mmx1mm 8-ld, 0.65mm pitch)

Ordering Information

PART NUMBER	MARKING	PACKAGE	AMBIENT TEMP. RANGE	SHIPPING CARRIER	QUANTITY
P9090-0NLGI	P9090I	NLG8 - QFN-8 3x3x1mm	-40°C to +125°C	Tube	25
P9090-0NLGI8	P9090I	NLG8 - QFN-8 3x3x1mm	-40°C to +125°C	Tape and Reel	2,500

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