

### Description

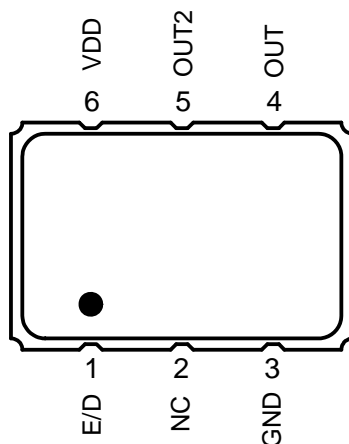
The XLL is an LVDS crystal oscillator with 0.89ps typical phase jitter over 12kHz to 20MHz bandwidth. Available in a wide frequency range from 0.750MHz to 1350MHz, the IDT XLL series crystal oscillator utilizes a family of proprietary ASICs, with a key focus on noise reduction technologies.

The 3rd order Delta Sigma Modulator reduces noise to the levels that are comparable to traditional bulk Quartz and SAW oscillators. With short lead-time, low cost, low noise, wide frequency range, excellent ambient performance, the XLL is an excellent choice over the conventional technologies. The XLL has stabilities as tight as  $\pm 20$ ppm with extremely quick delivery for both standard and custom frequencies

### Features

- Frequency range: 0.750MHz to 1350MHz
- Output type: LVDS
- Frequency stability:  $\pm 20$ ppm,  $\pm 25$ ppm,  $\pm 50$ ppm, or  $\pm 100$ ppm
- Supply voltage: 2.5V or 3.3V
- Phase jitter (1.875MHz to 20MHz): 225fs typical
- Phase jitter (12kHz to 20MHz): 0.89ps typical
- Package options: 3.2mm x 2.5mm x 1.0mm (JX6)  
5.0mm x 3.2mm x 1.2mm (JS6)  
7.0mm x 5.0mm x 1.3mm (JU6)
- Operating temperatures: -20°C to +70°C or -40°C to +85°C

### Pin Assignment



**6-pin CLCC**

### Pin Descriptions

Pin Number	Pin Name	Description
1	E/D	Enable/Disable <sup>1</sup> (0=Output Disabled)
2	NC	No connect
3	GND	Connect to ground
4	OUT	Output
5	OUT2	Complementary Output
6	VDD	Supply voltage

1. Pulled high internally.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the XLL. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
VDD	-0.5 to +5.0V
E/D	-0.5V to VDD + 0.5V
OUT	-0.5V to VDD + 0.5V
Storage Temperature	-55°C to 125°C
Theta Ja (Junction to Ambient)	102°C/W – Still Air

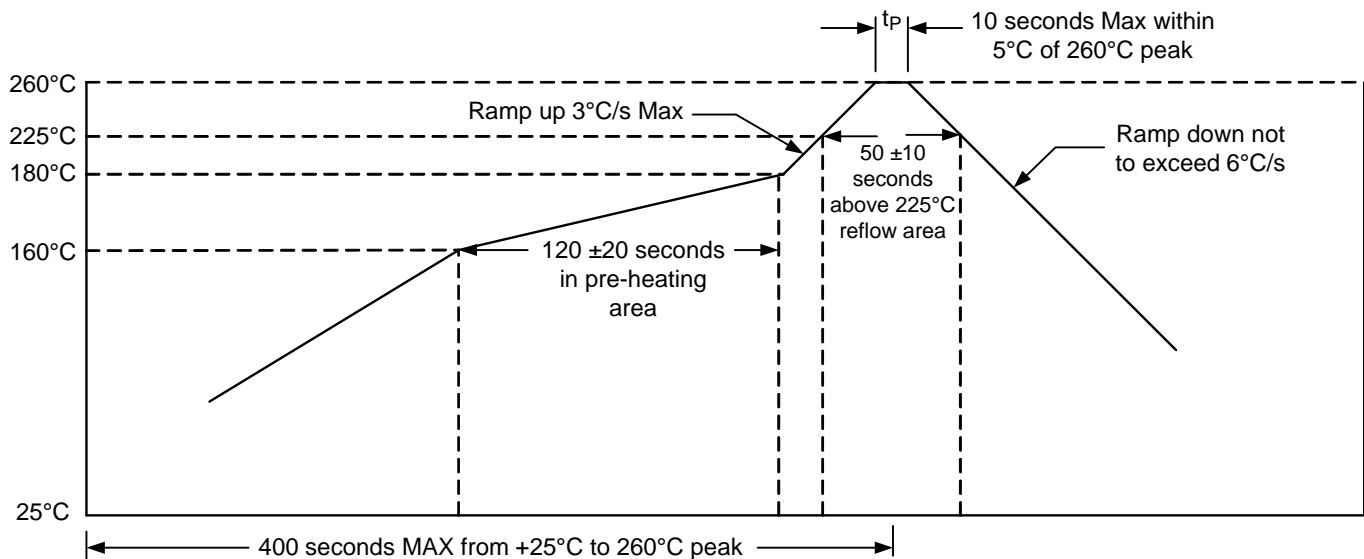
## ESD Compliance

Human Body Model (HBM)	1000V
Machine Model (MM)	150V

## Mechanical Testing

Parameter	Test Method
Mechanical Shock	Drop from 75cm to hardwood surface–3 times
Mechanical Vibration	10–55Hz, 1.5mm amplitude, 1 minute sweep 2 hours each in 3 directions (X, Y, Z)
High Temperature Burn-in	Under power at 125°C for 2000 hours
Hermetic Seal	He pressure: 4 ±1kgf/cm <sup>2</sup> 2 hour soak

## Solder Reflow Profile



## DC Characteristics

( $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ$  to  $+85^\circ C$ )

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply Current	$I_{DD}$	Common Frequencies			100	mA
Differential Output Voltage	$V_{OD}$	Standard LVDS load		0.6		V
Output Offset Voltage	$V_{OS}$	Standard LVDS load		1.3		V
Enable/Disable Input HIGH Voltage (Output enabled)*	$V_{IH}$		$70\%V_{DD}$			V
Enable/Disable Input LOW Voltage (Output disabled)	$V_{IL}$				$30\%V_{DD}$	V

\* A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

## AC Characteristics

( $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ$  to  $+85^\circ C$ )

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Frequency Range	$F_{OUTR}$		0.750		1350	MHz
Frequency Stability		Temperature = $-20^\circ C$ to $+70^\circ C$	$\pm 20$		$\pm 100$	ppm
		Temperature = $-40^\circ C$ to $+85^\circ C$	$\pm 25$		$\pm 100$	ppm
Aging (1 <sup>st</sup> year)		$T_a = 25^\circ C$			3	
Aging (10 years)		$T_a = 25^\circ C$			10	
Output Load		Differential		100		Ohms
Start-up Time	$T_{ST}$	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% $V_{PP}$			400	ps
Output Fall Time		80% to 20% $V_{PP}$			400	ps
Output Clock Duty Cycle	$T_{DTCY}$	50% $V_{P-P}$	45		55	%
Output Enable/ Disable Time	$T_{OE}$				100	ns
Period Jitter, RMS	$J_{PER}$	Frequency = 156.25MHz		3.0		ps
Random Jitter	$R_J$	Frequency = 156.25MHz		1.3		ps
Deterministic Jitter	$D_J$	Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		5.8		ps
Total Jitter	$T_J$			23.6		ps
Phase Jitter (12kHz – 20MHz)	$\phi_{JITTER}$	Common Frequencies		0.89		ps
Phase Noise Performance Frequency = 156.25MHz	$\phi_{NOISE}$	100Hz of Carrier		-80		dBc/Hz
		1kHz of Carrier		-115		dBc/Hz
		10kHz of Carrier		-118		dBc/Hz
		100kHz of Carrier		-124		dBc/Hz
		1MHz of Carrier		-142		dBc/Hz
		10MHz of Carrier		-151		dBc/Hz
Output Frequency (Common)	$F_{OUT}$	100MHz, 106.25MHz, 1258MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212.5MHz, 250MHz, 300MHz, 312.5MHz, 400MHz (Contact IDT for additional frequencies)				

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at 25°C. We do not recommend hand soldering the devices

## DC Characteristics

( $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ$  to  $+85^\circ C$ )

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply Current	$I_{DD}$	Common Frequencies	26		65	mA
Differential Output Voltage	$V_{OD}$	Standard LVDS load		0.4		V
Output Offset Voltage	$V_{OS}$	Standard LVDS load		1.25		V
Enable/Disable Input HIGH Voltage (Output enabled)*	$V_{IH}$		$70\%V_{DD}$			V
Enable/Disable Input LOW Voltage (Output disabled)	$V_{IL}$				$30\%V_{DD}$	V

\* A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

## AC Characteristics

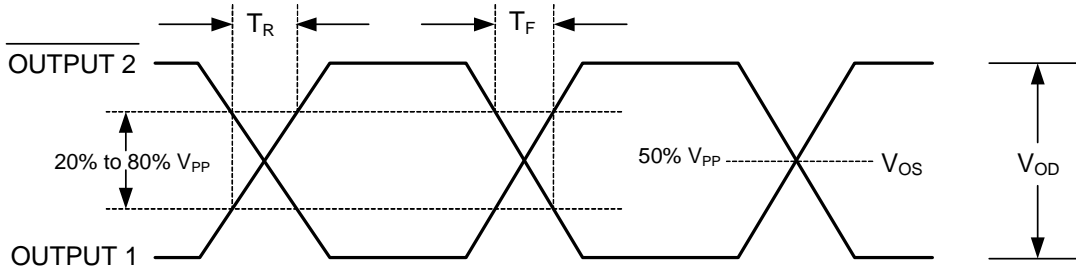
( $V_{DD} = 2.5 \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ$  to  $+85^\circ C$ )

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Frequency Range	$F_{OUTR}$		0.750		1000	MHz
Frequency Stability		Temperature = $-20^\circ C$ to $+70^\circ C$	$\pm 20$		$\pm 100$	ppm
		Temperature = $-40^\circ C$ to $+85^\circ C$	$\pm 25$		$\pm 100$	ppm
Output Load		Differential		100		Ohms
Start-up Time	$T_{ST}$	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% $V_{PP}$			400	ps
Output Fall Time		80% to 20% $V_{PP}$			400	ps
Output Clock Duty Cycle	$T_{DTCY}$	50% $V_{P-P}$	45		55	%
Output Enable/ Disable Time	$T_{OE}$				100	ns
Period Jitter, RMS	$J_{PER}$	Frequency = 156.25MHz		4.0		ps
Random Jitter	$R_J$	Frequency = 156.25MHz		1.4		ps
Deterministic Jitter	$D_J$	Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		9.2		ps
Total Jitter	$T_J$			29.2		ps
Phase Jitter (12kHz – 20MHz)	$\phi_{JITTER}$	Frequency = 156.25MHz		1.04		ps
Phase Noise Performance Frequency = 156.25MHz	$\phi_{NOISE}$	100Hz of Carrier		-83		dBc/Hz
		1kHz of Carrier		-105		dBc/Hz
		10kHz of Carrier		-113		dBc/Hz
		100kHz of Carrier		-119		dBc/Hz
		1MHz of Carrier		-137		dBc/Hz
		10MHz of Carrier		-146		dBc/Hz
Output Frequency (Standards)	$F_{OUT}$	100MHz, 106.25MHz, 125.8MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212.5MHz, 250MHz, 300MHz, 312.5MHz, 400MHz (Contact IDT for additional frequencies)				

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at 25°C. We do not recommend hand soldering the devices

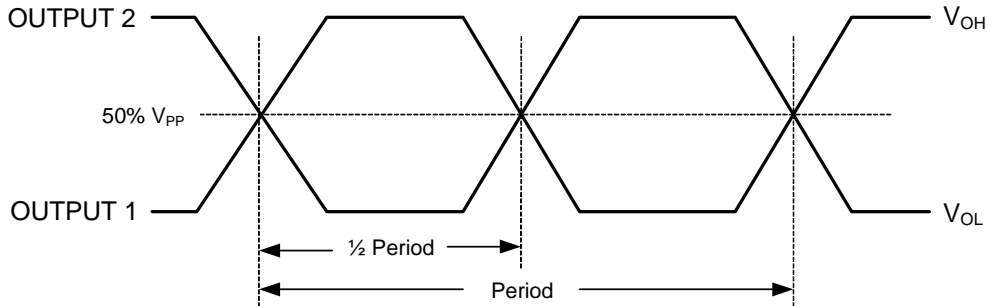
# Output Waveform

Output Levels/Rise Time/Fall Time Measurements

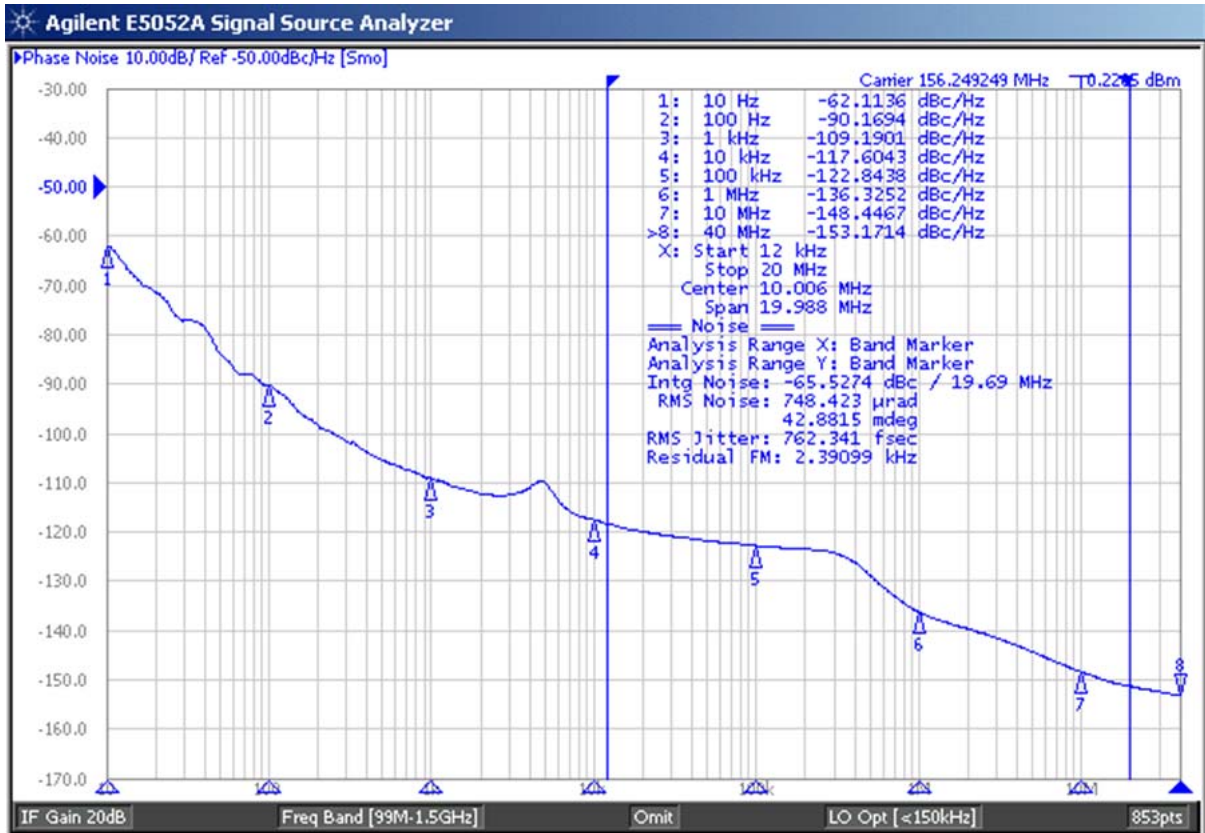


Oscillator Symmetry

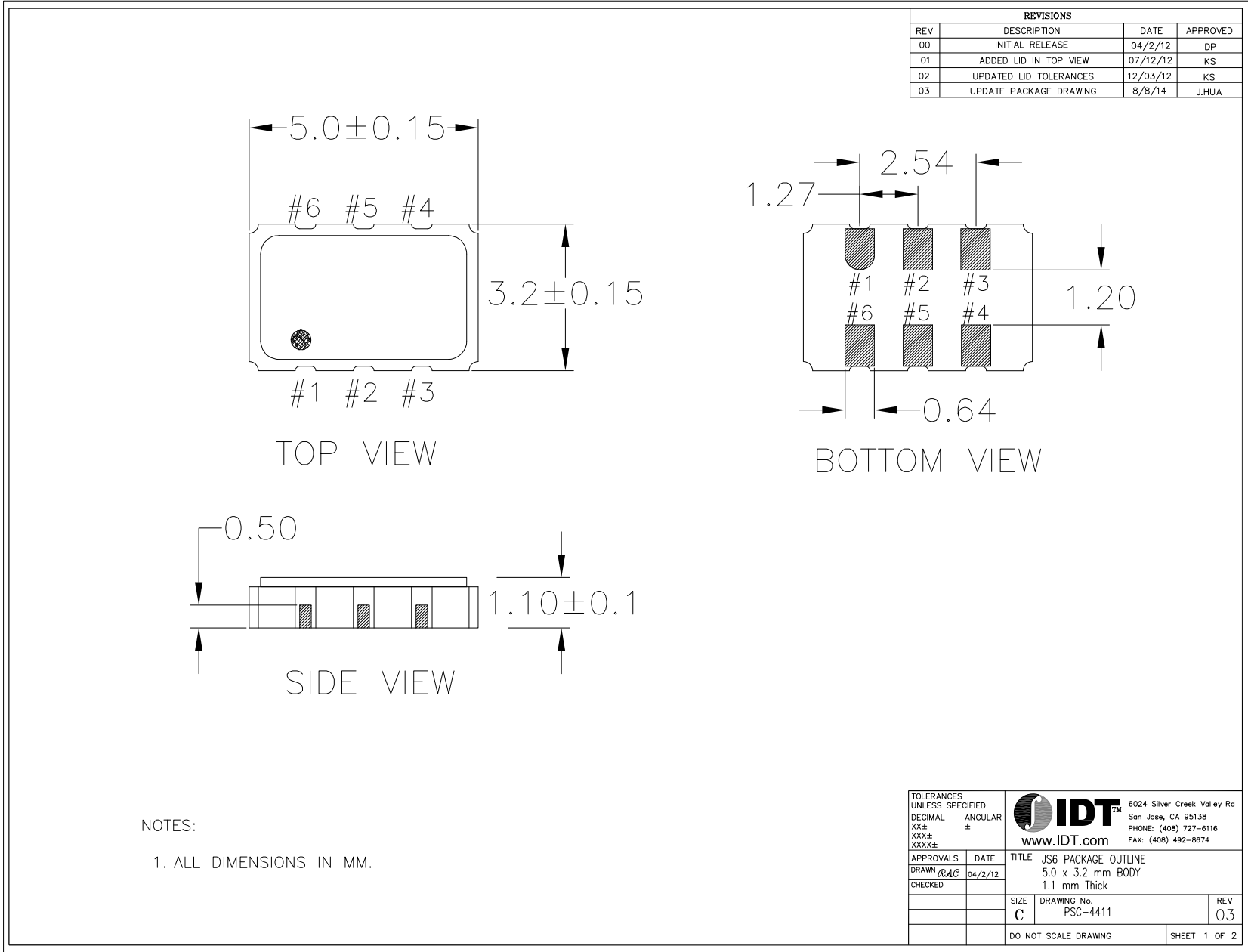
Ideally, Symmetry should be 50/50 for  $\frac{1}{2}$  period –Other expressions are 45/55 or 55/45



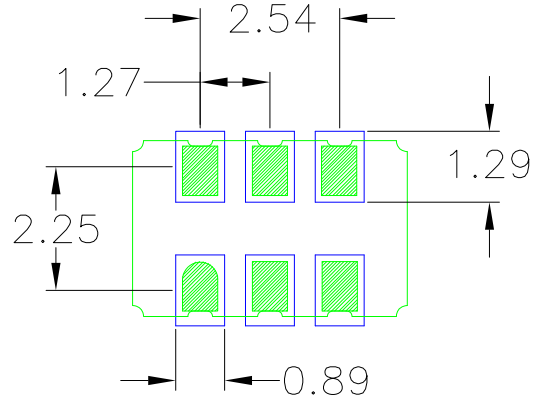
# Typical Phase Noise (3.3V)



# JS6 Package Outline and Dimensions



# JS6 Package Outline and Dimensions (cont.)



RECOMMENDED LAND PATTERN

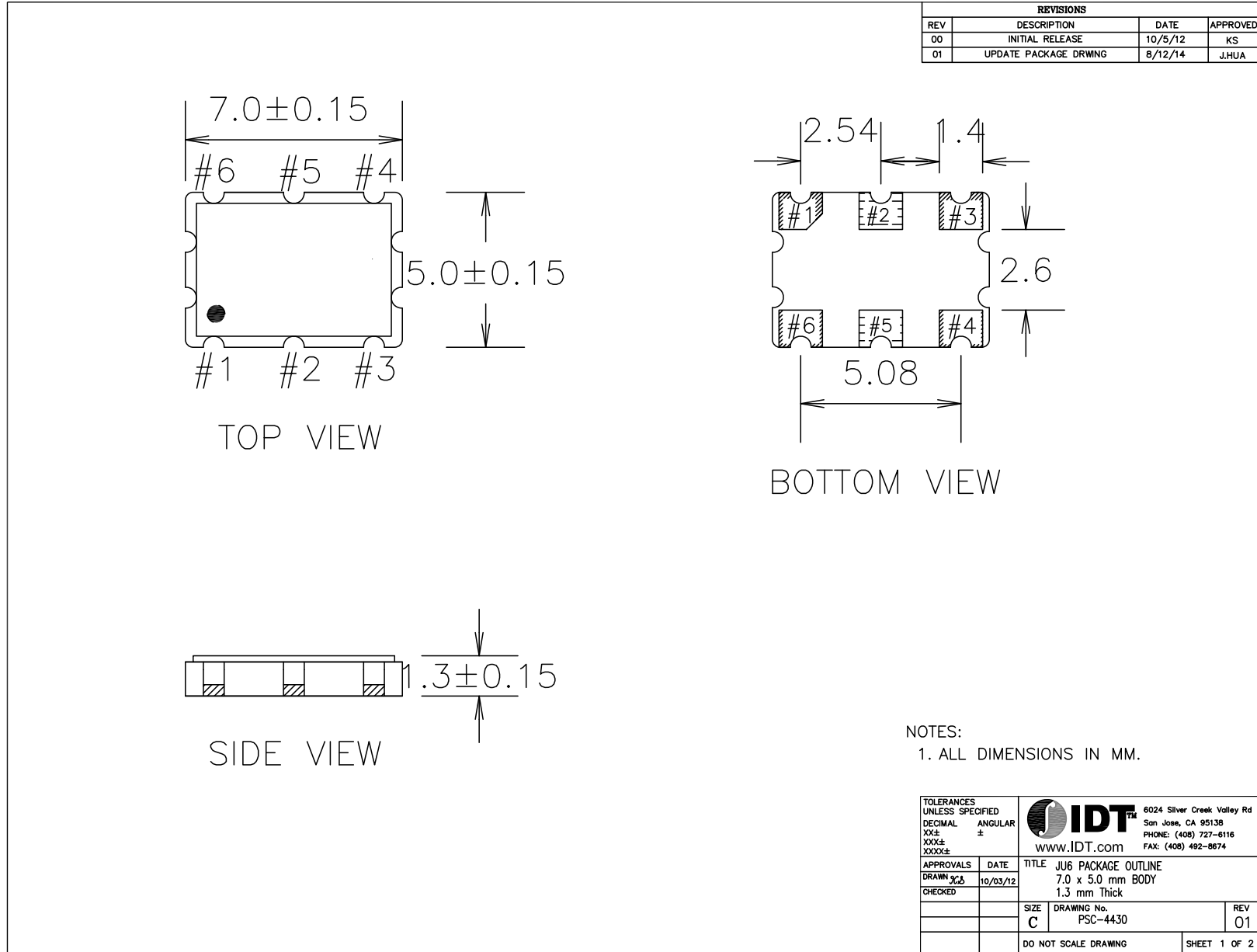
NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	04/2/12	DP
01	ADDED LID IN TOP VIEW	07/12/12	KS
02	UPDATED LID TOLERANCES	12/03/12	KS
03	UPDATE PACKAGE DRAWING	8/8/14	J.HUA

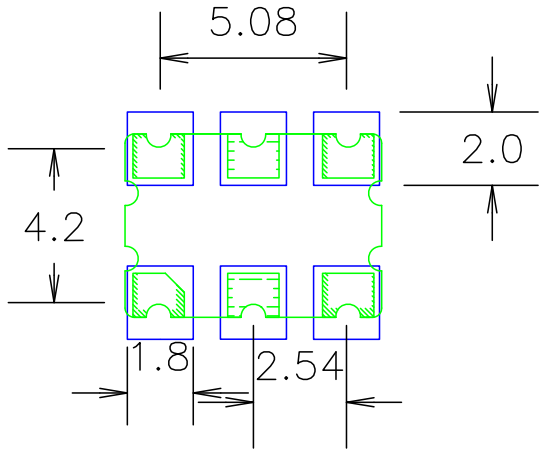
TOLERANCES UNLESS SPECIFIED		6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674 www.IDT.com
DECIMAL	ANGULAR	
XX±	±	
XXX±		
XXXX±		
APPROVALS	DATE	TITLE
DRAWN <i>gac</i>	04/2/12	JS6 PACKAGE OUTLINE 5.0 x 3.2 mm BODY 1.1 mm Thick
CHECKED		
SIZE	DRAWING No.	REV
C	PSC-4411	03
DO NOT SCALE DRAWING		SHEET 2 OF 2

# JU6 Package Outline and Dimensions





# JU6 Package Outline and Dimensions (cont.)



RECOMMENDED LAND PATTERN

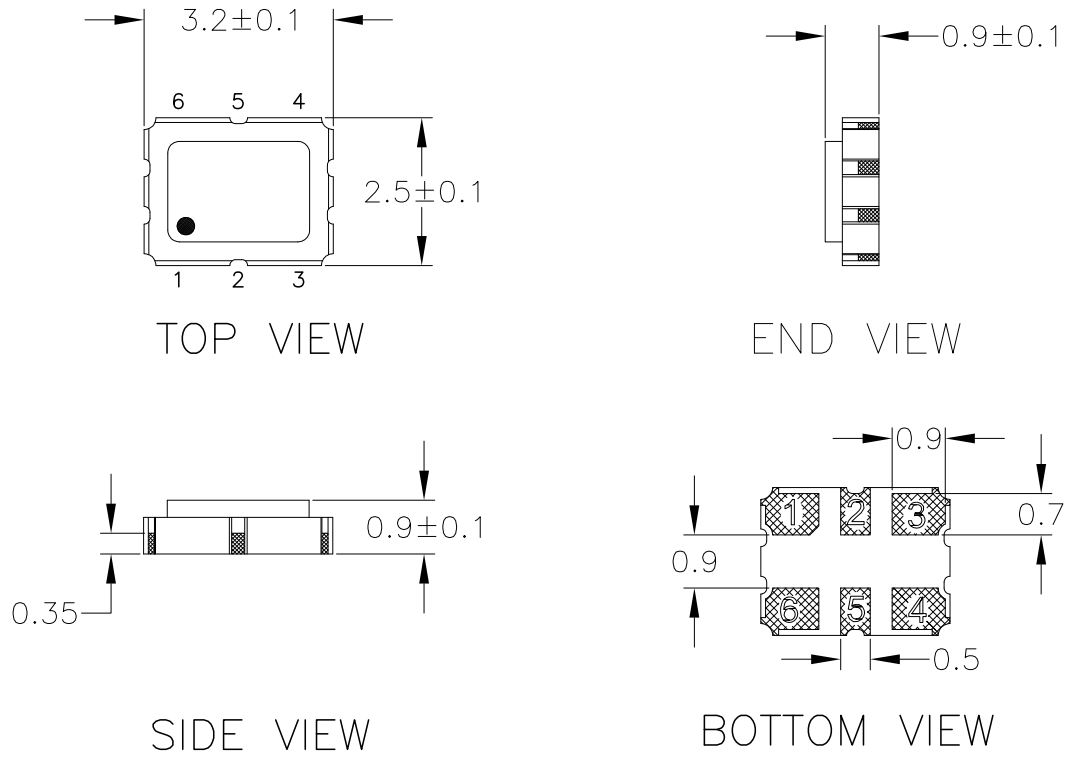
NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/5/12	KS
01	UPDATE PACKAGE DRWING	8/12/14	J.HUA

TOLERANCES UNLESS SPECIFIED		6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-8118 FAX: (408) 482-8874 www.IDT.com
DECIMAL	ANGULAR	
XX±	±	
XXX±		
APPROVALS	DATE	TITLE
DRAWN <i>JCB</i>	10/03/12	JU6 PACKAGE OUTLINE
CHECKED		7.0 x 5.0 mm BODY
		1.3 mm Thick
SIZE	DRAWING No.	REV
C	PSC-4430	01
DO NOT SCALE DRAWING		SHEET 2 OF 2

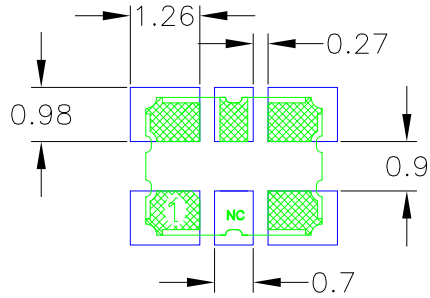
# JX6 Package Outline and Dimensions



NOTES:  
1. ALL DIMENSIONS IN MM.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	8/11/14	J.HUA

TOLERANCES UNLESS SPECIFIED		6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-8116 FAX: (408) 492-8674 <a href="http://www.IDT.com">www.IDT.com</a>
DECIMAL	ANGULAR	
XXX±	±	
XXXX±		
APPROVALS	DATE	TITLE
DRAWN <i>BAC</i>	8/11/14	JX6 PACKAGE OUTLINE
CHECKED		3.2 x 2.5 mm BODY
		0.9 mm Thick
SIZE	DRAWING No.	REV
C	PSC-4412	00
DO NOT SCALE DRAWING		SHEET 1 OF 2



1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.

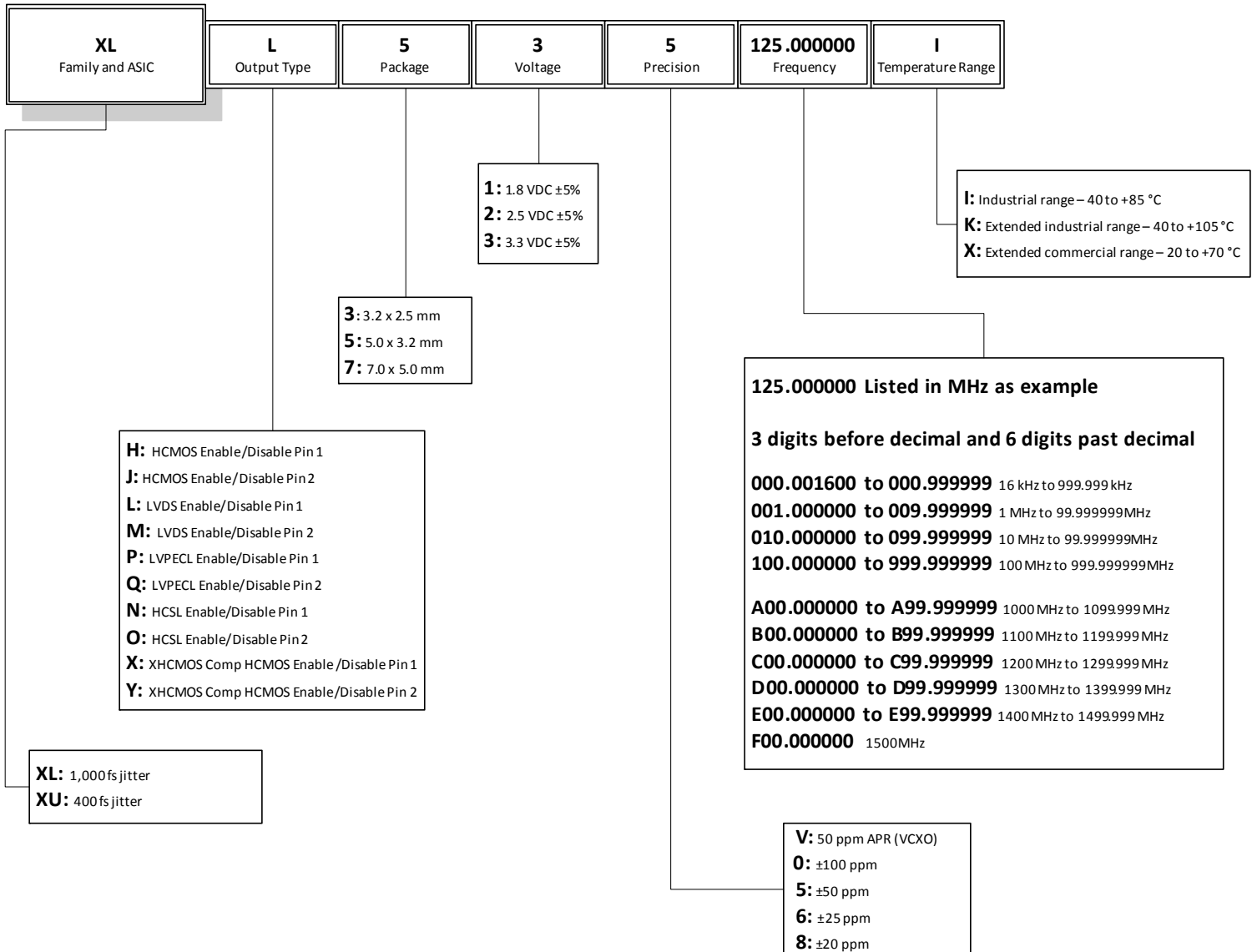
NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	8/11/14	J.HUA

TOLERANCES UNLESS SPECIFIED		6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 www.IDT.com FAX: (408) 492-8674
DECIMAL	ANGULAR	
XX±	±	
XXX±		
XXXX±		
APPROVALS	DATE	TITLE
DRAWN <i>RAC</i>	8/11/14	JX6 PACKAGE OUTLINE 3.2 x 2.5 mm BODY 0.9 mm Thick
CHECKED		
SIZE	DRAWING No.	REV
C	PSC-4412	00
DO NOT SCALE DRAWING		SHEET 2 OF 2

# IDT Ordering Information



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## Revision History

Date	Originator	Description of Change
10/28/16	P. Jenkins	Update ordering information decoder tables by separating them into Scheme 1 and Scheme 2; add note to distinguish the two tables.
06/13/17	L.S.	Removed "Ordering Information Scheme #1 (for reference only)". Replaced with a single ordering information table.



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