General Description

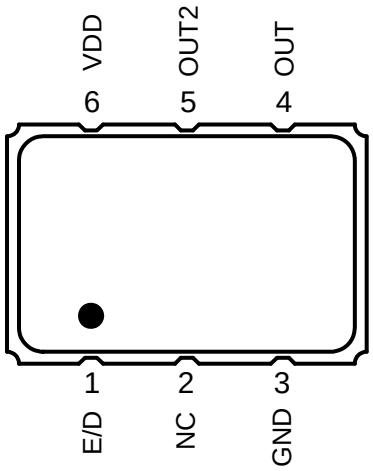
The XUL is an Ultra Precision LVDS Crystal Oscillator with 300 fs typical phase jitter over 12kHz to 20 MHz bandwidth. Available in a wide frequency range from 16kHz to 1500MHz, the IDT XUL Series Crystal Oscillator utilizes a family of proprietary ASICs, with a key focus on noise reduction technologies.

The 4th order Delta Sigma Modulator reduces noise to the levels that are comparable to traditional Bulk Quartz and SAW oscillators. With short lead-time, low cost, low noise, wide frequency range, excellent ambient performance, the XUL is an excellent choice over the conventional technologies. The XUL has stabilities as tight as +/- 20ppm with extremely quick delivery for both standard and custom frequencies

Features

- Frequency range: 0.016 to 1500 MHz
- Output Type: LVDS
- Frequency Stability: ± 20ppm, ± 25ppm, ± 50ppm, or ± 100 ppm
- Supply Voltage: 1.8V, 2.5V, or 3.3V
- Phase Jitter (1.875MHz to 20MHz): 100fs typical
- Phase Jitter (12kHz to 20MHz): 300fs typical
- Package options: 5.0mm x 3.2mm x 1.2mm (JS6)
  7.0mm x 5.0mm x 1.3mm (JU6)
- Operating Temperatures: -20°C to +70°C or -40°C to +85°C

Pin Assignment



6-pin CLCC

Pin Descriptions

Pin Number	Pin Name	Description
1	E/D	Enable/Disable[1] (0=Output Disabled)
2	NC	No connect
3	GND	Connect to ground
4	OUT	Output
5	OUT2	Complementary output
6	VDD	Supply Voltage

1. Pulled high internally.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the XUL. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
VDD	-0.5 to +5.0 V
E/D	-0.5 V to VDD + 0.5 V
OUT	-0.5 V to VDD + 0.5 V
Storage Temperature	-55°C to 125°C
Theta Ja (Junction to Ambient)	102°C/W – Still Air

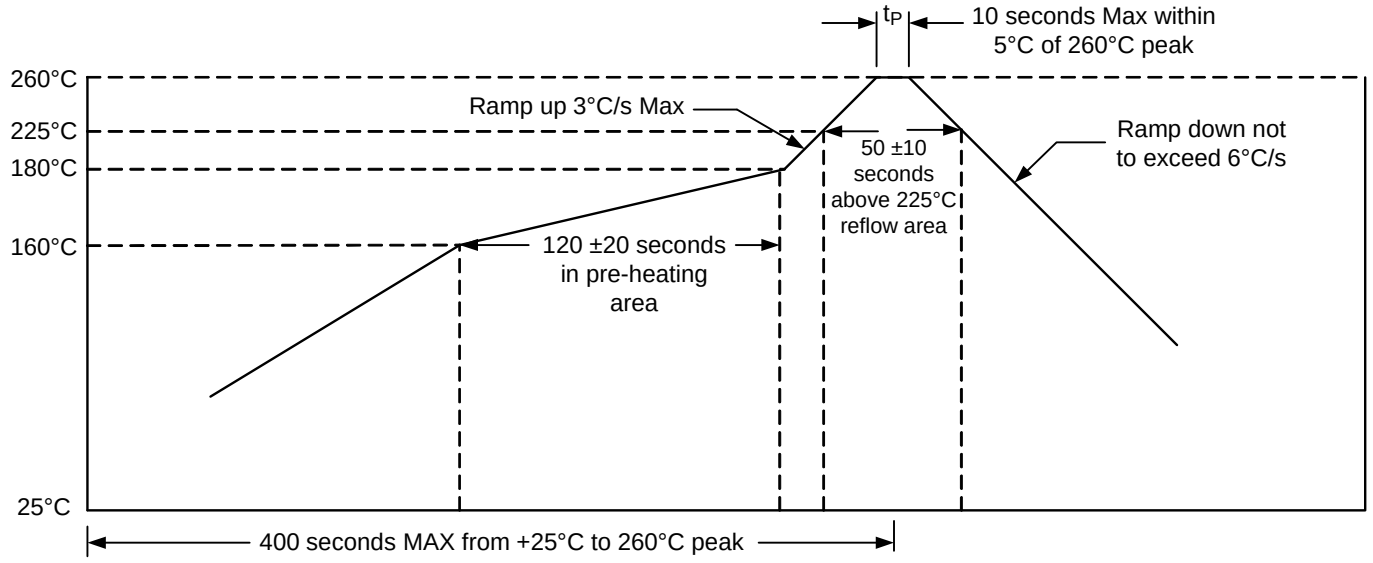
ESD Compliance

Human Body Model (HBM	1000V
Machine Model (MM)	150V

Mechanical Testing

Parameter	Test Method
Mechanical Shock	Half-Sine wave with 0.3ms 3000G X, Y, Z each direction 1 time
Mechanical Vibration	Frequency: 10 to 55 MHz Amplitude: 1.5mm Frequency: 55~2000Hz Peak value: 20G Duration time: 4H for each X,Y,Z axis Total 12hours
High Temp Operating Life (HTOL)	2000 Hours 125°C (under power)
Hermetic Seal	Gross leak (Air leak test) Fine leak (Helium leak test) He-pressure: 6kgf/cm² 2 hours

Solder Reflow Profile



DC Characteristics

(V_{DD}= **3.3 V** ± 5%, T_A= - 20°C to +70°C; -40° to +85°C). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply Current	I_{DD}	Standard Frequencies		79	97	mA
Differential Output Voltage	V_{OD}	Std LVDS load	0.25	0.5	0.6	V
Output Offset Voltage	V_{OS}	Std LVDS load	1.0	1.17	1.375	V
Enable/Disable Input HIGH Voltage (Output enabled)*	V_{IH}		70%V_{DD}			V
Enable/Disable Input LOW Voltage (Output disabled)	V_{IL}				30%V_{DD}	V

* A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

AC Characteristics

(V_{DD}= **3.3 V** ± 5%, T_A= - 20°C to +70°C; -40° to +85°C). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Frequency Range	F_{OUTR}		0.016		1500	MHz
Frequency Stability		Temperature = -20°C to +70°C	±20		±100	ppm
		Temperature = -40°C to +85°C	±25		±100	ppm
Aging (1st year)		Ta = 25°C			±3	
Aging (10 years)		Ta = 25°C			±10	
Output Load		Differential		100		Ohms
Start-up Time	T_{ST}	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% V_{PP}		275	380	ps
Output Fall Time		80% to 20% V_{PP}		275	380	ps
Output Clock Duty Cycle	T_{DTCY}	@ 50% V_{PP}	45		55	%
Output Enable/ Disable Time	T_{OE}				100	ns
Period Jitter, RMS	J_{PER}	Frequency = 156.25MHz		3.5	8	psec
Random Jitter	R_J	Frequency = 156.25MHz Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		0.9	1.5	psec
Deterministic Jitter	D_J			12	26	psec
Total Jitter	T_J			25	44	psec
Phase Jitter (12kHz – 20MHz)	ϕ_{JITTER}	@25°C & 3.3V		300	400	fsec
Phase Noise Performance Frequency = 156.25 MHz	ϕ_{NOISE}	100Hz of Carrier		-97		dBc/Hz
		1kHz of Carrier		-112		dBc/Hz
		10kHz of Carrier		-122		dBc/Hz
		100kHz of Carrier		-131		dBc/Hz
		1MHz of Carrier		-146		dBc/Hz
		10MHz of Carrier		-153		dBc/Hz
Output Frequency (Standards)	F_{OUT}	100MHz, 106.25MHz, 125MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212,5MHz, 250MHz, 300MHz, 312.5MHZ, 400MHz (Contact IDT for additional frequencies)				

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at 25°C. We do not recommend hand soldering the devices

DC Characteristics

(V_{DD}= **2.5 V** ± 5%, T_A= - 20°C to +70°C; -40° to +85°C). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply Current	I_{DD}	Standard frequencies		75	90	mA
Differential Output Voltage	V_{OD}	Std LVDS load	0.25	0.45	0.55	V
Output Offset Voltage	V_{OS}	Std LVDS load	1.0	1.17	1.375	V
Enable/Disable Input HIGH Voltage (Output enabled)*	V_{IH}		70%V_{DD}			V
Enable/Disable Input LOW Voltage (Output disabled)	V_{IL}				30%V_{DD}	V

* A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

AC Characteristics

(V_{DD}= **2.5 V** ± 5%, T_A= - 20°C to +70°C; -40° to +85°C). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Frequency Range	F_{OUTR}		0.016		1350	MHz
Frequency Stability		Temperature = -20°C to +70°C	±20		±100	ppm
		Temperature = -40°C to +85°C	±25		±100	ppm
Output Load		Differential		100		Ohms
Start-up Time	T_{ST}	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% V_{PP}		300	400	ps
Output Fall Time		80% to 20% V_{PP}		300	400	ps
Output Clock Duty Cycle	T_{DTCY}	@ 50% V_{PP}	45		55	%
Output Enable/ Disable Time	T_{OE}				100	ns
Period Jitter, RMS	J_{PER}	Frequency = 156.25MHz		5	9	psec
Random Jitter	R_J	Frequency = 156.25MHz Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		0.9	1.3	psec
Deterministic Jitter	D_J			10	18	psec
Total Jitter	T_J			25	36	psec
Phase Jitter (12kHz – 20MHz)	ϕ_{JITTER}	@25°C & 2.5V		400	500	fsec
Phase Noise Performance Frequency = 156.25MHz	ϕ_{NOISE}	100Hz of Carrier		-97		dBc/Hz
		1kHz of Carrier		-114		dBc/Hz
		10kHz of Carrier		-120		dBc/Hz
		100kHz of Carrier		-127		dBc/Hz
		1MHz of Carrier		-146		dBc/Hz
		10MHz of Carrier		-153		dBc/Hz
Output Frequency (Standards)	F_{OUT}	100MHz, 106.25MHz, 125MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212,5MHz, 250MHz, 300MHz, 312.5MHZ, 400MHz (Contact IDT for additional frequencies)				

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at 25°C. We do not recommend hand soldering the devices

DC Characteristics

(V_{DD}= **1.8 V** ± 5%, T_A= - 20°C to +70°C; -40° to +85°C). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply Current	I_{DD}	Standard frequencies			65	mA
Differential Output Voltage	V_{OD}	Std LVDS load	0.25	0.4	0.5	V
Output Offset Voltage	V_{OS}	Std LVDS load		1.17		V
Enable/Disable Input HIGH Voltage (Output enabled)*	V_{IH}		70%V_{DD}			V
Enable/Disable Input LOW Voltage (Output disabled)	V_{IL}				30%V_{DD}	V

* A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

AC Characteristics

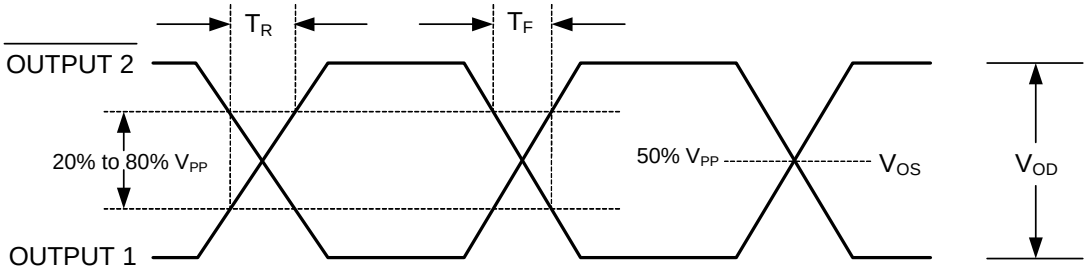
(V_{DD}= **1.8 V** ± 5%, T_A= - 20°C to +70°C; -40° to +85°C). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Frequency Range	F_{OUTR}		0.016		1000	MHz
Frequency Stability		Temperature = -20°C to +70°C	±20		±100	ppm
		Temperature = -40°C to +85°C	±25		±100	ppm
Output Load		Differential		100		Ohms
Start-up Time	T_{ST}	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% V_{PP}		250	315	ps
Output Fall Time		80% to 20% V_{PP}		250	315	ps
Output Clock Duty Cycle	T_{DTCY}	≤156.25MHz	45		55	%
		>156.25MHz	40		60	%
Output Enable/ Disable Time	T_{OE}				100	ns
Period Jitter, RMS	J_{PER}	Frequency = 156.25MHz		5	10	psec
Random Jitter	R_J	Frequency = 156.25MHz Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		2.0	3.8	psec
Deterministic Jitter	D_J			27	36	psec
Total Jitter	T_J			60	80	psec
Phase Jitter (12kHz – 20MHz)	ϕ_{JITTER}	@25°C & 1.8V		800	1200	fsec
Phase Noise Performance Frequency = 156.25MHz	ϕ_{NOISE}	100Hz of Carrier		-91		dBc/Hz
		1kHz of Carrier		-107		dBc/Hz
		10kHz of Carrier		-111		dBc/Hz
		100kHz of Carrier		-121		dBc/Hz
		1MHz of Carrier		-143		dBc/Hz
		10MHz of Carrier		-147		dBc/Hz
Output Frequency (Standards)	F_{OUT}	100MHz, 106.25MHz, 125MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212,5MHz, 250MHz, 300MHz, 312.5MHZ, 400MHz (Contact IDT for additional frequencies)				

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at 25°C. We do not recommend hand soldering the devices

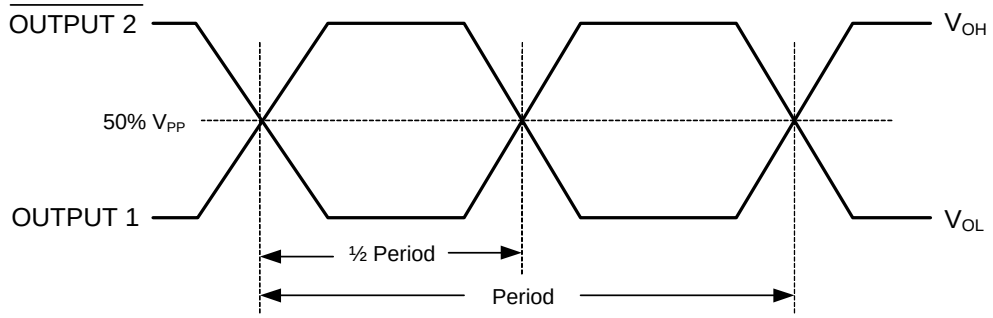
Output Waveform

Output Levels/Rise Time/Fall Time Measurements

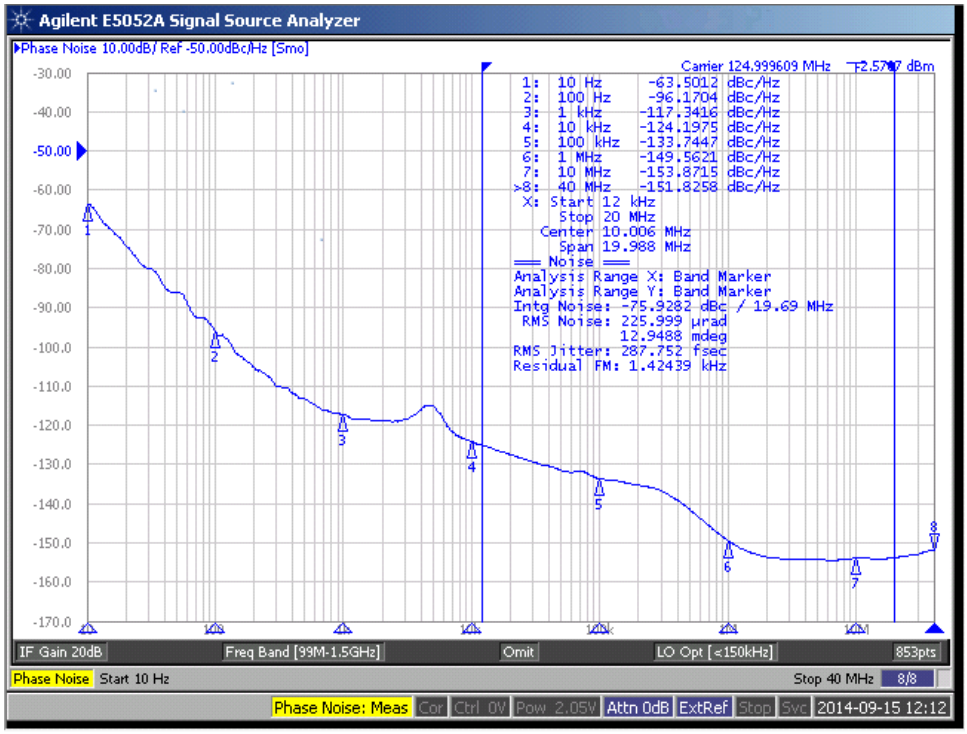


Oscillator Symmetry

Ideally, Symmetry should be 50/50 for ½ period –Other expressions are 45/55 or 55/45

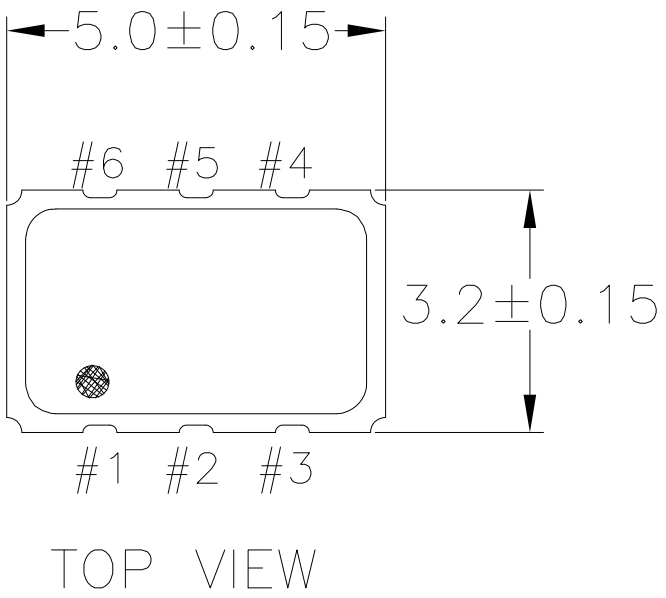


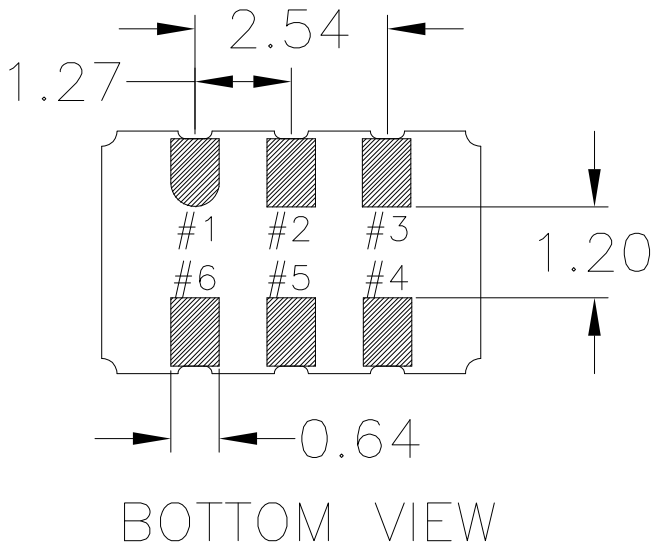
Typical Phase Noise

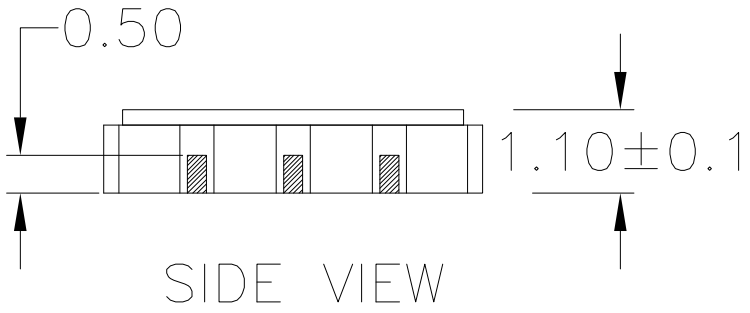


JS6 Package Outline and Dimensions

REV	DESCRIPTION	DATE	APPRO
00	INITIAL RELEASE	04/2/12	DP
01	ADDED LID IN TOP VIEW	07/12/12	KS
02	UPDATED LID TOLERANCES	12/03/12	KS
03	UPDATE PACKAGE DRAWING	8/8/14	J.HU







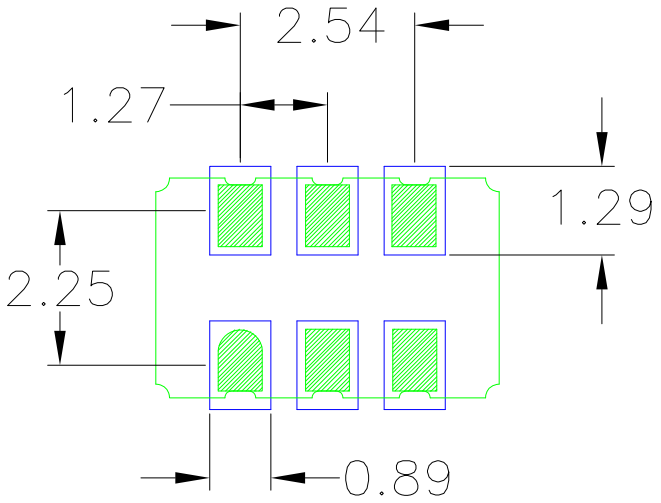
NOTES:

1. ALL DIMENSIONS IN MM.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±		IDT™ www.IDT.com	6024 Silver Creek Valle San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674
APPROVALS	DATE	TITLE	JS6 PACKAGE OUTLINE 5.0 x 3.2 mm BODY 1.1 mm Thick
DRAWN RAC	04/2/12		
CHECKED			
		SIZE C	DRAWING No. PSC-4411

JS6 Package Outline and Dimensions (cont.)

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	04/2/12	DP
01	ADDED LID IN TOP VIEW	07/12/12	KS
02	UPDATED LID TOLERANCES	12/03/12	KS
03	UPDATE PACKAGE DRAWING	8/8/14	J.HUA



RECOMMENDED LAND PATTERN

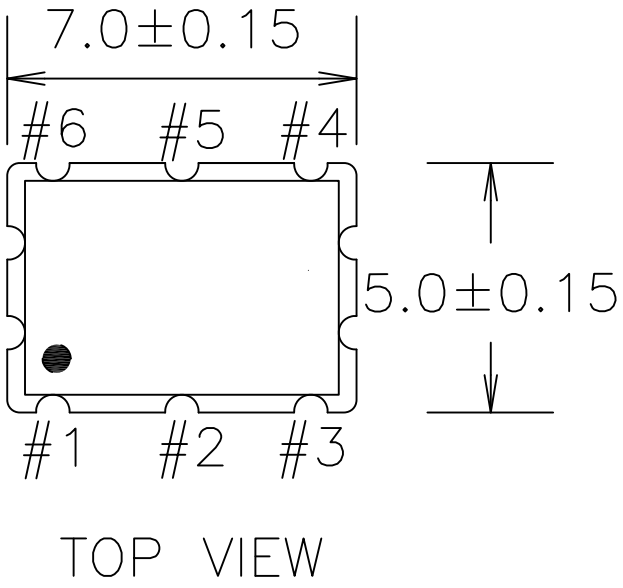
NOTES:

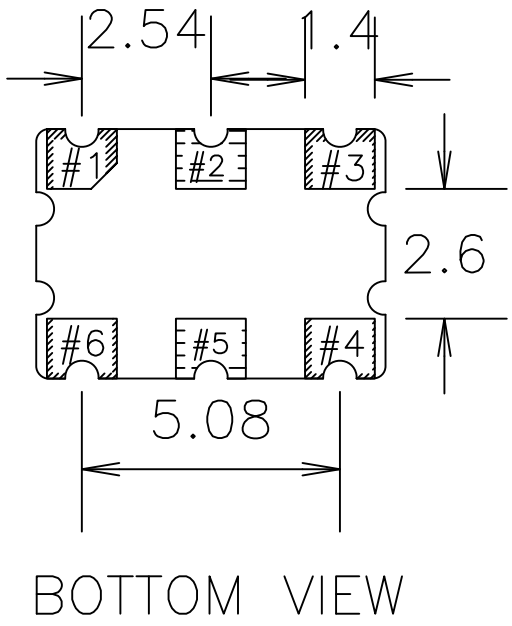
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

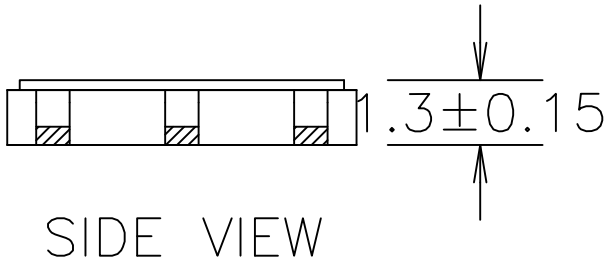
TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±		IDT™ www.IDT.com	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674
APPROVALS	DATE	TITLE	JS6 PACKAGE OUTLINE 5.0 x 3.2 mm BODY 1.1 mm Thick
DRAWN P&AC	04/2/12		
CHECKED			
		SIZE C	DRAWING No. PSC-4411 REV 03
		DO NOT SCALE DRAWING	SHEET 2 OF 2

JU6 Package Outline and Dimensions

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/5/12	KS
01	UPDATE PACKAGE DRWING	8/12/14	J.HUA







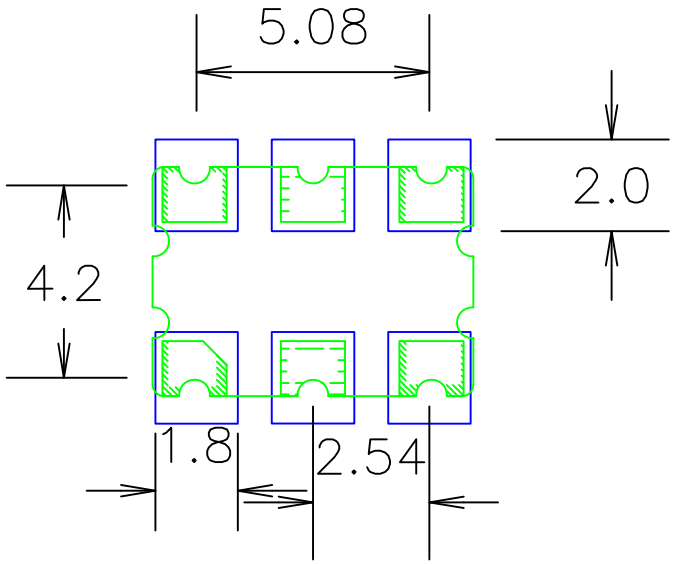
NOTES:

1. ALL DIMENSIONS IN MM.

TOLERANCES UNLESS SPECIFIED DECIMAL XX± XXX± XXXX± ANGULAR ±		IDT™ www.IDT.com	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674
APPROVALS	DATE	TITLE	JU6 PACKAGE OUTLINE 7.0 x 5.0 mm BODY 1.3 mm Thick
DRAWN KcB	10/03/12		
CHECKED			
		SIZE C	DRAWING No. PSC-4430 / REV 01

JU6 Package Outline and Dimensions (cont.)

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/5/12	KS
01	UPDATE PACKAGE DRWING	8/12/14	J.HUA

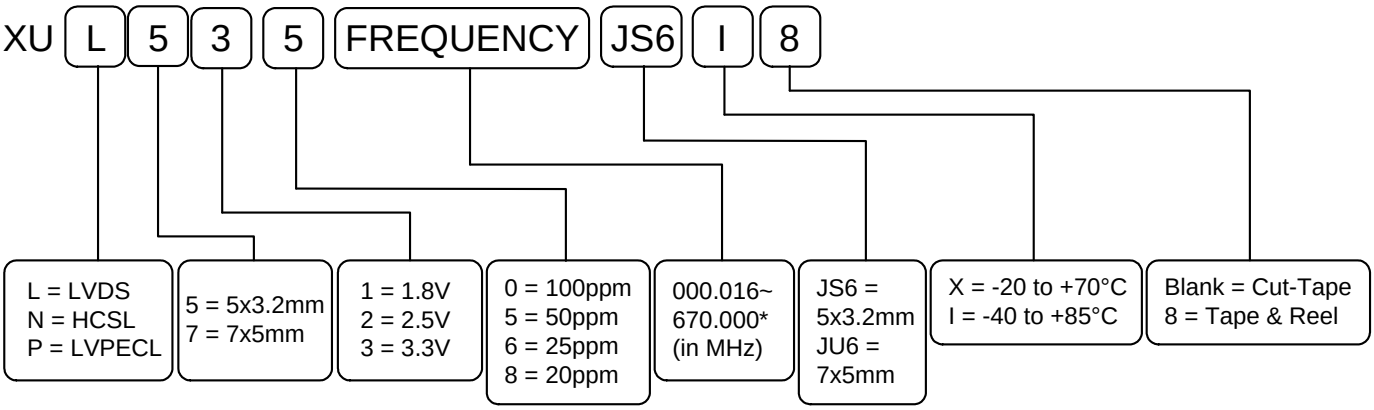


RECOMMENDED LAND PATTERN

NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±		IDT™ www.IDT.com	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674
APPROVALS	DATE	TITLE	JU6 PACKAGE OUTLINE 7.0 x 5.0 mm BODY 1.3 mm Thick
DRAWN JCB	10/03/12		
CHECKED			
		SIZE C	DRAWING No. PSC-4430 REV 01
		DO NOT SCALE DRAWING	SHEET 2 OF 2

Ordering Information



* See table or contact IDT for custom frequencies

Revision History

Rev.	Date	Originator	Description of Change
A	10/01/14	B. Chandhoke	1. Corrected typo in spec for Enable/Disable Low Voltage; from ≥30%VDD to ≤30%VDD. 2. Moved from Advance to Preliminary.
B	12/15/14	B. Chandhoke	1. Added 7 x 5 x 1.3mm JU6 package option and package dimension/landing pattern drawings. 2. Updates to all DC char tables. 3. Updates to all AC char tables. 4. Updates to Output Waveform diagram. 5. Updated ordering information table/graphic to show JU6 package option.

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