HARRIS

RFL1N08
RFL1N10

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 1A, 80V and 100V
- $R_{DS(on)} = 1.2\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

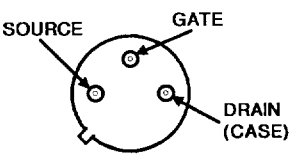
Description

The RFL1N08 and RFL1N10 are n-channel enhancement mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package.

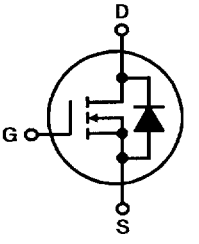
Package

TO-205AF



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFL1N08	RFL1N10	UNITS
Drain-Source Voltage	V_{DSS}	80	100	V
Drain-Gate Voltage (R_{GS} = 1MΩ)	V_{DGR}	80	100	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Drain Current, RMS Continuous	I_D	1	1	A
Pulsed	I_{DM}	5	5	A
Power Dissipation Total @ T_C = 25°C	P_D	8.33	8.33	W
Derating Above T_C = 25°C		0.0667	0.0667	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procdures should be followed.

File Number **1385.1**

Electrical Characteristics (T_C = +25°C), Unless Otherwise Specified

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL1N08		RFL1N10		
			MIN	MAX	MIN	MAX	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0	80	–	100	–	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65V	–	1	–	–	μA
		V_{DS} = 80V	–	–	–	1	μA
		T_C = +125°C, V_{DS} = 65V	–	50	–	–	μA
		V_{DS} = 80V	–	–	–	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0	–	100	–	100	nA
Drain-Source On-Voltage	$V_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	1.2	–	1.2	V
		I_D = 2A, V_{GS} = 10V	–	3.3	–	3.3	V
Static Drain-Source On Resistance	$r_{DS(on)}$*	I_D = 1A, V_{GS} = 10V	–	1.2	–	1.2	Ω
Forward Transconductance	g_{fs}*	I_D = 1A, V_{DS} = 10V	400	–	400	–	S (℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	–	200	–	200	pF
Output Capacitance	C_{OSS}		–	80	–	80	pF
Reverse-Transfer Capacitance	C_{RSS}		–	25	–	25	pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 1A, V_{DD} = 50V, R_{GEN} = R_{GS} = 50Ω, V_{GS} = 10V	17 (typ)	25	17 (typ)	25	ns
Rise Time	t_r		30 (typ)	45	30 (typ)	45	ns
Turn-Off Delay Time	$t_{d(off)}$		30 (typ)	45	30 (typ)	45	ns
Fall Time	t_f		30 (typ)	50	30 (typ)	50	ns
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		–	15	–	15	°C/W

Source-Drain Diode Ratings and Characteristics

CHARACTERISTIC	SYMBOLS	TEST CONDITIONS	LIMITS				UNITS
			RFL1N08		RFL1N10		
			MIN	MAX	MIN	MAX	
Diode Forward Voltage	V_{SD}*	I_{SD} = 1A	–	1.4	–	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/dt = 50A/μs	100 (typ)	100 (typ)	100 (typ)	100 (typ)	ns

* Pulsed: Pulse duration = 300μs max., duty cycle = 2%.

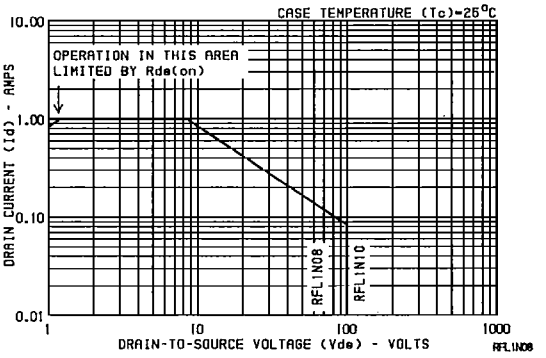


Fig. 1 - Maximum operating areas for all types.

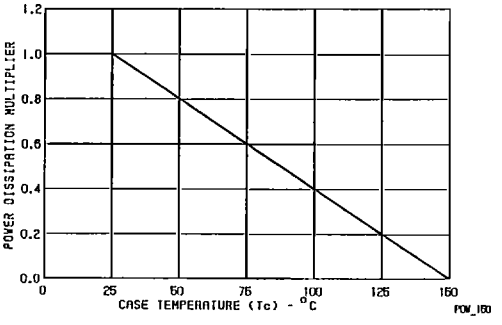


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

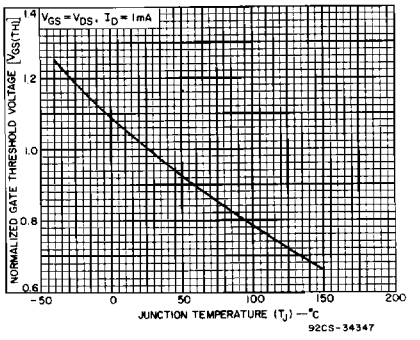


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

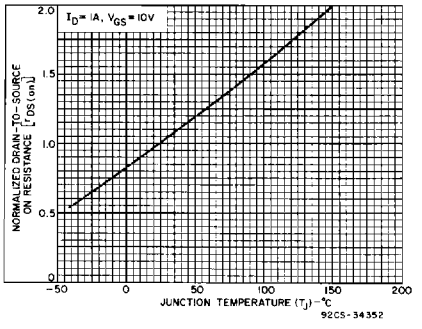


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

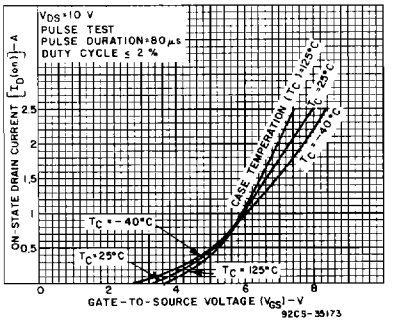


Fig. 5 - Typical transfer characteristics for all types.

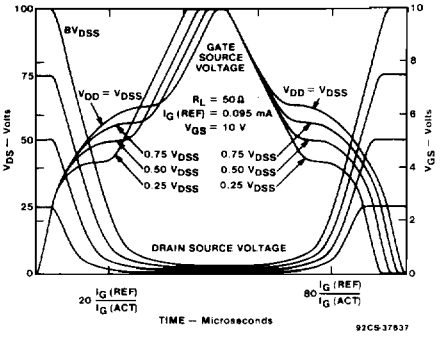


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN-7254 and AN-7260.

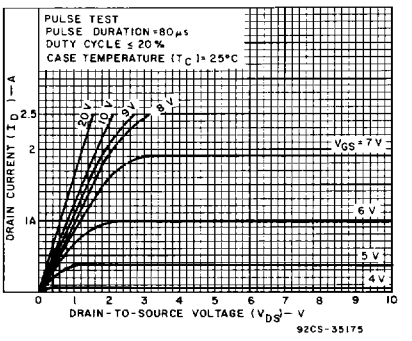


Fig. 7 - Typical saturation characteristics for all types.

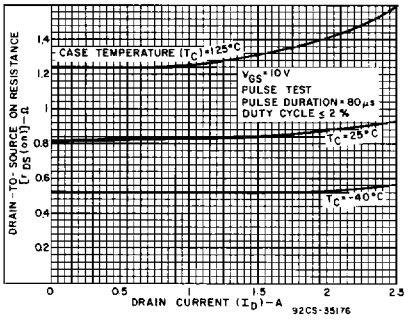


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

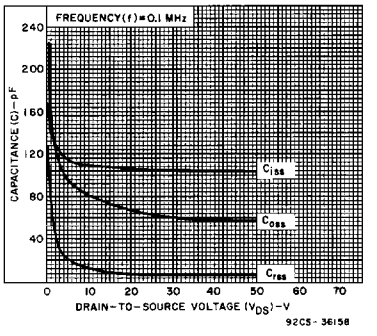


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

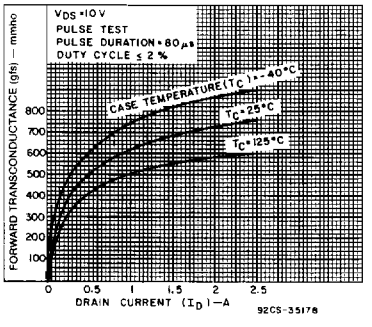


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

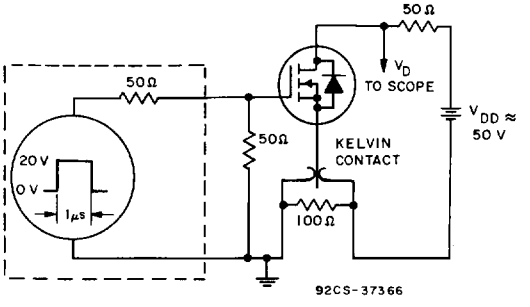


Fig. 11 - Switching Time Test Circuit.