
HN62435 Series

262144-word $\times$ 16-bit/524288-word $\times$ 8-bit CMOS Mask
Programmable ROM

HITACHI

ADE-203-472A(Z)

Rev. 1.0

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Description

The HN62435 is a 4-Mbit CMOS mask-Programmable ROM organized either as 262144 words by 16 bits or 524288 words by 8 bits. Realizing a access speed of 120/150 ns (max) depend upon technology of a high speed circuit.

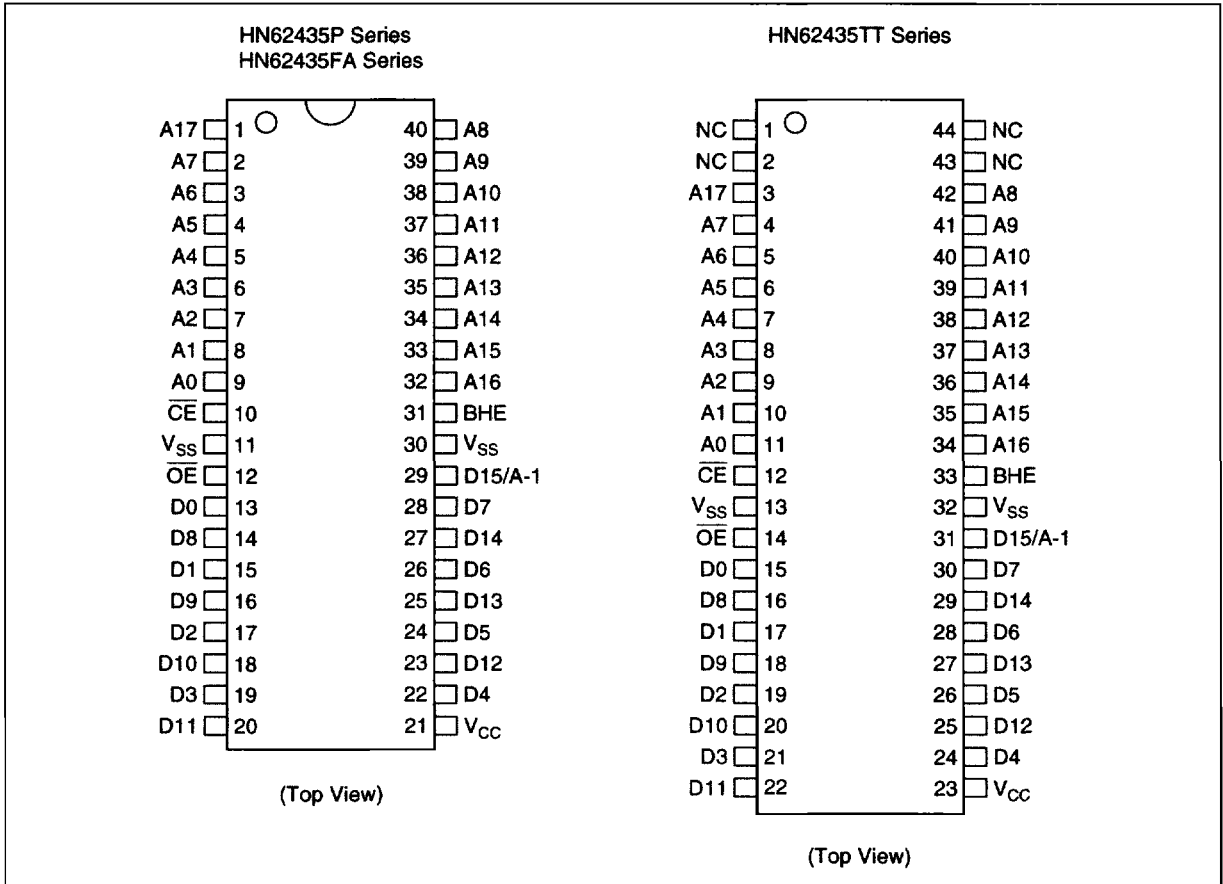
Features

- Single 5 V supply
- High speed
Access time: 120/150 ns (max)
- Low power
Active: 275 mW (max)
Standby: 165 μ W (max)
- Byte-wide or word-wide data organization (Switched by BHE terminal)
- Three-state data output for or-tying
- Directly TTL compatible
All inputs and outputs
- Pin compatible with 4 Mbit EPROM (HN27C4000G/FP)

Ordering Information

Type No.	Access time	Package
HN62435P-12	120 ns	600 mil 40-pin plastic DIP (DP-40)
HN62435P-15	150 ns	
HN62435FA-12	120 ns	525 mil 40-pin plastic SOP (FP-40D)
HN62435FA-15	150 ns	
HN62435TT-12	120 ns	400 mil 44-pin plastic TSOP II (TTP-44D)
HN62435TT-15	150 ns	

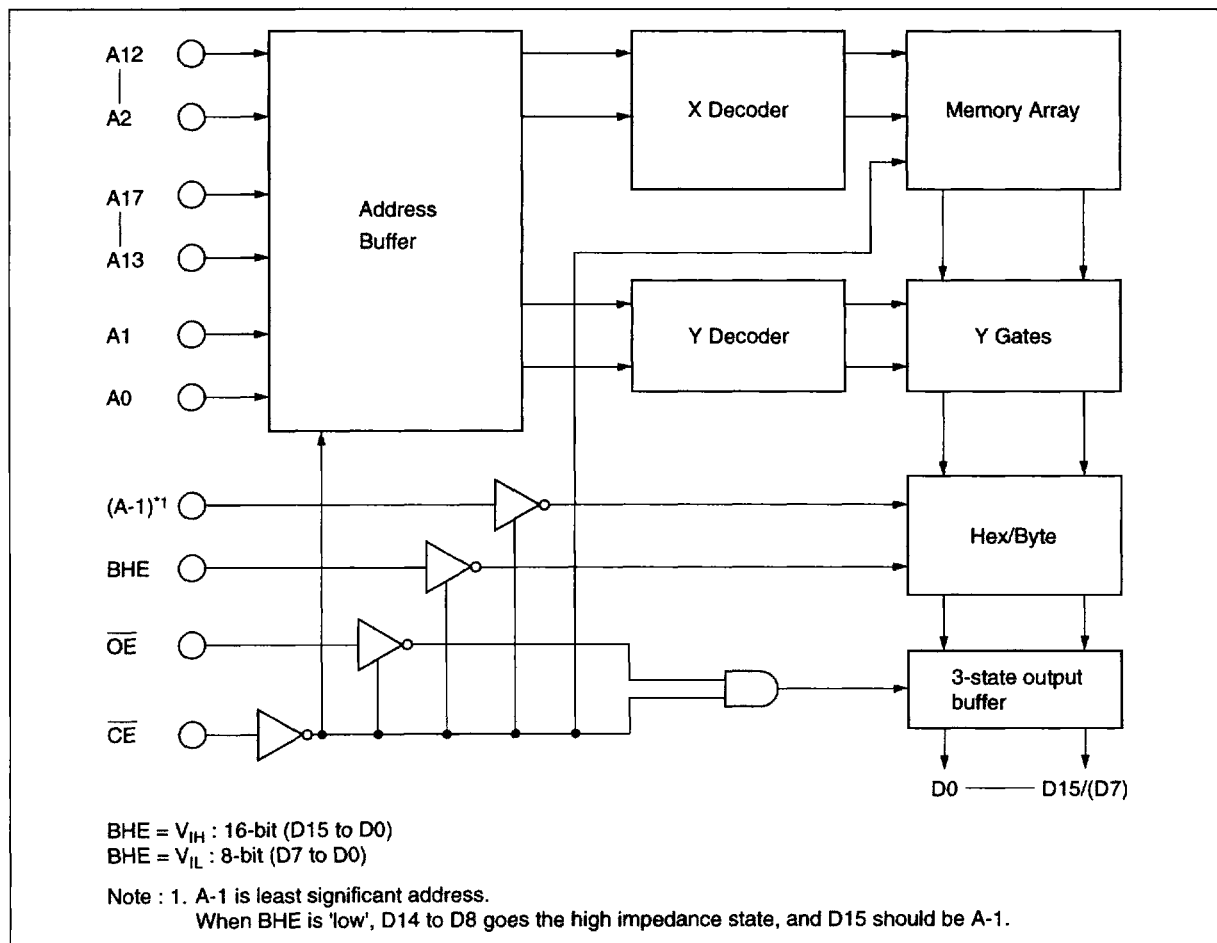
Pin Arrangement



Pin Description

Pin name	Function
A-1, A0 to A17	Address inputs
D0 to D15	Data outputs
BHE	8/16 bit (byte/word) mode switch
$\overline{\text{CE}}$	Chip enable
OE	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Mode Selection

Mode	Pin				Data output		Address input	
	$\overline{CE}$	$\overline{OE}$	BHE	D15/A-1	D0-D7	D8-D15	LSB	MSB
Standby	H	x ¹	x	x	High-Z ²	High-Z	—	—
Output disable	L	H	x	x	High-Z	High-Z	—	—
Read (16-bit)	L	L	H	Dout	D0 to D7	D8 to D15	A0	A17
Read (8-bit)	L	L	L	L	D0 to D7	High-Z	A-1	A17
Read (8-bit)	L	L	L	H	D8 to D15	High-Z	A-1	A17

Notes: 1. x: Don't care.

2. High-Z: High impedance

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage ¹	V_{CC}	-0.3 to +7.0	V
All input and output voltage ¹	V_{in}, V_{out}	-0.3 to $V_{CC} + 0.3$	V
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	-55 to +125	°C
Temperature under bias	T_{bias}	-20 to +85	°C

Note: 1. With respect to V_{SS} .

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	$V_{CC} + 0.3$	V
	V_{IL}	-0.3	—	0.8	V

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DC Characteristics ($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$, $T_a = 0 \text{ to } +70^\circ\text{C}$)

Parameter		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{CC}	—	50	mA	$V_{CC} = 5.5 \text{ V}$, $I_{DOUT} = 0 \text{ mA}$, $t_{RC} = \min$
	Standby	I_{SB1}	—	30	μA	$V_{CC} = 5.5 \text{ V}$, $\overline{CE} \geq V_{CC} - 0.2 \text{ V}$
	Standby	I_{SB2}	—	3	mA	$V_{CC} = 5.5 \text{ V}$, $\overline{CE} \geq 2.2 \text{ V}$
Input leakage current		$ I_{IL} $	—	10	μA	$V_{in} = 0 \text{ to } V_{CC}$
Output leakage current		$ I_{OL} $	—	10	μA	$\overline{CE} = 2.2 \text{ V}$, $V_{out} = 0 \text{ to } V_{CC}$
Output voltage		V_{OH}	2.4	—	V	$I_{OH} = -205 \mu\text{A}$
		V_{OL}	—	0.4	V	$I_{OL} = 1.6 \text{ mA}$

Capacitance ($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$, $T_a = 25^\circ\text{C}$, $V_{in} = 0 \text{ V}$, $f = 1\text{MHz}$)

Parameter		Symbol	Min	Max	Unit
Input capacitance ^{*1}		C_{in}	—	10	pF
Output capacitance ^{*1}		C_{out}	—	15	pF

Note: *1. This parameter is sampled and not 100% tested. D15/A-1 pin is output.

AC Characteristics ($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$, $T_a = 0 \text{ to } +70^\circ\text{C}$)

- Output load: 1TTL + $C_L = 100 \text{ pF}$ (including jig)
- Input pulse level: 0.6 to 2.4 V
- Input and output timing reference levels: 1.5 V
- Input rise and fall time: 5 ns

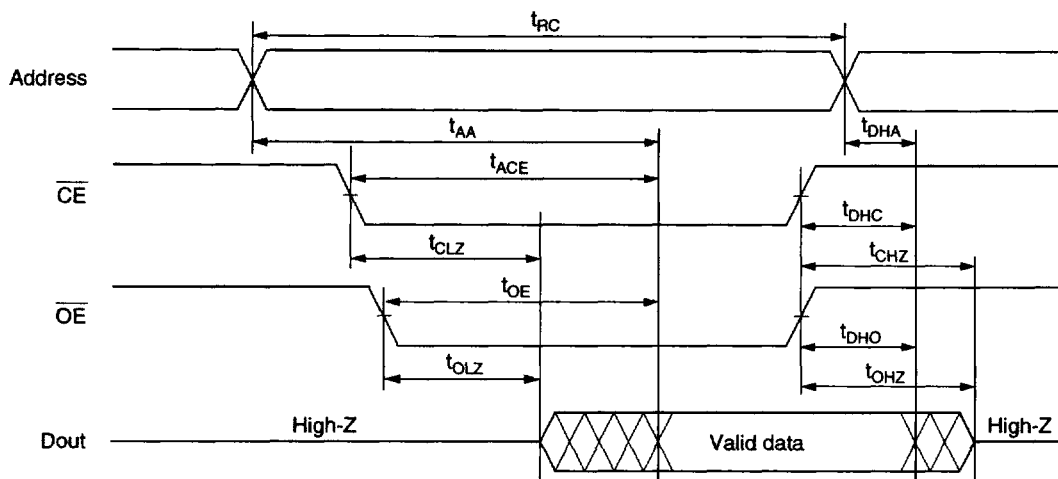
Parameter	Symbol	HN62435-12		HN62435-15		Unit	Note
		Min	Max	Min	Max		
Read cycle time	t_{RC}	120	—	150	—	ns	
Address access time	t_{AA}	—	120	—	150	ns	
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	ns	
$\overline{OE}$ access time	t_{OE}	—	60	—	70	ns	
BHE access time	t_{BHE}	—	120	—	150	ns	
Output hold time from address change	t_{DHA}	0	—	0	—	ns	
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns	
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns	
Output hold time from BHE	t_{DHB}	0	—	0	—	ns	
$\overline{CE}$ to output in high-Z	t_{CHZ}	—	60	—	70	ns	1
$\overline{OE}$ to output in high-Z	t_{OHZ}	—	60	—	70	ns	1
BHE to output in high-Z	t_{BHZ}	—	60	—	70	ns	1
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	5	—	ns	
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	5	—	ns	
BHE to output in low-Z	t_{BLZ}	5	—	5	—	ns	

Note: 1. t_{CHZ} , t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

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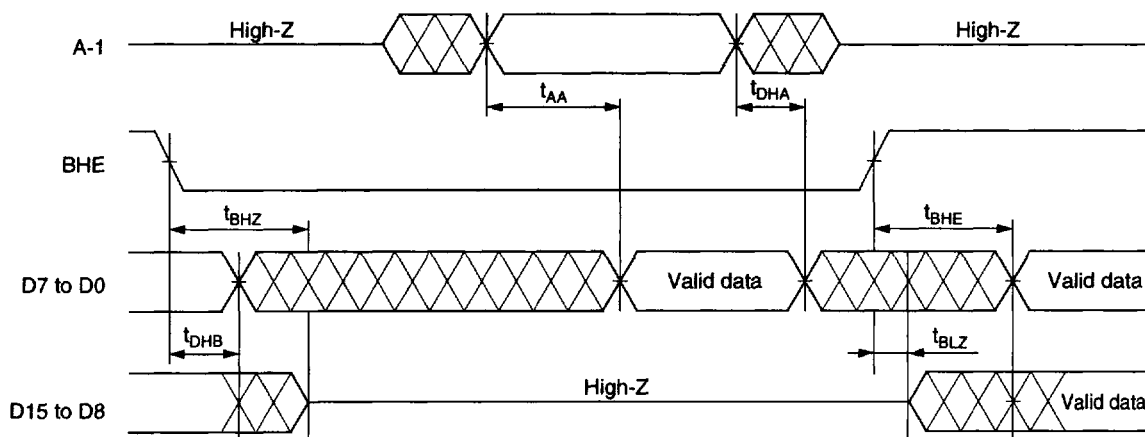
Timing Waveforms

Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')



- Notes :
1. t_{DHA} , t_{DHC} , t_{DHO} : Determined by faster.
 2. t_{AA} , t_{ACE} , t_{OE} : Determined by slower.
 3. t_{CLZ} , t_{OLZ} : Determined by slower.

Word Mode, Byte Mode Switch



- Notes :
1. $\overline{CE}$ and $\overline{OE}$ are enable, A17 to A0 are valid.
 2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable.
Therefore, the input signals of opposite phase to the output must not be applied to them.